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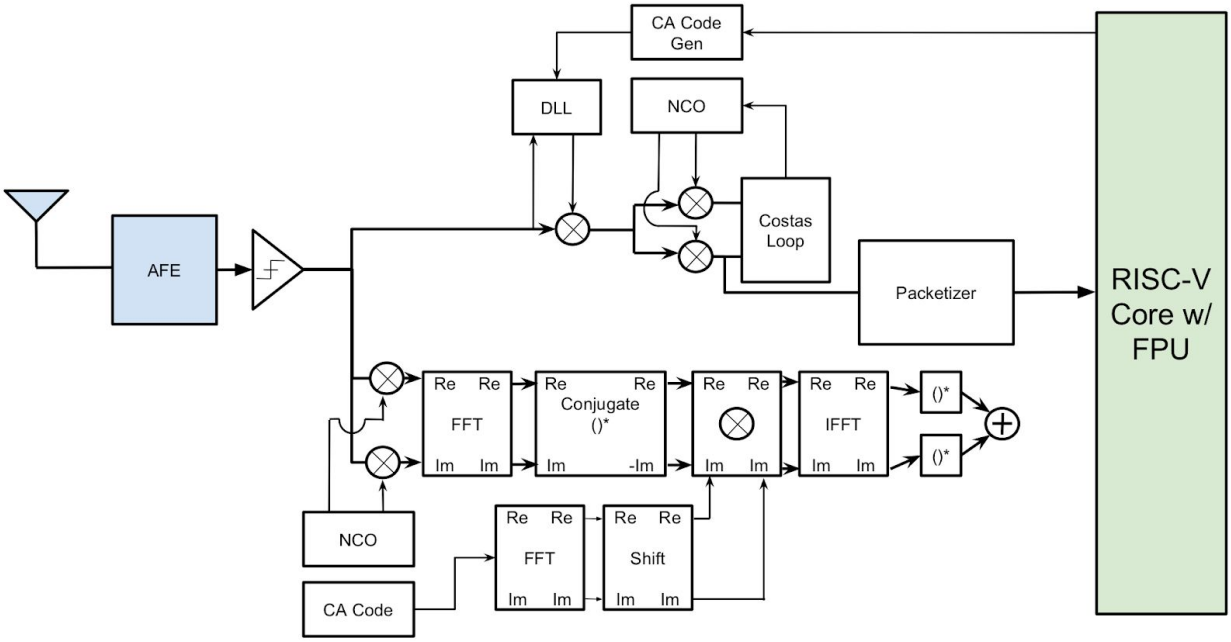
EE 290C: GPS Project Proposal

Introduction:

The objective is to develop a GPS receiver with separate acquisition and tracking capabilities connected to a RISC-V processor for a positioning application. We plan on testing the system on an FPGA target at the end of the semester with an RF front end to acquire real GPS data for positioning.

Block Diagram:



Responsibilities:

Block	**Person**
multiplier/accumulators	Daniel
NCO -> Costas Loop	Olivia
Costas Loop	Zhongkai
DLL Loop	Avi
C/A Code Generation	Nick
Positioning/Rocket/FPU	Dinesh

FFT	Zhaokai
Mat Mul and Selection	Ruocheng

Timeline:

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Tape #	**Implementation Goals**	**Testing Goals**	**Physical Goals**
Tape in 1 (10/26)	In Chisel, define Interfaces and clock domains with null blocks Chisel Implementation of each Block	Python model of each block Block Level Unit Tests / Connecting each block to rocket chip with necessary registers/memory interfaces / Some Code Written	Pick Front End Module or IC and FPGA and Design any necessary boards/peripherals/etc
Tape in 2 (11/15)	Integration amongst Blocks	Full Chain test with dummy data (no Rocket) and With Rocket	Get it working/Acquire real data
Tape Out (11/28)	Full Implementation connected to Rocket Chip	Connect to FPGA hardware	Measure real GPS signal with FPGA!