

SCuM-V23 Specification

Version v1.0

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1. Resource Index

Resource	Description	Link
SCuM-V23 End of Semester Review	Final design review from Sp23	Google Slides
SCuM-V23 Mid-Semester Review	Mid-semester design review from Sp23	Google Slides
Analog RF Simulations	Locations and information on running RF analog simulations	Google Doc
SCuM-V22 Bringup Status	Archive of SCuM-V22 bringup measurements	Google Slides

2. Overview

This document describes the Single-Chip Micro Mote V (SCuM-V), a 16nm system-on-chip (SoC) for internet-of-things (IoT) applications, developed as part of the 2022 offering of EE194/EE290C Special Topics in Circuit Design class.

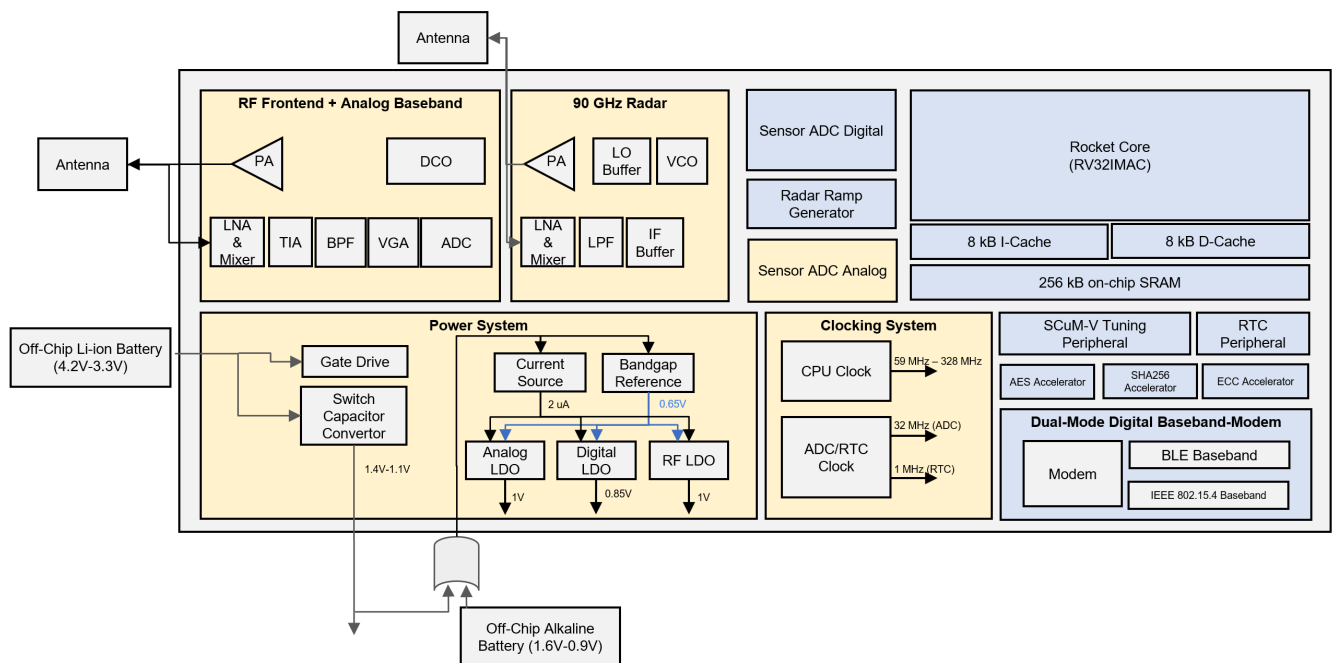
The SoC is designed around the RISC-V 5-stage in-order Rocket processor, generated by the RocketChip generator, embedded in the Chipyard framework. It features a crystal-free design with custom dual-mode IEEE 802.15.4 and Bluetooth Low Energy (BLE) transceiver. The SoC is implemented in the INTEL16 FinFET process.

The SCuM-V chip offers several GPIO pins, a single UART bus, QSPI Flash, and an on-chip, crystal-free RTC with capture and compare registers. This iteration of the chip did not support I2C or an AES accelerator.

SCuM-V23 has several new features introduced over its predecessor SCuM-V22:

- 32b Rocket core w/cryptography acceleration
- Switched capacitor DC-DC converter cascaded with LDOs
- 90 GHz FMCW radar
- 18-bit μ V-precision ADC

2.1. Block Level Diagram + Chip Features



2.2. 32-bit RISC-V Core

The SoC includes a 32-bit Rocket, which has a high-performance single-issue in-order execution pipeline, with a peak sustainable execution rate of one instruction per clock cycle. The core supports Machine and User privilege modes as well as standard Integer, Multiply, Atomic, Floating-

Point and Compressed RISC-V extensions (RV32IMAFIC).

Detailed description of the core is in Chapter 3.

2.3. On-Chip Memory System

The Rocket core has a 8kB I\$ and D\$ and a 256kB scratchpad acting as L2 memory.

2.4. Busses

The design includes a system, peripheral, control, and front bus. The Rocket Tile communicates through the system bus to the remaining three buses. The control bus accesses BootROM, PLIC/CLINT, and the debug interface. The frontend bus handles DMA devices.

2.5. Interrupts

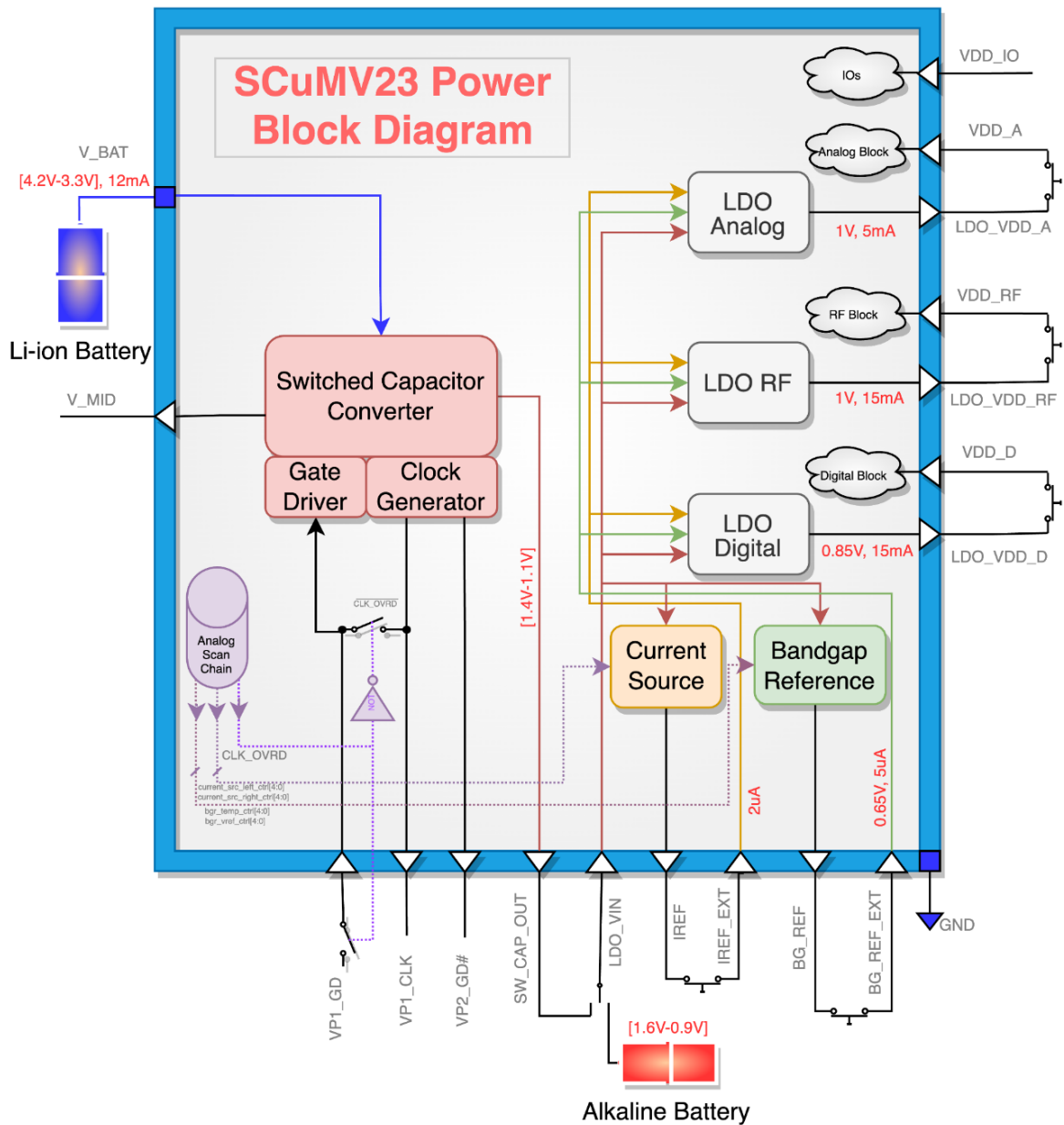
Two interrupt controllers for handling MMIO are attached to the control bus, the platform level interrupt controller and the core local interrupts. Core local interrupts are used for timer and the software while the PLIC interacts with the peripherals.

2.6. Dual-Mode BLE/IEEE 802.15.4 Transceiver

A dual-mode transceiver that supports both Bluetooth Low-Energy and IEEE 802.15.4 modes of operation. In the Bluetooth LE operating mode, the transceiver is capable of sending and receiving BLE Link Layer packets at a rate of 1Msym/s. In IEEE 802.15.4 operating mode, the transceiver sends and receives 802.15.4 PHY packets at 2 Msym/s.

The CPU is able to provide packet payloads to the digital baseband using DMA. Incoming packets will trigger multiple interrupts and provide the packet to the CPU via DMA. Control, status, and tuning registers are exposed to the CPU via MMIO. This includes a large suite of parameters of the transceiver (e.g. radio mode, channel tuning) that are accessed with these memory-mapped registers.

3. Power System



SCuM-V23 has 3 power domains:

1. VDD_A - 1V, 5mA expected
2. VDD_RF - 1V, 15mA expected
3. VDD_D - 0.85V, 15mA expected

3.1. Switched Capacitor Converter

Ladder 3:1 Topology

- All capacitors & switches are rated at Vout.
- Externally Reconfigurable for 3:1, 2:1, 3:2 for exploiting full battery voltage range.

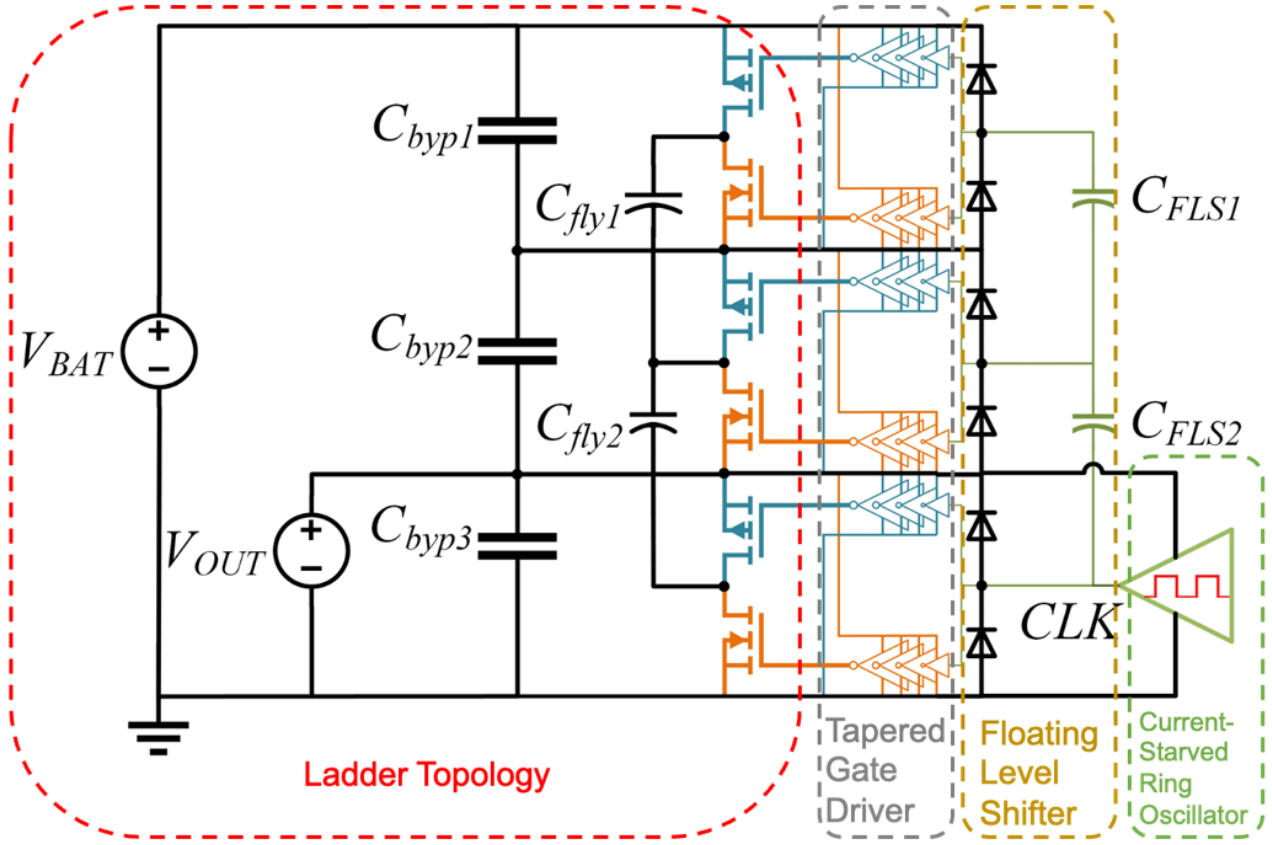


Figure 1. Switched capacitor converter schematic

Simulated Efficiency Variation with Load

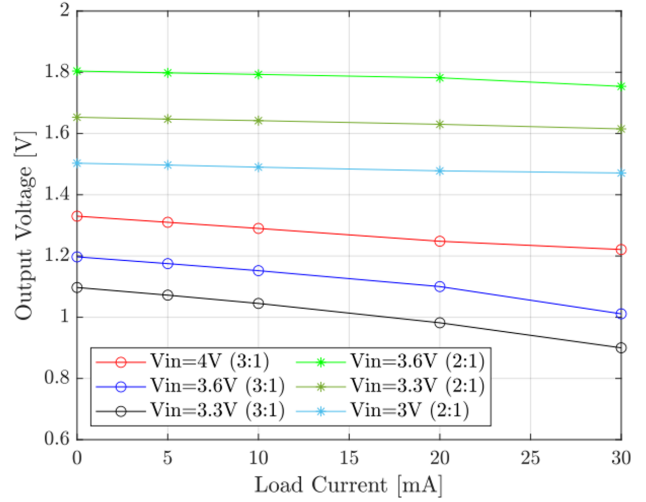
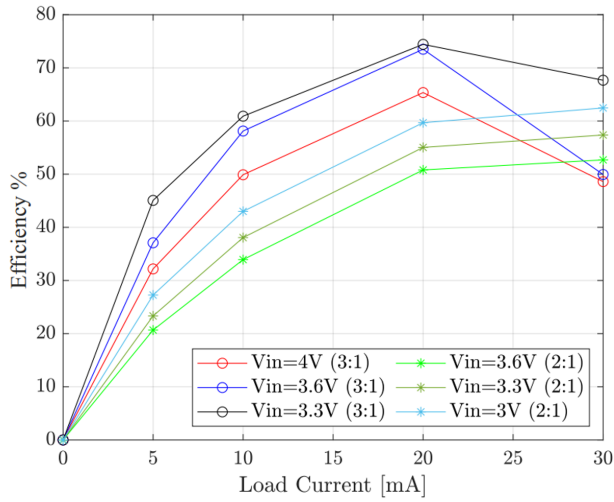


Figure 2. (Left) Efficiency Variation with Load. (Right) Vout Variation with Load

Table 1. Simulated performance

Simulated Performance Parameters	Details
Clock Frequency	85MHz-120MHz
Peak Power Efficiency	75% (Pre-layout)
Full-load Efficiency	68% (Pre-layout) and <50% (Post-layout)
Max Vout_ripple (pk-pk)	50 mVpp

Simulated Performance Parameters	Details
Power Density at full-load	65mW/mm ² @100MHz

Table 2. Overview of High-Level Power Converter Design

Parameters	Details
Total Capacitance	6.5nF
Capacitor Type	MOM+MOS
Vin Range	4.2 V-3V
Vout Range	1.8V-1.1V
Conversion Ratios	3:1, 2:1
Load Range	5mA to 30mA
Switched-Capacitor Area	450,000 um ² (75% of Power Block)
Max Output Power	30 mW

3.2. Low Dropout (LDO) Voltage Regulators

Table 3. Simulated performance

	LDO_RF (1 V)	LDO_Digital (0.85 V)	LDO_Analog (1 V)
Vin	1.8 V - 1.2 V	1.8 V - 1.2 V	1.8 V - 1.2 V
Vout range (at full load)	1.08 V - 0.81 V	0.83 V - 0.73 V	1.19 V - 0.978 V
Max Output Power	15 mW	15 mW	5 mW

3.3. Current Reference

Distributes 2 uA current reference to other blocks, includes a start-up circuit.

Parasitic extraction results:

- Typical conditions yields reference current ranging from 1.98 uA to 2.4 uA (~20% variation)
- Large variation with corners
- Worst case: ff_hot at 3.04 uA

3.4. Bandgap Reference

3.5. Utility Current DAC

Parameter	Spec
Output @ 1.6 V	Up to 63 * IREF
Power @ 126 uA	~50 uW

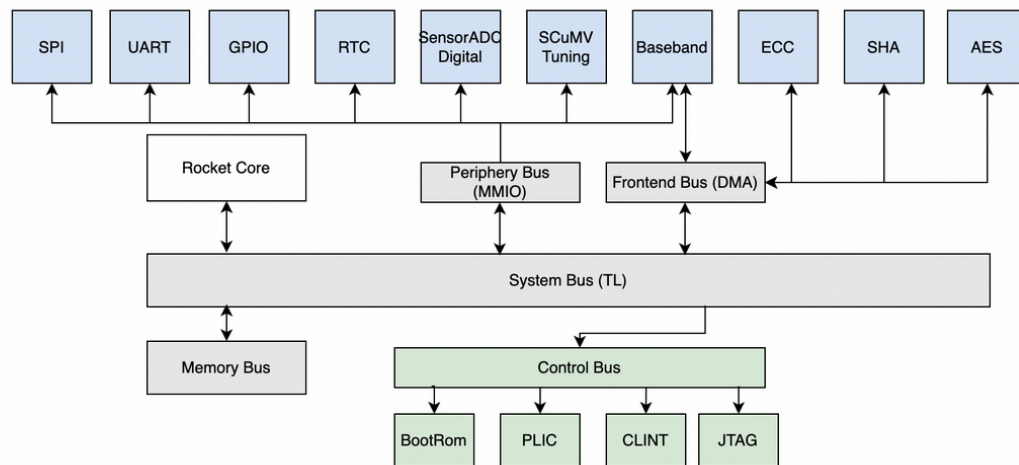
Parameter	Spec
Input Current Range	[0.1 μ A, 20 μ A]
Load Voltage	\sim 150 mV
Average DNL Error	1.73%
Overall INL Error	\sim 2 μ A
Estimated Area	800 μ m ²

- 6-bit binary weighted current mirror scaling
- Uses IREF input as LSB

4. Oscillators

- What clock domains are present?
- How is the system intended to work if fully functional?
- What tuning accessibility do we have?
- What are minimum/maximum frequencies?

5. Digital Core



- Core architecture
- How much memory
- How do we boot
- Where do we find simulations/programs that were run previously?
- Where is the toolchain?
- Is this the right memory map?

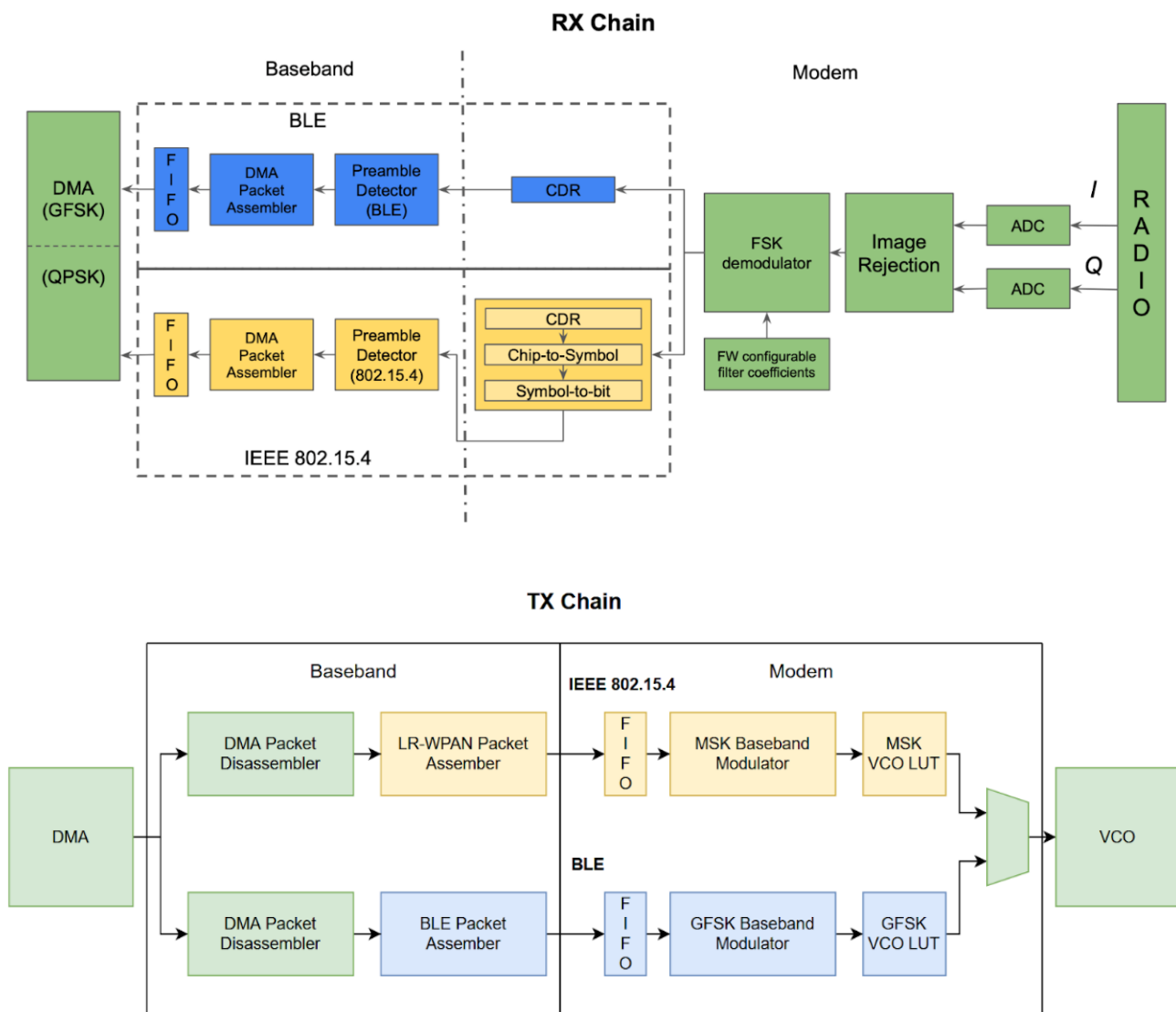
6. Digital Baseband-Modem

6.1. Dual-Mode Baseband-Modem

The Dual-Mode Baseband-Modem (BM) is responsible for handling the transmission and reception of both Bluetooth LE and IEEE 802.15.4 packets. For Bluetooth Low Energy, the BM handles Bluetooth Low Energy 1M Uncoded Link Layer Packets. For IEEE 802.15.4, the BM handles packets transmitted according to the PHY standard for the O-QPSK modulation in the 2.4 GHz band. Additionally the BM exposes an interface for the CPU to read/write various information (e.g. tuning bits) to the analog RF.

There are two primary sub-components in the Baseband-Modem, the Baseband, and the Modem. The baseband is responsible for the bit-stream processing of incoming and outgoing packets. The modem is responsible for modulation on the TX side, and digital image rejection and demodulation on the RX side.

6.1.1. Architecture Overview



6.1.2. Baseband-Modem Frontend

Commands and MMIO Registers

The baseband-modem (BM) block contains a set of memory mapped registers used for passing commands to the BM, tuning analog RF components, and making BM status visible to the CPU. The address map is shown below. Note that the addresses are relative to the BM's base attachment address. For example, if the BM is attached at 0x8000, then the address of 0x04 corresponds to 0x8004.

ADDR	DATA	Size (bits)	Description
0x00	Instruction	32	Instruction received from processor. Contains 4 bits of primary instruction, 4 bits of secondary instruction, then 24 bits of data.
0x04	Additional Data	32	Additional data to write. Set data before writing instructions when applicable.
0x08	Status 0	32	[2:0] Assembler State [5:3] Disassembler State [7:6] TX State [10:8] RX Controller State [12:11] TX Controller State [15:13] Controller State [23:16] ADC I data [31:24] ADC Q data
0x0C	Status 1	32	[5:0] Modulation LUT index [10:6] I AGC LUT index [15:11] I DCOC LUT index [20:16] Q AGC LUT index [25:21] Q DCOC LUT index
0x10	Status 2	32	[31:0] BLE CDR bit count
0x14	Status 3	32	[31:0] LRWPAN CDR bit count
0x18	Status 4	32	[31:0] LO/32 counter
0x1C	General trim 0	8	General trim bits (N/C)
0x1D	General trim 1	8	[0] LO/32 input (external, not implemented)
0x1E	General trim 2	8	General trim bits (N/C)
0x1F	General trim 3	8	General trim bits (N/C)
0x20	General trim 4	8	General trim bits (N/C)
0x21	General trim 5	8	General trim bits (N/C)
0x22	General trim 6	8	General trim bits (N/C)
0x23	General trim 7	8	Debug Enable (0 = debug enable)
0x24	I VGA gain control	10	Manual VGA value if not using I AGC

ADDR	DATA	Size (bits)	Description
0x26	I VGA attenuation reset	1	reset the I AGC
0x27	I VGA attenuation useAGC	1	use I AGC (manual VGA value if not)
0x28	I VGA attenuation sample window	8	I AGC sample window
0x29	I VGA attenuation ideal peak to peak	8	I AGC ideal peak to peak
0x2A	I VGA tolerance peak to peak	8	I AGC peak to peak tolerance
0x2B	I BPF CHP 0 & 1	8	I bandpass filter tuning
0x2C	I BPF CHP 2 & 3	8	I bandpass filter tuning
0x2D	I BPF CHP 4 & 5	8	I bandpass filter tuning
0x2E	I BPF CLP 0 & 1	8	I bandpass filter tuning
0x2F	I BPF CLP 2	4	I bandpass filter tuning
0x30	Q VGA gain control	10	Manual VGA value if not using Q AGC
0x32	Q VGA attenuation reset	1	reset the Q AGC
0x33	Q VGA attenuation useAGC	1	use Q AGC (manual VGA value if not)
0x34	Q VGA attenuation sample window	8	Q AGC sample window
0x35	Q VGA attenuation ideal peak to peak	8	Q AGC ideal peak to peak
0x36	Q VGA tolerance peak to peak	8	Q AGC peak to peak tolerance

ADDR	DATA	Size (bits)	Description
0x37	Q BPF CHP 0 & 1	8	Q bandpass filter tuning
0x38	Q BPF CHP 2 & 3	8	Q bandpass filter tuning
0x39	Q BPF CHP 4 & 5	8	Q bandpass filter tuning
0x3A	Q BPF CLP 0 & 1	8	Q bandpass filter tuning
0x3B	Q BPF CLP 2	4	Q bandpass filter tuning
0x3C	I DCO use	1	toggle using I DCO
0x3D	I DCO reset	1	reset the I DCO
0x3E	I DCO gain	8	set gain for I DCO (unsigned FixedPoint w/ 2 bit binary point)
0x3F	Q DCO use	1	toggle using Q DCO
0x40	Q DCO reset	1	reset the Q DCO
0x41	Q DCO gain	8	set gain for Q DCO (unsigned FixedPoint w/ 2 bit binary point)
0x42	DCOC tuning 1	6	Manual I current DAC for stage 2 VGA value if not using I DCO
0x43	DCOC tuning 2	6	Manual Q current DAC for stage 2 VGA value if not using Q DCO
0x46	MUX debug in	10	Debug configuration, input
0x48	MUX debug out	10	Debug configuration, output
0x4A	Enable RX I	5	Manual enable RX I values {3'b0, mix, buf, vga_s1, vga_s2, bpf}
0x4B	Enable RX Q	5	Manual enable RX Q values {3'b0, mix, buf, vga_s1, vga_s2, bpf}
0x4C	Enable VCO LO	2	Manual enable VCO LO {6'b0, vco_lo, lna}
0x50	LUT command	32	LUT set instruction [3:0] LUT ID [9:4] address (index) [31:10] value
0x54	RX error message	32	Interrupt message, RX error message
0x58	RX finish message	32	Interrupt message, RX finish message
0x5C	TX error message	32	Interrupt message, TX error message

ADDR	DATA	Size (bits)	Description
0x60	FIR command	32	FIR filter reprogramming instruction, [3:0] FIR ID [9:4] coefficient (index) [31:10] value
0x64	I VGA attenuation gain increase	8	I AGC gain increase step size (by LUT index)
0x65	I VGA attenuation gain decrease	8	I AGC gain decrease step size (by LUT index)
0x66	Q VGA attenuation gain increase	8	Q AGC gain increase step size (by LUT index)
0x67	Q VGA attenuation gain decrease	8	Q AGC gain decrease step size (by LUT index)

In order to pass commands to the BM, two 32-bit registers at addresses 0x00 and 0x04 are utilized. The register at 0x04 contains the additional data field for a given command while the register at 0x00 contains the instruction. Writing to the register at 0x00 is the trigger for the BM to execute a given command. Accordingly, **the processor should always write to the additional data register prior to writing to the instruction register for a given command.** The format for a BM instruction and a list of available instructions are detailed below.

Bits	31-8	7-4	3-0
Field	Data	Instruction 2	Instruction 1

List of Commands

Configure Command

Configure baseband constants. The constant is selected using the instruction 2 field and set to the value specified in the additional data field. In the case that the secondary instruction is set to CONFIG_LUT, reference the LUT addresses provided in the explanations below/

Field	Data	Instruction 2	Instruction 1
Value	X unless CONFIG_LUT, then LUT address	See table	0

Field	Additional Data
Value	Value for the constant to be set to

Instruction 2	Name
0x0	CONFIG_RADIO_MODE
0x1	CONFIG_CRC_SEED

Instruction 2	Name
0x2	CONFIG_ACCESS_ADDRESS
0x3	CONFIG_SHR
0x4	CONFIG_BLE_CHANNEL_INDEX
0x5	CONFIG_LRWPAN_CHANNEL_INDEX

Configuration instruction descriptions

(0x0) CONFIG_RADIO_MODE

Specify the following in the Additional Data register (0x04) prior to issuing the instruction 0: Set the radio transceiver mode to Bluetooth Low Energy 1: Set the radio transceiver mode to IEEE 802.15.4 LR-WPAN Valid in any radio mode.

(0x1) CONFIG_CRC_SEED

Set the CRC (cyclic redundancy check) seed for the BLE and LR-WPAN CRC circuits to the value in the Additional Data register (0x04). This value changes for BLE and should be 0 for LR-WPAN

(0x2) CONFIG_ACCESS_ADDRESS

Set the BLE Access Address for the BLE uncoded packet. This value must be provided by the CPU. More information may be found in the BLE Baseband section. NOTE: An access address of 0xFFFFFFFF6 disables whitening of transmitted BLE packets

(0x3) CONFIG_SHR

Set the LRWPAN SHR to match with for receiving a LRWPAN packet. This value must be provided by the CPU. According to 802.15.4 spec, it should be a fixed value of 0xA700 (only 2 bytes are matched due to lower hardware cost), but is programmable for flexibility.

(0x4) CONFIG_BLE_CHANNEL_INDEX

Values for the channel index can range from 0 to 39, corresponding to BLE channel frequencies beginning at 2402 MHz until 2480 MHz. It is critical to note that the channel index from 0 to 39 is a direct mapping to channel frequencies - NOT the BLE channel numbering scheme that considers advertising channels separately.. For example, setting CONFIG_BLE_CHANNEL_INDEX to 0 will result in a transmission with center frequency at 2402 MHz. This corresponds to BLE channel 37. More information: <https://www.rfwireless-world.com/Terminology/BLE-Advertising-channels-and-Data-channels-list.html>

(0x5) CONFIG_LRWPAN_CHANNEL_INDEX

Values for the channel index can range from 0 to 15, corresponding to LR-WPAN channel frequencies beginning at 2405 MHz until 2480 MHz.

Send Command

Transmit a specified number of PDU header and data bytes. Bytes are retrieved by the BM by loading them from the specified address.

Field	Data	Instruction 2	Instruction 1
Value	Number of bytes	X	1

Field	Additional Data
Value	Load address

Receive Enter Command

Place the device into receive mode. If a message is picked up, it will be stored starting at the specified address address.

Field	Data	Instruction 2	Instruction 1
Value	X	X	2

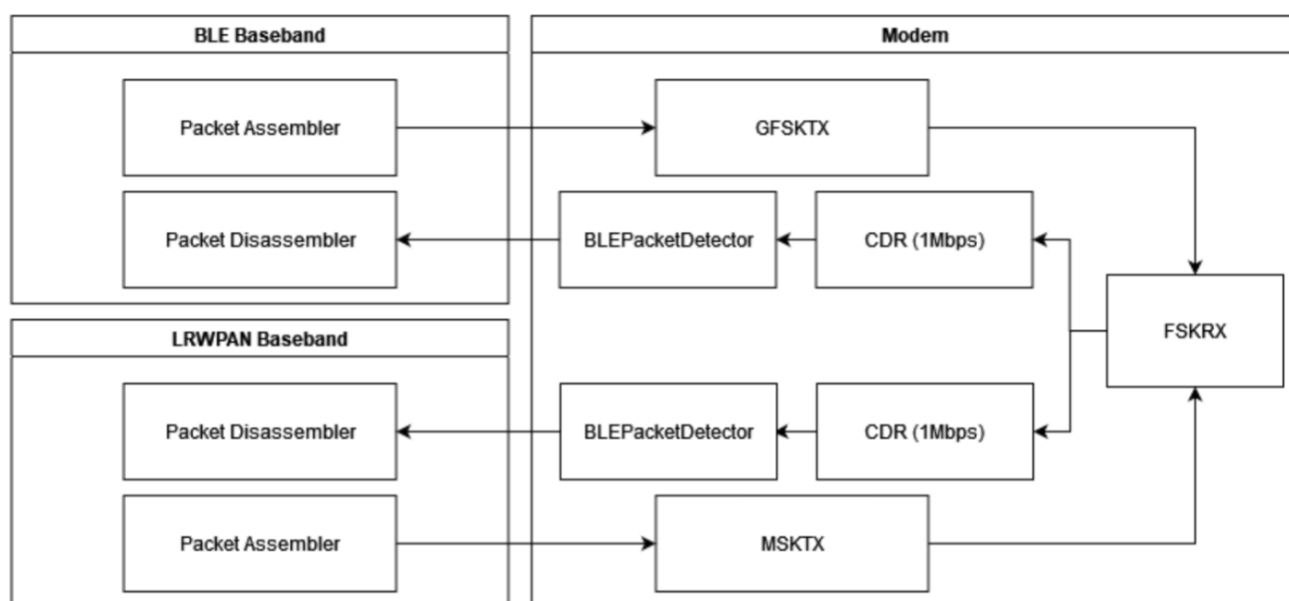
Field	Additional Data
Value	Storage address

Receive Exit Command

Exit the device from receive mode. This command will succeed as long as the device has not yet matched an instruction preamble.

Field	Data	Instruction 2	Instruction 1
Value	X	X	3

Field	Additional Data
Value	X



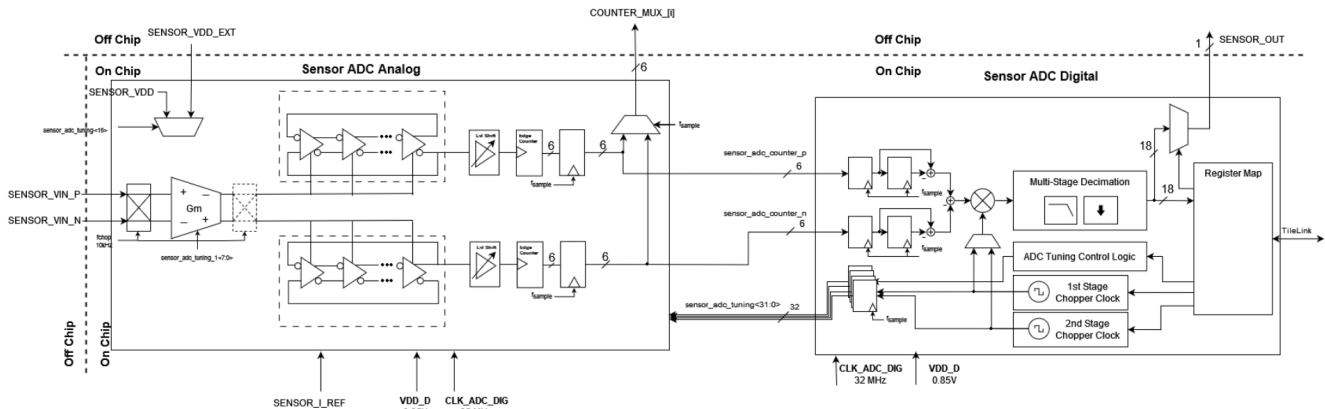
7. 2.4 GHz Transceiver Analog Frontend

8. 94 GHz FMCW Radar

How does the debug architecture work here? Is there any digital control?

9. uV-Precision Sigma-Delta ADC

9.1. System-level Diagram and Description



9.2. Analog Front-End

Input impedance? Mins and maxs?

9.3. Digital Signal Processing

The sigma-delta ADC's DSP chain is implemented as a cascaded integrator comb (CIC) decimation filter for noise shaping. The key CIC filter parameters for this design are $N=4$, $R=8000$, $M=1$

The digital frontend features self-generated, software-programmable chopper clock generators for 1st and 2nd stage choppers. A digital de-chopper/mixer with configurable clock delay to match delay of the analog front-end is also implemented.

9.4. Register Map

Register	Name	Size	Function
0x00	ADC_STATUS	32	ADC_STATUS<11:6> - ADC Counter P ADC_STATUS<5:0> - ADC Counter N
0x04	ADC_DATA	20	Read ADC sample from FIFO
0x08	ADC_TUNING_0	8	ADC_TUNING_0<5:0> - Current DAC ADC_TUNING_0<6> - BIAS P + ADC_TUNING_0<7> - BIAS N
0x09	ADC_TUNING_1	8	Reserved
0x0A	ADC_TUNING_2	8	ADC_TUNING_2<0> - Sensor VDD mux select
0x0B	ADC_TUNING_3	8	ADC_TUNING_3<7:0> - Reserved
0x0C	ADC_CHOP_CLK_DIV_1	32	1st stage chopper clock divider

Register	Name	Size	Function
0x10	ADC_CHOP_CLK_DIV_2	32	2nd stage chopper clock divider
0x14	ADC_CHOP_CLK_EN	2	ADC_CHOP_CLK_EN<0> - Enable 1st stage chopper ADC_CHOP_CLK_EN<1> - Enable 2nd stage chopper
0x18	ADC_DSP_CTRL	8	ADC_DSP_CTRL<0> - Enable dechopper in DSP chain ADC_DSP_CTRL<1> - Select chopper clock used in the dechopper ADC_DSP_CTRL<5:2> - Dechopping clock delay, from 0 to 15 cycles

10. Electrical Characteristics

Include tables or descriptive text for various electrical characteristics...

11. Usage Scenarios

Describe various application scenarios, operating modes, etc.

12. Revision History

- v1.0 - Initial release
- v0.9 - Preliminary draft

13. Appendix

Additional details, references, or supplementary material...