EE251B Advanced Digital Integrated Circuits **Spring 2022.**

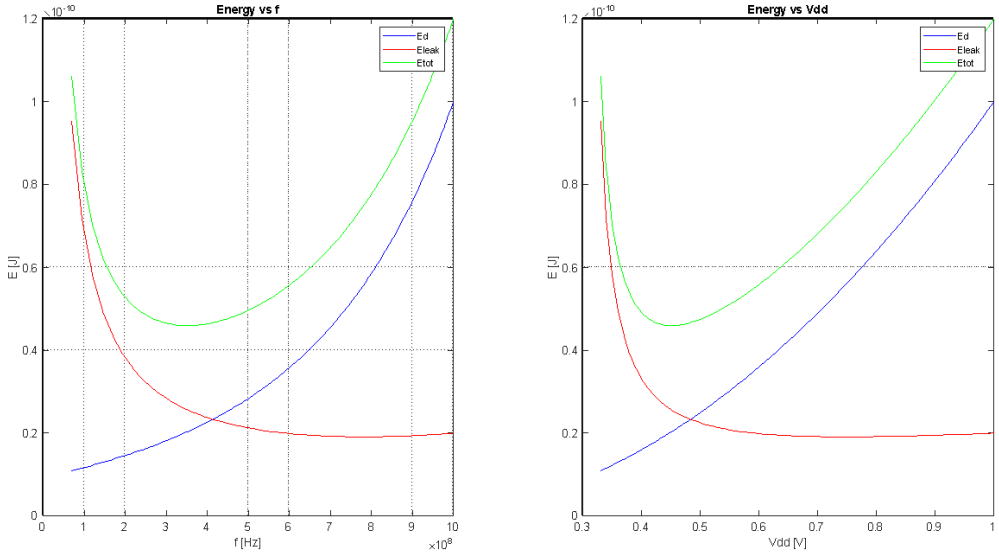
HOMEWORK 4. **Due: Friday, April 22, 2022.**

This is an individual assignment!

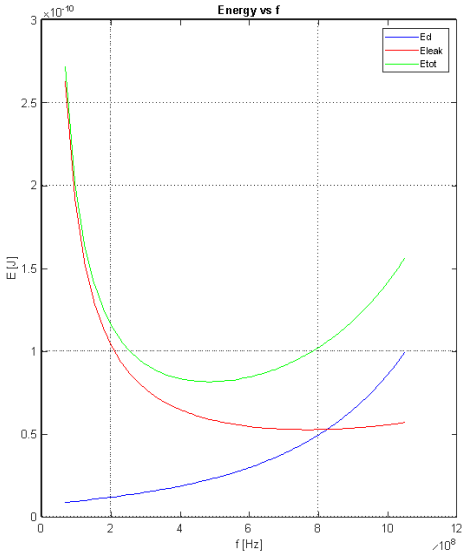
1. DVFS and Leakage

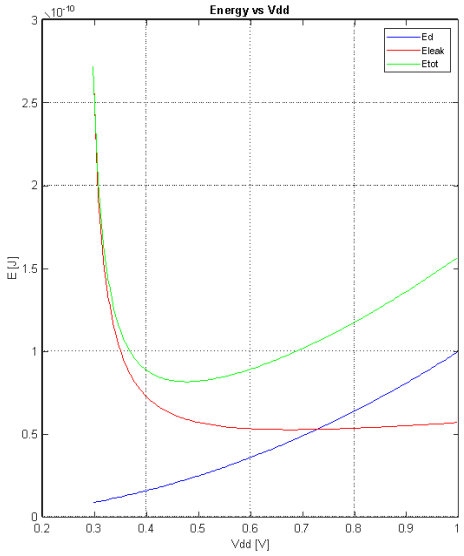
Plot the leakage energy, dynamic energy and total energy per clock cycle for a digital block with specifications listed below and determine the operational frequency and supply voltage that lead to minimum total energy per clock cycle, for SS, TT and FF corners.
Block parameters are:
Ceff = 100pF (effective switching capacitance of the digital block)
Vdd,nom = 1V
Vth_tt = 0.3V, Vth_ff = 0.27V, Vth_ss = 0.33V
Assume that the leakage power is 20% of the dynamic power at nominal clock frequency of 1GHz at Vdd,nom in TT corner, and that leakage current is 3x higher in FF corner and 3x smaller in SS corner. You can also assume that the DVFS controller scales the clock frequency ~$(Vdd-Vth)^{1.2}/Vdd$.

Solution:
TT:

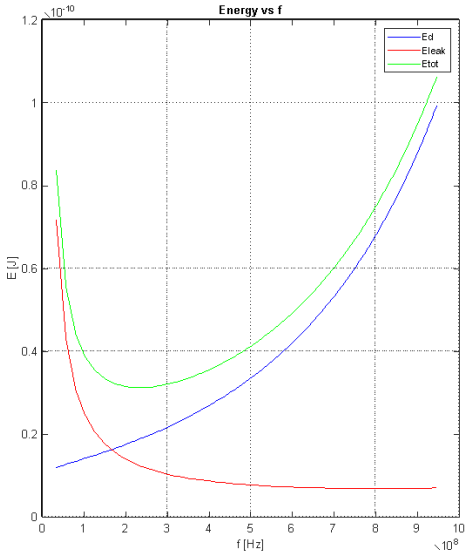


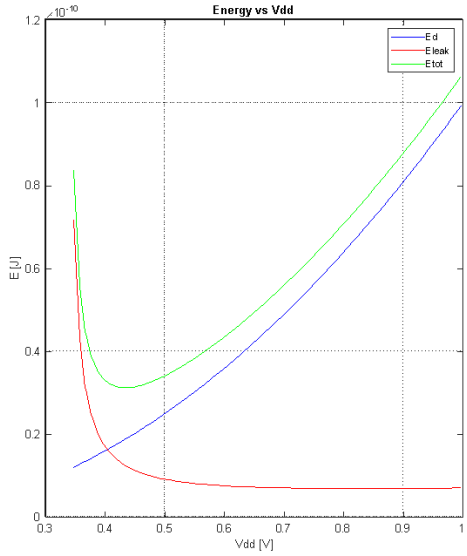
FF:





SS:






```
close all; clear all;
Ceff = 100e-12;
Vdd_nom = 1;
Vth_nom = 0.3;
Vth = 0.33; % 0.33, 0.3
corner_factor = 1/3; % 1/3, 1
f_nom = 1e9;
leak_factor = 0.2*corner_factor;
Vdd = (1.05*Vth):0.01:Vdd_nom;
f = f_nom.*((Vdd-Vth).^1.2./Vdd)./((Vdd_nom-Vth_nom).^1.2./Vdd_nom);
Ed = Ceff*Vdd.^2;
Ileak_nom = leak_factor*f_nom*Ceff*Vdd_nom;
Eleak = Ileak_nom.*Vdd./f;
```

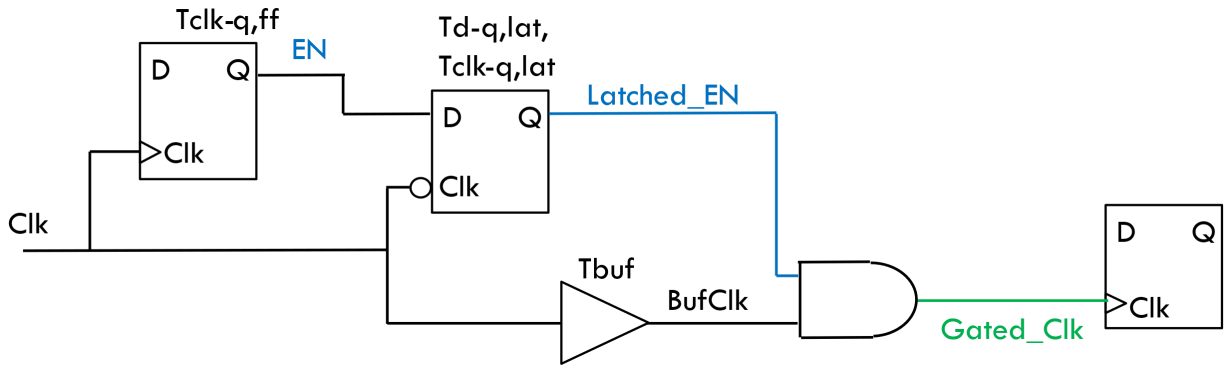
```
Etot = Ed + Eleak;

figure(1)
subplot(1,2,1)
plot(f,Ed,'b-',f,Eleak,'r-',f,Etot,'g-');
grid on;
title("Energy vs f");
xlabel("f [Hz]"), ylabel("E [J]");
legend("Ed","Eleak","Etot");

subplot(1,2,2)
plot(Vdd,Ed,'b-',Vdd,Eleak,'r-',Vdd,Etot,'g-');
grid on;
title("Energy vs Vdd");
xlabel("Vdd [V]"), ylabel("E [J]");
legend("Ed","Eleak","Etot");
```

Problem 2. Clock gating

In the clock gating scheme below, define the required relationship of the listed flip-flop, latch and buffer delay parameters and clock cycle Tclk in order to avoid the glitching on the Gated_Clk signal.
Draw a timing diagram for the case that violates this relationship causing the glitching in Gated_Clk.



Solution:
Tbuf < Tclk-q, lat
Tclk-q,ff < Tclk/2

Problem 3. Power Gating

Digital block has the following parameters:
C_{eff} = 100pF (effective switching capacitance)
C_{rail} = 200pF (supply rail capacitance)
$I_{peak,dyn}/I_{avg,dyn}$ = 10 (peak to average current ratio)
I_{leak} = 20% Iavg,dyn (leakage current is 20% of average dynamic switching current)
fnom = 1GHz
$V_{dd,nom}$ = 1V

a) Design a power gate that has a maximum voltage droop of 5% of $V_{dd,nom}$. Assume that $R_{on,n} = R_{on,p} = 1kOhm\mu m$.
b) Determine the energy pulled from the supply to switch the power gate. Assume Cg = 1fF/µm
c) Determine the energy discharged from the block after the power gate is turned off. Assume that the supply rail capacitance is the capacitance of the virtual (i.e. gated supply rails).
d) Determine the minimum off time for the block at which the leakage savings break even with the energy required to switch the power gate and re-charge the virtual rails.

Solution:

a) $I_{peak,dyn} = 10*f_{nom}*Ceff*Vdd_{nom}^2 = 1A$
$Ileak = 0.2*0.1A = 0.02A$
$dV = 50mV \Rightarrow R_{pg} = dV/(I_{peak,dyn} + I_{leak}) = 49mOhm$
$W_{pg} = R_{on,p}/R_{pg} = 20400\mu m$

b) $E_{pg} = W_{pg}*C_g*V_{dd,nom}^2 = 20.4pJ$

c) $E_{discharged} = Erail + Epg,d + Elogic = 0.5*(Crail + Cd,pg + Ceff)*Vdd,nom^2 = 160.02pJ$

d) $E_{re\text{-}charge} = 2*E_{discharged} = 320.04pJ$
$T_{off,min} = E_{re\text{-}charge}/(I_{leak}*V_{ddnom}) = 16.002ns$