

**HOMEWORK 1.****Due: Friday, March 4, 2022.****This is an individual assignment!****1. System interconnect**

You have been tasked with building a system-interconnect for a system-on-chip with 256 processing cores. You are considering several options for the on-chip system interconnect network: (1) a 16-ary 2-mesh, (2) a 16-ary 2-cube, (3) an 8-ary 2-Cmesh4 and (4) 16-ary 3-fly Clos. The application requires a packet size of 1024 bits.

- a) Calculate the required number of bits per unidirectional channel, for each network option, such that each of the networks can support the ideal throughput of 64 bits/cycle/core under uniform random traffic.
- b) Show the worst-case zero-load latency breakdown for each interconnect network.  
Assume the flit size of 64b and shortest (core-to-core) channel latency of 1 cycle. For Clos, assume that the middle stages are located at the center of the chip.

**2. Transistor sizing**

In this problem, we will explore optimal transistor sizing.

- a) By using SPICE and 7nm RVT model with 0.7V supply, find the required width of the PMOS transistor that minimizes the propagation delay  $(t_{pHL} + t_{pLH})/2$  for the CMOS inverter. NMOS transistor width is fixed at 100nm. We will call this an optimally or symmetrically sized inverter.
- b) Find the intrinsic delay of this inverter,  $p$ . It is set by the ratio of diffusion to gate capacitances, but it is better to find it from the delay measurements with varying fanout.
- c) What is the optimal inverter fanout in this technology? Is it close to the expected value?
- d) Optimally size the CMOS NAND2 gate. Find the required width ( $W$ ) for the NMOS transistors in the pull-down, such that the equivalent resistance of the pull-down network is the same as the equivalent resistance of the pull down transistor in an inverter from part a). Use hand analysis with parameters from Problem 1. (In case you haven't been able to solve Problem 1, you can use  $E_C L = 0.7V$ ,  $V_{DD} = 0.7V$ , and  $V_{Th} = 0.2V$ ). Compare with SPICE and discuss any discrepancies.
- e) Find the logical effort and the intrinsic delay of the NAND2 gate from part c).
- f) Now find a library cell for the NAND2 gate in the class standard cell library. Find the logical effort and the intrinsic delay from the .lib file.
- g) Repeat part c) for a NAND3 gate. Compare with SPICE and discuss any discrepancies. Find the logical effort of this gate.

- h) Optimally size NOR2 gate by using SPICE to match the inverter from part a). Find the logical effort.