① $\frac{W}{L} = 12$

$V_{DD} = 0.75\,V$

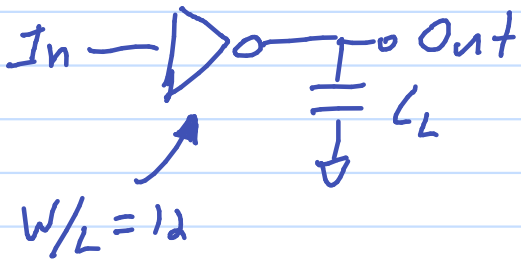
$C_g = C_d = 2fF/\mu m$

$V_{tn} = |V_{tp}| = 0.3V$

$t_{FO4} = 12ps$

a) Let's find the delay of both scenarios and set them equal and solve for C_L.

First, the single inverter scenario:



We know that delay is $d = t_{p0}\left(\frac{gh}{\gamma} + p'\right)$ and we can assume $\gamma \simeq 1$. For an inverter, we also know that $g = 1$ and $p' = 1$ such that

$$d_{1\text{-}inv} = t_{p0}\left(\frac{1 \cdot h}{1} + 1\right) = t_{p0}(h+1)$$

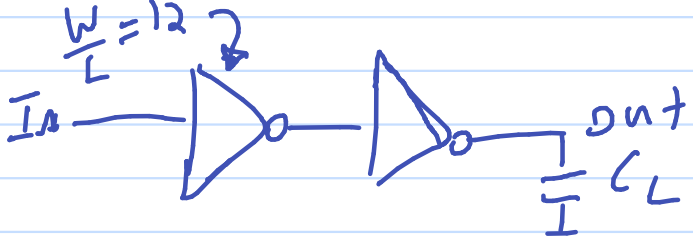
The path fanout, F, will not change for the two scenarios and thus we can express the delay in terms of F which is $\frac{C_L}{C_{in}}$.

$$d_{1\text{-}inv} = t_{p0}(F+1)$$

Inverter fanout h is same as path fanout F in this case

① cont...

Now solve for the delay for 2 inverters!



Important to note that the first inverter's size does not change!

We know that we have the same path fanout F and that to get minimum delay through this path we should have $\sqrt{F}$ fanout for each inverter.

$$d_{2\text{-inv}} = t_{p_0}(\sqrt{F}+1) + t_{p_0}(\sqrt{F}+1)$$

$$d_{2\text{-inv}} = 2t_{p_0}(\sqrt{F}+1)$$

Now we can solve for F that makes $d_{2\text{-inv}}$ smaller than $d_{1\text{-inv}}$.

$$d_{2\text{-inv}} < d_{1\text{-inv}}$$

$$2t_{p_0}(\sqrt{F}+1) < t_{p_0}(F+1)$$

$$2\sqrt{F}+2 < F+1$$

$$2\sqrt{F} < F-1$$

squaring both sides adds additional erroneous solution for F

$$4F < F^2-2F+1$$

$$F^2-6F+1 > 0$$

$$F = 5.83, 0.17$$

Doesn't satisfy original inequality

(1) cont...

Now we know $F = \frac{C_L}{C_{in}} = 5.83$.

For any F larger than this it makes sense to use 2 inverters.

To get C_L we solve for C_{in}

$$C_{in} = (2 \text{ tran/inverter})(2 fF/\mu m) W_1$$

W_1 is the width of the first inverter.

We know that $\frac{W}{L} = 12$ and that $L = 20nm$ for a min-sized transistor in the ASAP7 process.

$$C_{in} = (2)(2 fF/\mu m)(12 \times 20nm)$$

$$C_{in} = 0.96 fF$$

And now we can calculate C_L

$$C_L = 5.83 \cdot 0.96 fF \approx 5.6 fF$$

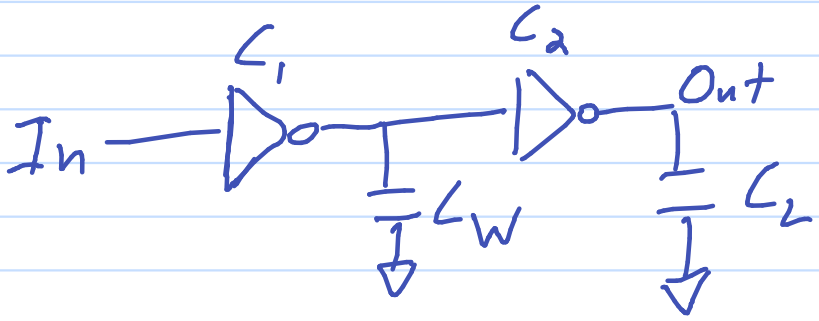
For any $C_L > 5.6 fF$ we get a smaller delay for 2 inverters than for 1 inverter

(1) cont...

b) $C_1 = 1.5\,fF$

$C_w = 1\,fF$

$C_L = 17.5\,fF$



First, write out the delay from in to out using the method of logical effort.

$$d_{abs} = t_{p0}\left(\frac{C_2 + C_w}{C_1} + 1\right) + t_{p0}\left(\frac{C_L}{C_2} + 1\right)$$

$$d_{abs} = t_{p0}\left(2 + \frac{C_2 + C_w}{C_1} + \frac{C_L}{C_2}\right)$$

Now take the derivative of the delay w/ respect to C_2 and set it to 0.

$$\frac{d\,d_{abs}}{dC_2} = \frac{d}{dC_2}\left(t_{p0}\left(2 + \frac{C_2 + C_w}{C_1} + \frac{C_L}{C_2}\right)\right) = 0$$

$$t_{p0}\left(\frac{1}{C_1} - \frac{C_L}{C_2^2}\right) = 0$$

(1) cont...

$$\frac{1}{C_1} - \frac{C_L}{C_2^2} = 0$$

Now solve for C_2

$$\frac{C_L}{C_2^2} = \frac{1}{C_1}$$

$$C_2^2 = C_L \cdot C_1$$

$$\boxed{C_2 = \sqrt{C_L \cdot C_1}}$$

The second inverter's fanout is then $\frac{C_L}{\sqrt{C_L \cdot C_1}}$

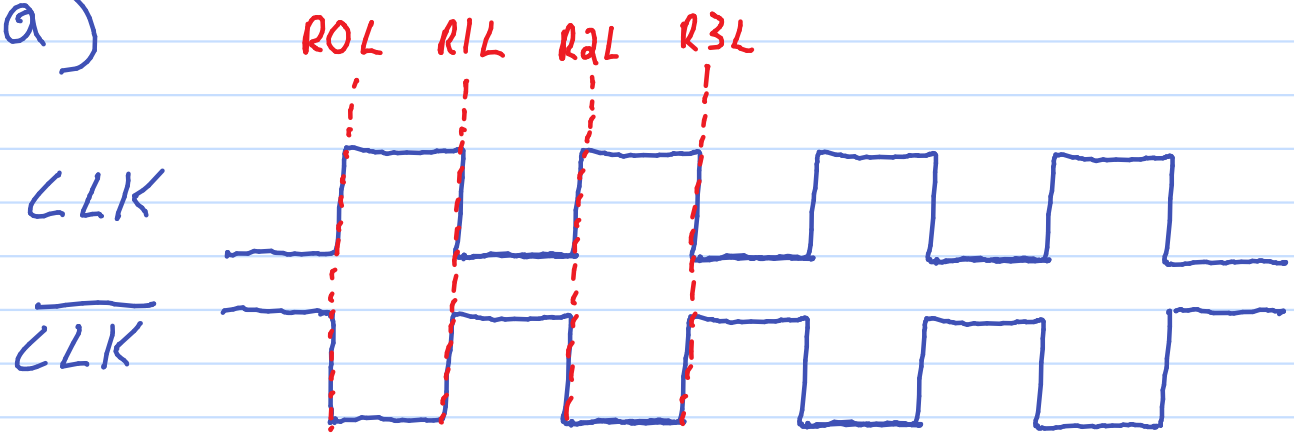
This is the same result as if C_w was not there. I.e. $h_2 = \sqrt{F} = \sqrt{\frac{C_L}{C_1}} \cdot \frac{\sqrt{C_L}}{\sqrt{C_L}} = \frac{C_L}{\sqrt{C_L C_1}}$

This is intuitive only because we are optimizing only the second inverter while the first inverter is fixed. C_w adds a static delay that cannot be optimized for by sizing only the second inverter.

(2) $t_{s1} = 600ps$ $t_{s2} = 400ps$ $t_{s3} = 550ps$

$t_{rQL} = t_{DQL} = t_{suL} = 150ps$ $t_{cQR} = 100ps$

a)



Let's list out all timing arcs

R0 → R1

$T_{min} = t_{cQR} + t_{s1} + t_{suL} = 100ps + 600ps + 150ps = 850ps$

R1 → R2

$T_{min} = t_{DQL} + t_{s2} + t_{suL} = 150ps + 400ps + 150ps = 700ps$

R2 → R3

$T_{min} = t_{DQL} + t_{s3} + t_{suL} = 150 + 550ps + 150ps = 850ps$

R2 → R1

$T_{min} = t_{DQL} + t_{s1} + t_{suL} = 150ps + 600ps + 150ps = 900ps$

$R_2 \rightarrow R_1$ is the longest timing arc. This will use a full period w/ slack borrowing thus

$$\boxed{T_{min} = 900ps}$$

(2)

b) First, express delay as a function linearly dependent on the inverse of I_{on} (as I_{on} increases delay decreases and vice versa).

Made up factor →

$$\text{Delay} = \frac{\alpha}{I_{on}} = \frac{\alpha}{k(V_{DD} - V_{thz})}$$

Now we know that the ratio of the max delay to the nominal delay is 1.15 as this represents a 15% increase.

$$\frac{\text{Delay}_{max}}{\text{Delay}_{nom}} = 1.15$$

Now replace delay w/ its definition above and solve for $V_{thz,max}$.

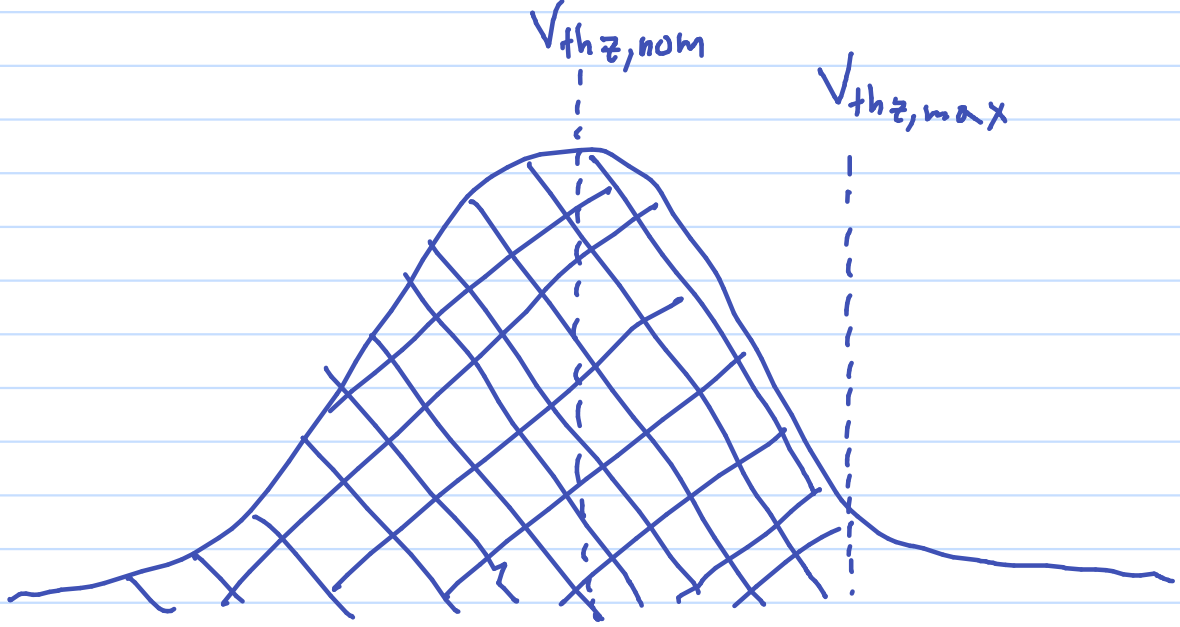
$$\frac{\text{Delay}_{max}}{\text{Delay}_{nom}} = \frac{\cancel{\alpha}}{\cancel{k}(V_{DD} - V_{thz,max})} \cdot \frac{\cancel{k}(V_{DD} - V_{thz,nom})}{\cancel{\alpha}}$$

$$\frac{V_{DD} - V_{thz,nom}}{V_{DD} - V_{thz,max}} = 1.15$$

$$V_{thz,max} = V_{DD} - \frac{V_{DD} - V_{thz,nom}}{1.15} = 0.36\,V$$

(2)

c) $\sigma = 0.05\ V$
$\mu = 0.3\ V$
} ← V_{thz} normally distributed

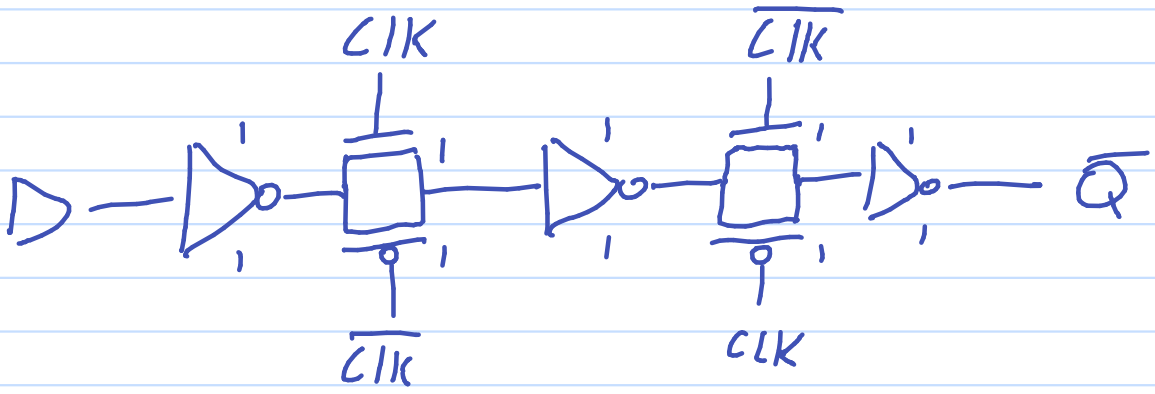


The yield is the percentage of transistors that have $V_{thz} < V_{thz,max}$. This can be found by computing the z-score and using a z-score table.

$$z = \frac{V_{thz,max} - \mu}{\sigma} = \frac{0.36 - 0.3}{0.05} = 1.2$$

From the z-score table the yield is 88.5%

(3)



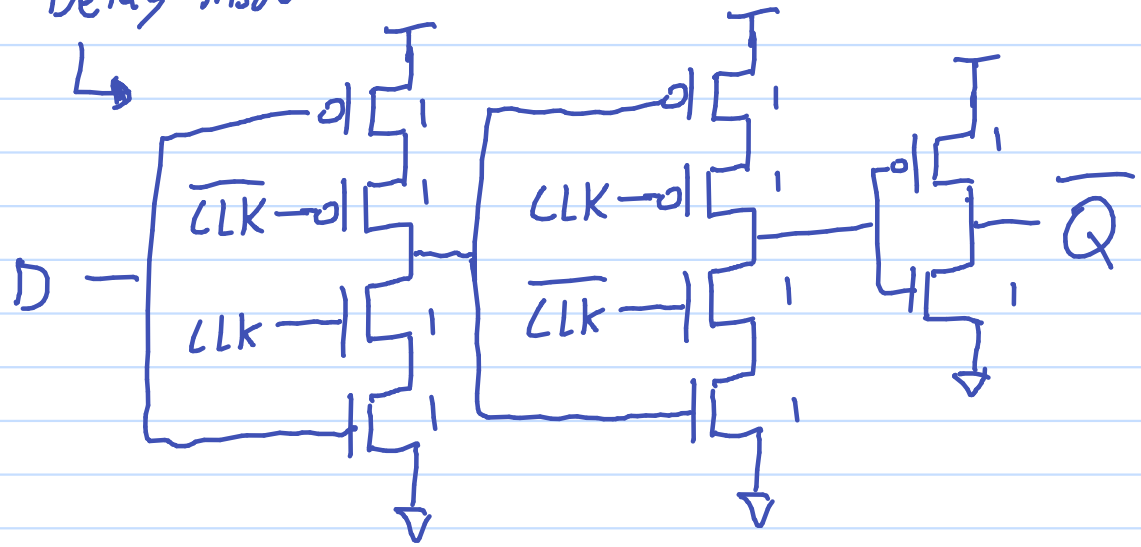
$C_g = C_d = 1fF$

$R_{on} = 2.5K\Omega$

a) The second pass gate is on when clock is low thus this flip-flop is <u>negatively edge triggered</u>

b) We can simplify the problem by translating the inverters followed by pass gates into C^2MOS gates

Delay model



(3)

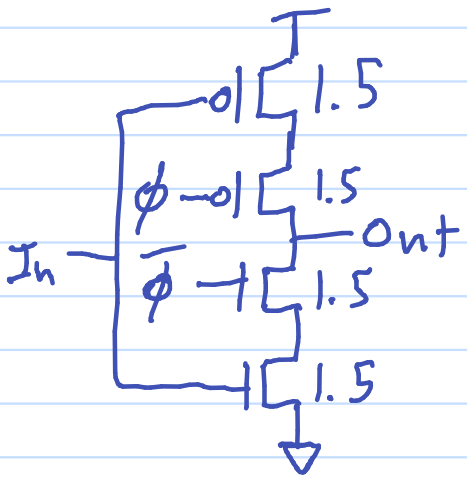
CLK-$\bar{Q}$ delay assumes that the the inpnt of the second latch is already fully charged/discharged before CLK's falling edge. This delay then becomes the delay through the 2nd C²MOS gate plus the delay through the last inverter

$$d_{c\bar{q}} = d_{c^2mos} + d_{inv}$$

$$d_{c\bar{q}} = t_{po}(g_{c^2mos} h_{c^2mos} + p_{c^2mos}) + t_{po}(g_{inv} h_{inv} + p_{inv})$$

To find g & p we have to know that the stack of 2 transistors requires 1.5x width to get same res as single transistor

Template C²MOS



Important Note

0→1 transition means that we need to consider the ϕ input when looking at the delay through this gate. 1→0 transition would force us to also consider the delay to generate $\bar{\phi}$ when looking at CLK-to-$\bar{q}$ delay

$$g_\phi = \frac{C_t}{C_{inv}} = \frac{1.5C_g}{2C_g} = 0.75$$

$$p_\phi = \frac{C_{pt}}{C_{pinv}} = \frac{3C_d}{2C_d} = 1.5$$

(3)

Now we can plug in our values to get the delay

Assume unloaded output inverter

$$d_{c\text{-}\bar{q}} = t_{p_0}\left((0.75)\left(\frac{2C_g}{1.5C_g}\right)+1.5\right) + t_{p_0}\left(1.0^{d}+1\right)$$

$$d_{c\text{-}\bar{q}} = t_{p_0}(1+1.5) + t_{p_0}(1)$$

$$\boxed{d_{c\text{-}\bar{q}} = 3.5\,t_{p_0}}$$

We can approximate $t_{p_0} \simeq 0.7 R_{inv} C_{p\text{-}inv}$

$$t_{p_0} = 0.7(2.5k\Omega)(2\cdot 1fF)$$

2x drain cap for min inverter

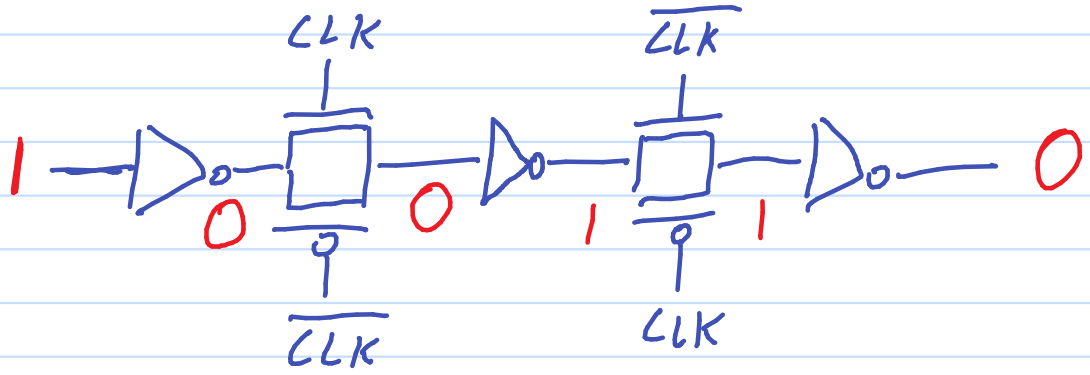
$$\boxed{t_{p_0} \simeq 3.5ns}$$

Now we can plug this in and get

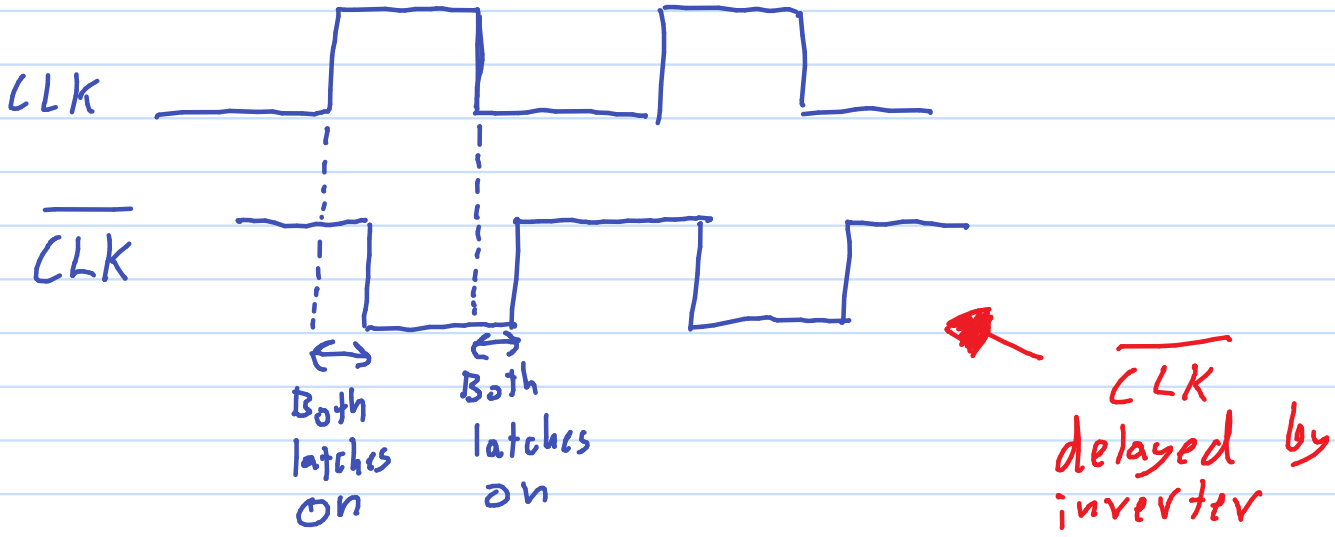
$$\boxed{d_{c\text{-}\bar{q}} \simeq 12.25\,ns}$$

3

c) Let's draw out the circuit for D=1



The logic levels throughout the circuit are annotated in red. After either edge of the clock there is a brief period where a single conductive path exists from D to $\overline{Q}$



The period where both latches are on is the same for D=1 and D=0 and is equal to the delay through a single inverter.

$$t_{hold} = d_{inv} = t_{p_0}(gh+p') = 3.5\,ns\,((1)(\tfrac{1}{4})+1) = 5.25\,ns$$