EE241B HW1 Solution (Spring 2021)

1 Models

Instructor's grading note: since it was unclear in the problem and on Piazza, the required W of 100nm as specified in the problem is technically not achievable. By examining the model card, the width of 1 fin is 27nm, which means the W parameter doesn't do anything and 4 fins = 108nm would be the closest value. For the following solutions, the default of 1 fin was used, so the values for 4 fins would be different but full credit is given for the correct analysis methodology rather than the final numbers.

a) V_{TH} by Extrapolation

The following plots PMOS and NMOS I_{DS} vs V_{GS} for low V_{DS} = 100mV. V_{TH} is found by linear extrapolation about the point of maximum g_m and finding the intercept with the x-axis.

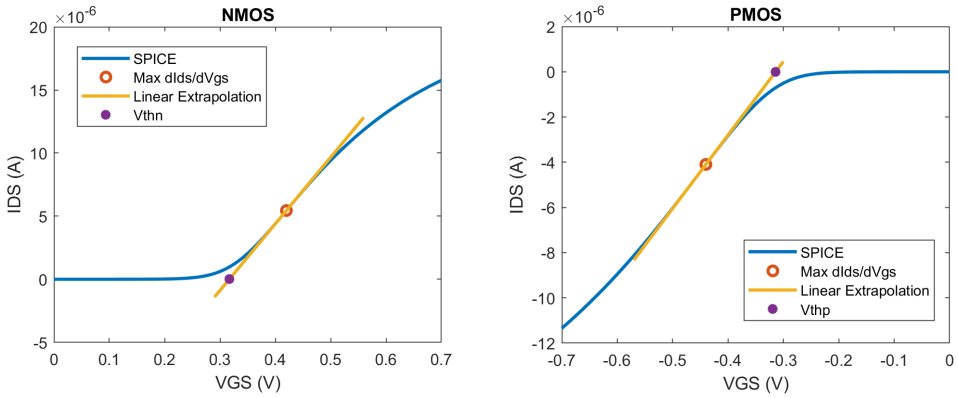
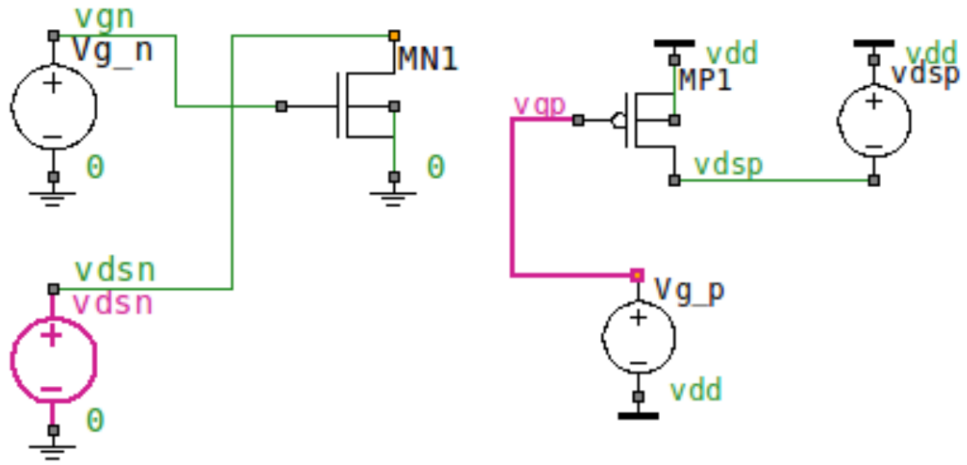


Figure 1: $\boldsymbol{V_{THN} = 317mV}$; $\boldsymbol{V_{THP} = -314mV}$

The DC operating points from simulation (using `.op`) are 332mV and -307mV for NMOS and PMOS respectively (4.7% and 2.2% error respectively). The device setup is shown below (NMOS left, PMOS right).

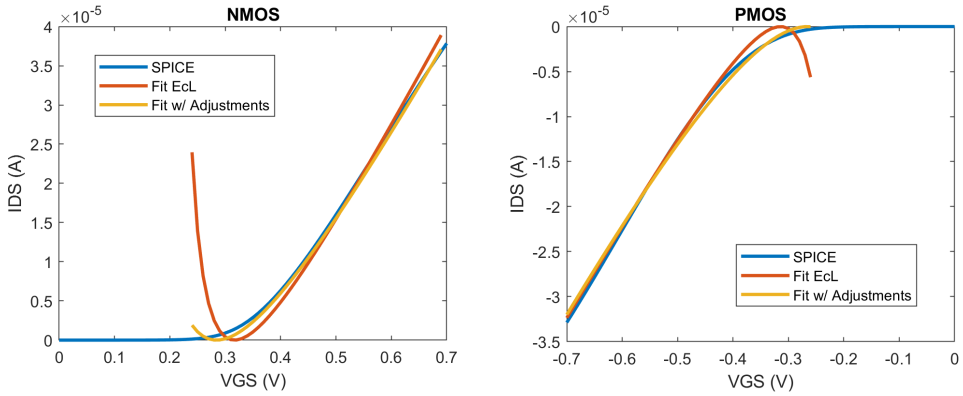


b) E_CL Fit

Here we fit to:

$$I_{DSAT} = \frac{W}{L}\frac{\mu C_{ox} E_C L}{2}\frac{(V_{GS}-V_{TH})^2}{(V_{GS}-VTH)+E_CL} = \frac{\beta}{2}\frac{(V_{GS}-V_{TH})^2}{(V_{GS}-VTH)+E_CL}$$

$\beta = \frac{W}{L}\mu C_{ox}$ can be extracted from SPICE by probing the `lv21` parameter. For this part (and the rest of the parts in this problem), $V_{DS} = 0.7$V so that the short channel effects can be observed.
Using MATLAB's `lqscurvefit` is reportedly highly variable depending on the starting input values, and making β and V_{TH} free variables gets better fits with this method. Other students have much better fitting with Python's `scipy.optimize.curve_fit`. **Note: it is imperative to fit only in the region of $V_{GS} > V_{TH}$.**
The fitting results are below for β and V_{TH} not free and as free parameters in Matlab:



Fitting just E_CL:
$$\boldsymbol{E_CL_n = 100mV} \text{ ; } \boldsymbol{E_CL_p = 110mV}$$

Fitting E_CL, V_{TH}, and β:
$$\boldsymbol{E_CL_n = 180mV},\ \boldsymbol{V_{THN} = 284mV},\ \boldsymbol{\beta_n = 1.5m}$$
$$\boldsymbol{E_CL_p = 262mV},\ \boldsymbol{V_{THP} = -266mV},\ \boldsymbol{\beta_p = 0.9m}$$

c) I_{DSat} Ratio

Plug the new length into the equation from part b.

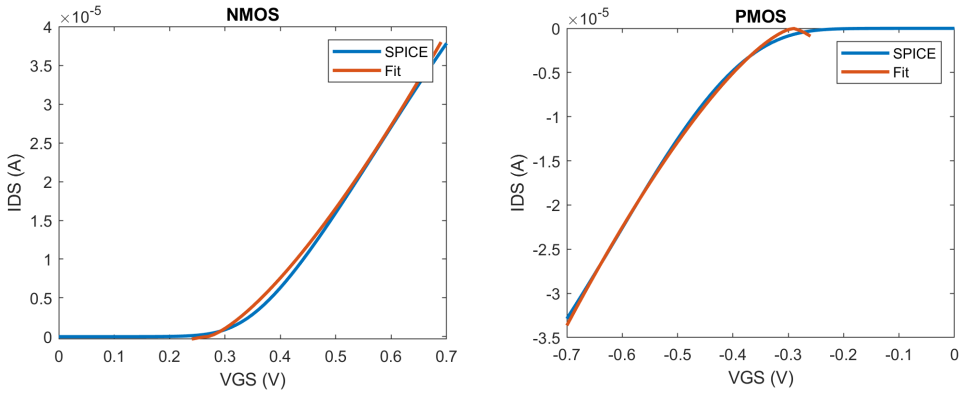
$$\frac{I_{DSat2L}}{I_{DSatL}} = \frac{W}{2L}\frac{u_{eff}C_{ox}E_C 2L}{2}\frac{(V_{GS}-V_{TH})^2}{(V_{GS}-V_{TH})+E_C 2L} * \frac{L}{W}\frac{2}{u_{eff}C_{ox}E_CL}\frac{(V_{GS}-V_{TH})+E_CL}{(V_{GS}-V_{TH})^2}$$
$$\frac{I_{DSat,2L}}{I_{DSat,L}} = \frac{(V_{GS}-V_{TH})+E_CL}{(V_{GS}-V_{TH})+E_C2L}$$

For $(V_{GS}-V_{TH}) >> E_CL$ as in short channel devices like ASAP7,

$$\boldsymbol{\frac{I_{DSat,2L}}{I_{DSat,L}} \approx 1}$$

d) K, V_{TH}, α Fit

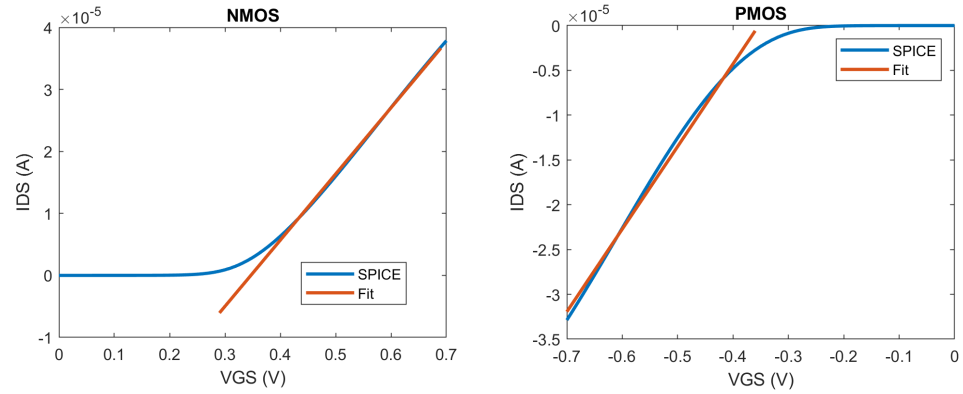
Fitting to $I_{DSAT} = K(V_{GS}-V_{TH})^{\alpha}$ with `lsqcurvefit`:



For NMOS: $\boldsymbol{K = 1.26 * 10^{-4}}$,$\boldsymbol{V_{TH} = 268mV}$, $\boldsymbol{\alpha = 1.39}$
For PMOS: $\boldsymbol{K = 1.21 * 10^{-4}}$, $\boldsymbol{V_{TH} = -292mV}$, $\boldsymbol{\alpha = 1.43}$

e) V_{TH}, Fit for $\alpha = 1$

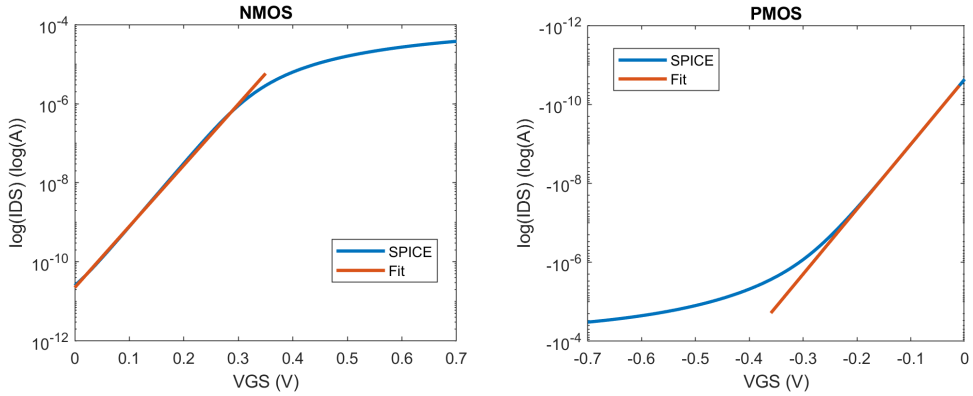
Fitting to $I_{DSAT} = K(V_{GS} - V_{TH})$ with `lsqcurvefit`:



For NMOS: $\boldsymbol{K = 1.07 * 10^{-4}}$,$\boldsymbol{V_{TH} = 347mV}$
For PMOS: $\boldsymbol{K = 9.22 * 10^{-5}}$, $\boldsymbol{V_{TH} = -354mV}$

f) Subthreshold Slope

Fitting to $log(I_{DSat})$ vs V_{GS} in the subthreshold region:.



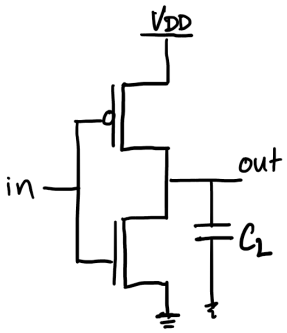
NMOS Subthreshold slope: **64.7mV/dec**
PMOS Subthreshold slope: **-60.7mV/dec**

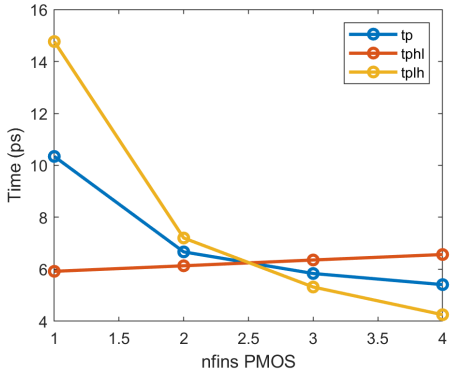
2 Transistor Sizing

a) Inverter Sizing

The testbench should have an NMOS of fixed fin count and a PMOS of variable fin count. A step or pulse source should be injected with the delay measured by SPICE for both transition edges.

Starting with a 2-fin NMOS, 1fF loading, and 1ps input transition time, an equal tp occurs at a ratio of 2:2.5. This is close to a **1:1 ratio**. In general, with other values of the fixed NMOS fins, the resulting 1:1 ratio is also achieved. Note that the propagation delay is as low as **just under 2ps** with much lower





output capacitance.

b) Inverter Intrinsic Propagation Delay

Simulating the 2-fin inverter with no load, $t_{pHL} = 911fs$, $t_{pLH} = 949fs$, and $t_p = 930fs$.

c) Optimum Inverter Fanout

To find the optimal fanout, use the equation:

$$f_{opt} = e^{1+\frac{\gamma}{f_{opt}}}$$

Finding γ requires two measurements: 1) $delay_1$ = the delay from a FO1-loaded 2 fin inverter, and 2) $delay_2$ = the intrinsic propogation delay above:

$$\begin{aligned} delay_1 &= ln2R_{eq}C_{inv}(\gamma + \frac{C_{inv}}{C_{inv}}) = 1.91ps \\ delay_2 &= ln2R_{eq}C_{inv}(\gamma) = 930fs \\ delay_1 - delay_2 &= ln2R_{eq}C_{inv} \\ \gamma &= \frac{delay_2}{delay_1 - delay_2} = 0.9529 \end{aligned}$$

This γ is close to 1 (typical approximation). Solving the fanout equation yields f_{opt} **= 3.55**. This is close to the typical wisdom of optimal fanout of 4.

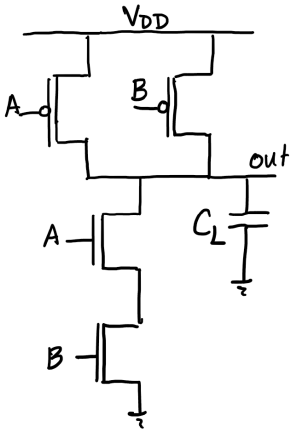
d) NAND2 Sizing

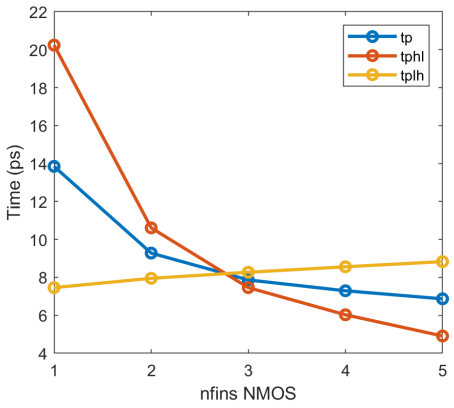
A stack of 2 NMOS transistors would be equivalent to having a length of 2L. For the same resistance, we need the I_{DSat} to remain the same. Using $E_C L = 0.7V$, $V_{TH} = 0.2$:

$$
\begin{aligned}
I_{DSatWinv} &= I_{DSatWNAND2} \\
\frac{W_{INV}}{L}\frac{u_{eff}C_{ox}E_C L}{2}\frac{(V_{GS}-V_{TH})^2}{(V_{GS}-V_{TH})+E_C L} &= \frac{W_{NAND2}}{2L}\frac{u_{eff}C_{ox}E_C 2L}{2}\frac{(V_{GS}-V_{TH})^2}{(V_{GS}-V_{TH})+E_C 2L} \\
\frac{W_{INV}}{1}\frac{E_C L}{2}\frac{1}{(V_{GS}-V_{TH})+E_C L} &= \frac{W_{NAND2}}{2}\frac{E_C 2L}{2}\frac{1}{(V_{GS}-V_{TH})+E_C 2L} \\
\frac{W_{NAND2}}{W_{INV}} &= \frac{E_C L * 4(V_{GS}-V_{THN}+E_C 2L)}{2E_C 2L(V_{GS}-V_{THN}+E_C L)} \\
&= \frac{0.7*4*((0.7-0.2)+1.4)}{1.4*2*((0.7-0.2)+0.7)} \\
&= 1.58
\end{aligned}
$$

Using $E_C L = 180mV$ and $V_{TH} = 284mV$ from 1b: $\frac{W_{NAND2}}{W_{INV}} = 1.30$.
Using $E_C L = 100mV$ and $V_{TH} = 317mV$ from 1b when fitting only $E_C L$: $\frac{W_{NAND2}}{W_{INV}} = 1.21$.

None of these are quantized to an integer multiple of fins. From SPICE simulations sweeping Wn while holding the bottom input high, we see that the optimal fin count is about 2.7/2=1.35 larger than the inverter fin count:





Sources of discrepancy may stem from imperfect fitting to the used models in problem 1 and NAND2 gate resistances following a different trajectory that does not reach the expected Req values as discussed in lecture.

e) Logical Effort and Intrinsic Delay of NAND2

The logical effort is:

$$g = \frac{C_{inNAND2}}{C_{inINV}}$$

Using symmetrical effort sizing, the NMOS fin width should be 3 (1.5 normalized):

$$g = \frac{1.5 * fins + 1 * fins}{1 * fins + 1 * fins} = 1.25$$

Intrinsic delay: SPICE simulation of the unloaded symmetrically sized NAND2 gate yields $t_{pHL} = 1.43$ps, $t_{pLH} = 1.34$fs, and t_p **= 1.38ps**.

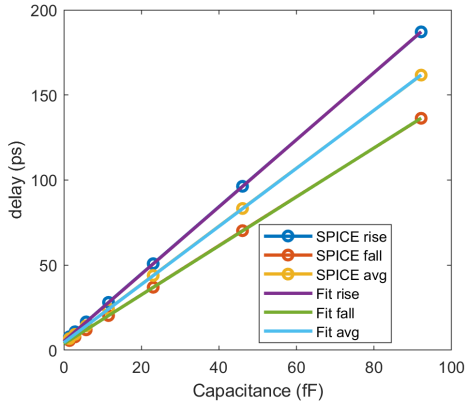
f) NAND2 Logical Effort and Intrinsic Delay from .lib

From the NAND2x2 cell from the TT library and extrapolating for pin A, use the `cell_rise` and `cell_fall` times. Index 1 (row) is the input transition time in ps, index 2 (column) is the capacitance in fF:

```
cell_fall (delay_template_7x7_x1) {
  index_1 ("5, 10, 20, 40, 80, 160, 320");
  index_2 ("1.44, 2.88, 5.76, 11.52, 23.04, 46.08, 92.16");
  values ( \
    "5.68567, 7.80473, 11.9661, 20.3491, 36.9879, 70.2487, 136.313", \
    "6.75933, 8.88777, 13.125, 21.5053, 38.0899, 71.3456, 137.311", \
    "8.34562, 10.8441, 15.156, 23.499, 40.2018, 73.347, 139.426", \
    "10.5202, 13.6981, 18.9513, 27.6791, 44.3997, 77.5414, 143.878", \
    "12.9208, 17.4459, 24.2987, 35.0985, 52.6797, 85.9863, 152.217", \
    "14.7737, 21.4324, 31.1568, 45.413, 67.1879, 102.533, 168.949", \
    "14.5634, 24.1866, 38.4263, 58.7031, 87.7034, 131.336, 202.258" \
  );
```

```
cell_rise (delay_template_7x7_x1) {
  index_1 ("5, 10, 20, 40, 80, 160, 320");
  index_2 ("1.44, 2.88, 5.76, 11.52, 23.04, 46.08, 92.16");
  values ( \
    "7.88536, 10.8263, 16.6254, 28.1067, 50.8377, 96.3349, 187.104", \
    "9.35012, 12.252, 17.9993, 29.5165, 52.2326, 97.6007, 188.727", \
    "12.5161, 15.4135, 21.1455, 32.5012, 55.4738, 100.884, 191.633", \
    "17.3971, 21.3043, 27.5431, 38.9515, 61.6827, 107.297, 198.178", \
    "24.5504, 30.0314, 38.6787, 51.6461, 74.3285, 119.783, 210.842", \
    "34.981, 42.6968, 55.0358, 73.0705, 99.8227, 145.617, 236.428", \
    "50.7793, 61.1333, 78.2723, 104.187, 142.019, 196.206, 287.382" \
  );
}
```

Extrapolating for the first row:



The found intrinsic values are: $t_{pLH} = 5.23$ps, $t_{pHL} = 3.72$ps, $t_p = \mathbf{4.47ps}$ (note this is higher than Spice sims due to a difference in transition time: 1ps vs. 5ps).

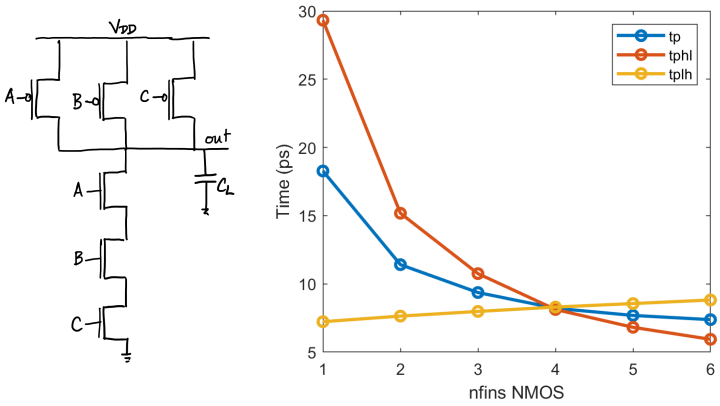
To find the logical effort, find the pin capacitances of the INVx2 input gate (pin A) and the NAND2x2 gate (either pin A or B), as these gates have similar drive strength. Plugging in the values:

$$g = \frac{C_{NAND2}}{C_{INV}} = \frac{1.38fF}{0.83fF} = 1.66$$

g) NAND3 Sizing

$$\begin{aligned}
I_{DSatWinv} &= I_{DSatWNAND3} \\
\frac{W_{INV}}{L}\frac{u_{eff}C_{ox}E_CL}{2}\frac{(V_{GS}-V_{TH})^2}{(V_{GS}-V_{TH})+E_CL} &= \frac{W_{NAND3}}{3L}\frac{u_{eff}C_{ox}E_C3L}{3}\frac{(V_{GS}-V_{TH})^2}{(V_{GS}-V_{TH})+E_C3L} \\
\frac{W_{INV}}{1}\frac{E_CL}{2}\frac{1}{(V_{GS}-V_{TH})+E_CL} &= \frac{W_{NAND2}}{3}\frac{E_C3L}{3}\frac{1}{(V_{GS}-V_{TH})+E_C3L} \\
\frac{W_{NAND3}}{W_{INV}} &= \frac{E_CL*9*((V_{GS}-V_{THN})+E_C3L)}{6E_CL((V_{GS}-V_{THN})+E_CL)} \\
&= \frac{0.7*9*((0.7-0.2)+2.1)}{2.1*2*((0.7-0.2)+0.7)} \\
&= 3.25
\end{aligned}$$

Using $E_CL = 180mV$ and $V_{TH} = 284mV$ from 1b: $\frac{W_{NAND2}}{W_{INV}} = 2.40$.
Using $E_CL = 100mV$ and $V_{TH} = 317mV$ from 1b when fitting only E_CL: $\frac{W_{NAND2}}{W_{INV}} = 2.12$.



From SPICE simulation, $t_{pHL} = 1.74$ps, $t_{pLH} = 1.70$fs, and $t_p = \mathbf{1.72ps}$ for a gate ratio of $\approx 2:1$. Logical effort from the SPICE results is:

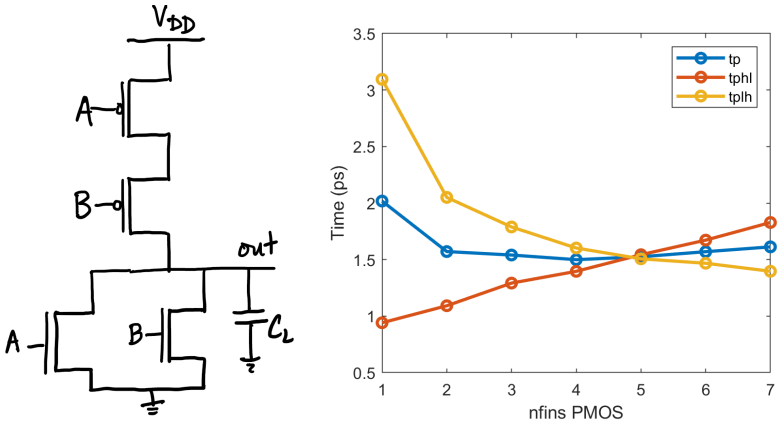
$$g = \frac{2 * fins + 1 * fins}{1 * fins + 1 * fins} = 1.5$$

h) NOR2 Sizing

$$\frac{W_{NOR2}}{W_{INV}} = \frac{E_C L * 4(V_{GS} - V_{THN} + E_C 2L)}{2E_C 2L(V_{GS} - V_{THN} + E_C L)}$$

For the homework provided $E_C L$ and V_{TH}: $\frac{W_{NOR2}}{W_{INV}} = 1.58$.
For fitted $E_C L = -262mV$, $V_{THP} = -266mV$: $\frac{W_{NOR2}}{W_{INV}} = 1.28$.
For fitted $E_C L = -110mV$, $V_{THP} = -314mV$: $\frac{W_{NOR2}}{W_{INV}} = 1.22$.

Using the optimal ratio of PMOS:NMOS width obtained in part (a) (2.5:2), the expected PMOS width is somewhere between 1.525 and 1.975 times that of the NMOS (quantized), resulting in about the same logical effort as NAND2 of 1.25. However, SPICE (below) shows a 2.5:1 PMOS:NMOS fin ratio to be symmetric sizing. Reasons for this are likely the same as those in part d.



The intrinsic delay of the 5 fin PMOS, 2 fin NMOS device with 1fF loading and 1ps input transition time is $t_{pHL} = 1.54$ps, $t_{pLH} = 1.51$fs, and $t_p = \mathbf{1.52ps}$. Logical effort from the SPICE-derived optimal sizing is:

$$g = \frac{2.5 * fins + 1 * fins}{1fins + 1fins} = 1.75$$