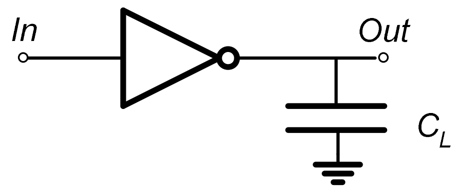
**EECS251B Advanced Digital Integrated Circuits** **Spring 2022.**

**HOMEWORK 2.** **Due: Monday, April 4, 2022.**

**This is an individual assignment!**

## 1. Delays

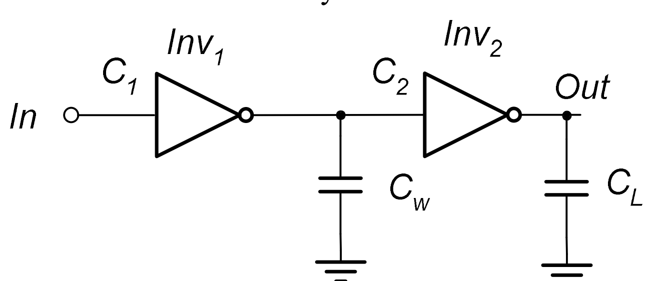
Consider an inverter driving a capacitive load in ASAP7 technology.




All transistors have W/L = 12, $V_{DD}$ = 0.75V. In this technology, you can assume that $C_g = C_d$ = 2fF/µm, transistor thresholds are 0.3V and fanout-of-4 inverter delay is 12ps.

a) For what range of sizes of the load capacitor, $C_L$, adding another inverter to drive the load reduces the delay?

b) If the input capacitance of the first inverter in the figure below is set to $C_1$ = 1.5fF, the wire capacitance $C_w$ is 1fF, how would you size the second inverter that is driving 17.5fF load to minimize the overall delay from *In* to *Out*? Is this result intuitive?




## 2. Latch timing

A timing path with a single register driving a latch-based system is shown in Figure 2. R0 is a rising-edge triggered register, while R1, R2, and R3 are level sensitive. There are two 50% duty cycle clock phases available, with clkb offset from clk by half a period. Both registers and latches have zero hold time, and there is no clock skew in the system. Registers have $t_{clk\text{-}Q}$ = 100 ps. Latches have $t_{clk\text{-}Q} = t_{D\text{-}Q} = t_{su}$ = 150 ps.

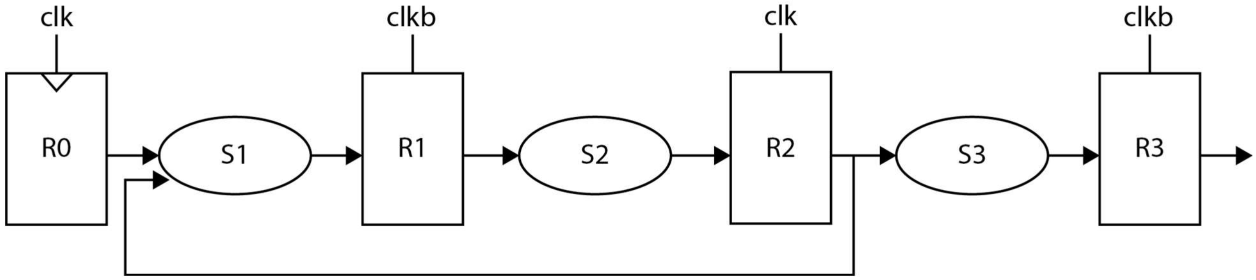



Figure 2.

a) The critical path of S1 is 600 ps, the critical path of S2 is 400 ps, and the critical path of S3 is 550 ps. Compute the minimum clock period.
b) Assume that we can model the on current with $I_{on} = K(V_{DD} - V_{thz})$, with $K = 0.002$, $V_{DD} =$ 0.75 V, and $V_{thz} = 0.3$ V. There is a systematic variation on $V_{thz}$. What is the maximum value of $V_{thz}$ that leads to a 15% increase in delay?
c) The systematic variation of $V_{thz}$ is normally distributed with $\sigma = 0.05$ V. What would be the yield in terms of timing if you are allowed a 15% margin on the clock period?

### 3. Flip-Flop

A flip-flop is shown in Figure 3.

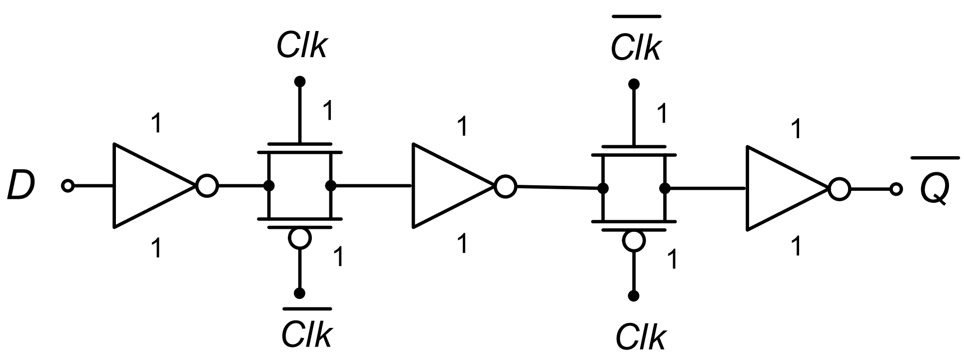



Figure 2.

In this process, a symmetrically sized inverter has $W_p = W_n$, and a unit-sized transistor has gate and drain capacitances of 1fF and the on-resistance of 2.5kΩ. The resistance of a stack of two devices is 1.5x of the resistance of a single transistor with the same width. You can assume that the true and complementary clocks are ideal, and the logical effort of creating $\overline{Clk}$ from $Clk$ is 1.

a) Is the flip-flop triggered by a rising or a falling edge of the *Clk*?
b) Calculate the $Clk - \overline{Q}$ delay for a 0→1 transition at the output and show your work.
c) Calculate the hold time for $D = 1$.