EE251B Advanced Digital Integrated Circuits and Systems **Spring 2022.**

HOMEWORK 3. **Due: Wednesday, April 13, 2021.**

This is an individual assignment!

1. SRAM assists

Consider a conventional 6-T SRAM cell, sized to be stable at nominal operating conditions. The cell is a part of a conventional, precharged bitline array. We would like to operate it at a reduced supply voltage, so we are considering assist techniques. Let's analyze the effect of peripheral signals on the operation of the cell. One-sentence answers, please!

a) How does decreased wordline voltage affect the read stability of the cell?
b) How does decreased wordline voltage affect the read access time of the cell?
c) How does decreased wordline voltage affect the writeability of the cell?
d) How does increased cell supply voltage (without changing other signal levels) affect the writeability of the cell?

2. SRAM yield

We will analyze a 2MB SRAM array, consisting of 128 x 128 bit subarrays. Four columns share one sense amplifier. Bitline capacitance is 1pF and the supply is 1V. SRAM cell Ion = 100μA, Ioff = 400nA, and they don't vary (at least not in this homework), and the target access time of 1ns is dominated by the bitline discharge.

If the sense amplifier offset has normal distribution, with zero mean and standard deviation of 15mV, would you expect this array to have a high yield? How many redundant columns would need to be added per subarray to have >99% yield (note that you may not have to do the exact calculation of this)?