inst.eecs.berkeley.edu/~eecs251b

EECS251B : Advanced Digital Circuits and Systems

Lecture 25 – Supplies and Clocks

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Time for course surveys!

Course Evaluations: Best Practices for Faculty

Reserve time in-class.
Give students time during class to complete the online course survey. Anecdotally, this is more effective when the time set aside is at the **start** of class.

Inform students about the purpose of evaluations.
Give students examples of useful feedback you have received in the past and **how** the course has changed or benefited.

Offer students incentives (e.g. extra credit).
To encourage broad, representative responses, instructors may choose to offer incentives to complete evaluations. An effective strategy has been to offer all students extra credit if a **minimum percentage** of students (e.g. 85%) respond.

85%

Berkeley UNIVERSITY OF CALIFORNIA

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Recap

- Basics of phase-locked loops
- Digital PLLs

2

Delay-Locked Loops

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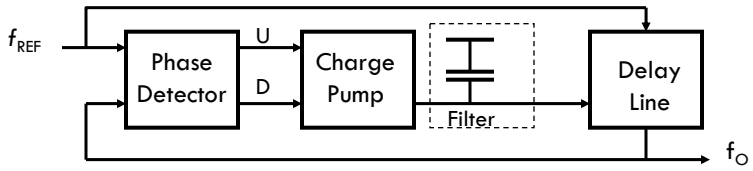
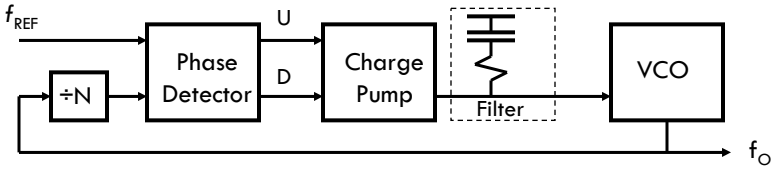
Clock Generation

Delay-Locked Loop (Delay Line Based)



Phase-Locked Loop (VCO/DCO-Based)



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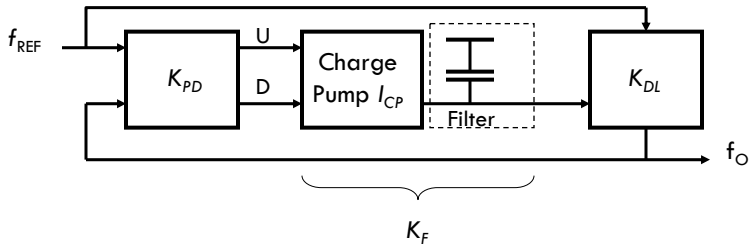
Delay-Locked Loop

- First order loop: inherently stable
- No filtering of input jitter
- Constant frequency (no synthesis)
- No phase error accumulation



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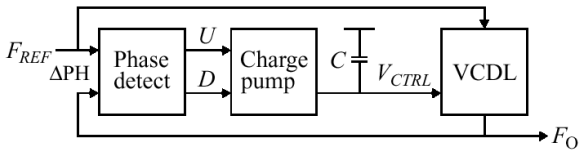
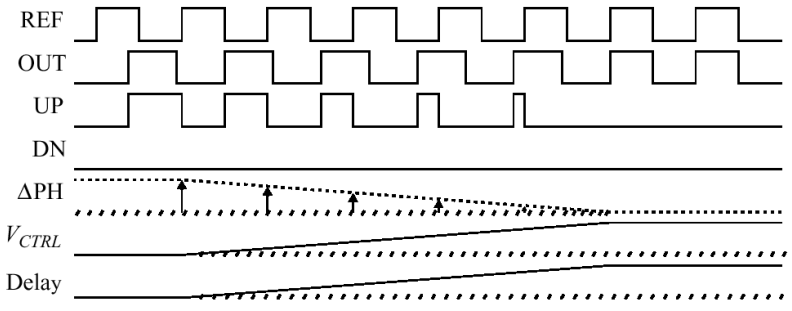
DLL Locking





Courtesy of IEEE Press, New York. © 2000

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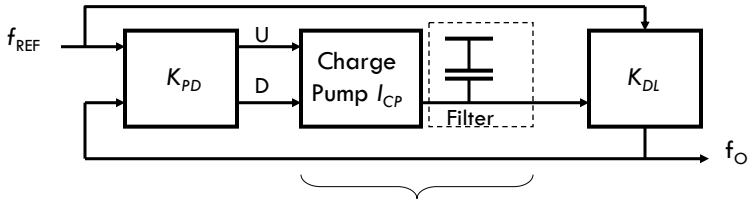
Delay-Locked Loop



- Open loop transfer function

$$\frac{D_O(s)}{D_I(s)-D_O(s)} = K_{PD}\frac{1}{sC}I_{CP}K_{DL}F_{REF} = \frac{1}{s}K_{PD}K_FK_{DL}$$

- Closed loop transfer function

$$H(s) = \frac{D_O(s)}{D_I(s)} = \frac{K_{PD}K_FK_{DL}}{s + K_{PD}K_FK_{DL}}$$

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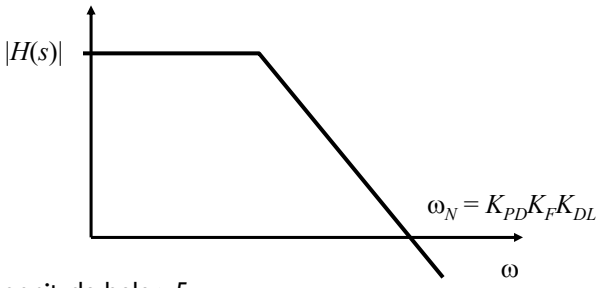
Delay-Locked Loop



- ω_N > an order of magnitude below F_{REF}
- Use of DLLs requires low-jitter input
- VCDL must span adequate delay range + reset to min delay
- Noise sources:
  - Delay line (Supply sensitivity)
  - Clock buffers that follow
  - Device noise (small)

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Announcements

- Final is in-class 4/28
  - 80min, 9:40am-11am
- Project presentations 5/5
  - 9am – 12:30pm
  - BWRC
  - 12min + 3min Q&A

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Clock Distribution

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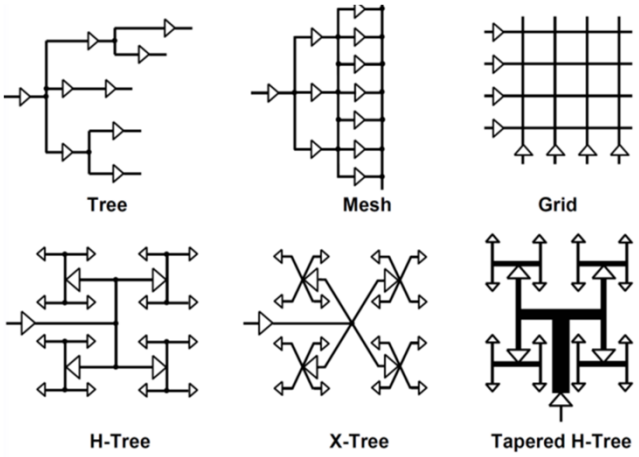
Clock Distribution



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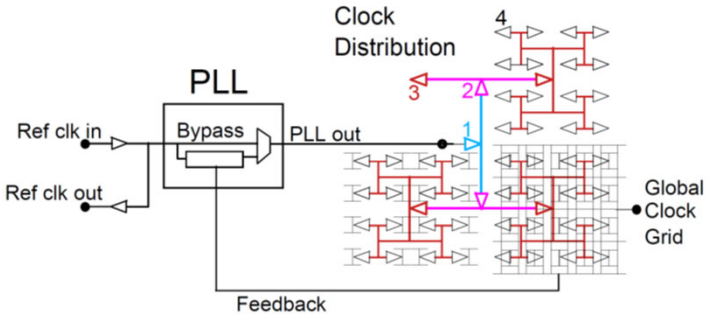
Example (Older) Clock System

- IBM Power 4



Restle, ISSCC'02

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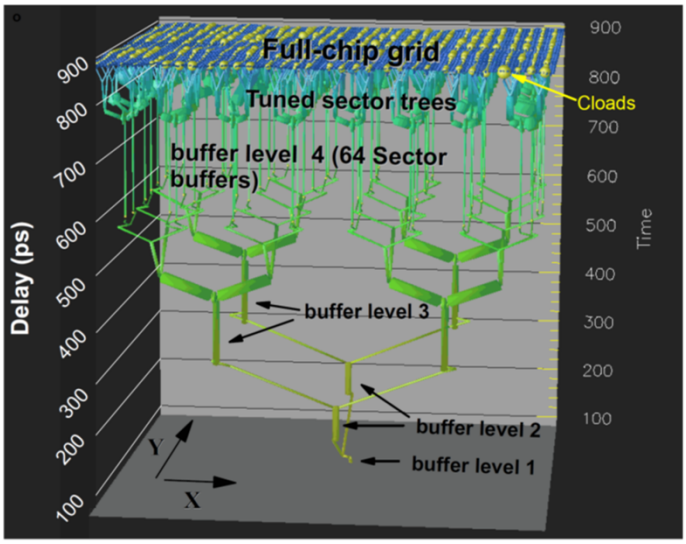
Clock Grid



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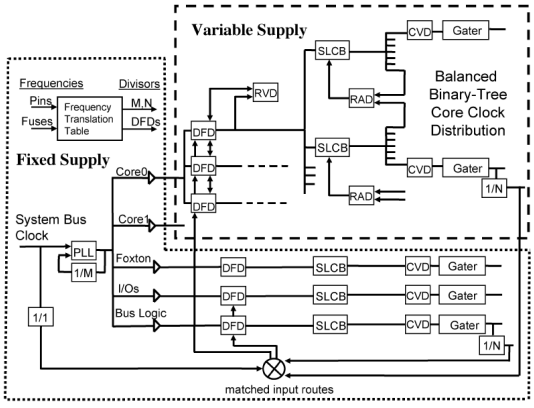
One PLL with multiple DLLs



- Single PLL, and two cores vary frequency through digital frequency dividers (DFDs) and DLLs
  - SLCB: Second-Level Clock Buffer
  - CVD: Clock Vernier Device – fine (static) delay tuning

Fischer, JSSC 1/06

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Deskewing and Synchronization

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Clock Domain Synchronization

Type	Frequency	Phase
Synchronous	Same	Same
Mesochronous	Same	Constant offset
Plesiochronous	Small difference	Slowly varying
Asynchronous	Different	Arbitrary

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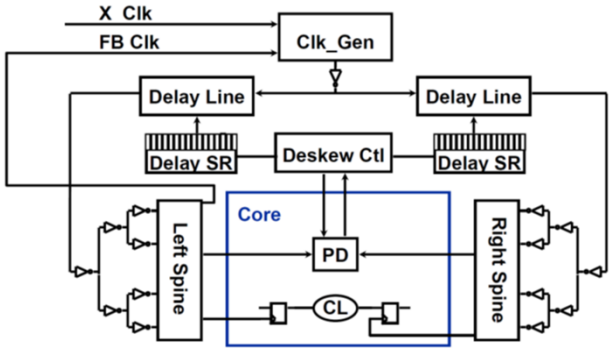
Deskew System (Mesochronous)



Geannopoulos, ISSCC'98

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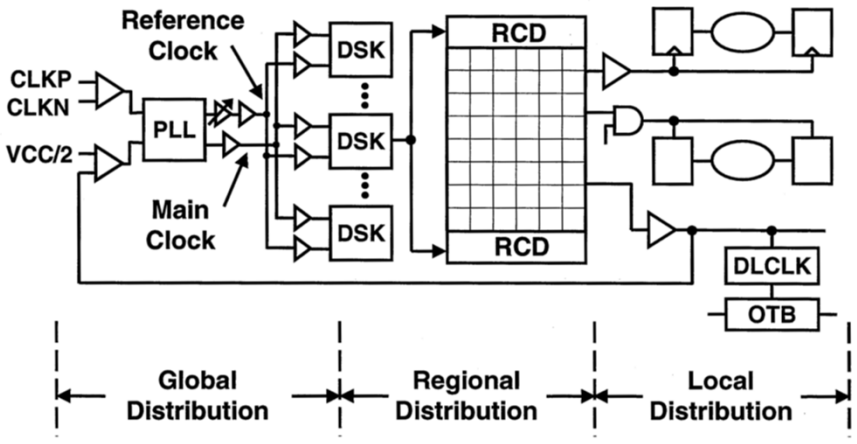
Deskew System



- Rusu, ISSCC'00

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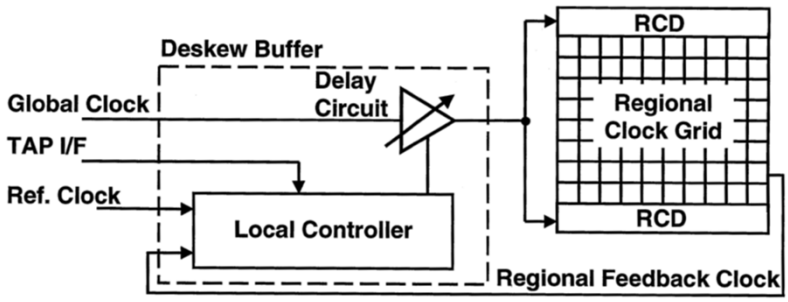
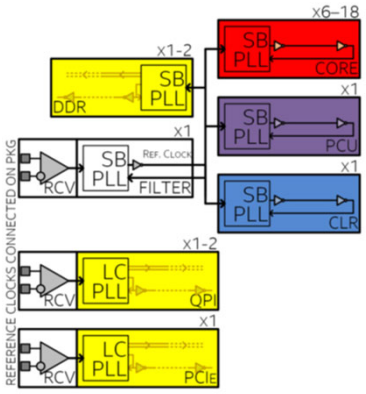
Deskew Buffer



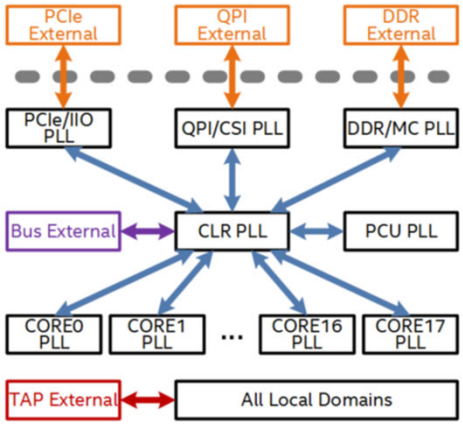
- Essentially a DLL to align regional clock with ref. clock

Clock Subsystem

- Intel Xeon – Bowhill, ISSCC'15
  - Independent clocks for 4-18 cores
- Self-biased (SB) and LC PLLs

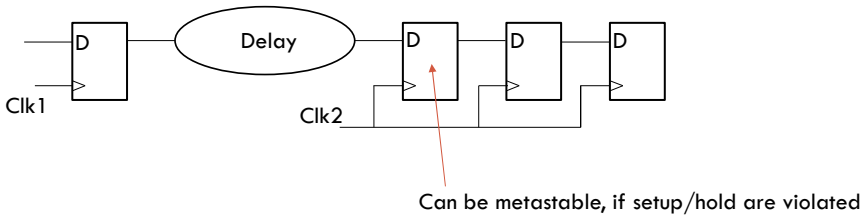


Clock Domain Crossings



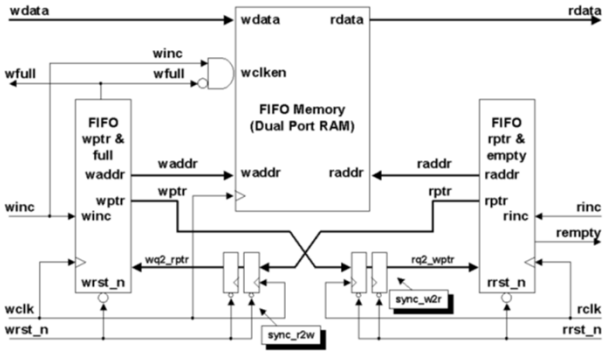
- Bowhill, ISSCC'15

Brute-Force Synchronizer



- Cascaded flip-flops reduce the probability of metastability

Clock Crossing FIFOs



- FIFO for clock crossings

http://www.sunburst-design.com/papers/CummingsSNUG2002SJ_FIFO1.pdf

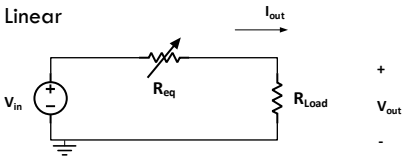
Supply Generation

Supply Generation

- Linear
  - Series or shunt
  - Linear regulation
  - Quiet
  - Inefficient (unless Vin-Vout is small)
- Switching (Capacitive)
  - Limited efficiency
  - Poor regulation
  - Voltage ripples
- Switching (Magnetic)
  - Efficient
  - Require external components
  - Noisy

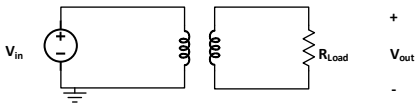
Linear vs. Switching Regulators

Linear

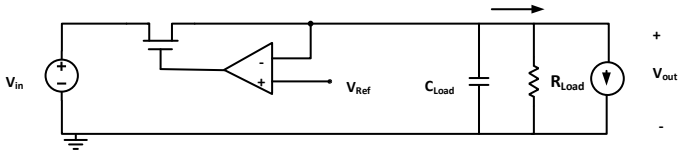


Efficiency η < Vout/Vin

Switching



Linear Voltage Regulator



Negative feedback sets low supply resistance
Voltage regulated to desired level

E.g. IBM Power7 has 48 linear regulators

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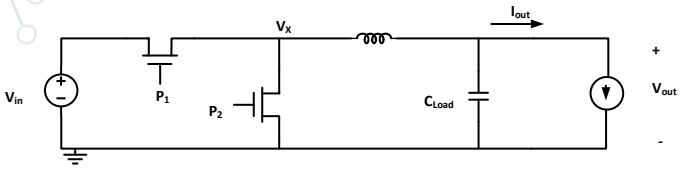
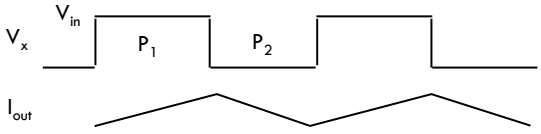
Switching Supply

- Buck Converter





Pulse-Width Modulation (PWM) regulates V_{out}

High switching frequency, interleaving reduce ripple

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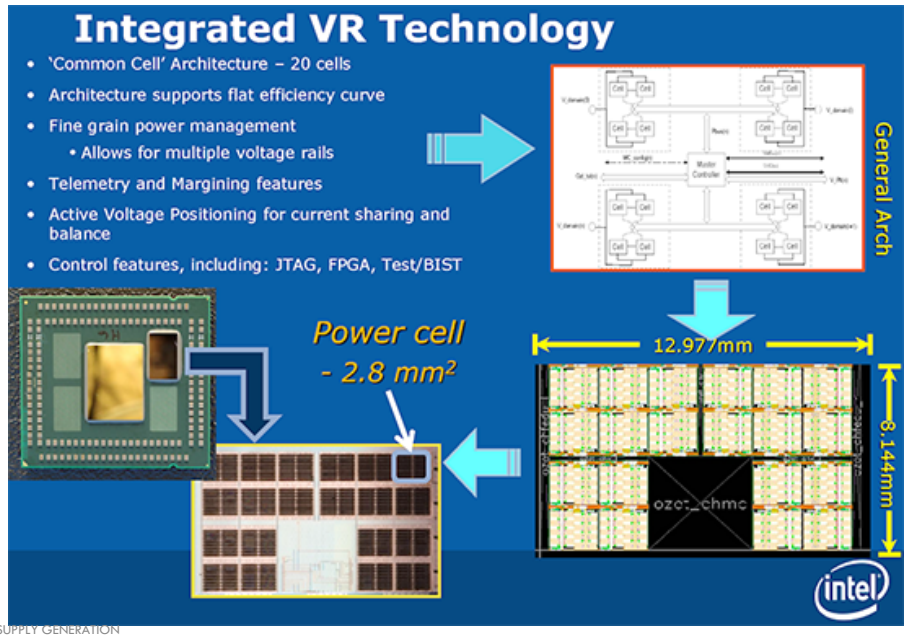
Inside Haswell



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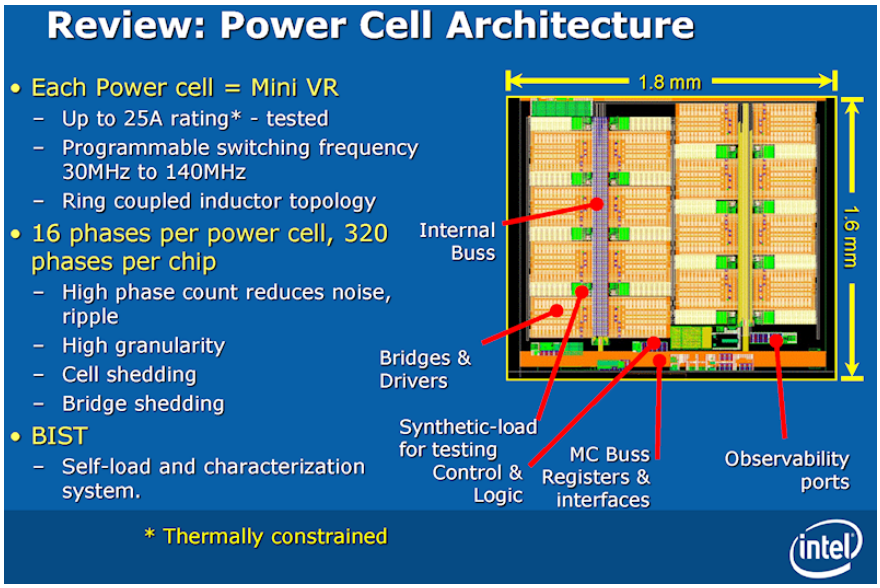
Inside Haswell



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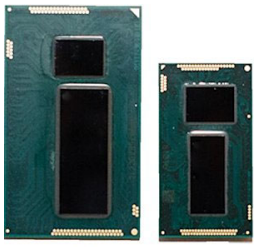
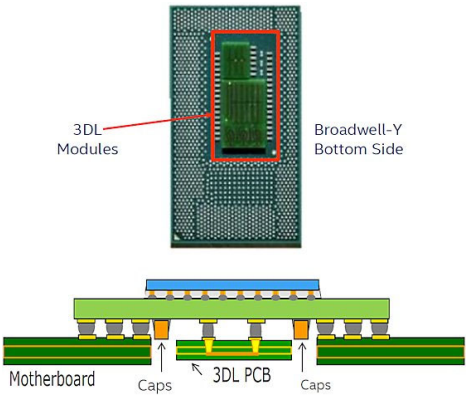
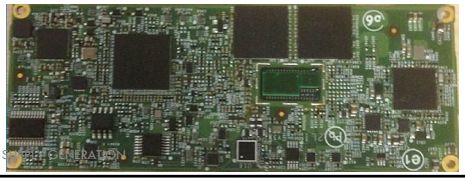
Intel Broadwell

- Inductors moved to a small PCB







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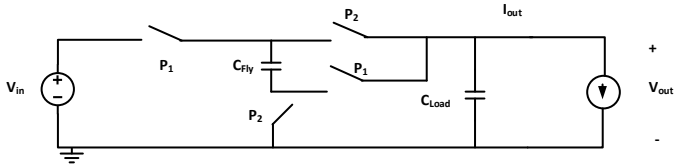
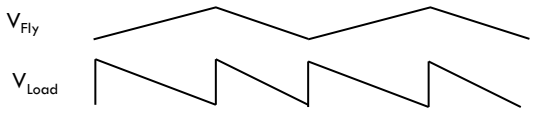
Switched-Capacitor Supply





Interleaving reduces ripple, but lowers efficiency

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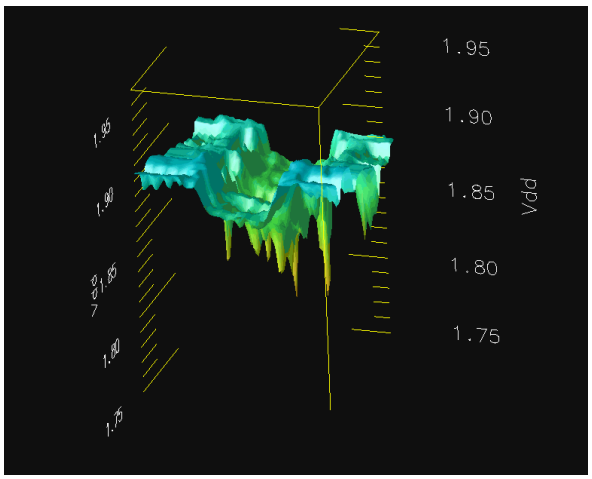
What happens with supply when load changes?

http://www.research.ibm.com/people/r/restle/Animations/DAC01top.html



Phillip Restle, IBM

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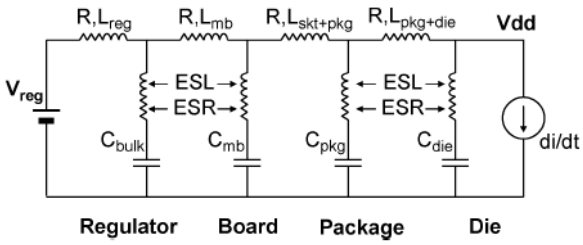
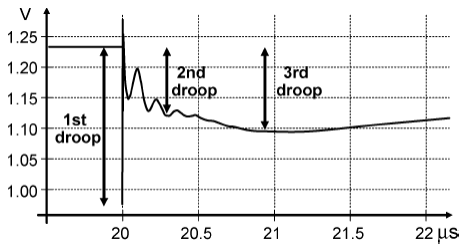
Power Delivery

- Typical model





Wong, JSSC'06

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Supply Resonances

- First droop
  - Package L + on-die C
- Second droop
  - Motherboard + package decoupling
- Third droop
  - Board capacitors

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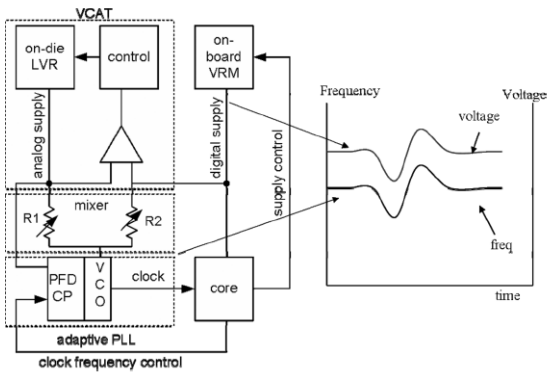
Clock and Supply

- Large digital systems can have large voltage transients
  - Can we filter impact of voltage on a clock generator?



Kurd, JSSC'09

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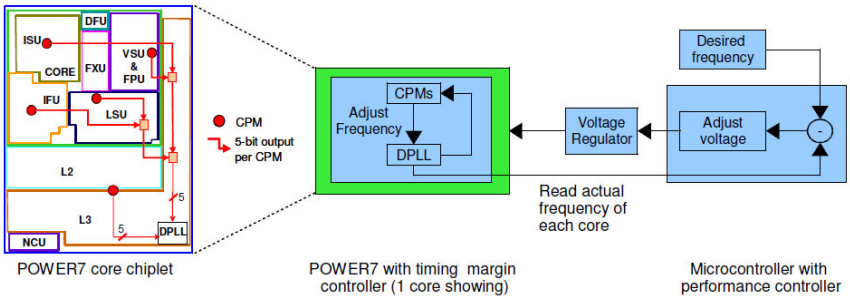
Clock and Supply



- IBM Power7, with one PLL per core

Lefurgy, MICRO'11

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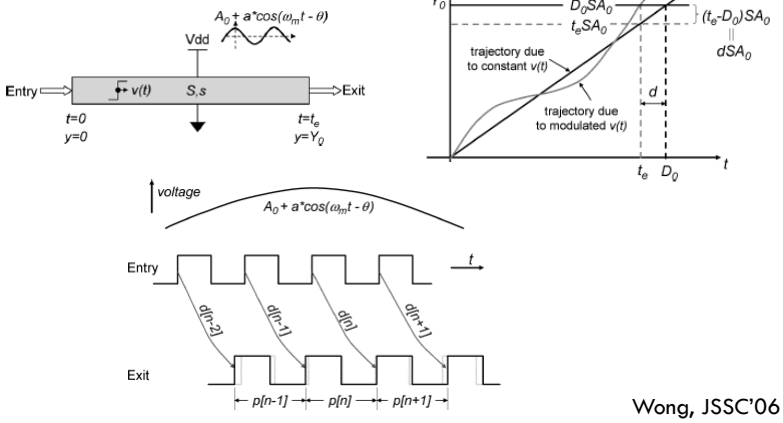
How to model

- Abstracted delay line



Wong, JSSC'06

Period modulation from successive modulated delays

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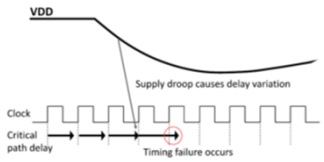
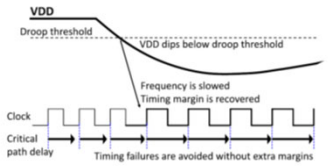
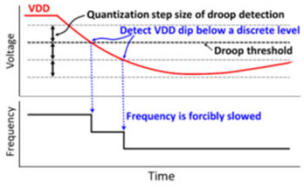
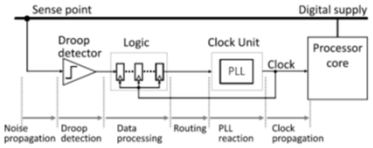
Droop Detection

- Hashimoto, JSSC 4/18









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Summary

- DLLs are used for phase alignment, deskewing
- Modern SoCs are globally asynchronous, locally synchronous
- Supply regulators
- Clock and supply interact

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Next Lecture

- Wrap-up