inst.eecs.berkeley.edu/~eecs251b

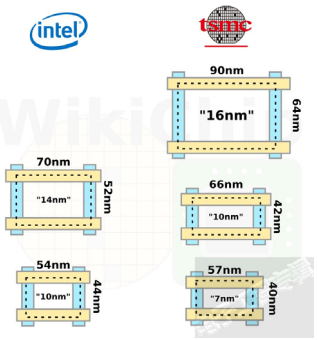
EECS251B : Advanced Digital Circuits and Systems

Lecture 7 – Features of Modern Technologies

Borivoje Nikolić, Vladimir Stojanović, Sophia Shao

Apple, Huawei Use TSMC, But Their 7nm SoCs Are Different. When talking about the most advanced semiconductor manufacturing processes, it seems that most of the SoCs in 2019 can be collectively classified as 7nm. But not all 7nm is equal.

EE Times, January 22, 2020.



Recap

- Accelerators don't exist in isolation.
- RoCC for tightly-coupled accelerators
- TileLink for loosely-coupled, MMIO accelerators
- Examples:
  - RoCC accelerators: SHA3
    - https://github.com/ucb-bar/sha3
  - RoCC + TL-UL: protobuf accelerator
    - https://github.com/ucb-bar/protoacc
  - RoCC + TL-UH: Gemmini accelerator
    - https://github.com/ucb-bar/gemmini
  - RoCC + TL-UH: Hwacha vector accelerator
    - https://github.com/ucb-bar/hwacha
  - TL-UH: IceNIC network interface controller for FireSim
- https://github.com/firesim/icenet

A Perspective on Scaling

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Key Points

- Technology scaling (Moore's law) is slowing down
  - But logic and memory are continuing to scale, possibly at different pace
  - We anyway can't power up all transistors we can put on a chip
- Dennard scaling has ended >10 years ago
  - We cover it for understanding of current issues
- There are many technology flavors available at the moment
  - We need to know what each one brings to us, so we can choose the right one for your project
    (may have to wait until the end of the class to figure out all options)
- Physical (velocity-saturated) models scale across technologies

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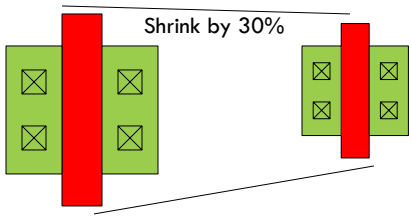
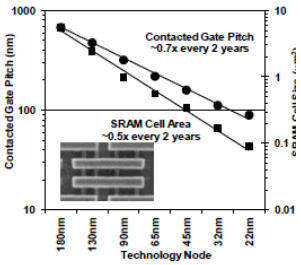
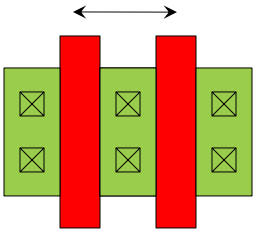
Transistor Scaling



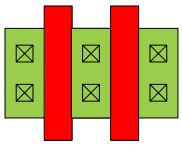


C. Auth, VLSI'12

"Contacted gate pitch"



Shrink by 30%



Gate pitch scales 0.7x every node

Intel	45nm	32nm	22nm	14nm	10nm
Contacted gate pitch	160nm	112.5nm	90nm	70nm	54nm

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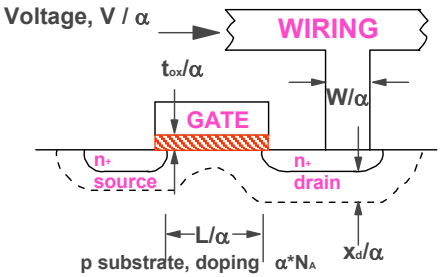
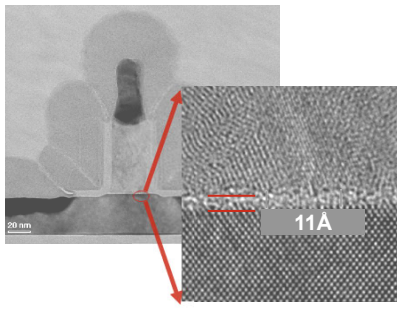
CMOS Scaling Rules (Dennard)





SCALING:

Voltage: V/α

Oxide: t_{ox}/α

Wire width: W/α

Gate length: L/α

Diffusion: x_d/α

Substrate: $\alpha * N_A$

RESULTS:

Higher Density: $\sim\alpha^2$

Higher Speed: $\sim\alpha$

Power/ckt: $\sim 1/\alpha^2$

Power Density: ~~Constant~~

R. H. Dennard *et al.*, *IEEE J. Solid State Circuits*, (1974).

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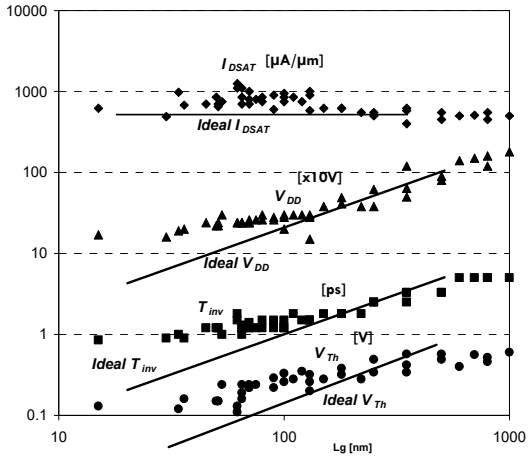
Ideal vs. Real Scaling

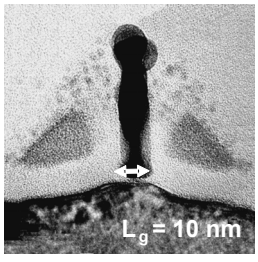
- Leakage slows down V_{Th}, V_{DD} scaling

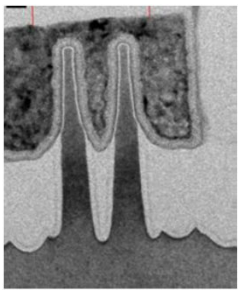
(Dennard's scaling ended somewhere on this picture)



Research vs. Production Devices

10nm device (Intel), circa 2003

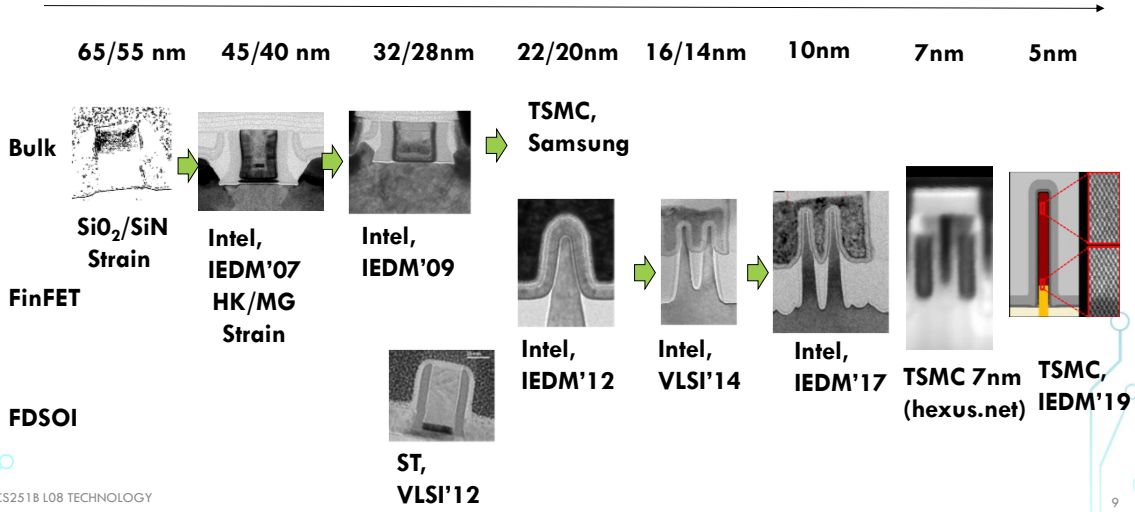




10nm node (Intel), IEDM'2017

Transistors are Changing

- From bulk to finFET and FDSOI



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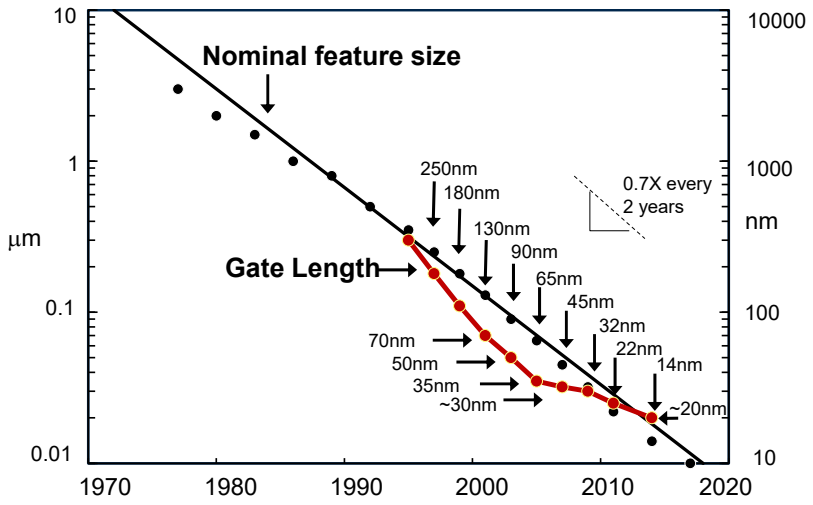
Physical Gate Scaling



Changes in slope at 250nm, 45nm
Minimum Leff for 5nm finFET is ~15nm

Source: Intel, IEDM presentations

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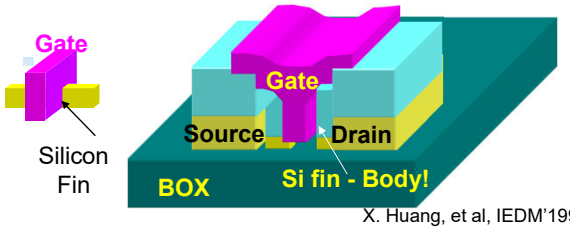
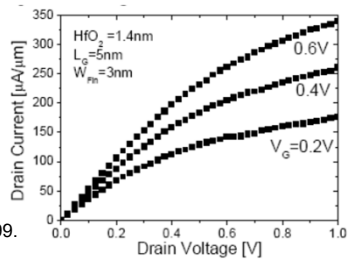
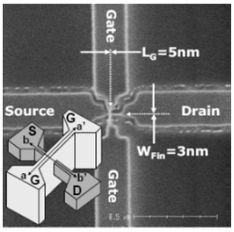
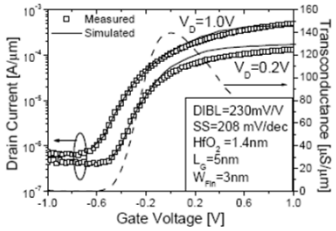
Sub-5nm FinFET



X. Huang, et al, IEDM'1999.







Lee, VLSI Technology, 2006

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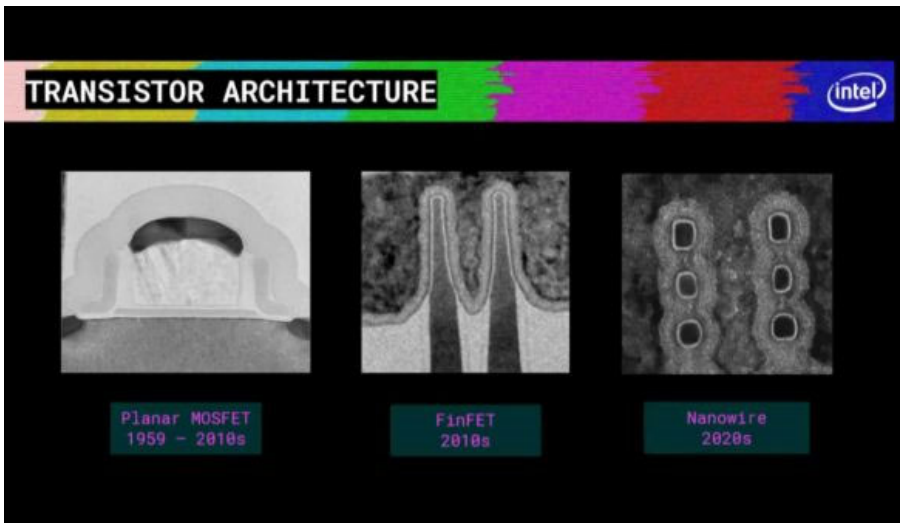
Beyond 5nm

- Gate-all-around transistors/nanowires



J. Keller, EECS Colloquium, UC Berkeley, Sept 2019.

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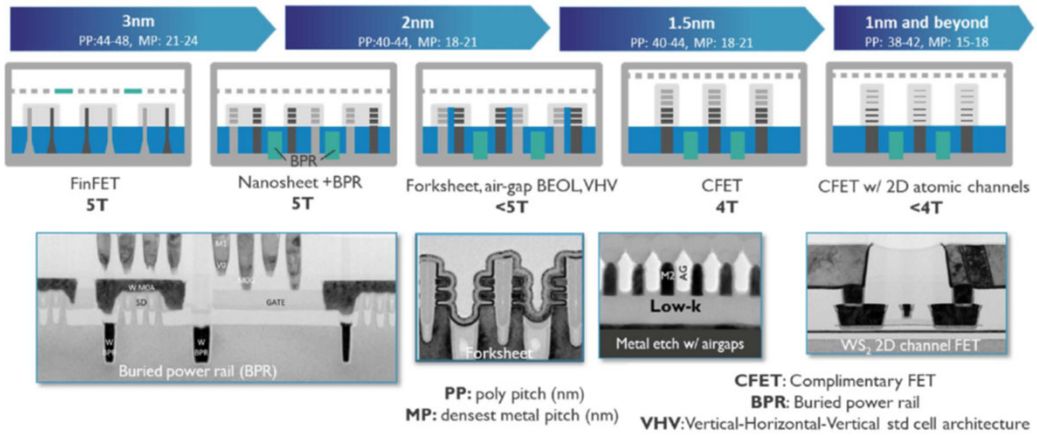
Current Perspective for <5nm



- Samavedam, et al, IEDM'20

Pitch Scaling

Intel	45nm	32nm	22nm	14nm	10nm
Contacted gate pitch	160nm	112.5nm	90nm	70nm	54nm
Shrink		0.7	0.8	0.78	0.77

- **Clearly not 0.7 anymore…**
- **But (Intel 14nm, Natarajan, IEDM'14)**
  - Fin pitch: 42nm (0.7x shrink)
  - Metal 0: 56nm (-)
  - Metal 1: 70nm (0.78x)
  - Metal 2: 52nm (0.65x)
  - **Intel's metric:**
    - CPP x MXP
    - 0.78 x 0.65 = 0.5!
  - **CPP & FP matter more**

Various Technology flavors

- Intel 14nm

	High Speed Logic Transistor		Ultra Low Power Transistor	High Volt. I/O Transistor
Options	(HP)	(SP)	(ULP)	(TG)
Vdd (Volt)	0.7	0.7	0.7	1.5-3.3
Gate Pitch(nm)	70	70	84	Min. 140
Fin Pitch (nm)	42	42	42	42
NMOS/PMOS Idsat/Ioff (mA/um)	1.3/ 1.2 @ 0.7 V, 100 nA/um	.85 / .72 @ 0.7 V, 1 nA/um	.50 / .32 @ 0.7 V 15 pA/um	1.15/1.11 @ 1.8 V 10 pA/um

Layer	Pitch	CPU [5]	SoC
Gate	70 nm	Gate	Gate
M0	56 nm	M0	M0
M1	70 nm	M1	M1
Metal 1x	52 nm	M2	M2/3/4/5
Metal 1.1x	56 nm	M3	N/A
Metal 1.5x	80 nm	M4	1-3 layers
Metal 2x	100 nm	M5	1-2 layers
Metal 3x	160 nm	M6-8	1-2 layers
Metal 5x	252 nm	M9/M10	1-2 layers
Metal Top	1080nm	M11	Top Metal
TM1	14 um	TM1	TM1

- Different foundries

Feature	Samsung 14 nm	Intel 14 nm	TSMC 16 nm
Fin pitch (nm)	48	42	48
1/3 fin pitch	16	14	16
Gate length (nm)	~30	~24	~33
Contacted gate pitch (nm)	78	70	90
Minimum metal pitch (nm)	64	52	64
6T SRAM cell area (μm^2)	0.08	0.059	0.074

Source:
Tech Insights
EETimes

Not All Technologies are Equal

Intel

Node	CPP	MxP	FP
65nm	230	230	
45nm	160	160	
32nm	112.5	112.5	
22nm	90	80	60
14nm	70	52	42
10nm	54	36	34
7nm	37	32	

Samsung

Node	CPP	MxP	FP
45nm	180	140	
32nm	130	100	
28nm	115	90	
20LPE	90	80	60
14LPE	78	64	48
10LPE	68	48	42
7LPP	54	36	27

TSMC

Node	CPP	MxP	FP
45nm	190	140	
40nm	170	130	
28nm	120	90	
20SoC	90	64	
16FF	90	64	48
16FFC	96	64	48
10FF	66	44	36
7FF	57	40	30
5FF	50	28	

- **CPP = Contacted poly pitch**
- **MxP = Minimum metal pitch**
- **FP = Fin pitch**

Source:
A. Wei, TechInsights
IEDM'17, IEDM'19, WikiChip, SemiWiki'20

Leading-Edge Nodes

Foundry 5nm and Intel 10nm Nodes

- Rapid new process introductions by the foundries have driven foundry density ahead of Intel.
- TSMC is now the clear industry leader.
- 5nm processes make increased use of EUV (10-15 layers)
- TSMC has a high mobility pFET, likely a SiGe channel.

	Intel	Samsung	TSMC
Year	2019	2019	2019
Process	FF	FF	FF
Node	10nm	5nm	5nm
CPP (nm)	54	54	50
MMP (nm)	44	36	28
Tracks	6.18	6.00	6.00
DDB/SDB	SDB	SDB	SDB
Density (MTx/mm2)	106.10	133.56	185.46
Density increase [1]	2.33	**1.33**	**1.82 [2]**
SRAM cell (um2)	0.0312	0.0262	0.0210
Size change [1]	0.53	0.86	0.60

[1] Intel versus 14nm, Samsung and TSMC versus 7nm (last major node for each). [2] Samsung reports 1.33x, TSMC reports 1.8x.

IC KNOWLEDGE LLC

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Many Nodes Co-Exist

Wafer Revenue by Technology	3Q20	2Q20	3Q19
5nm	8%	0%	0%
7nm	35%	36%	27%
10nm	0%	0%	2%
16nm	18%	18%	22%
20nm	1%	1%	1%
28nm	12%	14%	16%
40/45nm	8%	9%	10%
65nm	5%	6%	7%
90nm	2%	3%	2%
0.11/0.13um	2%	3%	2%
0.15/0.18um	7%	8%	9%
0.25um and above	2%	2%	2%

Net Revenue by Platform	3Q20	2Q20	3Q19
Smartphone	46%	47%	49%
High Performance Computing	37%	33%	29%
Internet of Things	9%	8%	9%
Automotive	2%	4%	4%
Digital Consumer Electronics	3%	5%	5%
Others	3%	3%	4%

Net Revenue by Geography	3Q20	2Q20	3Q19
North America	59%	58%	60%
China	22%	21%	20%
Asia Pacific	10%	10%	9%
EMEA	5%	6%	6%
Japan	4%	5%	5%

- TSMC revenue per node

https://semiwiki.com/semiconductor-manufacturers/292174-tsmc-sets-the-stage-for-a-great-2021/

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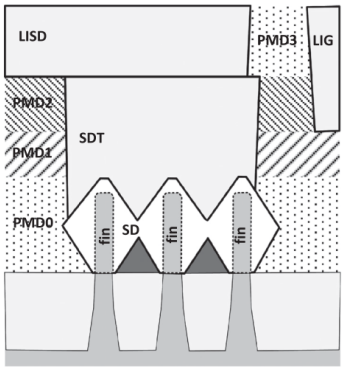
ASAP7

- Predictive technology kit used in this class
  - None of the above processes, but close

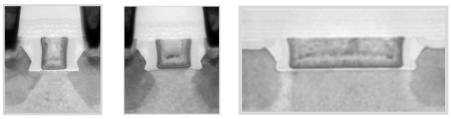


Layer	Lithography	Width/drawn (nm)	Pitch (nm)
Fin	SAQP	6.5/7	27
Active (horizontal)	EUV	54/16	108
Gate	SADP	21/20	54
SDT/LISD	EUV	25/24	54[b]
LIG	EUV	16/16	54
VIA0–VIA3	EUV	18/18	25[a]
M1–M3	EUV	18/18	36
M4 and M5	SADP	24/24	48
VIA4 and VIA5	LELE	24/24	34[a]
M6 and M7	SADP	32/32	64
VIA6 and VIA7	LELE	32/32	45[a]
M8 and M9	SE	40/40	80
VIA8	SE	40/40	57[a]

[a] Corner to corner spacing as drawn.
[b] Horizontal only.

32nm Technology Flavors (Intel)

Logic Transistor (HP or SP) | Low Power Transistor (LP) | HV I/O Transistor (1.8 V or 3.3 V)



Transistor Type	Logic (option for HP or SP)		Low Power	HV I/O (option for 1.8 or 3.3 V)	
	HP	SP	LP	1.8V	3.3V
EOT(nm)	0.95	0.95	0.95	~ 4	~ 7
Vdd (V)	.75/ 1	.75/ 1	0.75/1.2	1.5 /1.8	1.5 /3.3
Pitch(nm)	112.5	112.5	126	min. 338	min. 675
Lgate (nm)	30	34	46	>140	>320
NMOS Idsat (mA/um)	1.53 @ 1 V	1.12 @ 1 V	0.71 @ 1 V	0.68 1.8 V	0.7 3.3 V
PMOS Idsat (mA/um)	1.23 @ 1V	0.87 @ 1 V	0.55 @ 1 V	0.59 1.8 V	.34 @3.3 V
Ioff (nA/um)	100	1	0.03	0.1	<0.01

C.-H. Jan, IEDM'09, P. VanDerVoorn, VLSI Tech'10

5nm Flavors

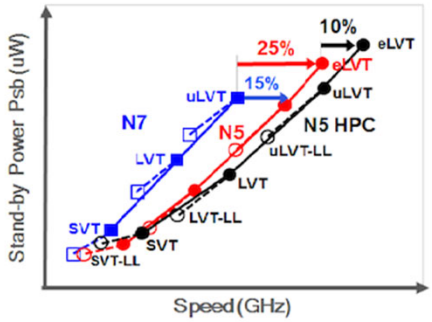
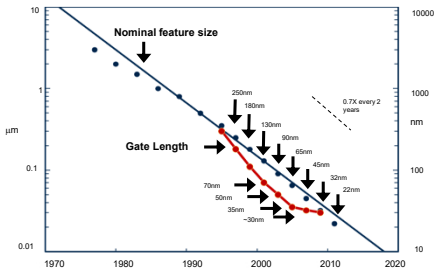
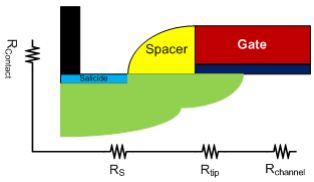


Fig.3 The 5nm also offers a set of critical HPC features. Extremely LVT (eLVT) for 25% faster peak speed over 7nm, and HPC 3-fin standard cell for additional 10% performance.

TSMC, IEDM'19

Lg, R, C scaling

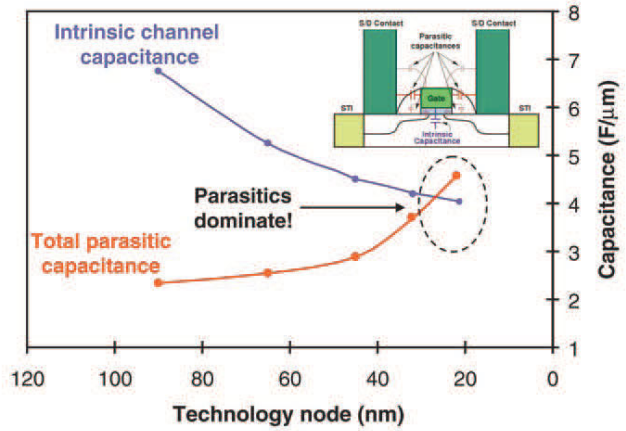




- With scaling L, need to scale up doping - scale junction depth (control leakage) – S/D resistance goes up
- External resistance limits current

$$I_D \approx V_{DS} / \left(R_{channel} + R_{ext} \right)$$

Parasitic Capacitance Scaling



Reality: Overlap + fringe can be 50% of $C_{channel}$ in 32nm

S. Thompson, *Materials Today*, 2006.

Announcements

- No lecture on February 22 (ISSCC)
- Project proposals due February 24
- Assignment 1 will be posted this week
- Lab 3 due this Friday
- Lab 4 posted this week, due in 2 weeks

Lithography Implications

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Lithography – Key Points

- Current lithography restricts features in design, affects variability
- This is changing with EUV
  - Long time to come
  - Deployed at 5nm (Samsung, TSMC, Intel) – transistors, contacts

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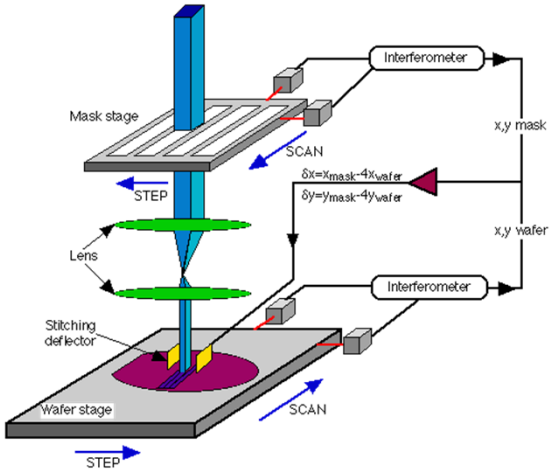
Step-and-Scan Lithography



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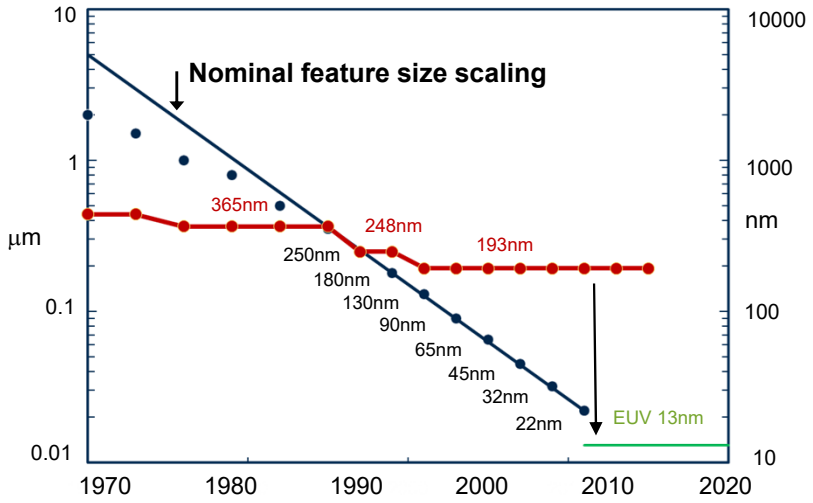
Lithography Scaling



EUV – Technology of the future (forever)?

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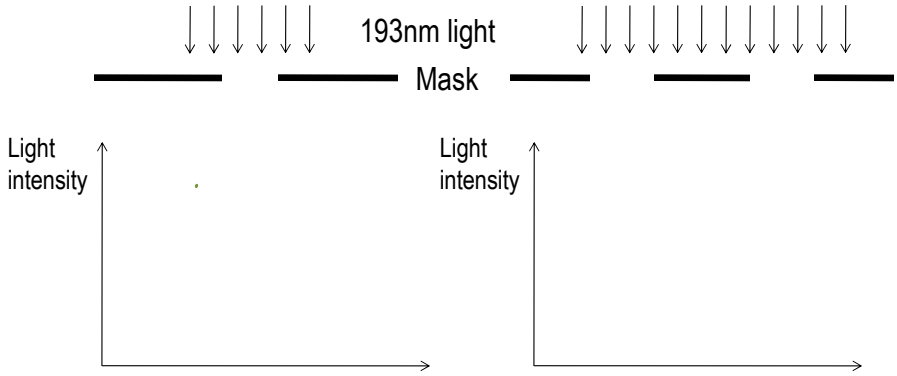
Sub-Wavelength Lithography

- Light projected through a gap



Sub-Wavelength Lithography

- CD ~ half pitch
- Decrease λ
  - Presently: 193 nm (ArF excimer laser)
  - (Distant?) future: EUV
- Increase $NA = n\sin\alpha$
  - Maximum n is 1 in air
  - Presently: ~0.92-1.35
  - Immersion
- Result: Shrinking k1
  - Presently: 0.35 – 0.4
  - Theoretical limit: 0.25

$$CD = k_1 \frac{\lambda}{NA}$$

$$CD_{min} = k_1 \frac{\lambda}{NA} = 0.25 \frac{193nm}{0.92} = 50nm$$

22nm pitches at (beyond) resolution limit

Intel

Node	CPP	MxP	FP
65nm	230	230	
45nm	160	160	
32nm	112.5	112.5	
22nm	90	80	60
14nm	70	52	42
10nm	54	36	34
7nm	37	32	

Litho: How to Enhance Resolution?

- Immersion
- Off-axis illumination
- Optical proximity correction
- Phase-shifting masks
- Double/multiple patterning
- EUV

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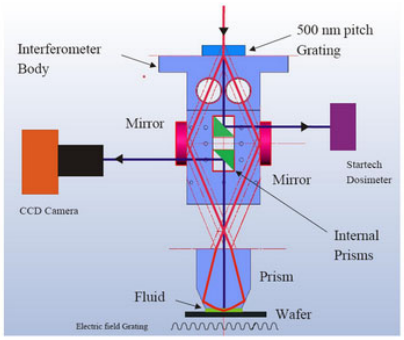
Litho (1): Immersion

- Project through a drop of liquid
- $n_{water} = 1.47$

$$CD_{\min} = k_1 \frac{\lambda}{NA} = 0.25 \frac{193nm}{1.35} = 35nm$$



IBM

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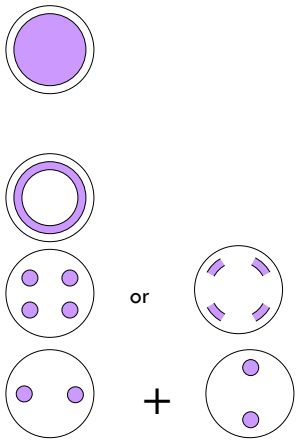
Litho (2): Illumination

- Amplifies certain pitches/rotations at expense of others
  - **Regular Illumination**
  - **Many off-axis designs (OAI)**
    - Annular
    - Quadrupole / Quasar
    - Dipole



A.Kahng, ICCAD'03

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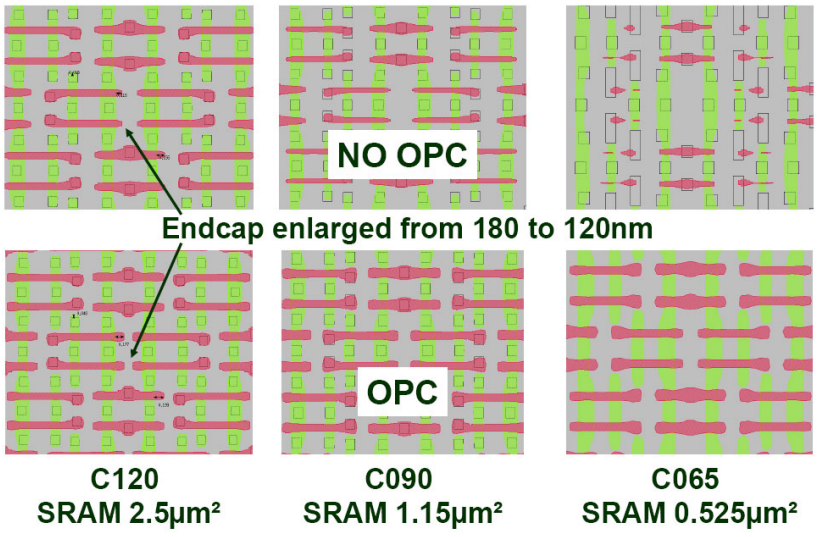
Litho (3): Resolution Enhancement



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Litho (3): OPC

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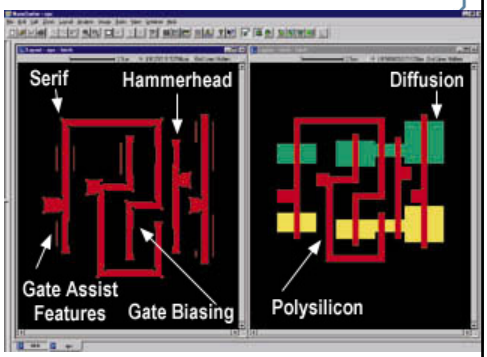
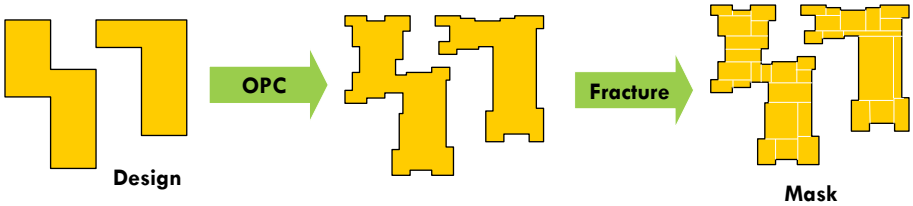
Litho (3): OPC

- Optical Proximity Correction (OPC) modifies layout to compensate for process distortions
  - Add non-electrical structures to layout to control diffraction of light
  - Rule-based (past) or model-based





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Inverse Lithograpphy Techniques

- OPC vs. ILT

Optical Proximity Correction | **Inverse Lithography Technology**

45nm node	28nm node	14nm node	7nm node
without OPC	normal OPC	normal ILT	ideal ILT

https://semiengineering.com/what-happened-to-inverse-lithography/

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Extreme Ultraviolet Lithography

- Wavelength $\lambda = 13.5$nm
- Lower wafer throughput
- Simpler design rules (single patterning)
- Used on critical layers
- First deployed by Samsung in 7nm node (Exynos 9825 SoC)
  - Also used by Intel in 7nm, TSMC in 5nm [J.C. Liu, IEDM'20]

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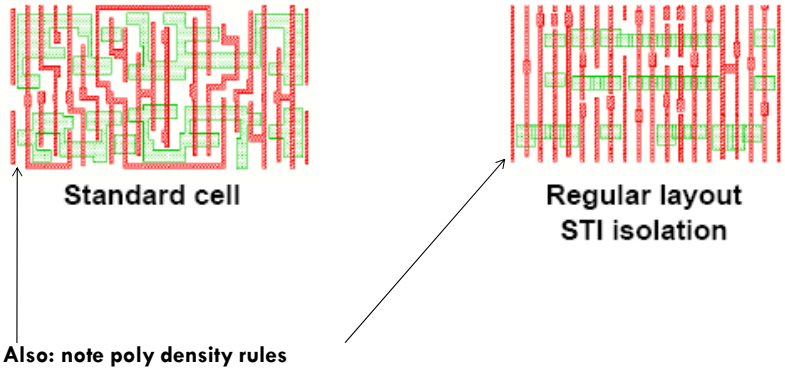
Litho (4): Restricted Design Rules



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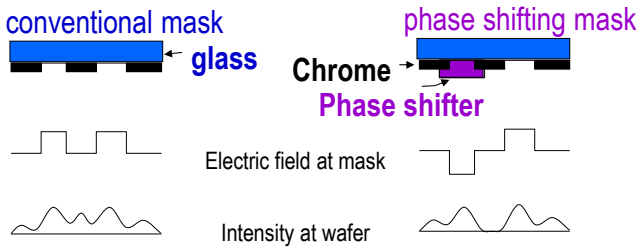
Litho (5): Phase-Shift Masks

- Phase Shifting Masks (PSM)
  - Creates interference fringes on the wafer →Interference effects boost contrast →Phase Masks can make extremely small lines



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Litho (6): Double Patterning

- Double exposure double etch
  - Double exposure double etch
  - Pitch split, litho-etch-litho-etch (LELE)
- Self-aligned methods
  - Self-aligned double patterning
  - Self-aligned quadruple patterning

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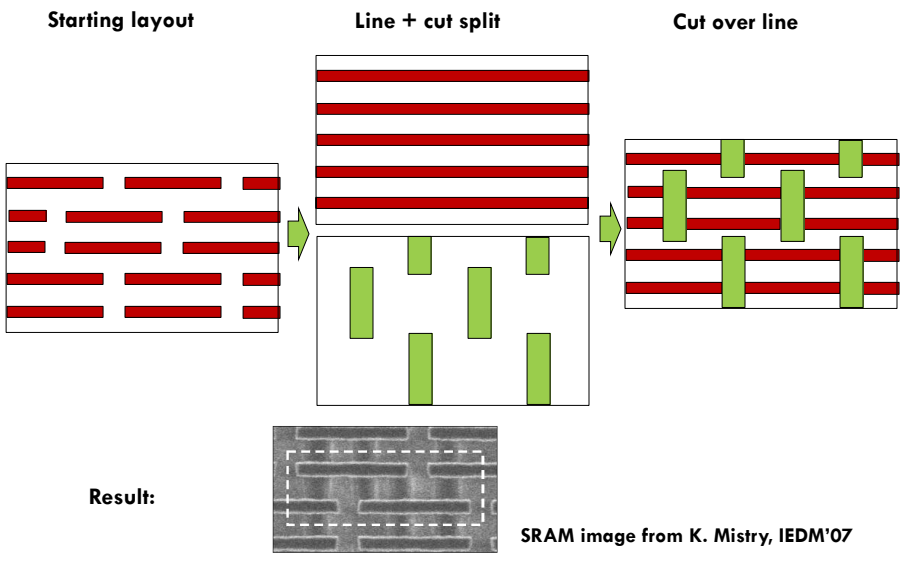
Double-Exposure Double-Etch



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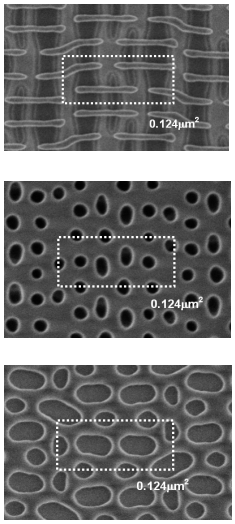
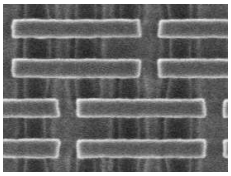
32nm Examples

Single exposure



Double exposure



IEDM'08

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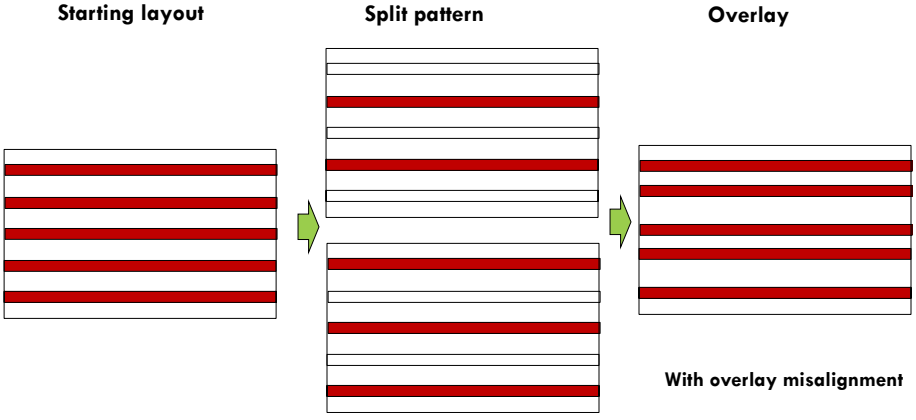
Pitch-Split Double Exposure



Also called litho-etch-litho-etch (LELE)

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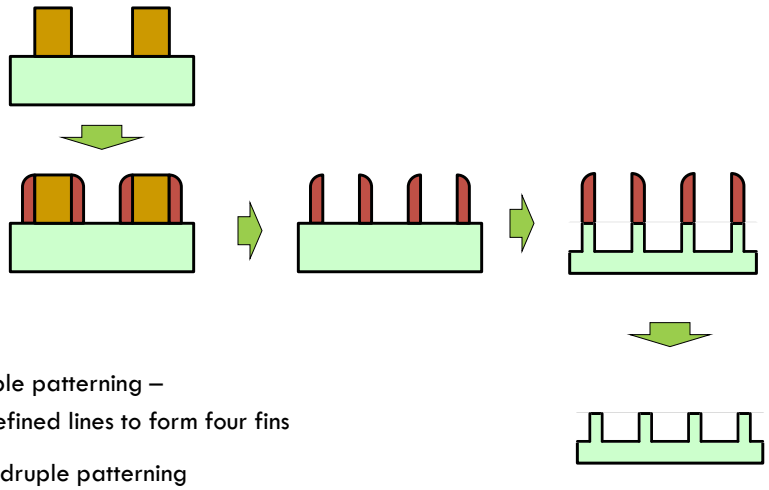
Self-Aligned Double Patterning (SADP)



- SADP: Double patterning –
  Two litho-defined lines to form four fins
- SAQP: Quadruple patterning

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Litho: Design Implications

- Forbidden directions
  - Depends on illumination type
  - Poly lines in other directions can exist but need to be thicker
- Forbidden pitches
  - Nulls in the interference pattern
  - Multiple patterning
- Forbidden shapes in PSM, multiple-patterning
- Assist features
  - If a transistor doesn't have a neighbor, let's add a dummy

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Litho: Current Options (Beyond 10nm)

- Multiple patterning
  - NA ~ 1.2-1.35
- EUV lithography
  - λ = 13.5nm

Normalized wafer cost adder*	
SE	1
LELE	2.5
LELELE	3.5
SADP	2
SAQP	3
EUV SE	4
EUV SADP	6

*TEL™ Internal calculation

Cost adder reduced with increased power/throughput of EUV

A. Raley, SPIE'16

Summary

- Transistors are changing
  - Dennard's scaling ended around 2005
  - Moore's Law is ending
- FinFET and FDSOI processes deployed now
  - Expected to be replaced by nanosheets
- Lithography and manufacturing restrict design rules
  - Need to be aware of implications on design
- More changes coming: forksheets, buried power rails, chiplets – 2.5D and 3D

Next Lecture

- Chiplets, 3D integration, interfaces
- Features of modern processes