inst.eecs.berkeley.edu/~eecs251b

# EECS251B : Advanced Digital Circuits and Systems

## Lecture 1 – Introduction

**Borivoje Nikolić**
**Vladimir Stojanović**
**Sophia Shao**

**Tuesdays and Thursdays 9:30-11am**

**Cory 540AB**



1

## Class Goals and Expected Outcomes

2

## Practical Information

- **Instructors:**
  - **Borivoje Nikolić**
    **Physical location (some day): Cory Courtyard , 3-9297, bora@eecs**
    **Office hours: Th 11am-12pm, or by appointment**
  - **Vladimir Stojanović**
    **Office hours: TBD**
  - **Sophia Shao (ysshao@berkeley.edu)**
    **Office hours: Tu 2pm-3pm, or by appointment**
- **GSI:**
  - **Erik Anderson erik.f.anderson@berkeley**

**Class Discussion**
**http://piazza.com/berkeley/spring2022/eecs251b**
**Sign up for Piazza!**

**Class Web page**
**inst.eecs.berkeley.edu/~eecs251b**

3

## Class Topics

- This course aims to convey a knowledge of advanced concepts of digital circuit and system design in state-of-the-art technologies.
  - Emphasis is on the circuit and system design and optimization for both energy efficiency and high performance for use in a broad range of applications, from edge computing to datacenters. Special attention will be devoted to the most important challenges facing digital circuit designers in the coming decade. The course is accompanied with practical laboratory exercises that introduce students to modern tool flows.
- We will use qualitative analysis when practical
- Many case studies will be used to highlight the enabling design techniques

4

## EECS251A vs. EE251B

- EECS 251A:
  - Emphasis on digital logic design
  - (Very) basic transistor and circuit models
  - Basic circuit design styles
  - First experiences with design – creating a solution given a set of specifications
  - A complete pass through the design process
- EECS 251B:
  - Understanding of technology possibilities and limitations
  - Transistor models of varying accuracy
  - Design under constraints: power-constrained, flexible, robust,…
  - Learning more advanced techniques
  - Study the challenges facing design in the coming years
  - Creating new solutions to challenging design problems, design exploration

5

## Special Focus in Spring 2021

- SoC systems and components
- Current technology issues
- Process variations
- Robust design
- Memory
- Energy efficiency
- Power management

6

## Class Topics

- Module 1: Fundamentals – SoC design template, languages (1.5 weeks)
- Module 2: Current technologies (1 wk)
- Module 2: Models – From devices to gates, logic and systems (2 wks)
- Module 3: Design for performance (1.5 wks)
- Module 4: Memory, SRAM, variability, scaling options (2.5 wks)
- Module 5: Energy-efficient design (3 wks)
- Module 6: Clock and power distribution (1 week)
- Project presentations, final exam (1 week)

7

## Class Organization

- 5 (+/-) assignments, with embedded labs (20%)
- 4 quizzes (10%)
- 1 term-long design project (40%)
  - Phase 1: Topic selection (Feb 24, after ISSCC)
  - Phase 2: Study (report by March 18, before Spring break)
  - Phase 3: Design (report in RRR week)
  - Presentations, May 2, afternoon
- Final exam (30%) (Thursday, April 28, in-class)

8

## Class Material

- Recommended text: J. Rabaey, "Low Power Design Essentials," Springer 2009.
  - Available at link.springer.com
- Other reference books:
  - "VLSI Design Methodology Development" by, T. Dillinger, Pearson 2019.
  - "Design of High-Performance Microprocessor Circuits," edited by A. Chandrakasan, W. Bowhill, F. Fox (available on-line at Wiley-IEEE), Wiley 2001.
  - "CMOS VLSI Design," 4th ed, by N.Weste, D. Harris
  - "Digital Integrated Circuits - A Design Perspective", 2nd ed. by J. M. Rabaey, A. Chandrakasan, B. Nikolić, Prentice-Hall, 2003.

9

## Class Material

- List of background material available on website
- Selected papers will be made available on website
  - Linked from IEEE Xplore and other resources
  - Need to be on campus to access, or use library proxy, library VPN (check http://library.berkeley.edu)
- Class notes on website

10

## Reading Assignments

- Three types of readings:
  - Assigned reading, that should be read before the class
  - Recommended reading that covers the key points covered in lecture in greater detail
  - Occasionally, background material will be listed as well

11

## Reading Sources

- IEEE Journal of Solid-State Circuits (JSSC)
- IEEE International Solid-State Circuits Conference (ISSCC)
- Symposium on VLSI Technology and Circuits (VLSI)
- Other conferences and journals

12

## Project Topics

- Focus this semester: Memories, power management, clocking
- Project teams: 2+ members, proportional to the size of the project
  - Can also do a bigger project merging with 290C or 252 classes
- More details in Week 2

13

## Tools

- 7nm predictive model (ASAP7), with (mostly) complete design kit
  - Or Intel 16 process if enrolled in 290C as well
- Cadence, Synopsys, available on instructional servers
- Berkeley's open-source flows and tools
  - Chipyard, Hammer
- Other open-source models

14

## Zoom

- Will post recordings. But focus on interactive lectures.
  - May pre-record some modules in advance
- Course notes available in advance.
- Be engaged in the discussions. You are part of the learning process.

15

## Trends and Challenges in Digital Integrated Circuit Design

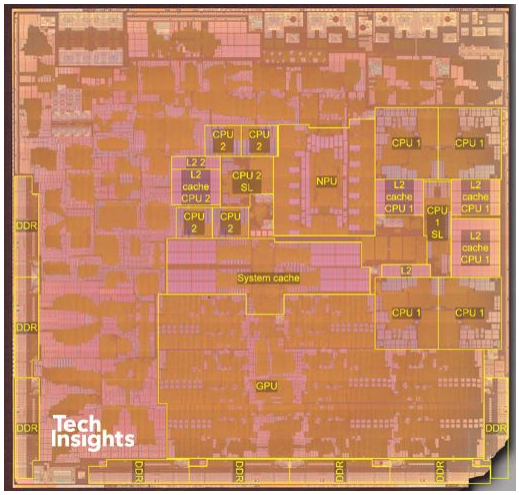
16

# Reading (Lectures 1 & 2)

- Assigned
  - Rabaey, LPDE, Ch 1 (Introduction)
  - G.E. Moore, *No exponential is forever: but "Forever" can be delayed!* Proc. ISSCC'03, Feb 2003.
  - T.-C. Chen, *Where CMOS is going: trendy hype vs. real technology.* Proc. ISSCC'06, Feb 2006.
- Recommended
  - Chandrakasan, Bowhill, Fox, Chapter 1 – Impact of physical technology on architecture (J.H. Edmondson),
  - S. Borkar, "Design challenges of technology scaling," IEEE Micro, vol.19, no.4, p.23-29, July-Aug. 1999.
- Background: Rabaey et al, DIC Chapter 3.
- The contributions to this lecture by a number of people (J. Rabaey, S. Borkar, etc) are greatly appreciated.

17

# Class in a Nutshell



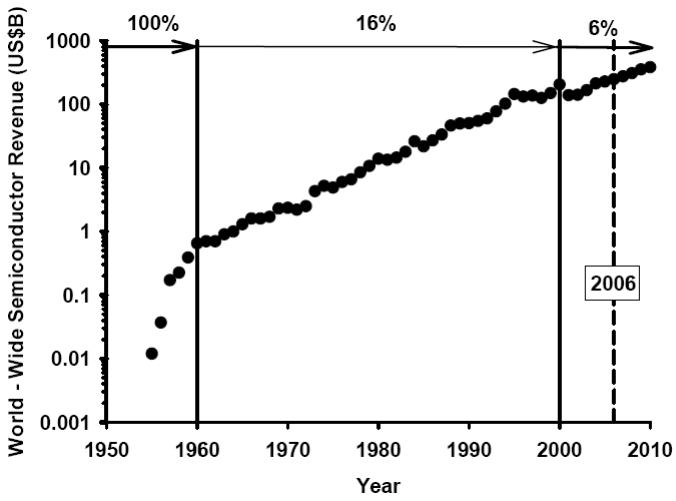

https://www.techinsights.com/blog/two-new-apple-socs-two-market-events-apple-a14-and-m1

- Design decisions needed to make a modern SoC
  - CPUs
  - SoC Components
  - Interconnect
  - Clocking
  - Memory
  - Power management



18

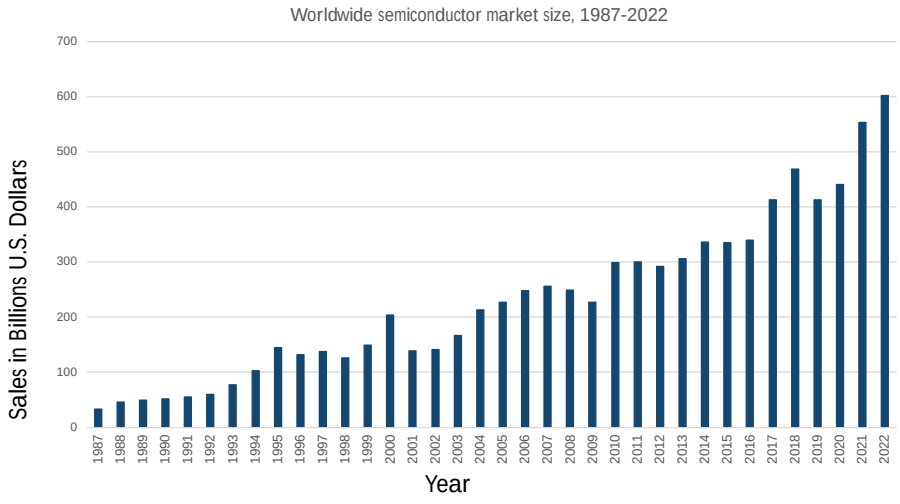
## Semiconductor Industry Revenues




M. Chang, "Foundry Future: Challenges in the 21st Century," ISSCC'2007

19

## Current State of Semiconductor Industry



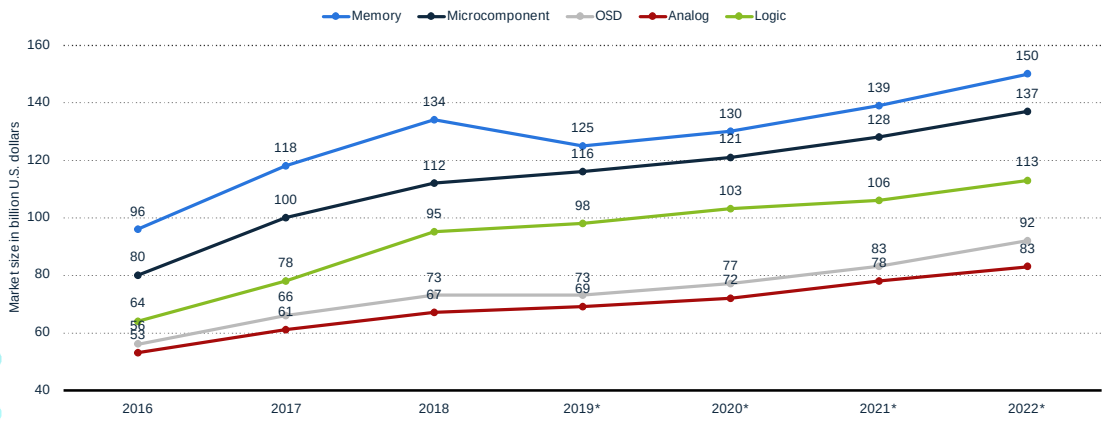

Source: Statista; https://www.statista.com/statistics/266973/global-semiconductor-sales-since-1988/

Current gross world product (GWP) ~ 88,000 billion (Wikipedia)

20

## Semiconductor industry market size by component worldwide from 2016 to 2022

Global semiconductor market size by component 2016-2022




**Note(s):** Worldwide; 2016 to 2019
Further information regarding this statistic can be found on page 8.
**Source(s):** PwC; ID 512593

statista

6

21

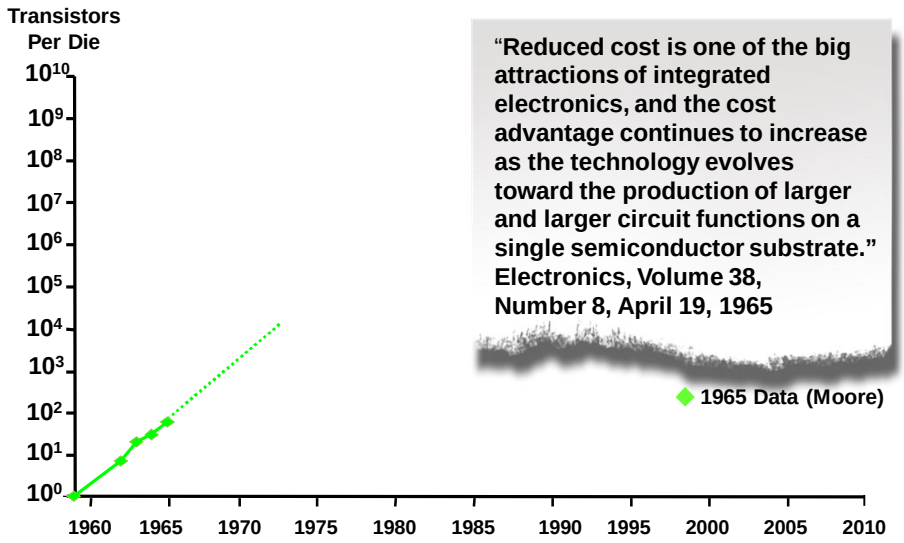
## Moore's Law

- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 12 months.
- He made a prediction that semiconductor technology will double its effectiveness every ~~12~~ ~~18~~ 24 months

"*The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term, this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000.*"
Gordon Moore, Cramming more Components onto Integrated Circuits, (1965).

22

# Moore's Law - 1965

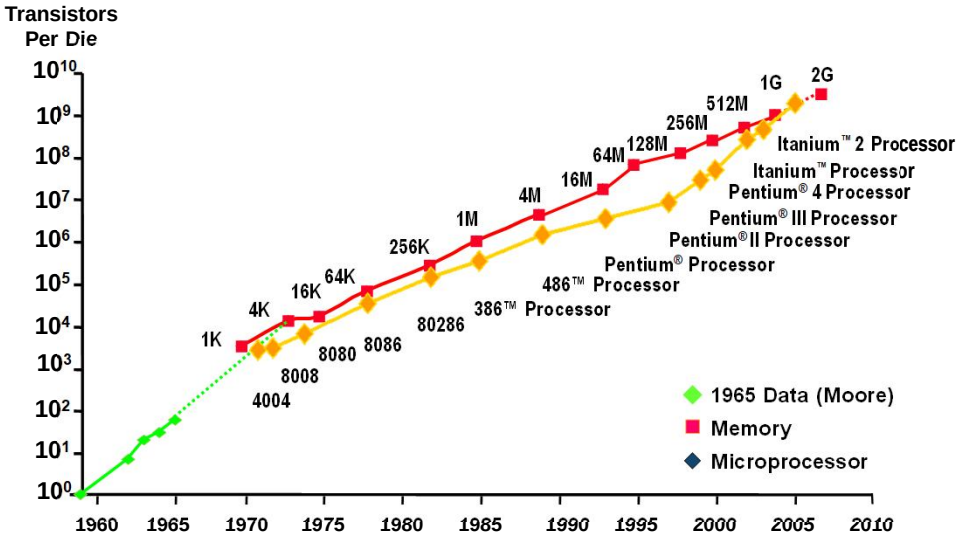



Graph from S.Chou, ISSCC'2005

Source: Intel

23

# Moore's Law - 2005

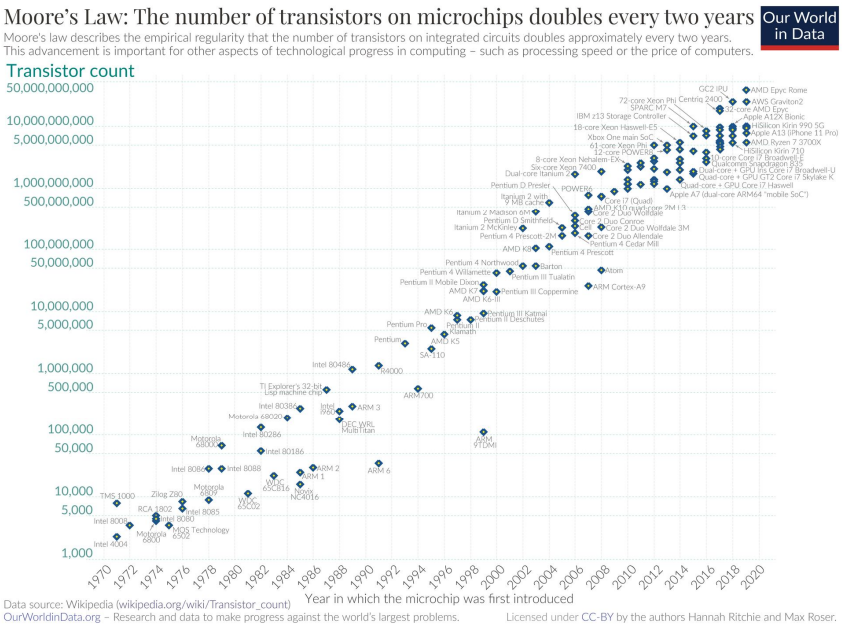



Graph from S.Chou, ISSCC'2005

Source: Intel

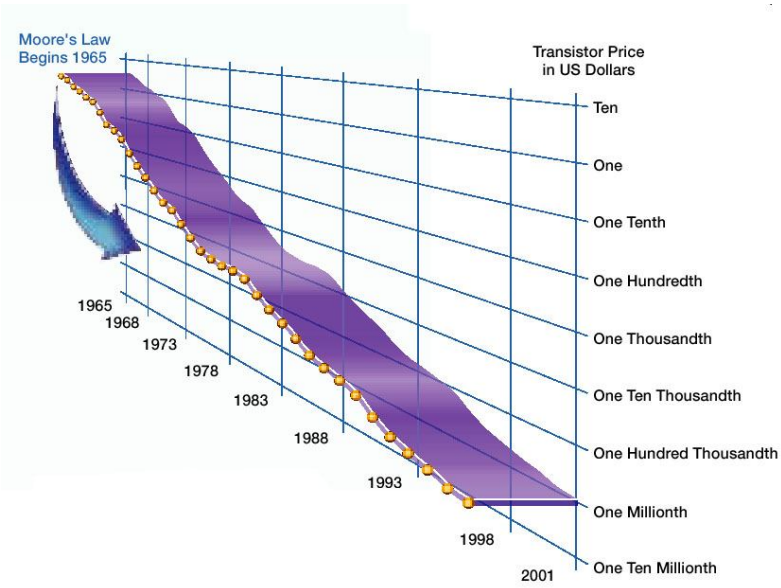
24

# Moore's Law - 2020




25

# Moore's Law and Cost



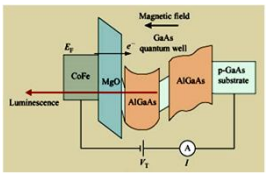

26

## Progress in Nano-Technology

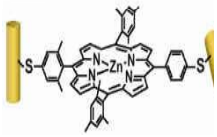
Spintronic Storage

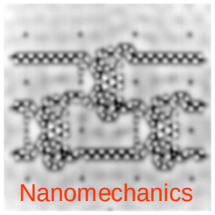
Millipede

Spintronic device



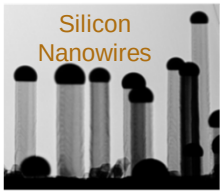

Molecular Electronics

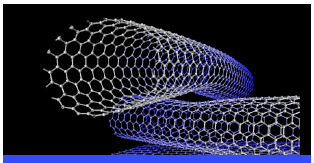




Nanomechanics

Silicon Nanowires





Carbon Nanotubes

T.C. Chen, Where Si-CMOS is going: Trendy Hype vs. Real Technology, ISSCC'06

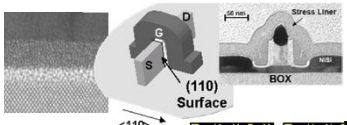
27

## Technology Strategy / Roadmap

2000 2005 2010 2015 2020 2025 2030

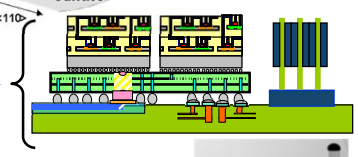
**Plan A: Extending Si CMOS**

R D



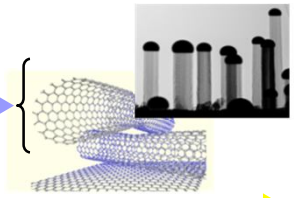

**Plan B: Subsytem Integration**

R D



**Plan C: Post Si CMOS Options**

R R&D



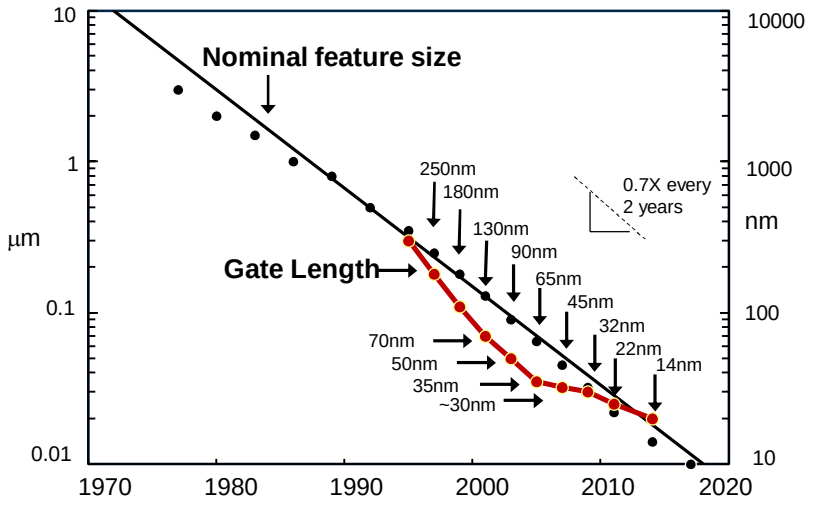
**Plan Q: Quantum Computing**

R D

T.C. Chen, Where Si-CMOS is going: Trendy Hype vs. Real Technology, ISSCC'06

28

## Printed vs. Physical Gate



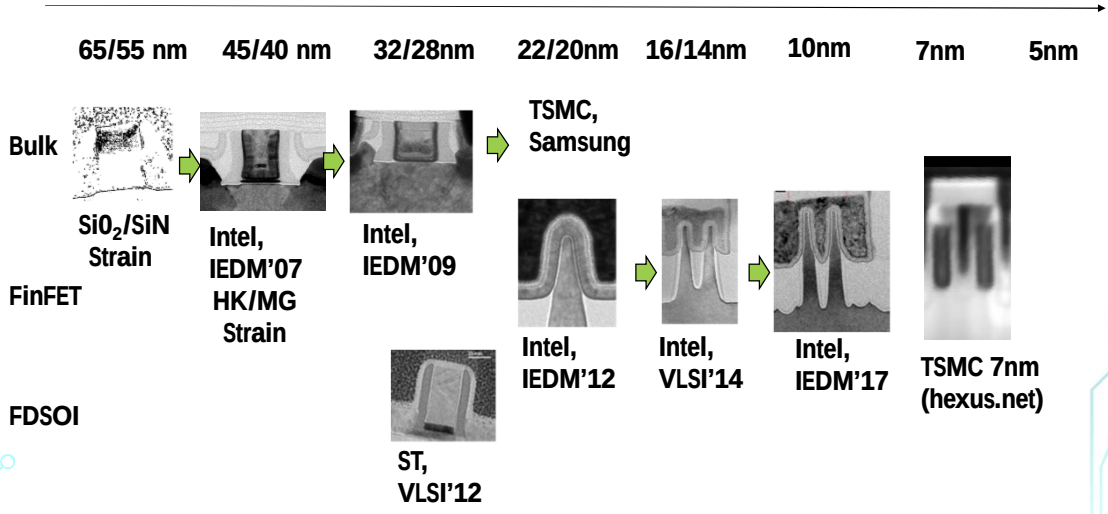

**Physical gate length > nominal feature size after 22nm**

Source: Intel, IEDM presentations

29

## Transistors are Changing

- From bulk to finFET and FDSOI

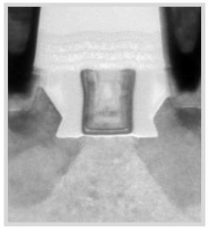


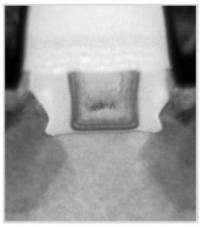

30

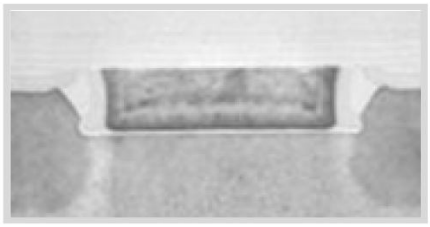
## Varying Flavors in Each Node

- 32nm (and 28nm): Various flavors - Intel

| Logic Transistor | Low Power Transistor | HV I/O Transistor |
|---|---|---|
| (HP or SP) | (LP) | (1.8 V or 3.3 V) |







**Lg = 30/34nm** **Lg = 46nm** **Lg > 140nm**

C.-H. Jan, IEDM'09, P. VanDerVoorn, VLSI Tech'10

31

## 5nm Flavors

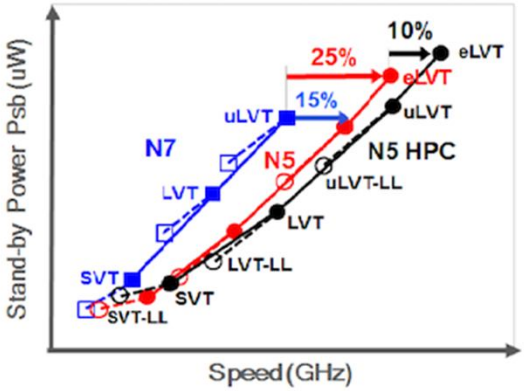


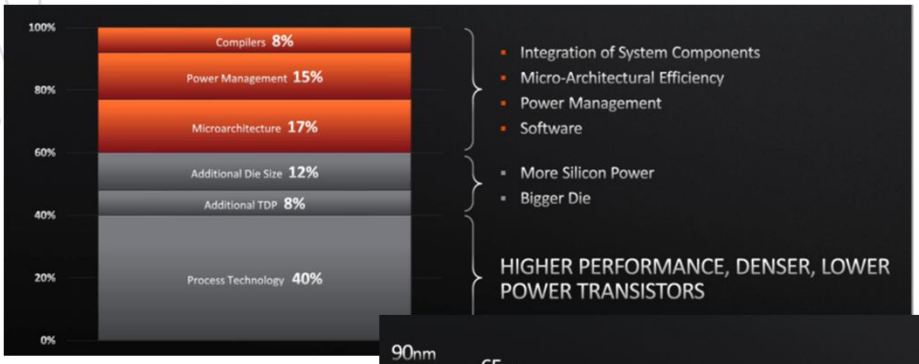

Fig.3 The 5nm also offers a set of critical HPC features. Extremely LVT (eLVT) for 25% faster peak speed over 7nm, and HPC 3-fin standard cell for additional 10% performance.

TSMC, IEDM'19

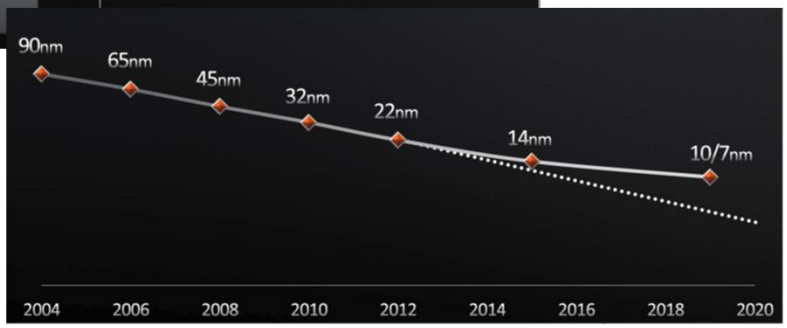


32

## Putting Scaling in Perspective




Performance gains over the past decade

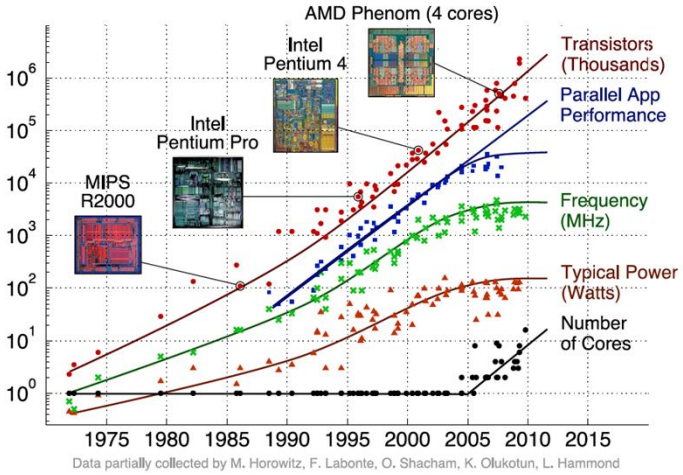



Lisa Su, HotChips'19 keynote



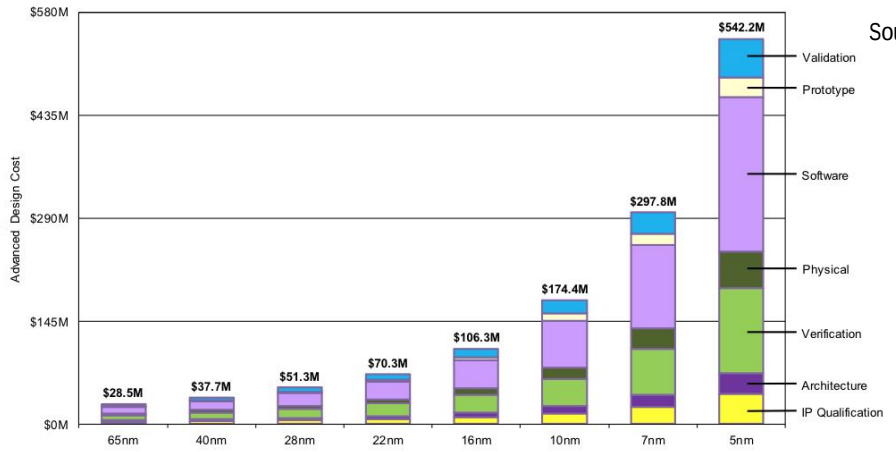


## Power and Performance Trends




- What do we do next?

## Cost Of Developing New Products




Source: IBS

- These are non-recurring (NRE) costs, need to be amortized over the lifetime of a product
- We will attempt to dismantle this…

35

## Major Roadblocks

1. Managing complexity
   How to design a 10 billion (100 billion) transistor chip?
   And what to use all these transistors for?
2. Cost of integrated circuits is increasing
   It takes >>$10M to design a chip
   Mask costs are many $M in 16nm technology
   Wafer costs are increasing
3. Power as a limiting factor
   End of frequency scaling
   Dealing with power, leakages
4. Robustness issues
   Variations, SRAM, memory, soft errors, signal integrity
5. The interconnect problem

36

## Next Lecture

- Chipyard as an SoC template

37