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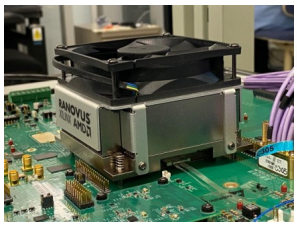
EECS251B : Advanced Digital Circuits and Systems

Lecture 14 – Latches

Borivoje Nikolić, Vladimir Stojanović, Sophia Shao

AMD Allies with Ranovus on Data Center Photonics Module
March 6, 2022, EETimes



The co-packaged optical (CPO) demonstration system built by Xilinx and Ranovus. It incorporates the former's Versal ACAP with the latter's Odin Analog-Drive CPO 2.0. (Source: Ranovus)

1

Recap

- Flip-flop-based (edge-triggered) timing dominates today
- Latch-based timing can increase performance, but needs extra care
- There is also asynchronous design

2

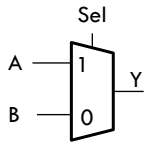
Design for Performance

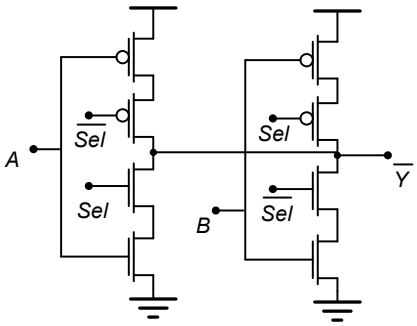
Latch Design

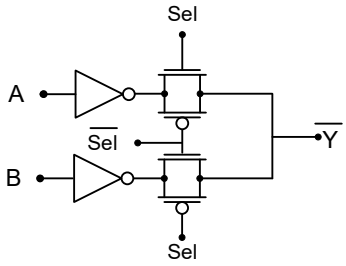
3

Review: MUX

- 2-input MUX

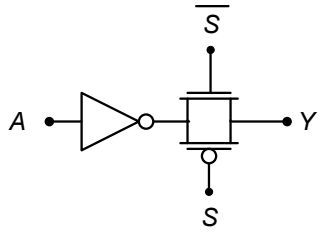


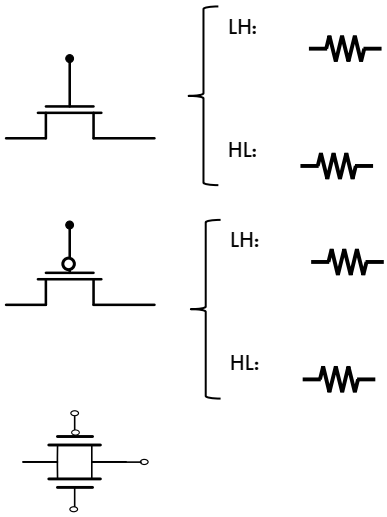




4

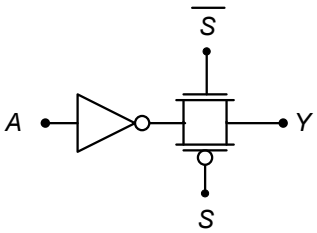
Review: Transmission Gates

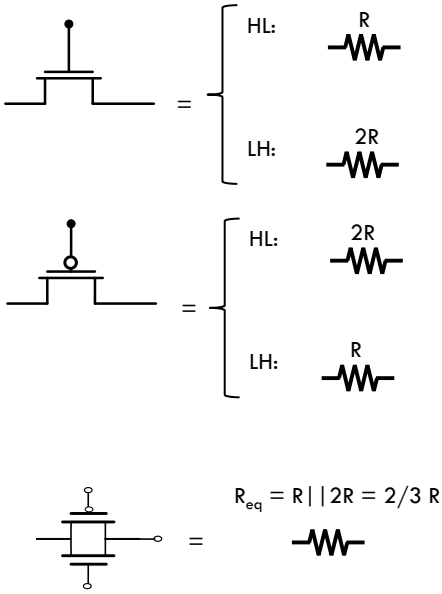




5

Review: Transmission Gates

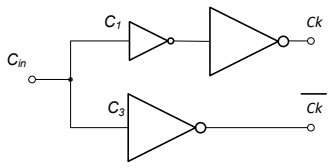




6

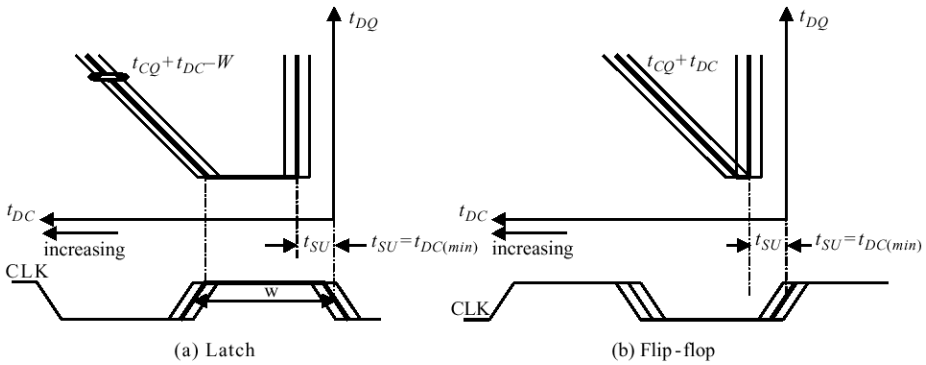
Generating Complementary Clocks

- Inverter fork



7

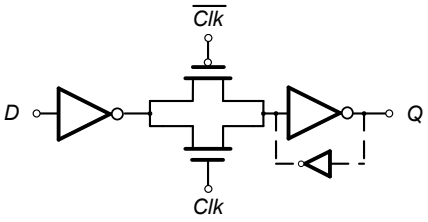
Latch vs. Flip-Flop



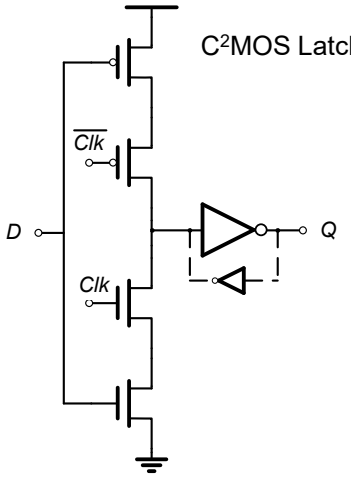
8

Latches

Transmission-Gate Latch



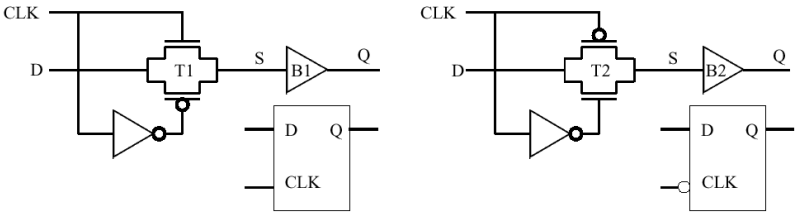
C²MOS Latch



Usually without contention

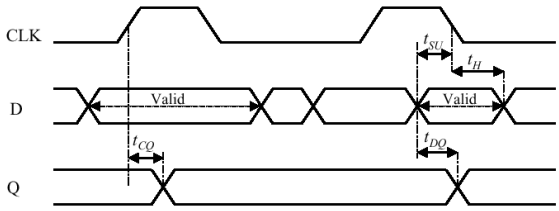
9

Latches



(a) The transparent high latch (THL)

(b) The transparent low latch (TLL)



(c) Timing waveforms for the THL

10

Announcements

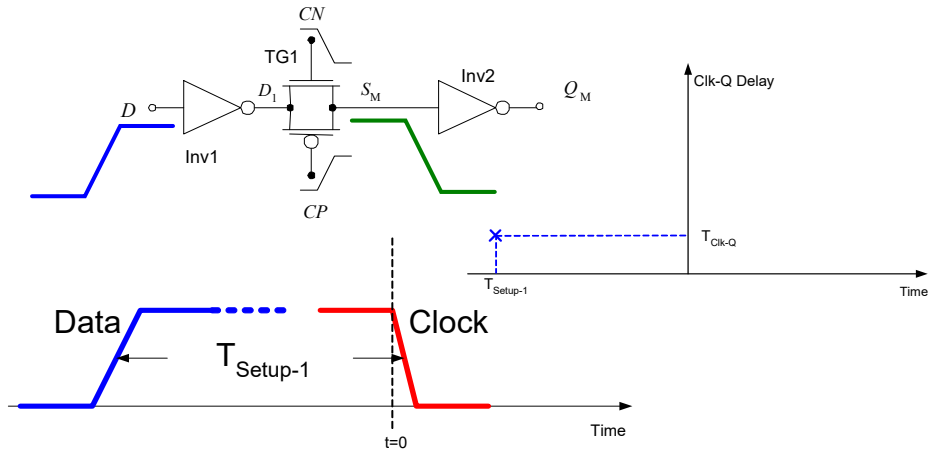
- Quiz 1 next Tuesday, in lecture
- Lab 5 due this week
- Midterm reports due next week
  - 4 pages, conference format

Design for Performance

Delay, Setup, Hold

Setup-Hold Time Illustrations

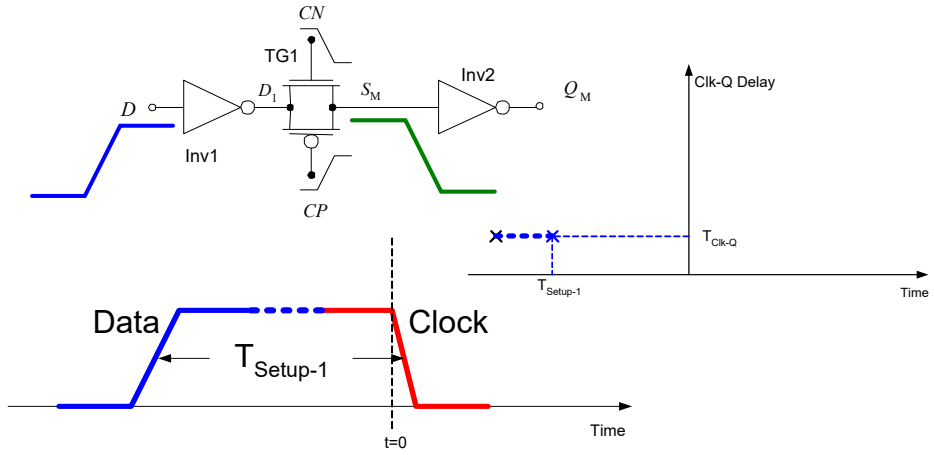
Circuit before clock arrival (Setup-1 case)



13

Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



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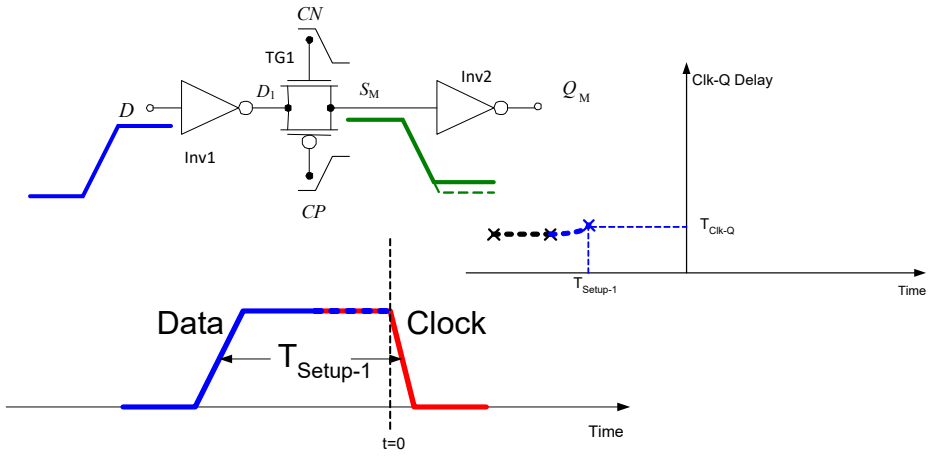
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



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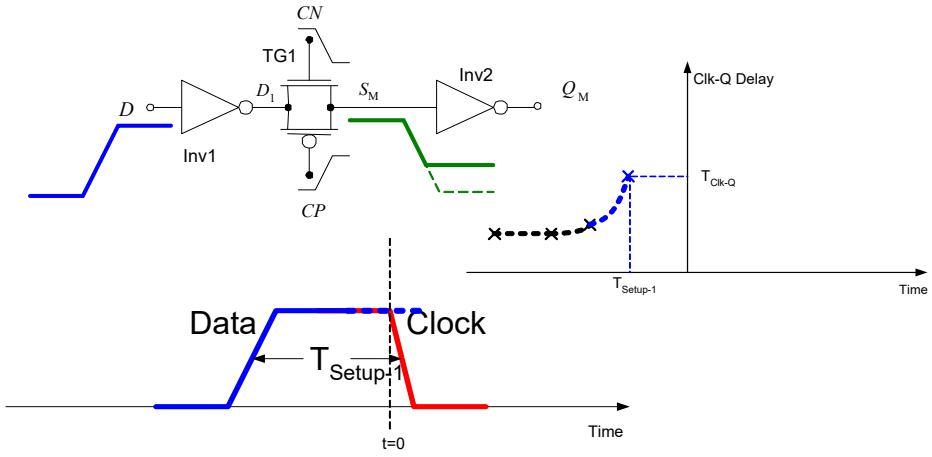
Setup-Hold Time Illustrations

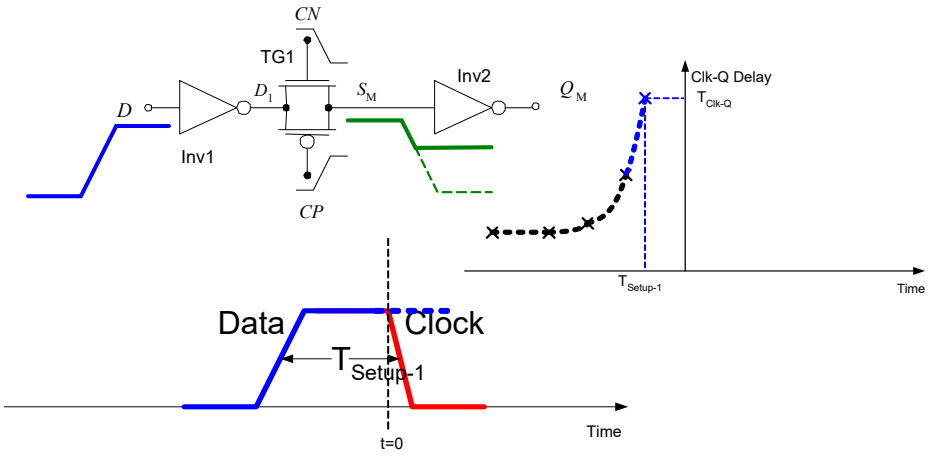
Circuit before clock arrival (Setup-1 case)



16

Setup-Hold Time Illustrations

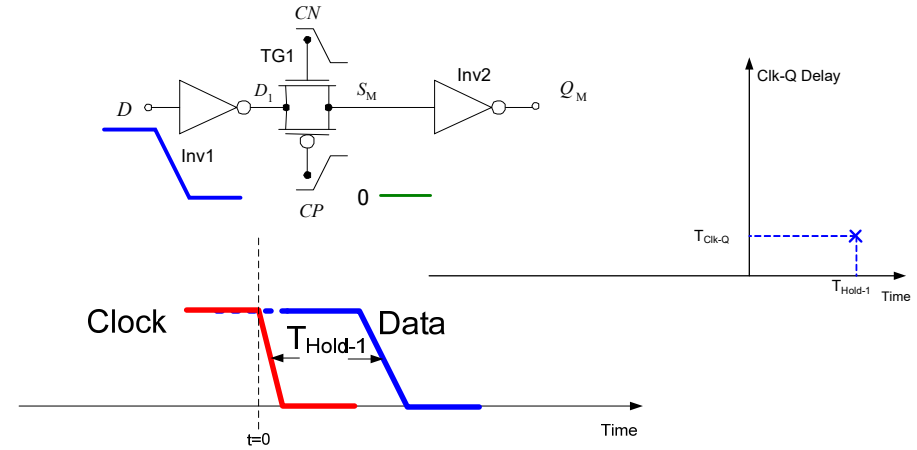
Circuit before clock arrival (Setup-1 case)



17

Setup-Hold Time Illustrations

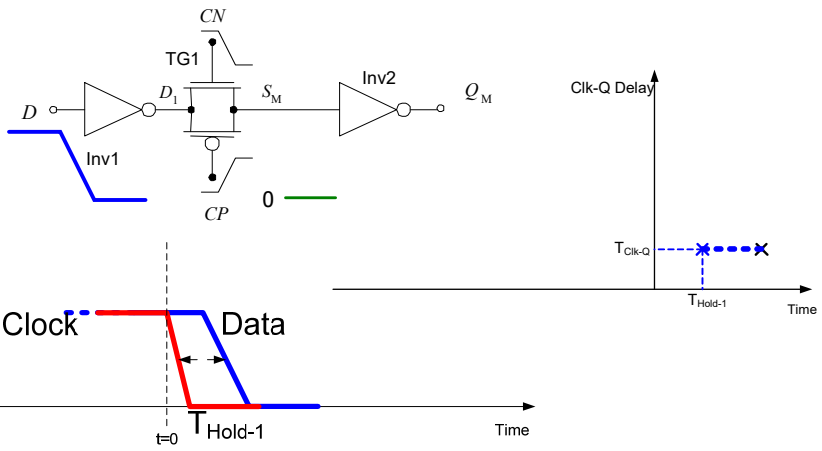
Hold-1 case



18

Setup-Hold Time Illustrations

Hold-1 case



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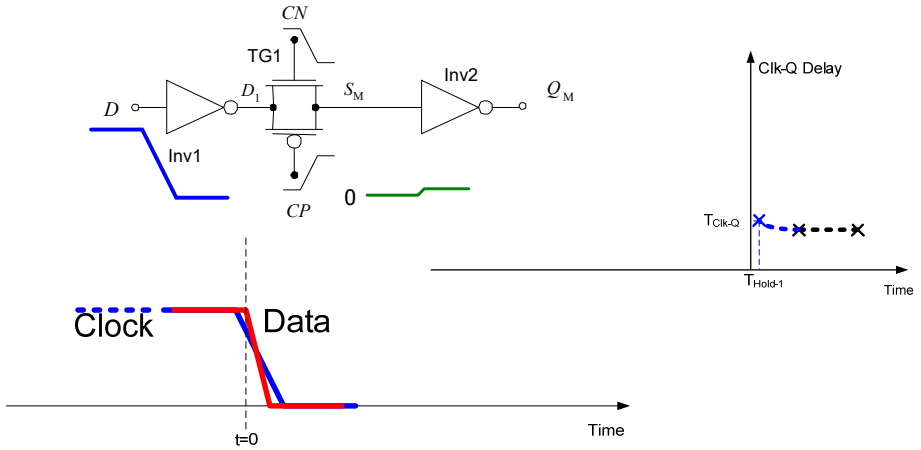
Setup-Hold Time Illustrations

Hold-1 case



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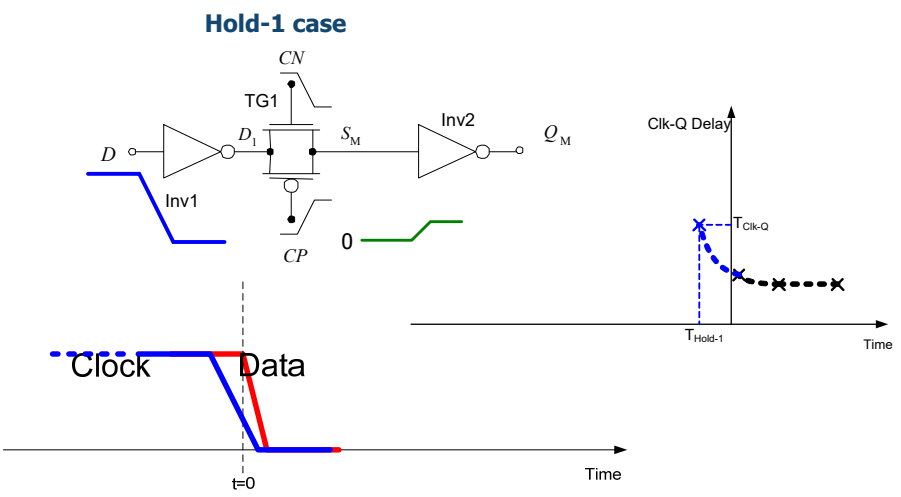
Setup-Hold Time Illustrations

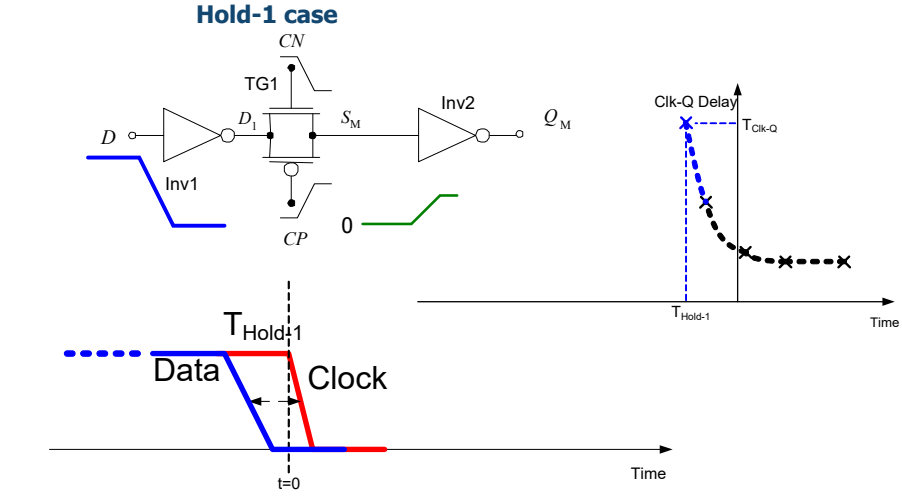
Hold-1 case



21

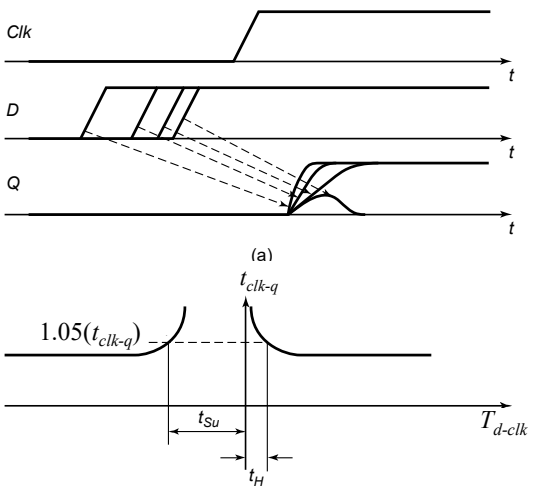
Setup-Hold Time Illustrations

Hold-1 case



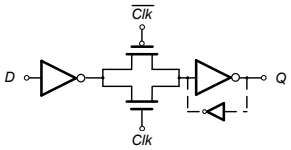
22

More Precise Setup Time



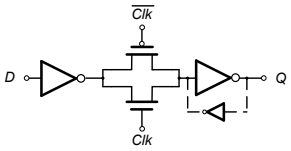
23

Latch t_{D-Q} and t_{Clk-Q}



24

t_{setup}



25

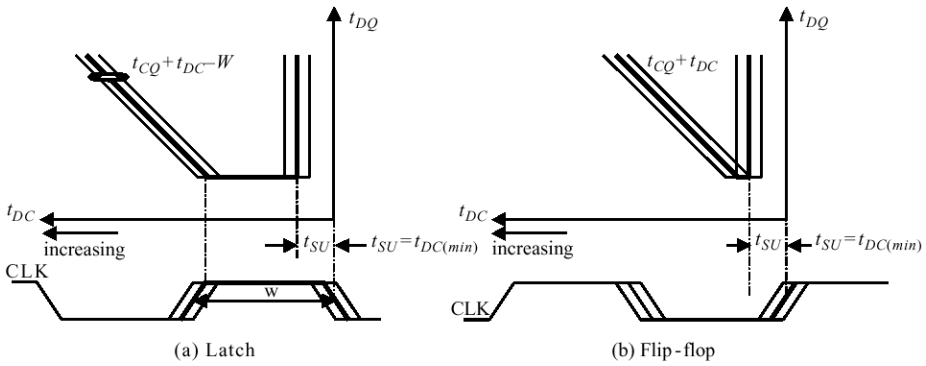
Flip-Flops

26

Key Point

- Two ways to design a flip-flop
  - Latch pair (large majority)
  - Pulsed latch

Latch vs. Flip-Flop



Flip-Flops

- Performance metrics
- Delay metrics
  - Insertion delay
  - Inherent race immunity
  - 'Softness' (Clock skew absorption)
  - Inclusion of logic
  - Small (+constant) clock load
- Power/Energy Metrics
  - Power/energy
- Design robustness
  - Noise immunity

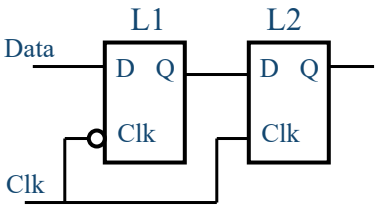
29

Scan Test

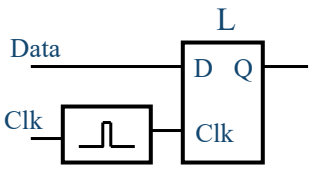
30

Types of Flip-Flops

Latch Pair

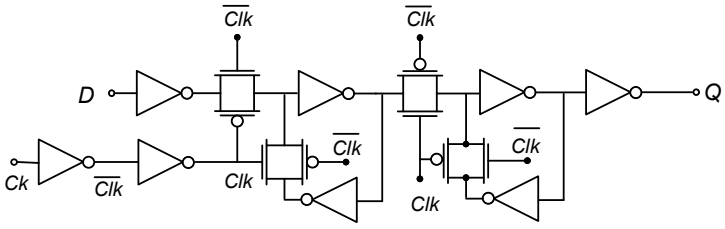


Pulse-Triggered Latch



31

Flip-Flop (Latch Pair) Clk-Q, setup, hold



32

Flip-Flop Timing Characterization

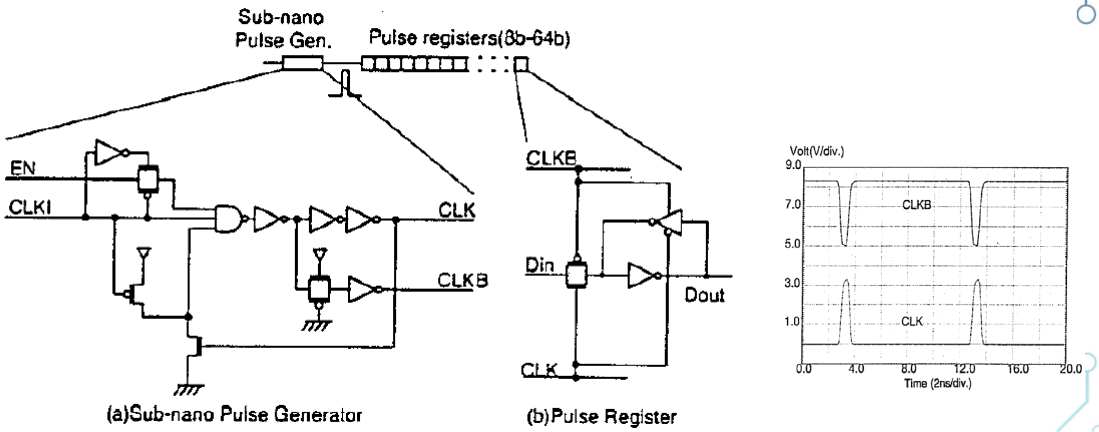
- Combinational logic delay is a function of output load and input slope
- Sequential timing (flip-flop):
  - t_{clk-q} is function of output load and clock rise time
  - t_{Su}, t_H are functions of D and Clk rise/fall times

Pulse-Triggered Latches

- First stage is a pulse generator
  - generates a pulse (glitch) on a rising edge of the clock
- Second stage is a latch
  - captures the pulse generated in the first stage
- Pulse generation results in a negative setup time
- Frequently exhibit a soft edge property
- Note: power is always consumed in the pulse generator
  - Often shared by a group (register)

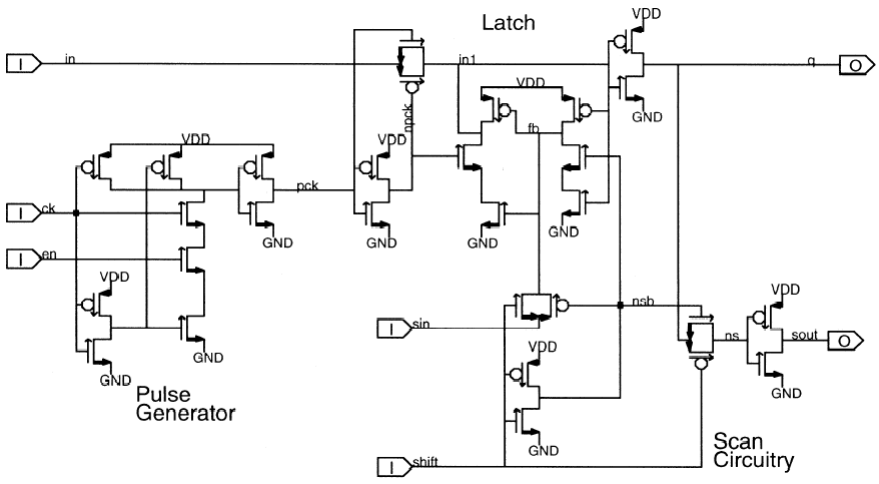
Pulsed Latch

Simple pulsed latch



Kozu, ISSCC'96

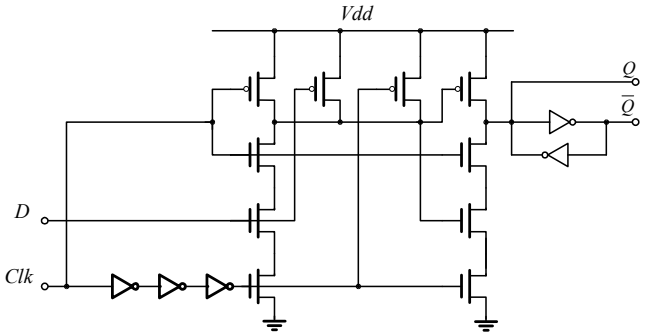
Intel/HP Itanium 2



Naffziger, ISSCC'02

Pulsed Latches

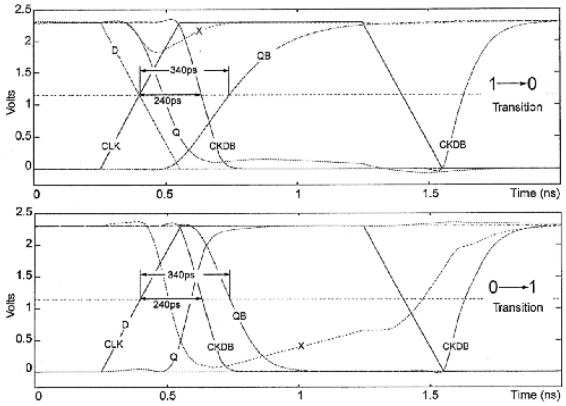
Hybrid Latch Flip-Flop, AMD K-6
Partovi, ISSCC'96



37

HLFF Operation

1-0 and 0-1 transitions at the input with 0ps setup time



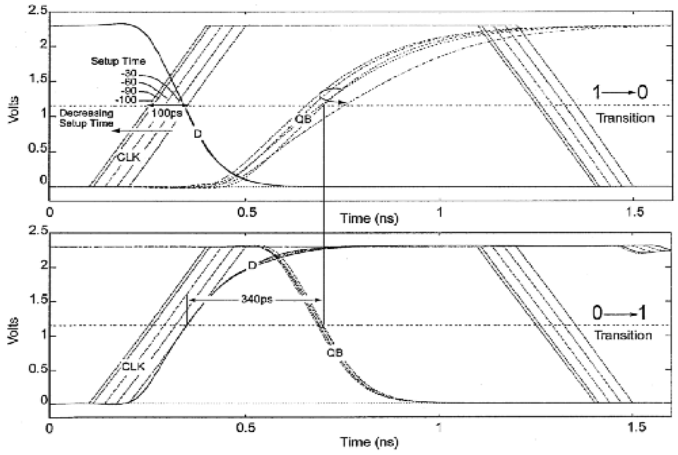
VDD=2.3v, 85°C, Typical Devices
C_{clk} = 60ff, C_{qb} = 300ff

$T_{cq} = T_{dq}$ = 340ps
T_{hold} = 180ps
$T_{su(min)}$ = -90ps

38

Hybrid Latch Flip-Flop

Skew absorption

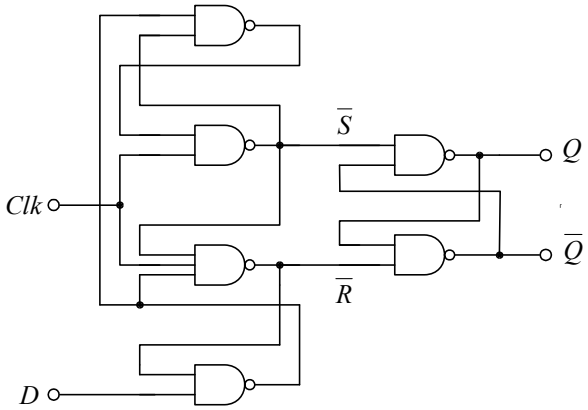


Partovi *et al*, ISSCC'96

39

Pulsed Latches

7474, from mid-1960's

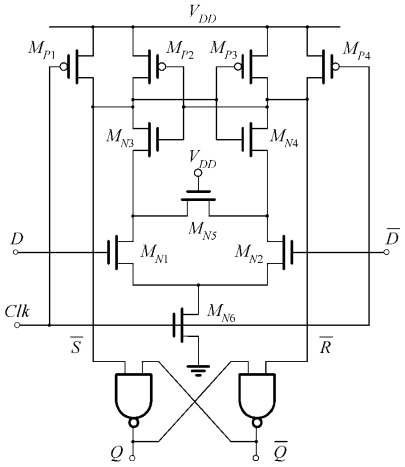


40

Pulsed Latches

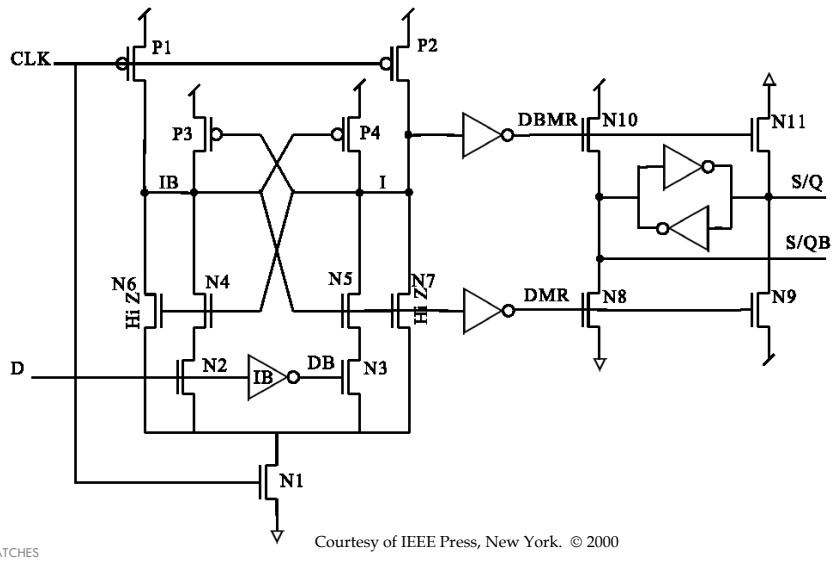
Sense-amplifier-based flip-flop, Matsui 1992.
DEC Alpha 21264, StrongARM 110

First stage is a sense amplifier, precharged to high, when *Clk* = 0
After rising edge of the clock sense amplifier generates the pulse on
S or *R*
The pulse is captured in
S-R latch
Cross-coupled NAND has different propagation delays of rising and falling edges



41

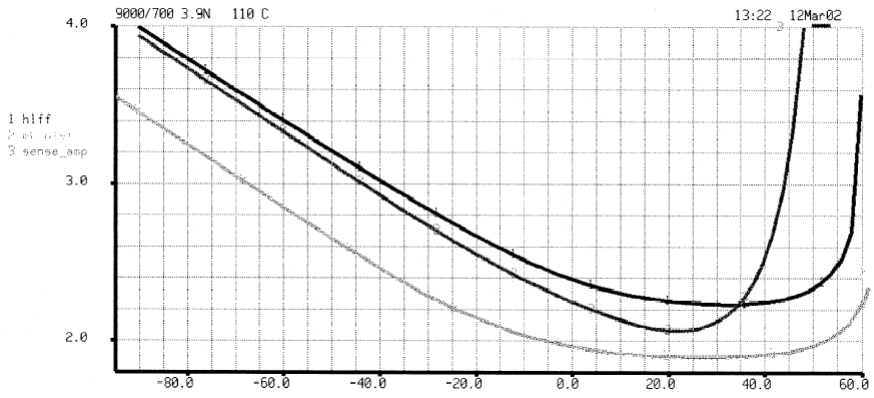
Sense Amplifier-Based Flip-Flop



Courtesy of IEEE Press, New York. © 2000

42

Sampling Window Comparison



Naffziger, JSSC 11/02

Summary

- Logical effort can be used to analyze latch timing
  - Clk-Q, setup, hold
- Flip-flops:
  - Latch pairs
  - Pulse triggered

Next Lecture

- Variability