EECS251B : Advanced Digital Circuits and Systems

Lecture 13 – Timing

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Universal Chiplet Interconnect Express (UCIe) Announced: Setting Standards For The Chiplet Ecosystem
March 2, 2022, AnandTech

To that end, today Intel, AMD, Arm, and all three leading-edge foundries are coming together to announce that they are forming a new and open standard for chiplet interconnects, which is aptly being named **Universal Chiplet Interconnect Express**, or **UCIe**.

www.uciexpress.org

UCIe
Universal Chiplet
Interconnect Express

Berkeley

Recap

- Standard cell architectures depend on technology, maximize density-performance-power
- Standard cell library
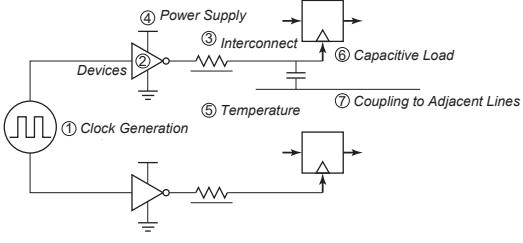   - Delay is tabulated, dependent on slope, load

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Design for Performance

Flip-Flop-Based Timing

Example Clock System

Courtesy of IEEE Press, New York. © 2000

Clock Nonidealities

- Clock skew
    - Spatial variation in temporally equivalent clock edges; deterministic + random, t_{SK}
- Clock jitter
    - Temporal variations in consecutive edges of the clock signal; modulation + random noise
    - Cycle-to-cycle (short-term) - t_{JS}
    - Long-term - t_{JL}
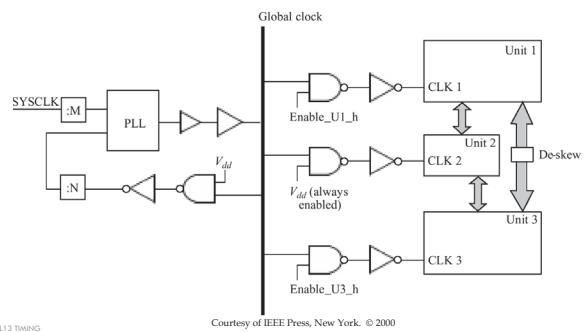- Variation of the pulse width
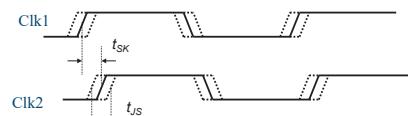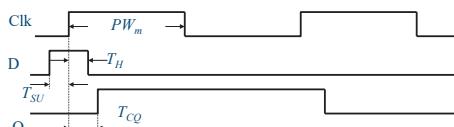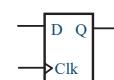   - for level-sensitive clocking

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Clock Skew and Jitter

- Both skew and jitter affect the effective cycle time
- Only skew affects the race margin, if jitter is from the source
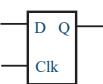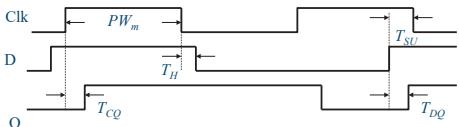   - Distribution-induced jitter affects both

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Clock Uncertainties

④ Power Supply
③ Interconnect
② Devices
⑥ Capacitive Load
① Clock Generation
⑤ Temperature
⑦ Coupling to Adjacent Lines

Sources of clock uncertainty

Flip-Flop Parameters

Delays can be different for rising and falling data transitions

Latch Parameters

D Q

Clk
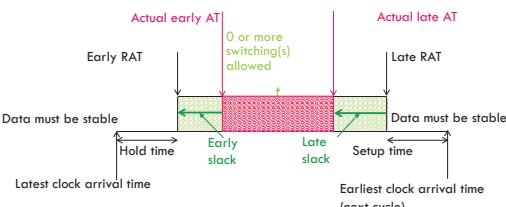
Unger and Tan
Trans. on Comp.
10/86

Clk PW_m

D

T_H

T_{SU}

Q

T_{CQ}

T_{DQ}

Delays can be different for rising and falling data transitions

Clock Constraints in Edge-Triggered Systems

Short path

De-skew

CL_{min}

D Q

CL_{max}

D Q

CLK1 CLK t_{CQ} Long path CLK2 CLK t_{CQ}

t_{SU}

$$t_{CL} \leq (t_{CY} - t_{SK} - t_{JS}) - (t_{SU} + t_{CQ})$$

$$t_{CL} \geq t_{SK} + (t_H - t_{CQ})$$

CLK1

$t_{CY} - t_{SK} - t_{JS}$

t_{SK}

CLK2

t_{SK}

t_{JS}

Pictorial View of Setup and Hold Tests

Actual early AT

Actual late AT

0 or more
switching(s)
allowed

Early RAT

Late RAT

Data must be stable

Data must be stable

Hold time

Early
slack

Late
slack

Setup time

Latest clock arrival time

Earliest clock arrival time
(next cycle)

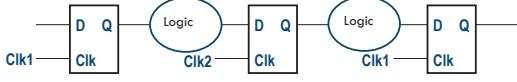ICCAD '07 Tutorial   Chandu Visweswariah

Latch Timing

Key Point
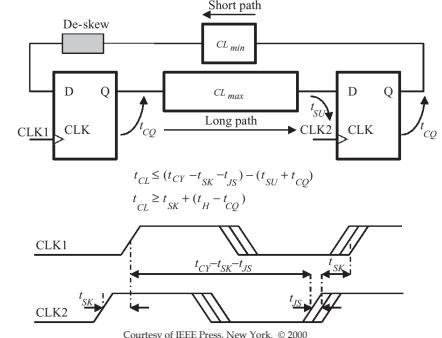
- Latch-based sequencing can improve performance, but is more complicated
  - Timing analysis not limited to a consecutive pair of latches
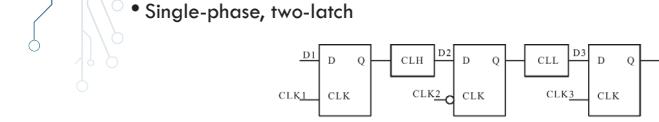
Latch Timing

t_{DQ}

D Q

Clk

t_{CQ}

**When data arrives
to transparent latch**

Latch is a 'soft' barrier

**When data arrives
to non-transparent latch**

Data has to be 're-launched'

Latch Sequencing

D Q

Logic

D Q

Clk Clk

Clk Clk

D Q

Logic

D Q

Logic

D Q

Clk1 Clk

Clk2 Clk

Clk1 Clk

Latch-Based Timing

- Single-phase, two-latch

D1 D Q CLH D2 D Q CLL D3 D Q

CLK1 CLK CLK2 CLK CLK3 CLK

t_{CY}

CLK1

t_{SU} $t_{SK} + t_{JS}$

D1

$t_{DQ} + t_{CLH}$

t_{SU} $t_{SK} + t_{JS}$

CLK2

$t_{DQ} + t_{CLL}$

D2

t_{SU} $t_{SK} + t_{JS}$

CLK3

t_{CY} D3

Pipe stage $i-1$ Pipe stage i Pipe stage $i+1$

As long as transitions are within the assertion period of the latch, no impact of position of clock edges
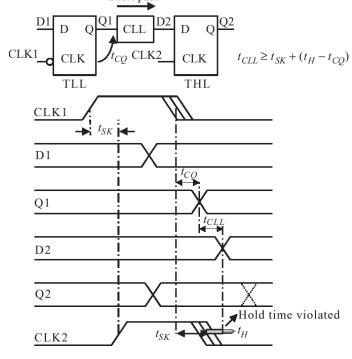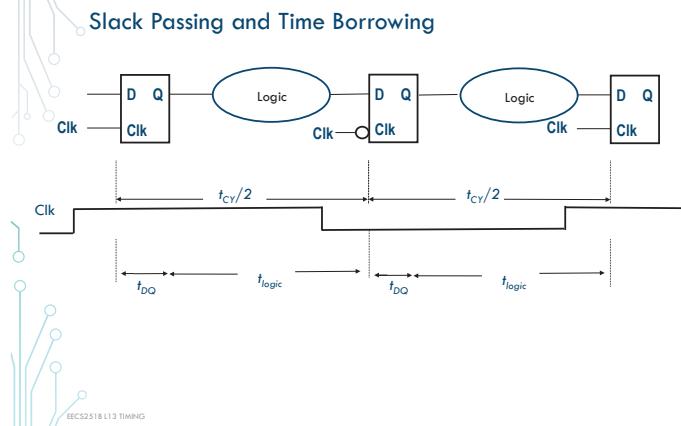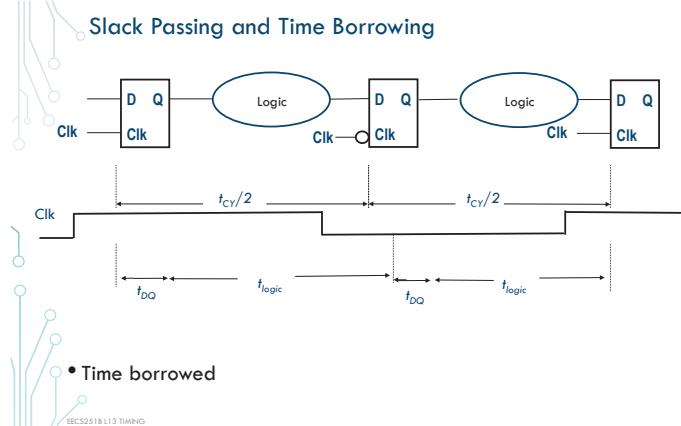
Latch Design and Hold Times

$$t_{CLL} \geq t_{SK} + (t_H - t_{CQ})$$
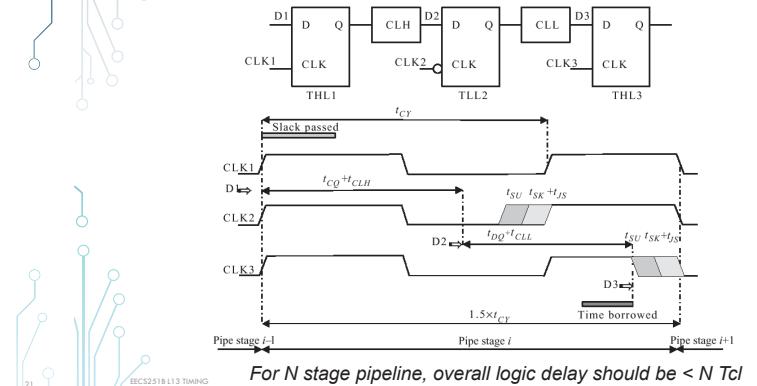
Soft-Edge Properties of Latches

- **Slack passing** – logical partition uses left over time (slack) from the *previous* partition
- **Time borrowing** – logical partition utilizes a portion of time allotted to the *next* partition
- Makes most impact in unbalanced pipelines

Bernstein et al, Chapter 8, Chandrakasan, Chap 11 (by Partovi)
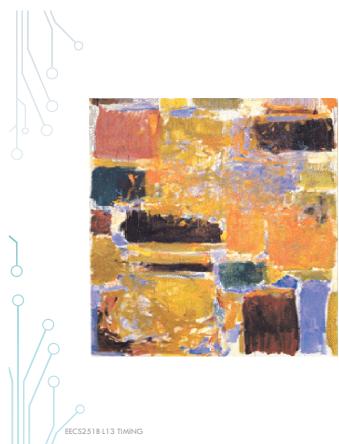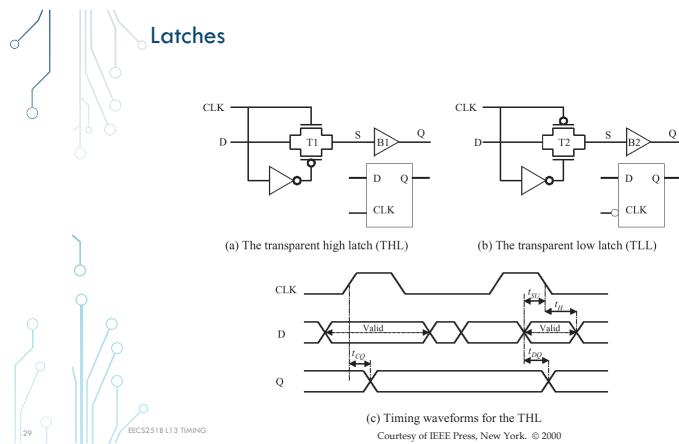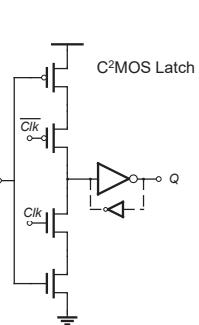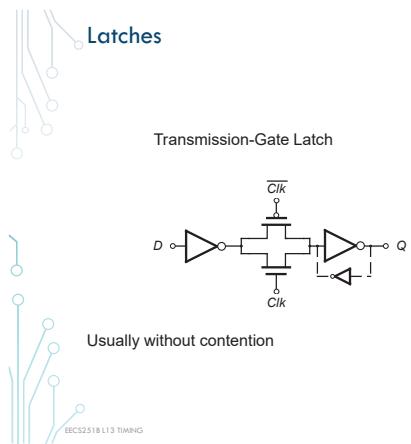
Slack Passing and Time Borrowing

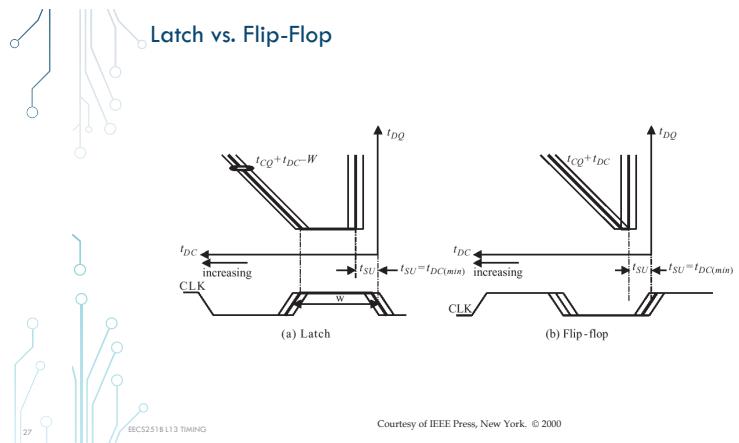## Slack Passing and Time Borrowing

- Slack passed

Slack Passing and Time Borrowing

- Time borrowed
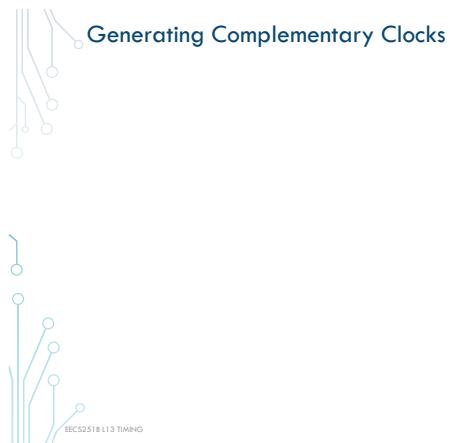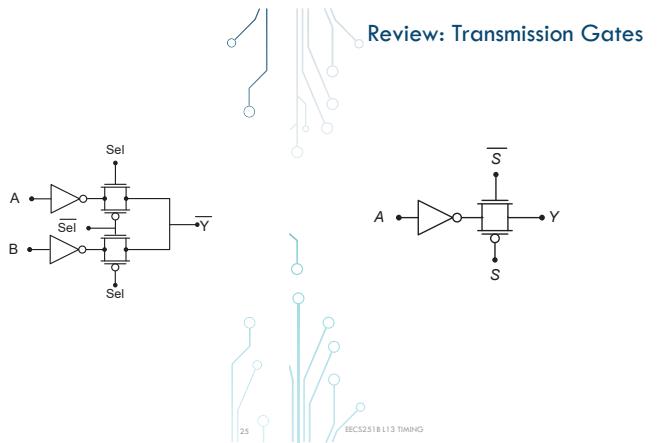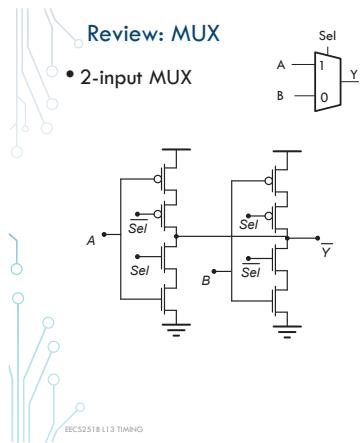
Slack-Passing and Cycle Borrowing

For N stage pipeline, overall logic delay should be < N Tcl

Announcements

- Assignment #1 due tomorrow
  - Quiz 1 next Tuesday, in lecture
- Lab 5 due next week
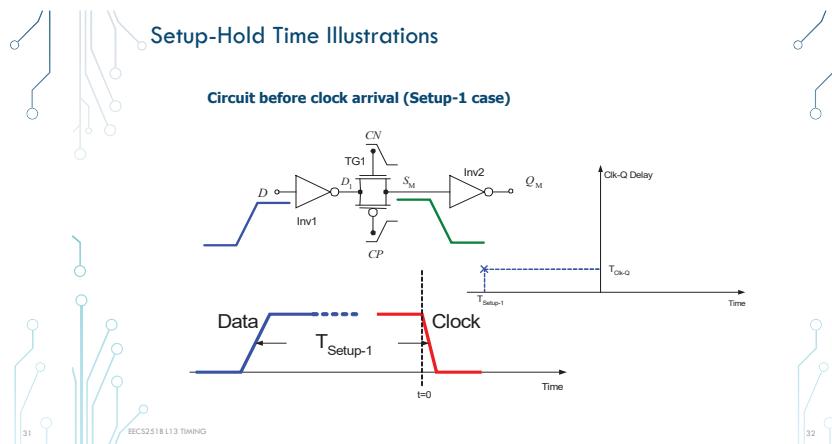
Design for Performance

Latch Design

Review: MUX

- 2-input MUX

Review: Transmission Gates

Generating Complementary Clocks

Latch vs. Flip-Flop

(a) Latch (b) Flip-flop

Courtesy of IEEE Press, New York. © 2000

Latches

Transmission-Gate Latch

C²MOS Latch

Usually without contention

Latches

(a) The transparent high latch (THL) (b) The transparent low latch (TLL)

(c) Timing waveforms for the THL

Courtesy of IEEE Press, New York. © 2000

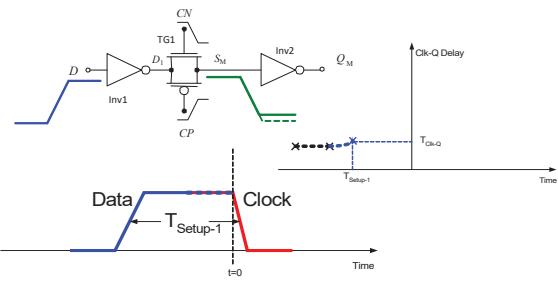## Design for Performance

Delay, Setup, Hold
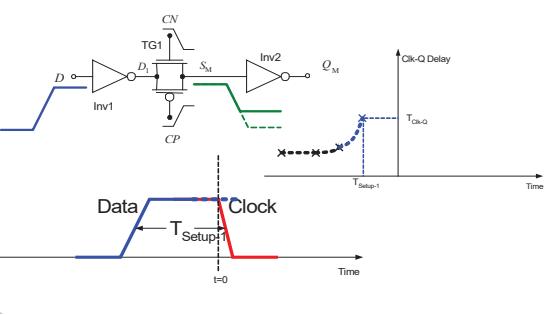
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)

Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)

Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)

Setup-Hold Time Illustrations

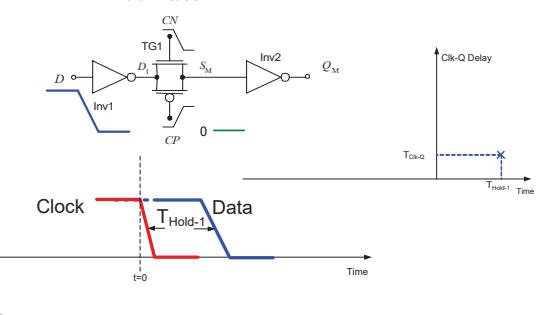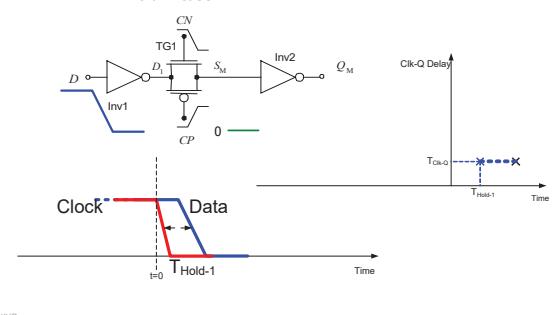### Circuit before clock arrival (Setup-1 case)

Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)
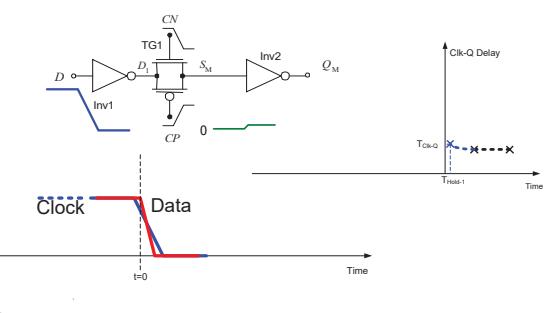
Setup-Hold Time Illustrations

Hold-1 case

Setup-Hold Time Illustrations

Hold-1 case

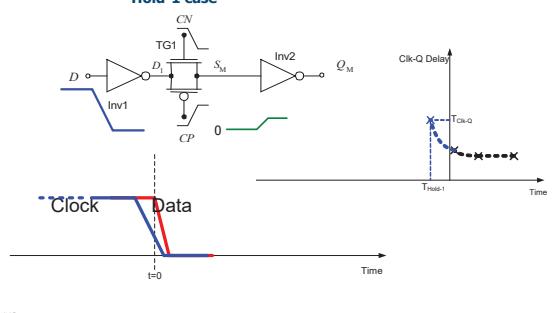## Setup-Hold Time Illustrations

Hold-1 case

Setup-Hold Time Illustrations

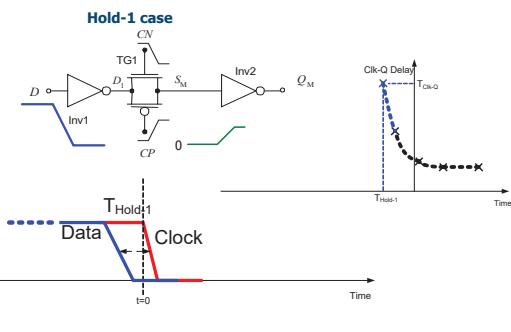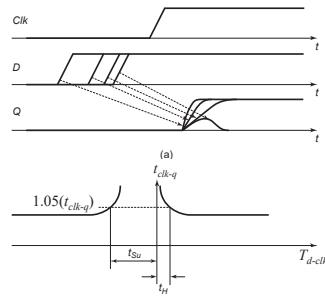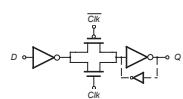### Hold-1 case

Setup-Hold Time Illustrations

Hold-1 case
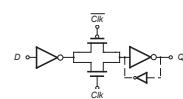
More Precise Setup Time

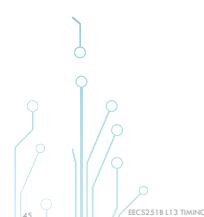## Latch t_{D-Q} and t_{Clk-Q}

t_{setup}

Summary

- Flip-flop-based (edge-triggered) timing dominates today
- Latch-based timing can increase performance, but needs extra care
- There is also asynchronous design
- Logical effort can be used to analyze latch timing

Next Lecture

- Flip-flops
- Variability