

EECS251B : Advanced Digital Circuits and Systems



Time for course surveys!

EECS251B L25 SUPPLY GENERATION

Lecture 25 – Supplies and Clocks

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Course Evaluations: Best Practices for Faculty

Reserve time in-class.

Give students time during class to complete the online course survey. Anecdotally, this is more effective when the time set aside is at the **start** of class.



Inform students about the purpose of evaluations.

Give students examples of useful feedback you have received in the past and **how** the course has changed or benefited.



Offer students incentives (e.g. extra credit).

To encourage broad, representative responses, instructors may choose to offer incentives to complete evaluations. An effective strategy has been to offer all students extra credit if a **minimum percentage** of students (e.g. 85%) respond.

85%
✓

Recap

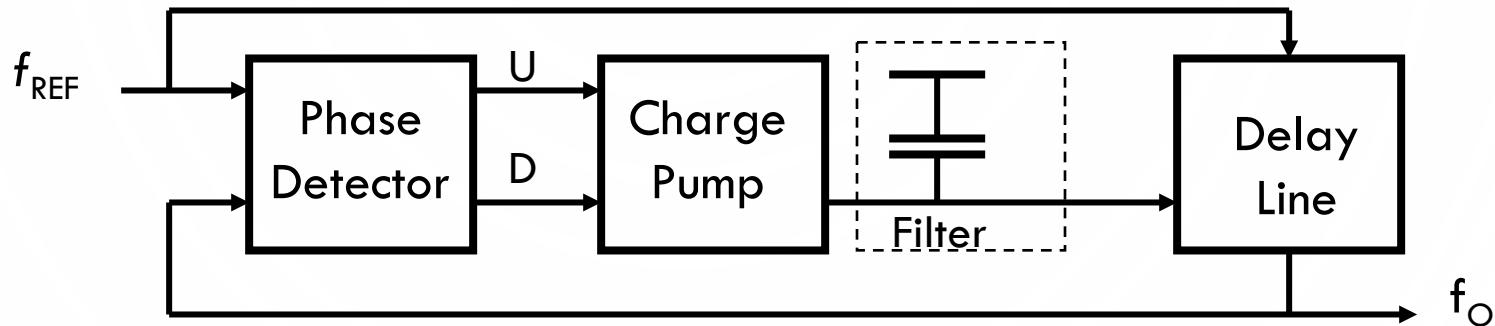
- Basics of phase-locked loops
- Digital PLLs



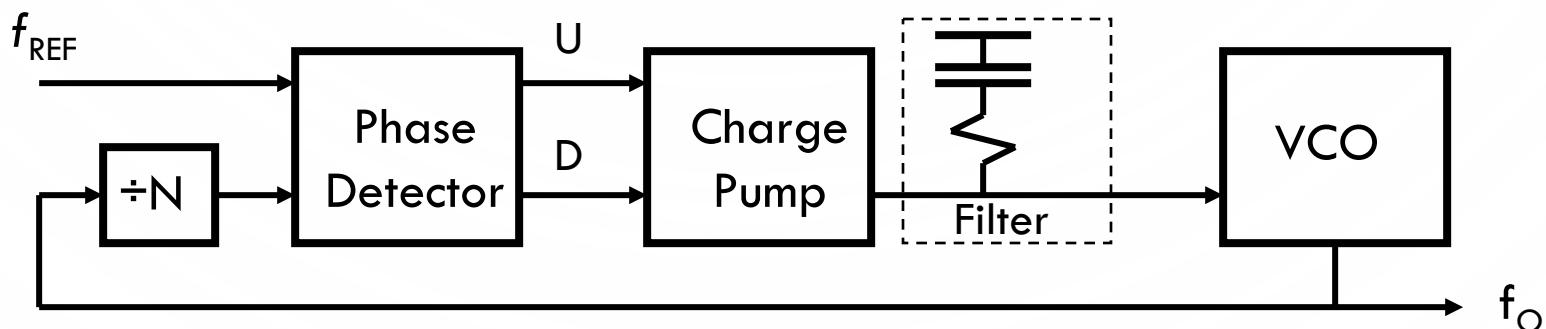
Delay-Locked Loops

Clock Generation

Delay-Locked Loop (Delay Line Based)

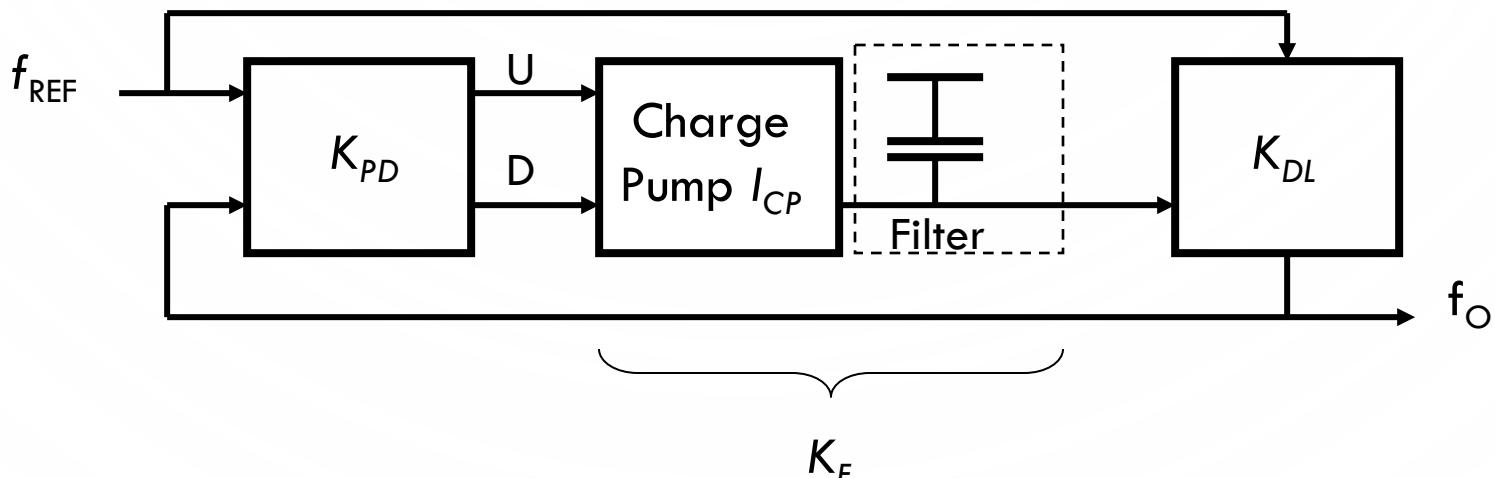


Phase-Locked Loop (VCO/DCO-Based)

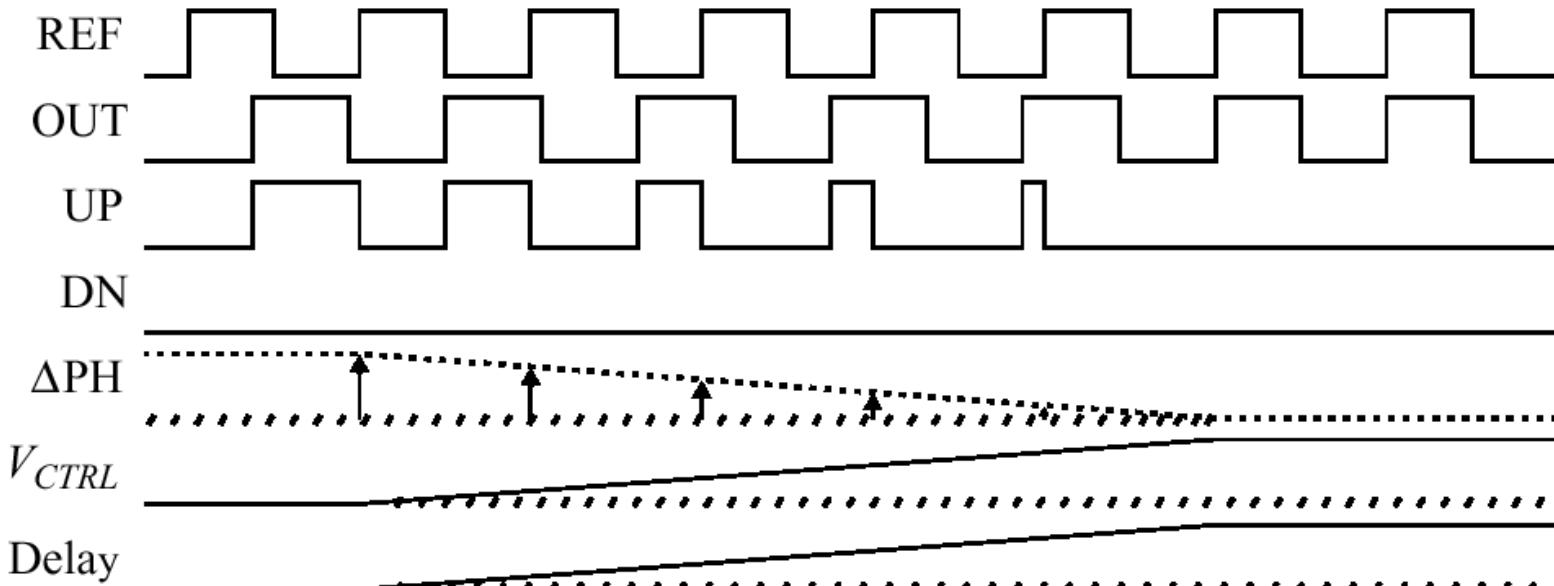
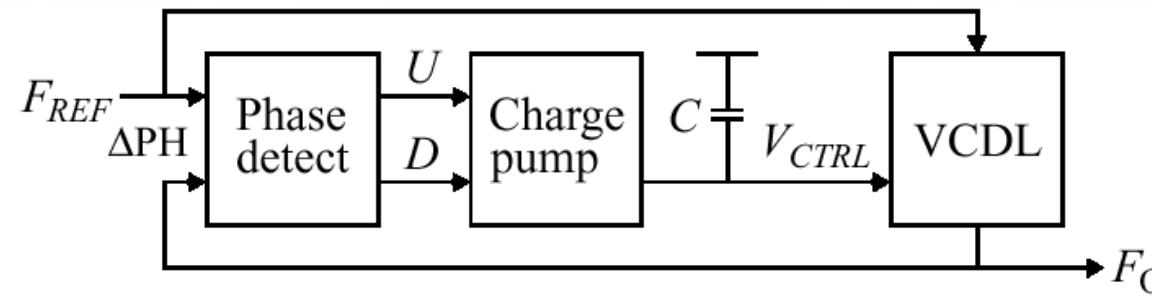


Delay-Locked Loop

- First order loop: inherently stable
- No filtering of input jitter
- Constant frequency (no synthesis)
- No phase error accumulation

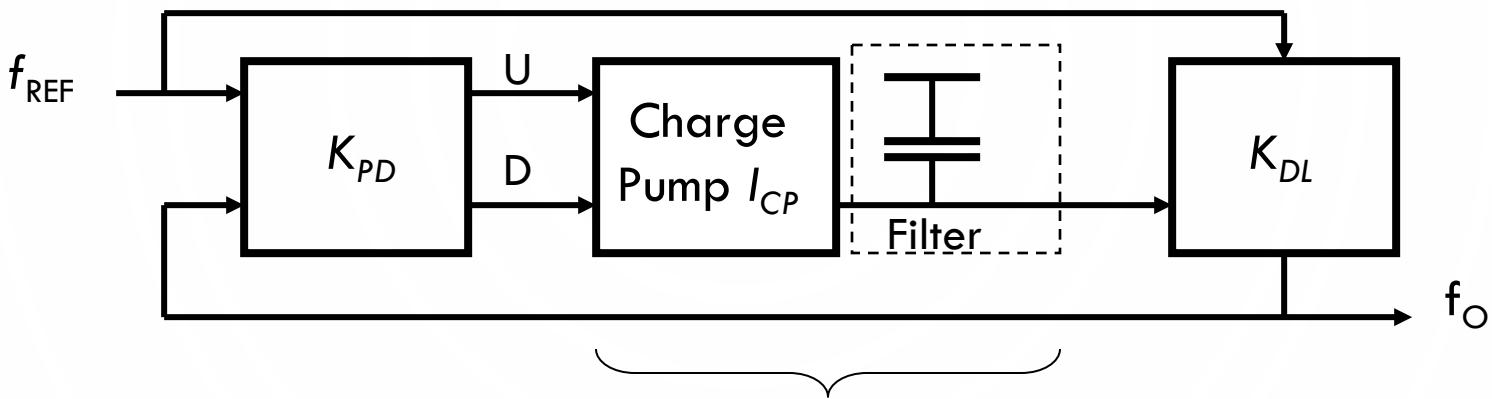


DLL Locking



Courtesy of IEEE Press, New York. © 2000

Delay-Locked Loop



► Open loop transfer function

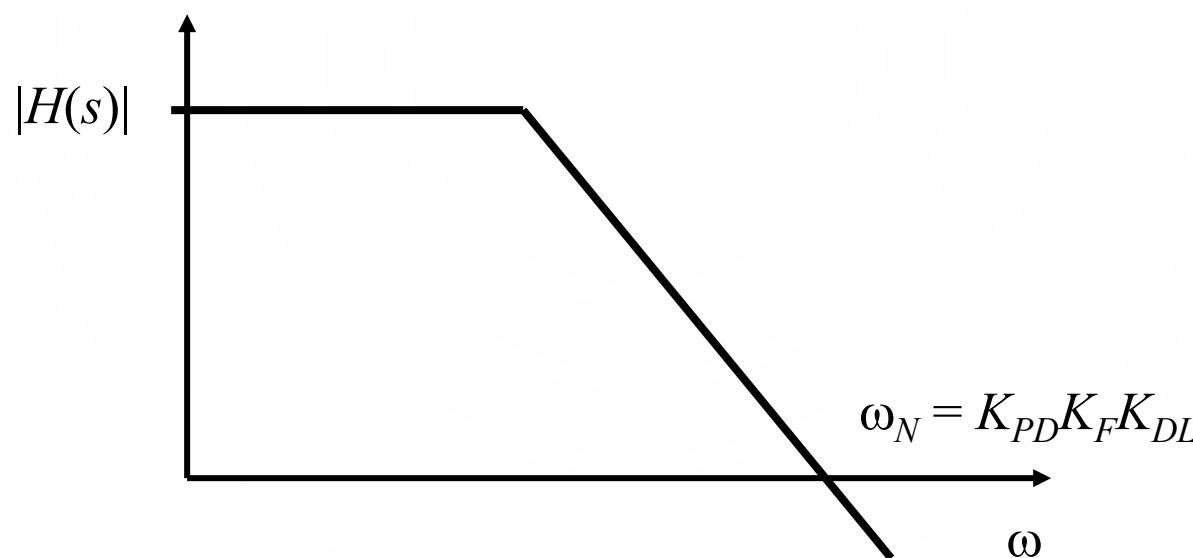
$$\frac{D_O(s)}{D_I(s) - D_O(s)} = K_{PD} \frac{1}{sC} I_{CP} K_{DL} F_{REF} = \frac{1}{s} K_{PD} K_F K_{DL}$$

K_F

► Closed loop transfer function

$$H(s) = \frac{D_O(s)}{D_I(s)} = \frac{K_{PD} K_F K_{DL}}{s + K_{PD} K_F K_{DL}}$$

Delay-Locked Loop



- $\omega_N >$ an order of magnitude below F_{REF}
- Use of DLLs requires low-jitter input
- VCDL must span adequate delay range + reset to min delay
- Noise sources:
 - Delay line (Supply sensitivity)
 - Clock buffers that follow
 - Device noise (small)

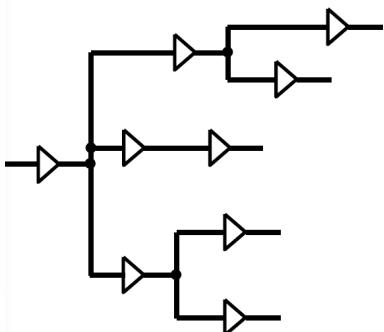
Announcements

- Final is in-class 4/28
 - 80min, 9:40am-11am
- Project presentations 5/5
 - 9am – 12:30pm
 - BWRC
 - 12min + 3min Q&A

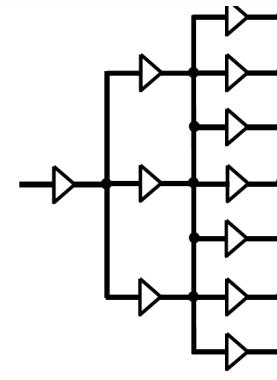


Clock Distribution

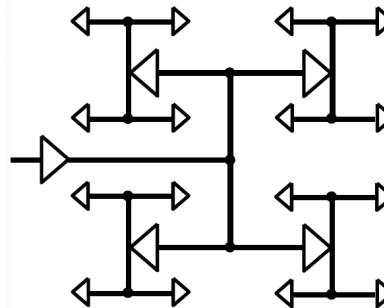
Clock Distribution



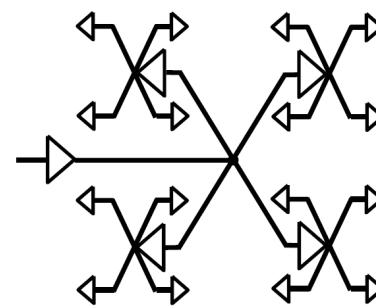
Tree



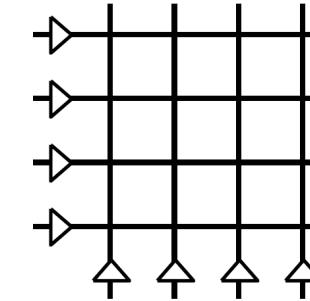
Mesh



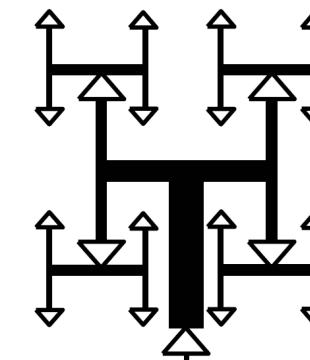
H-Tree



X-Tree



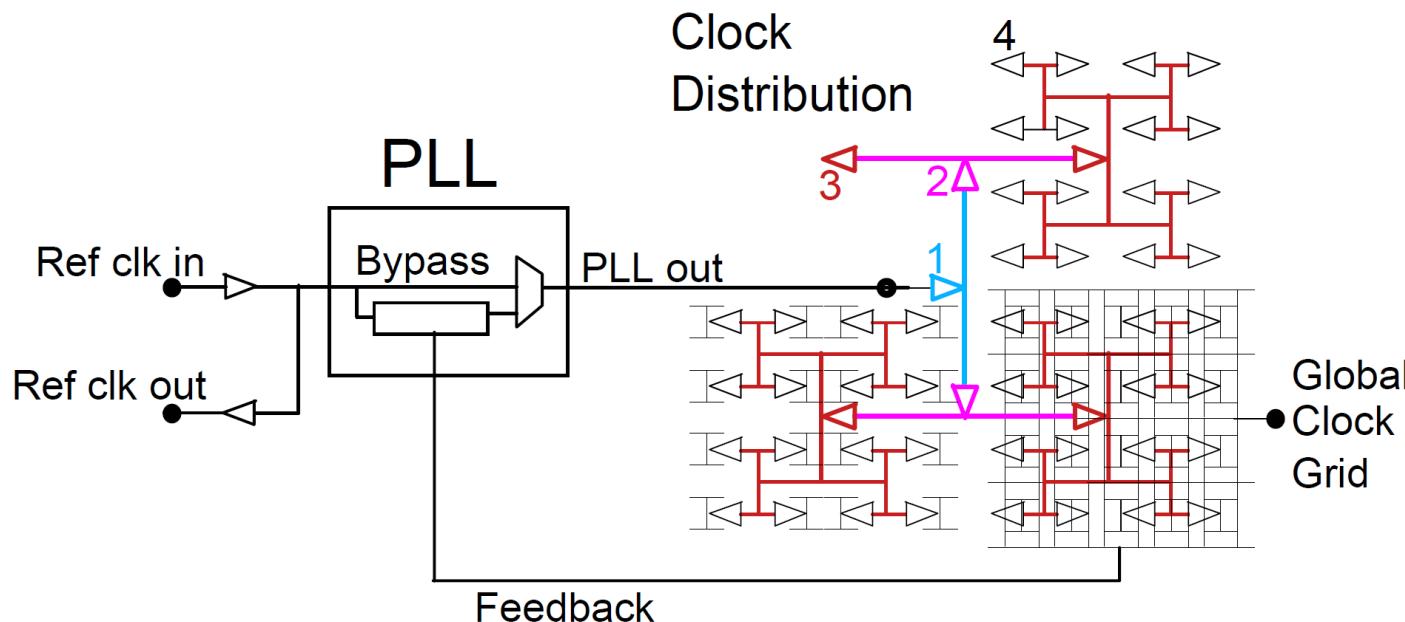
Grid



Tapered H-Tree

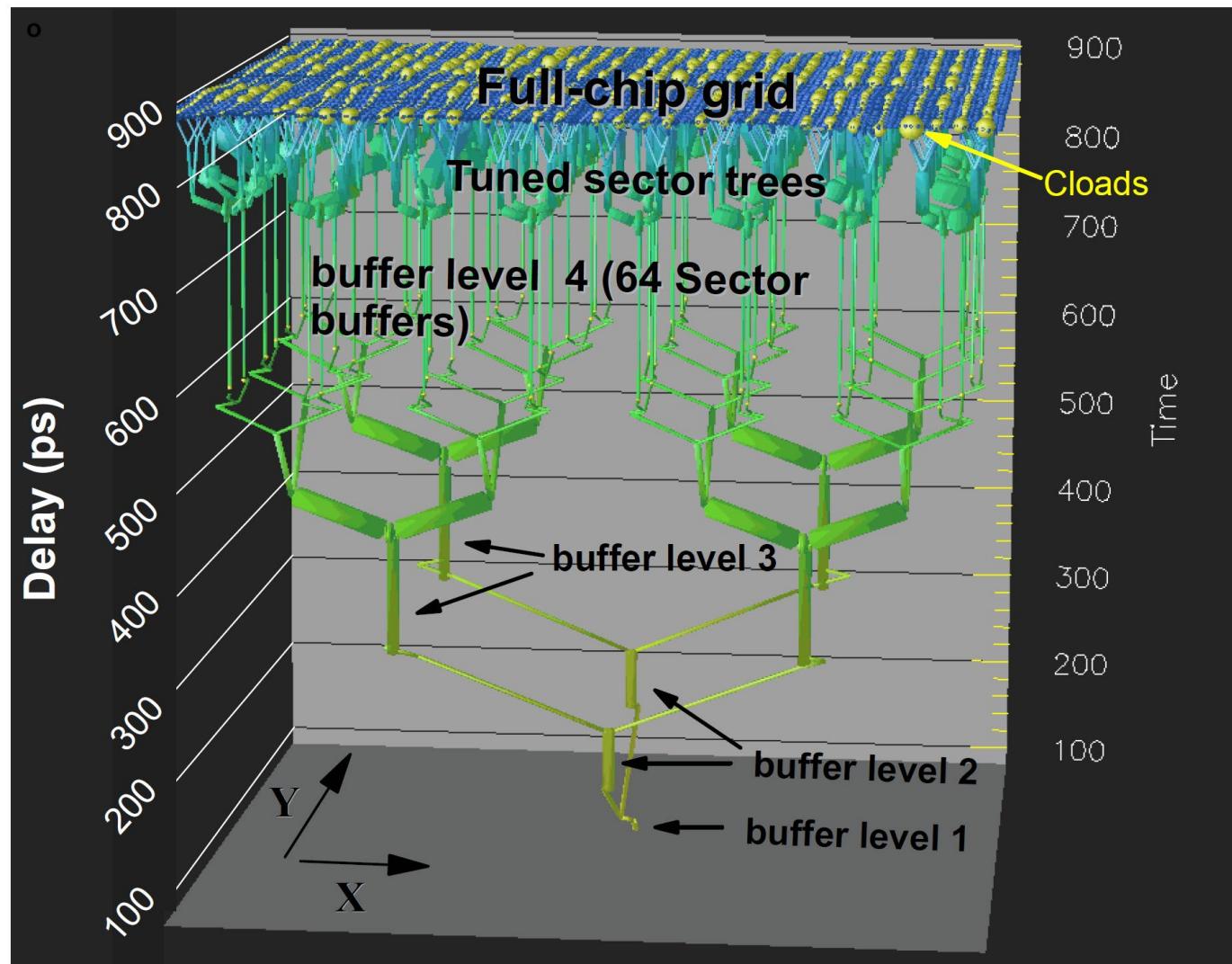
Example (Older) Clock System

- IBM Power 4

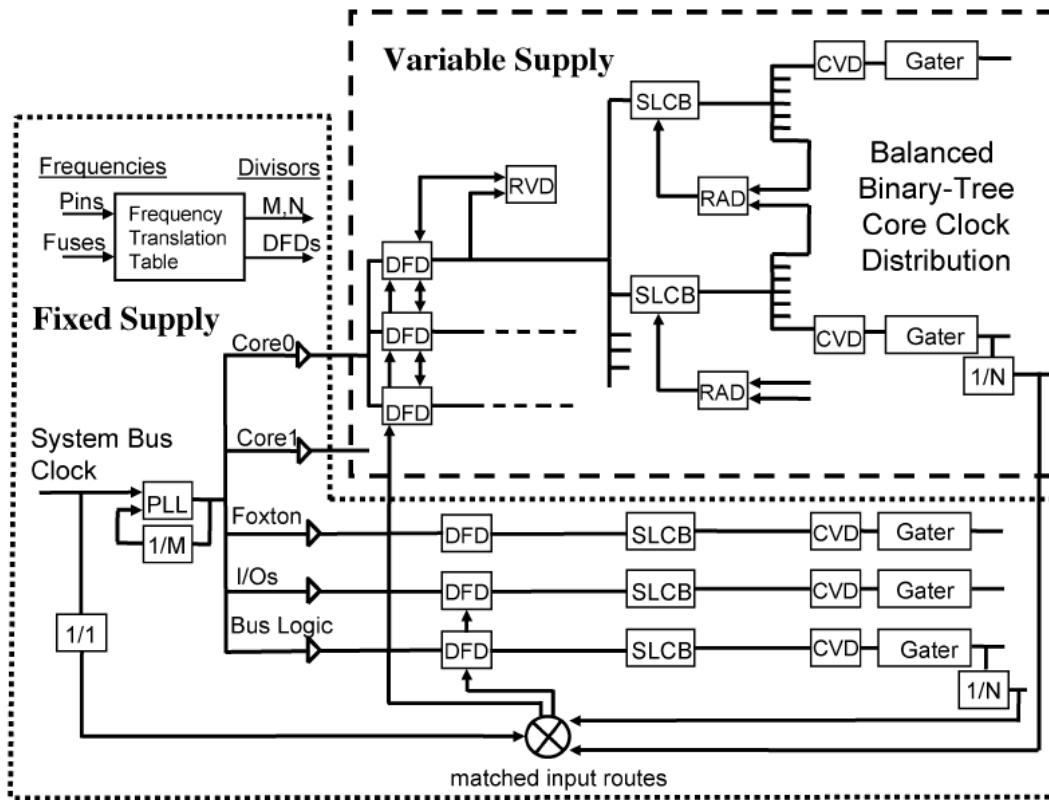


Restle, ISSCC'02

Clock Grid



One PLL with multiple DLLs



- Single PLL, and two cores vary frequency through digital frequency dividers (DFDs) and DLLs
 - SLCB: Second-Level Clock Buffer
 - CVD: Clock Vernier Device – fine (static) delay tuning

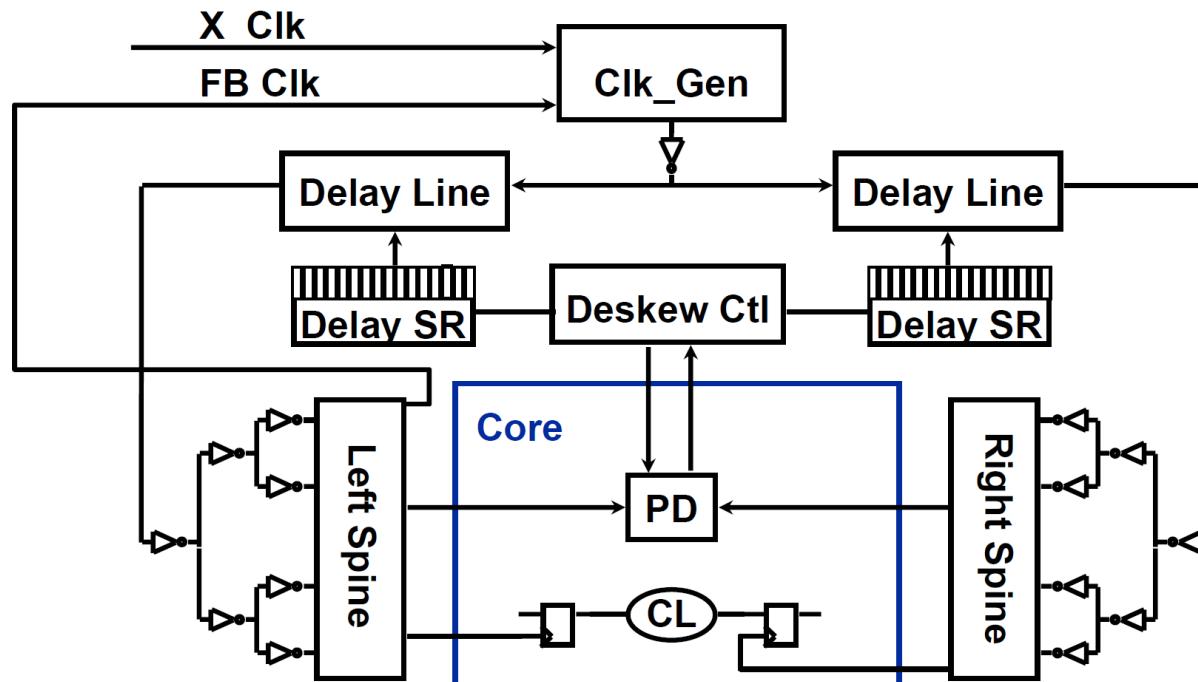


Deskewing and Synchronization

Clock Domain Synchronization

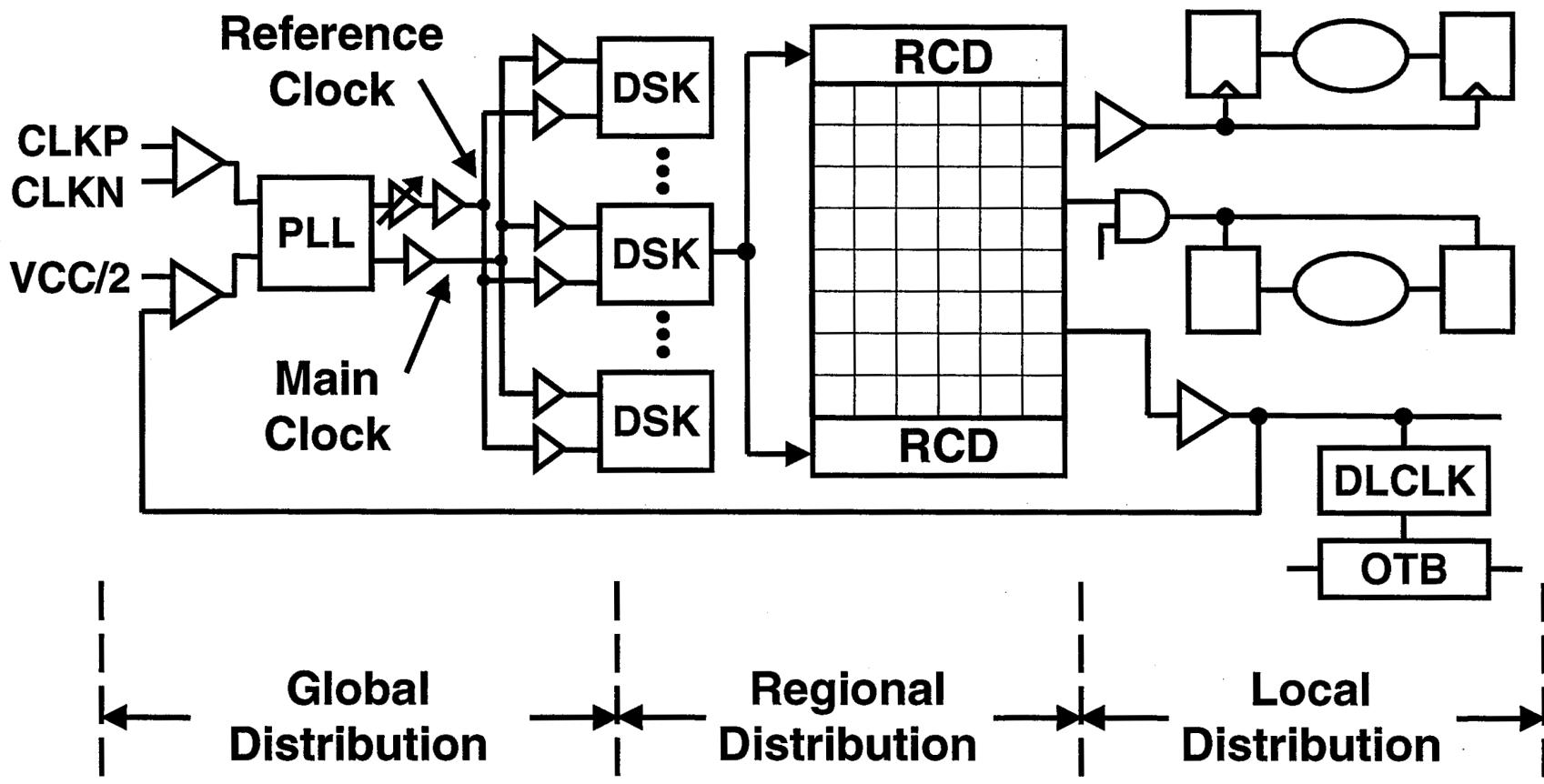
Type	Frequency	Phase
Synchronous	Same	Same
Mesochronous	Same	Constant offset
Plesiochronous	Small difference	Slowly varying
Asynchronous	Different	Arbitrary

Deskew System (Mesochronous)



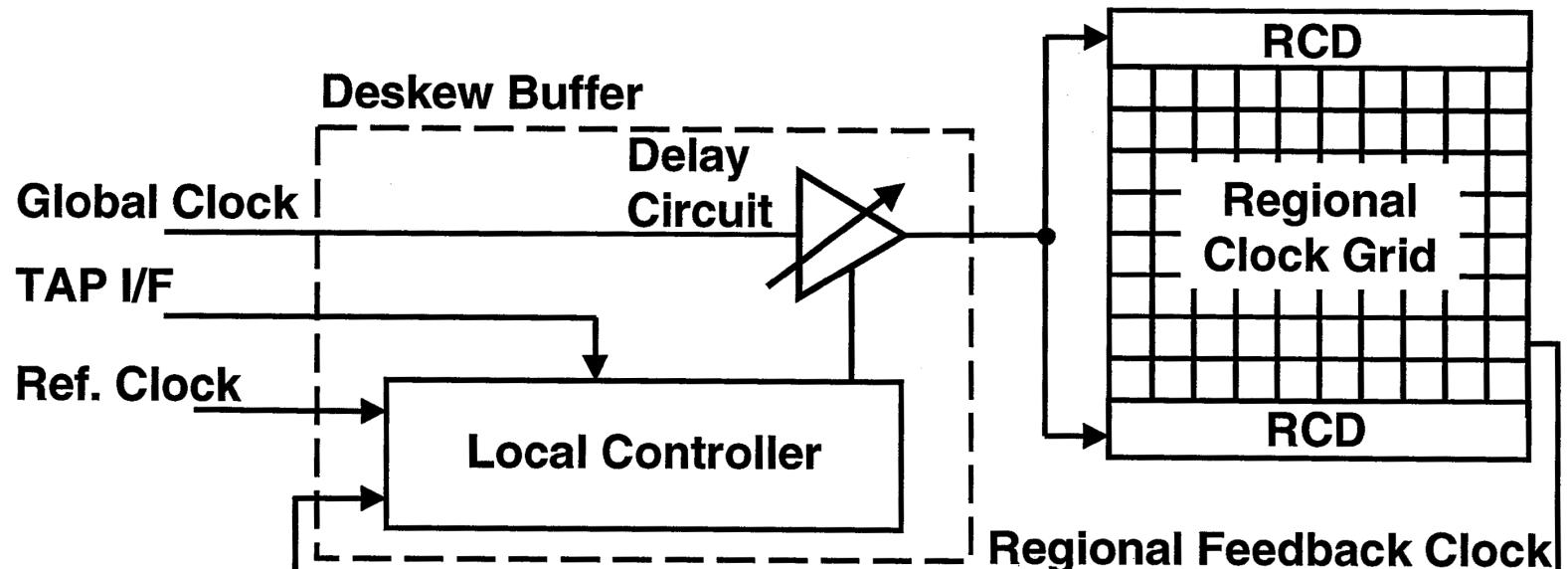
Geannopoulos, ISSCC'98

Deskew System



• Rusu, ISSCC'00

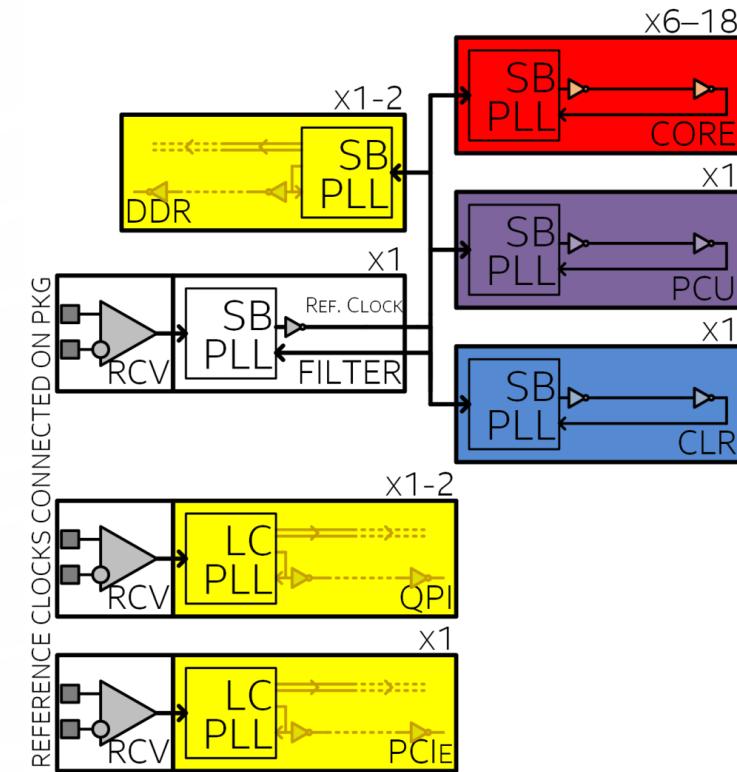
Deskew Buffer



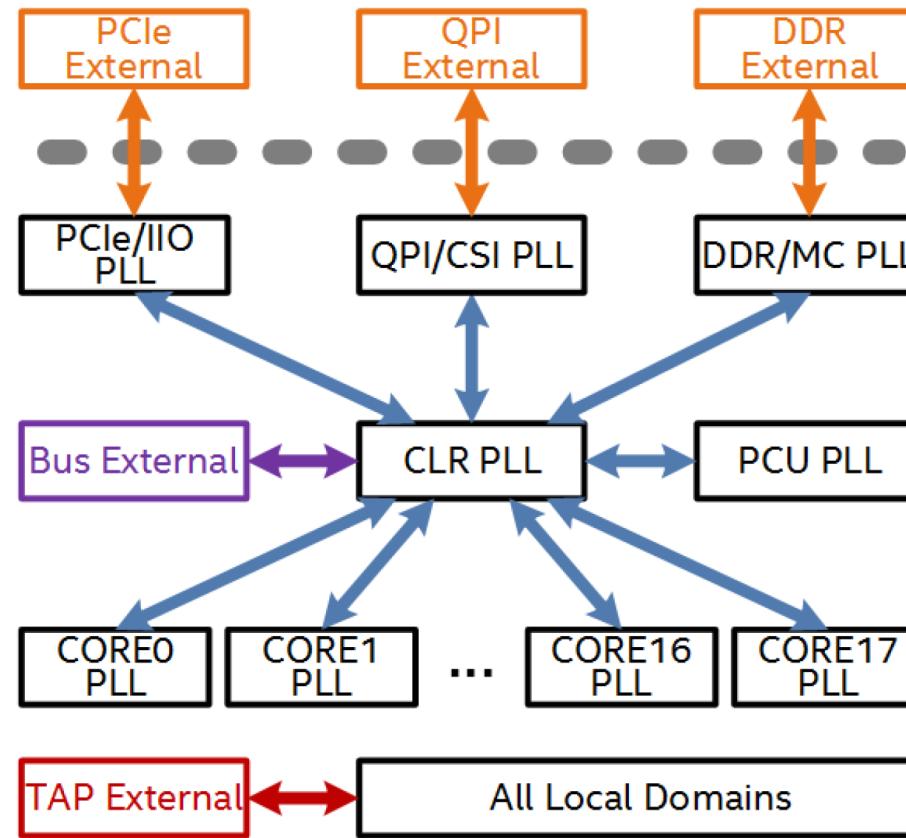
- Essentially a DLL to align regional clock with ref. clock

Clock Subsystem

- Intel Xeon – Bowhill, ISSCC'15
 - Independent clocks for 4-18 cores
- Self-biased (SB) and LC PLLs

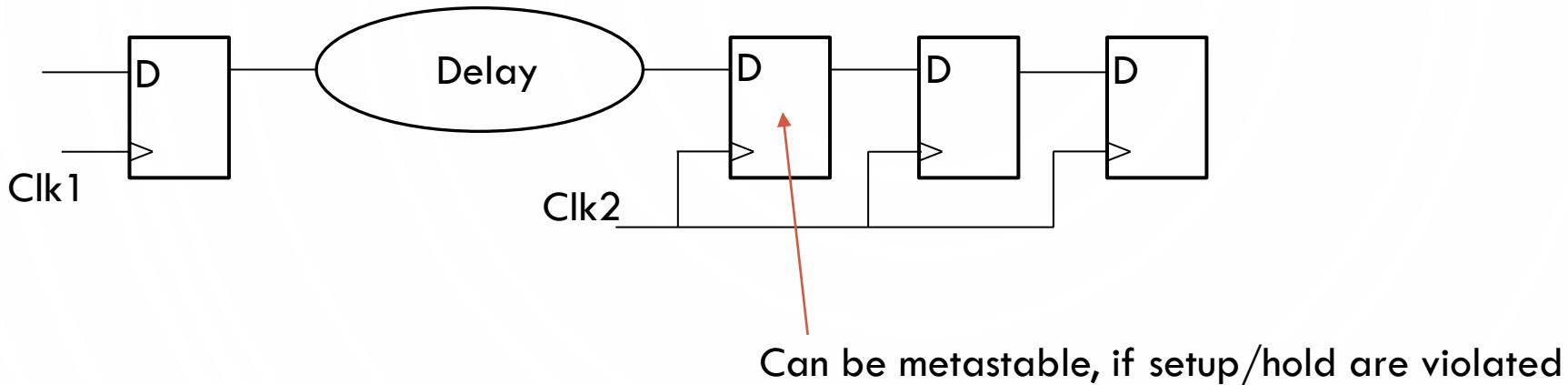


Clock Domain Crossings



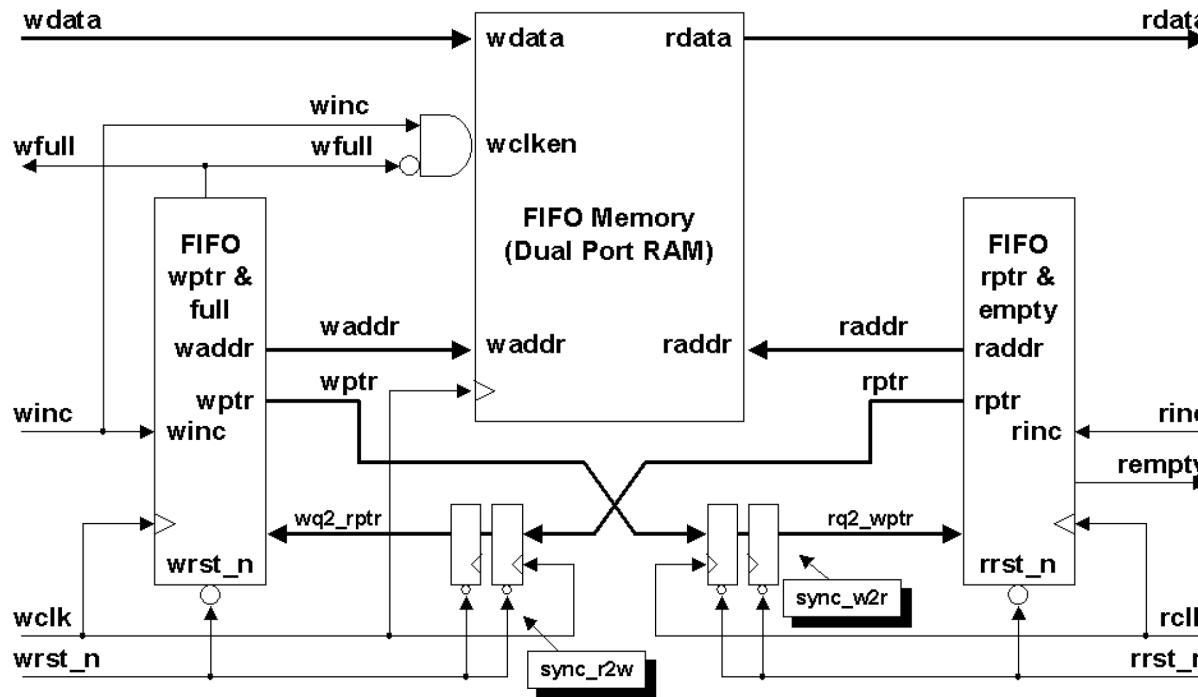
- Bowhill, ISSCC'15

Brute-Force Synchronizer



- Cascaded flip-flops reduce the probability of metastability

Clock Crossing FIFOs



- FIFO for clock crossings

http://www.sunburst-design.com/papers/CummingsSNUG2002SJ_FIFO1.pdf



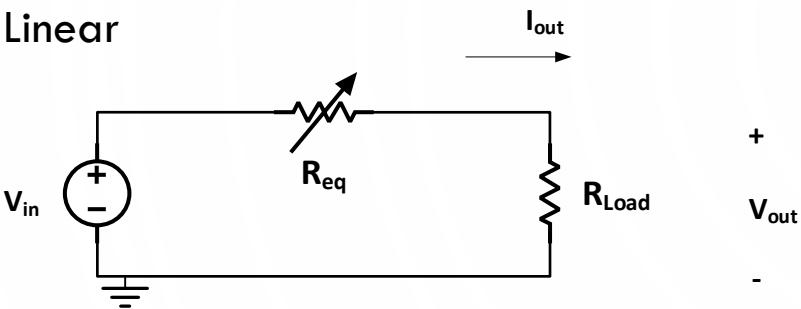
Supply Generation

Supply Generation

- Linear
 - Series or shunt
 - Linear regulation
 - Quiet
 - Inefficient (unless $V_{in}-V_{out}$ is small)
- Switching (Capacitive)
 - Limited efficiency
 - Poor regulation
 - Voltage ripples
- Switching (Magnetic)
 - Efficient
 - Require external components
 - Noisy

Linear vs. Switching Regulators

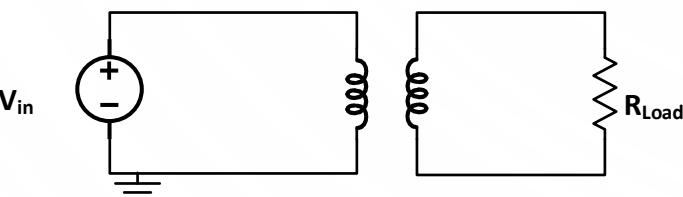
Linear



+
 V_{out}
-

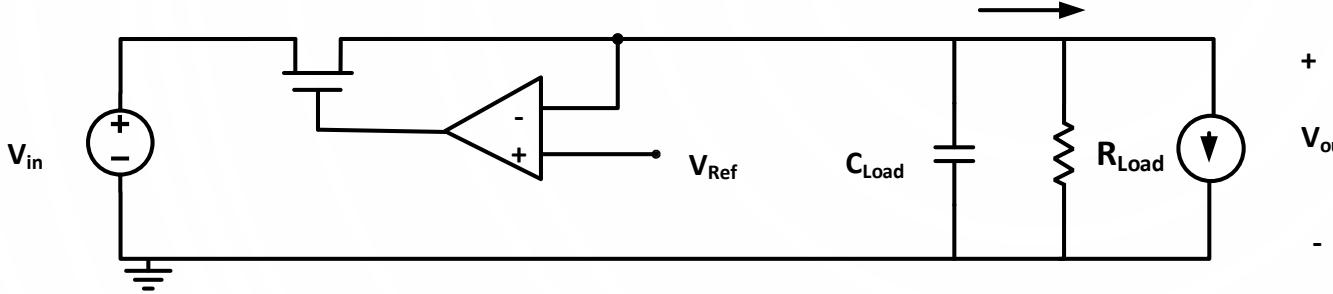
Efficiency $\eta < V_{out}/V_{in}$

Switching



+
 V_{out}
-

Linear Voltage Regulator

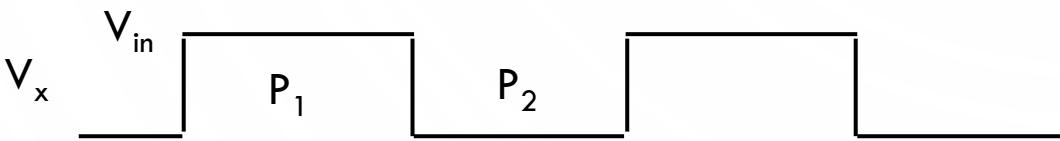
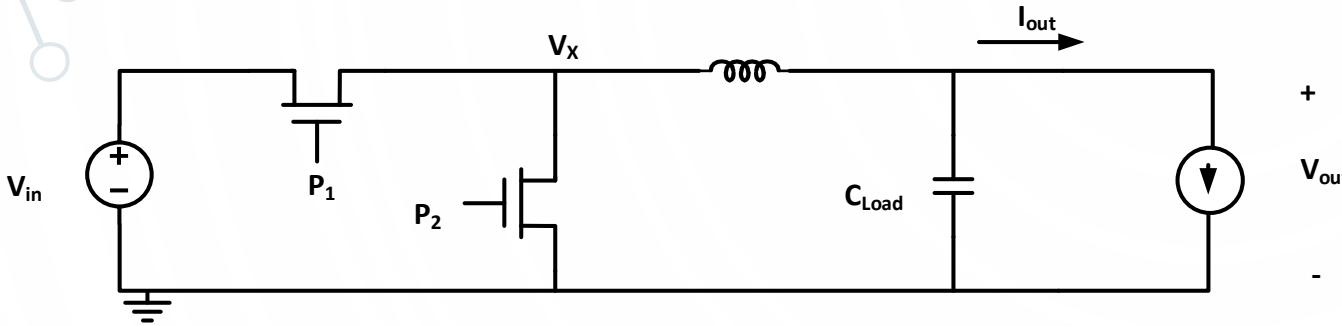


Negative feedback sets low supply resistance
Voltage regulated to desired level

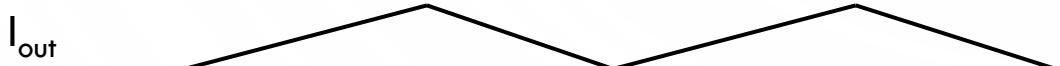
E.g. IBM Power7 has 48 linear regulators

Switching Supply

- Buck Converter



Pulse-Width Modulation (PWM) regulates V_{out}

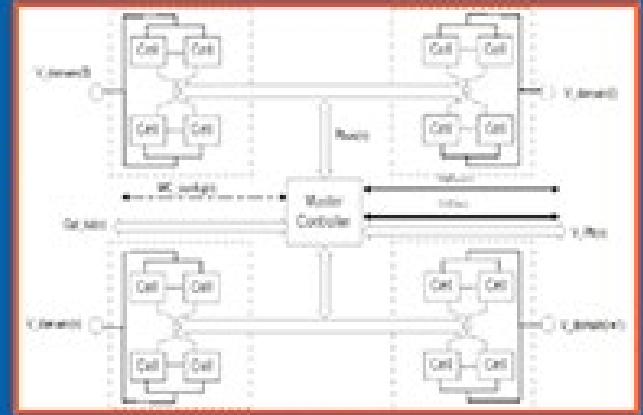


High switching frequency, interleaving reduce ripple

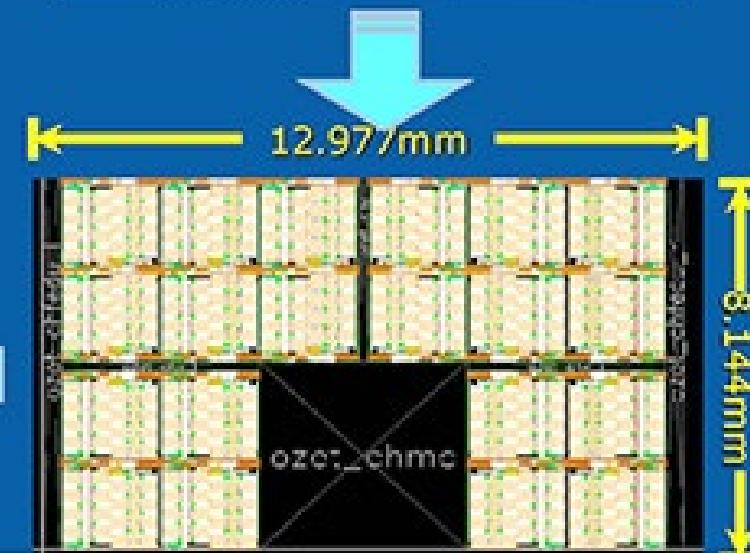
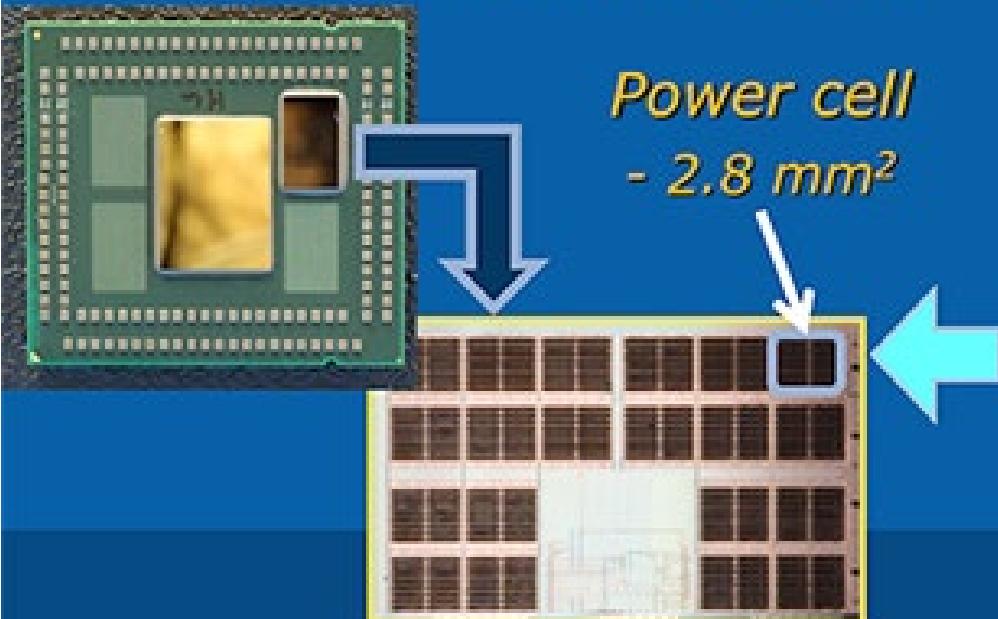
Inside Haswell

Integrated VR Technology

- 'Common Cell' Architecture – 20 cells
- Architecture supports flat efficiency curve
- Fine grain power management
 - Allows for multiple voltage rails
- Telemetry and Margining features
- Active Voltage Positioning for current sharing and balance
- Control features, including: JTAG, FPGA, Test/BIST



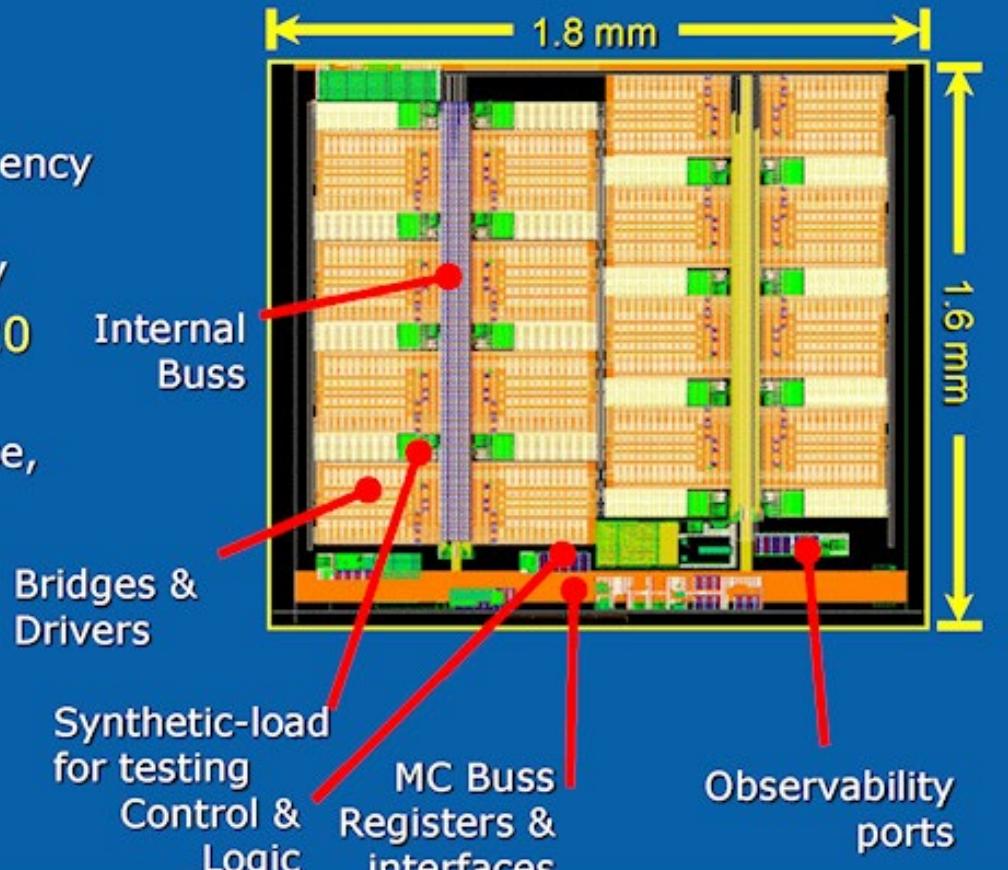
General Arch



Inside Haswell

Review: Power Cell Architecture

- Each Power cell = Mini VR
 - Up to 25A rating* - tested
 - Programmable switching frequency 30MHz to 140MHz
 - Ring coupled inductor topology
- 16 phases per power cell, 320 phases per chip
 - High phase count reduces noise, ripple
 - High granularity
 - Cell shedding
 - Bridge shedding
- BIST
 - Self-load and characterization system.

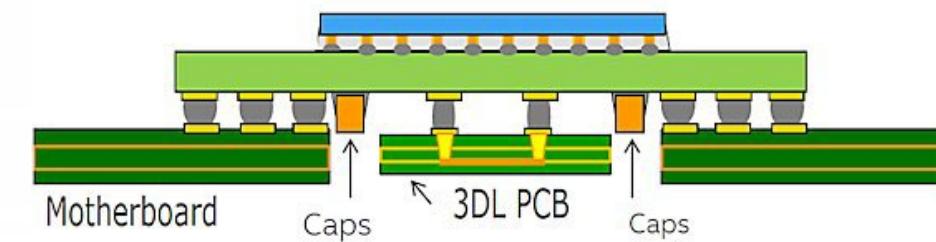
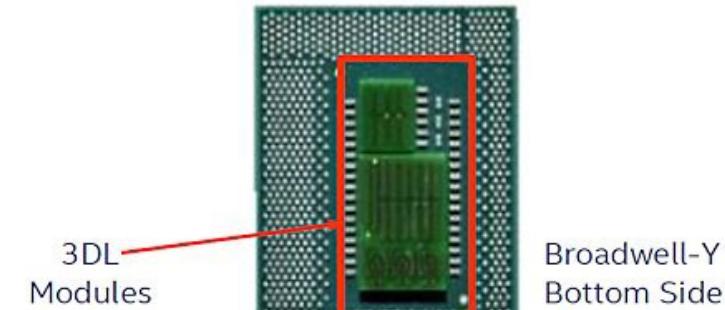


* Thermally constrained

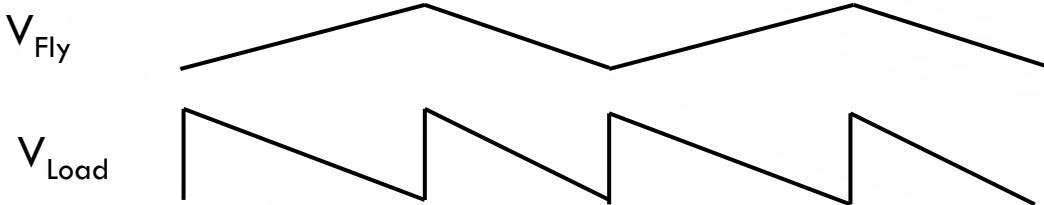
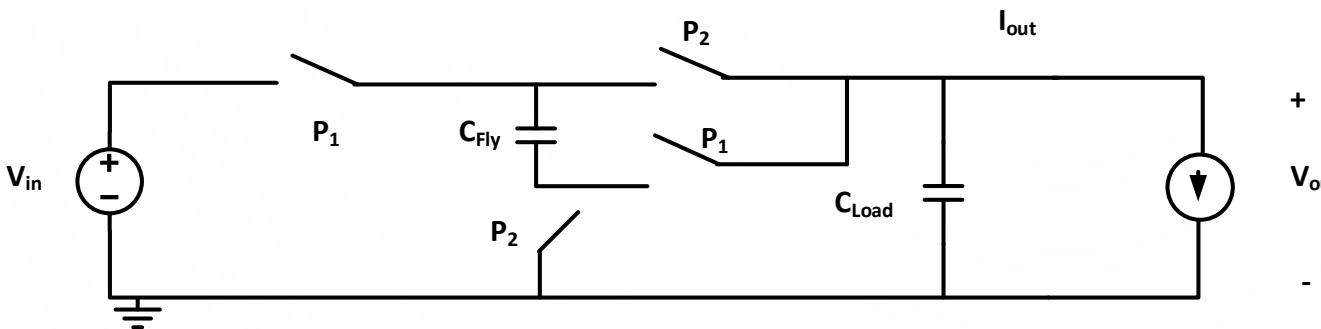


Intel Broadwell

- Inductors moved to a small PCB



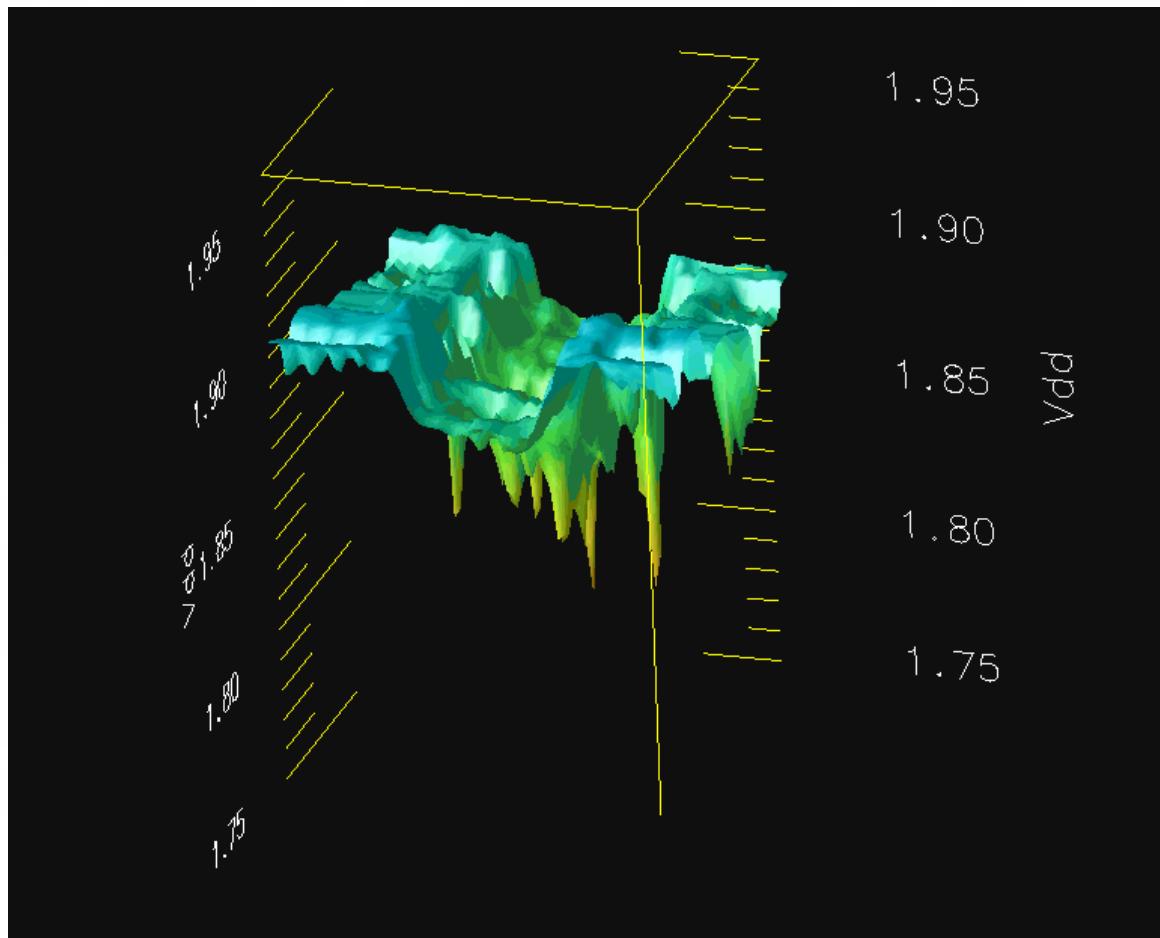
Switched-Capacitor Supply



Interleaving reduces ripple, but lowers efficiency

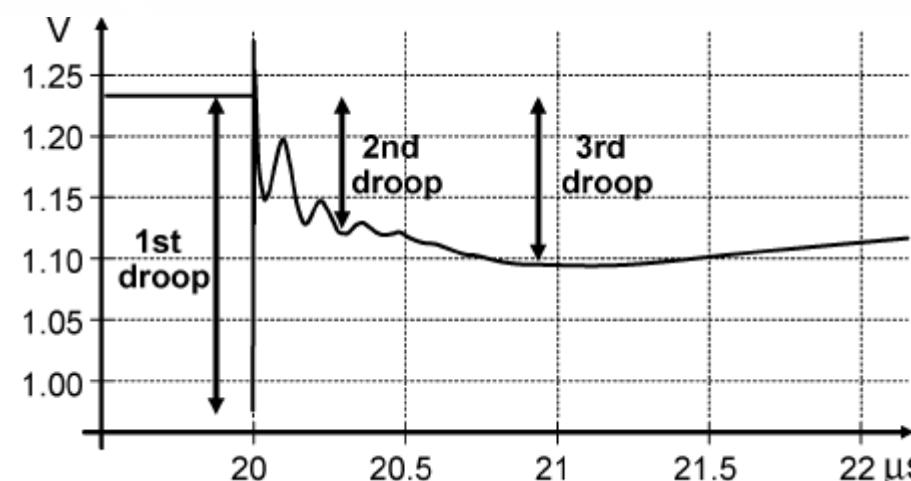
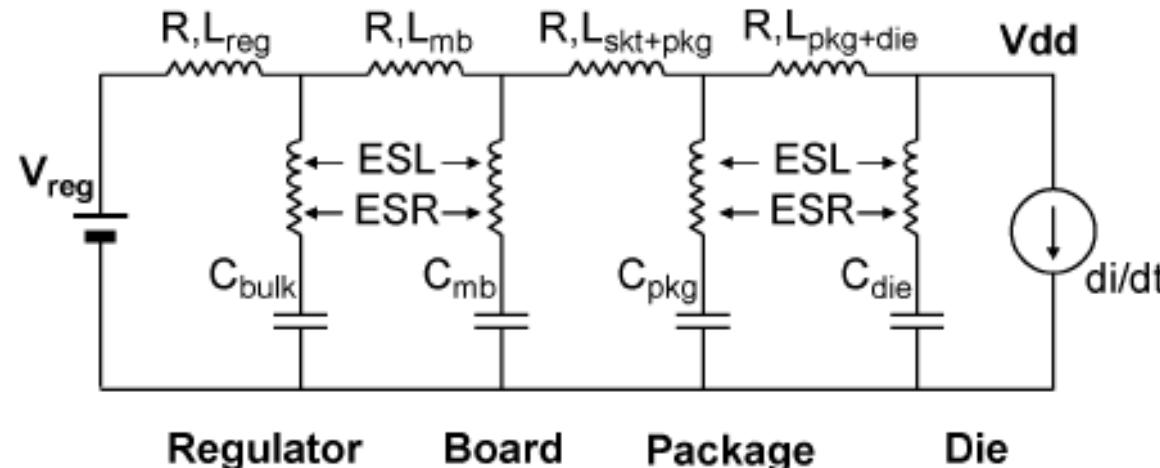
What happens with supply when load changes?

<http://www.research.ibm.com/people/r/restle/Animations/DAC01top.html>



Power Delivery

- Typical model



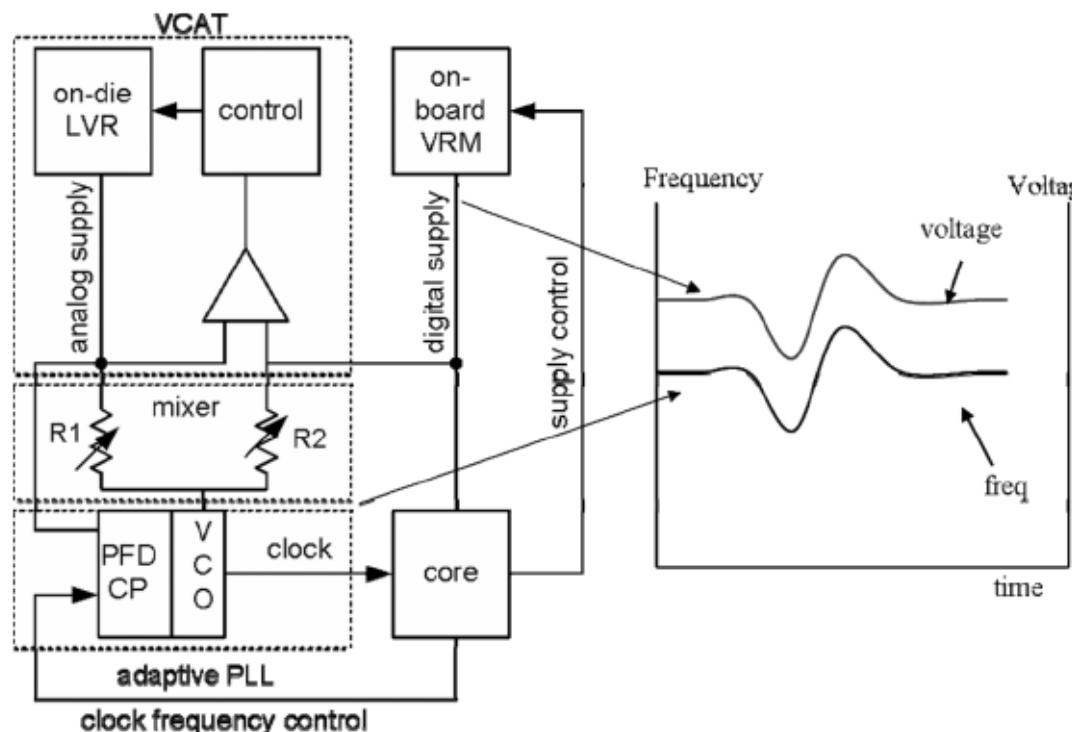
Wong, JSSC'06

Supply Resonances

- First droop
 - Package L + on-die C
- Second droop
 - Motherboard + package decoupling
- Third droop
 - Board capacitors

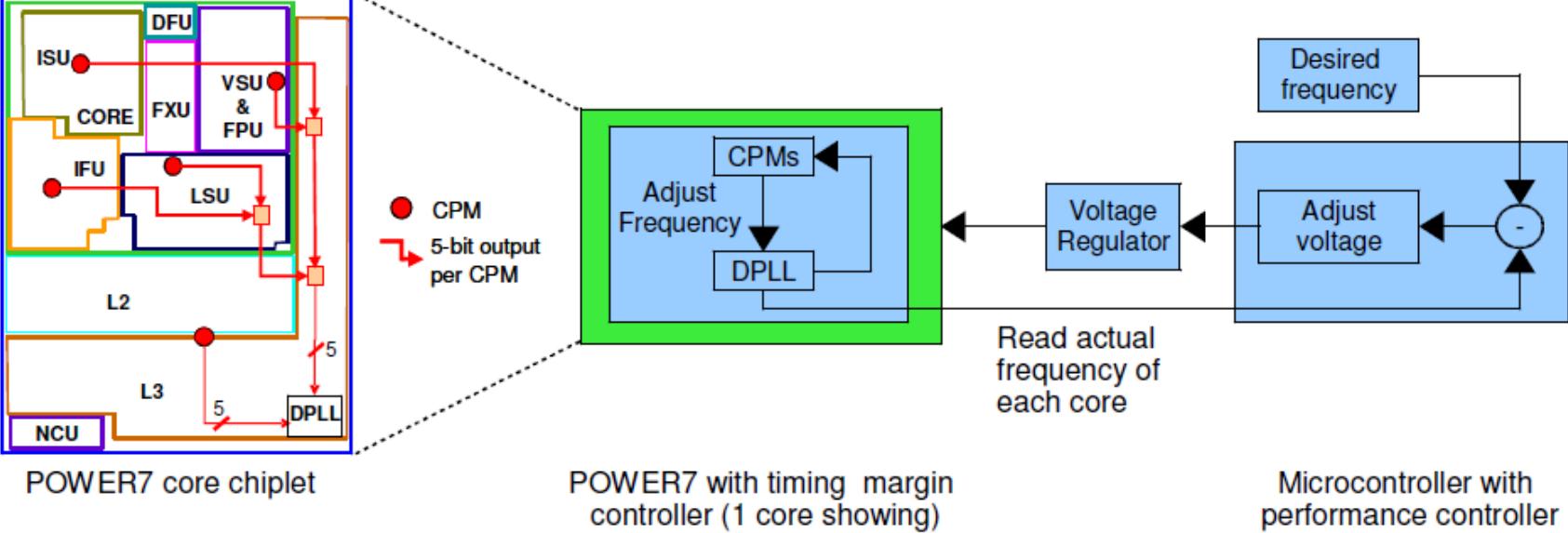
Clock and Supply

- Large digital systems can have large voltage transients
 - Can we filter impact of voltage on a clock generator?



Kurd, JSSC'09

Clock and Supply

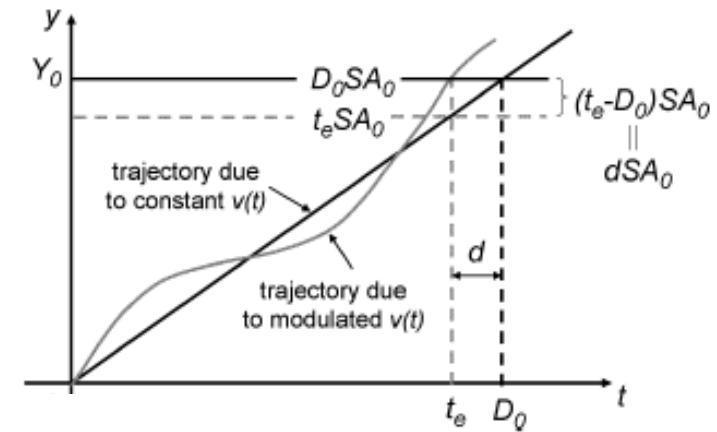
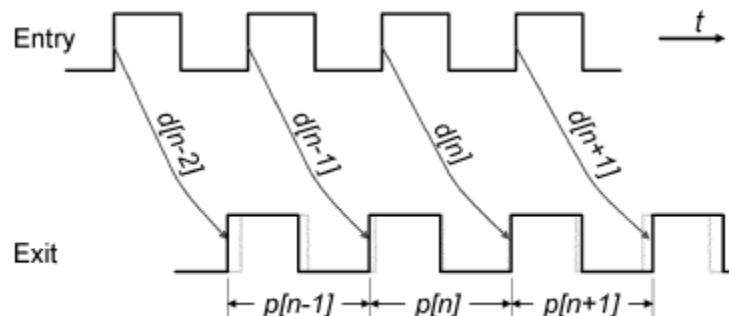
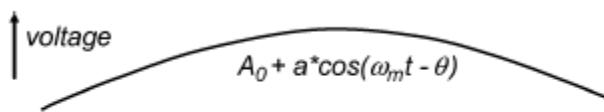
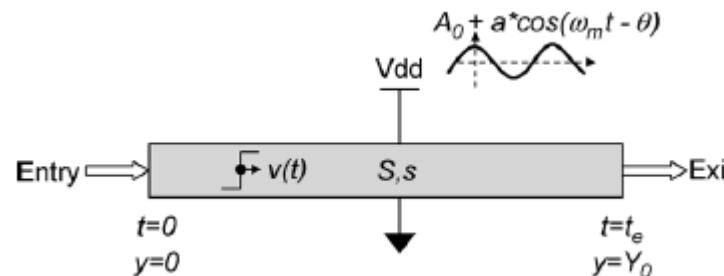


- IBM Power7, with one PLL per core

Lefurgy, MICRO'11

How to model

- Abstracted delay line

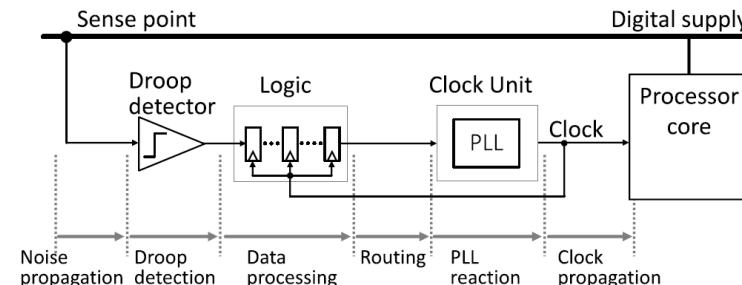
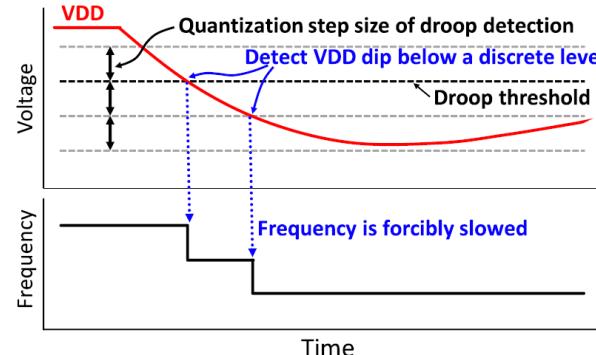
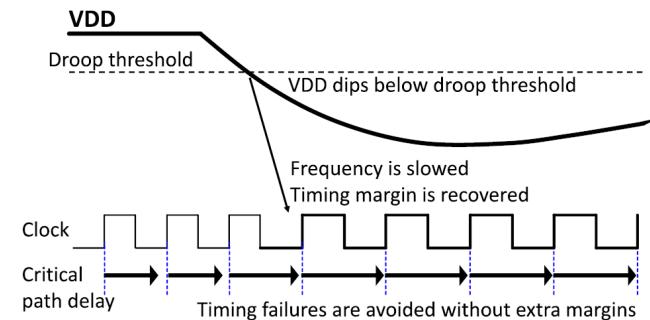
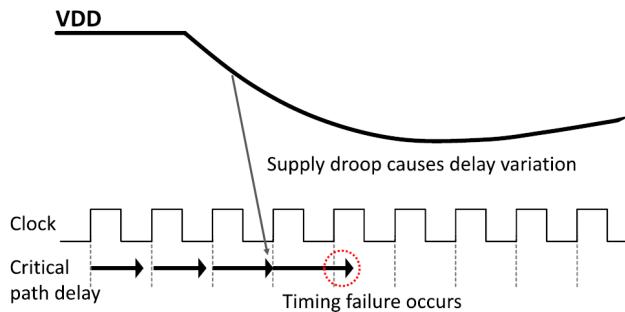


Wong, JSSC'06

Period modulation from successive modulated delays

Droop Detection

- Hashimoto, JSSC 4/18



Summary

- DLLs are used for phase alignment, deskewing
- Modern SoCs are globally asynchronous, locally synchronous
- Supply regulators
- Clock and supply interact

Next Lecture

- Wrap-up