EECS251B : Advanced Digital Circuits and Systems

Lecture 23 – Optimal Thresholds

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Broadcom launches Wi-Fi 7 chips

April 13, 2022 Nitin Dahad

Broadcom's new family of Wi-Fi 7 chips will help implement the speed, latency and determinism, and features like multi-link operation offered by the new Wi-Fi standard.

Broadcom's new Wi-Fi 7 product family. (Image: Broadcom)

Recap

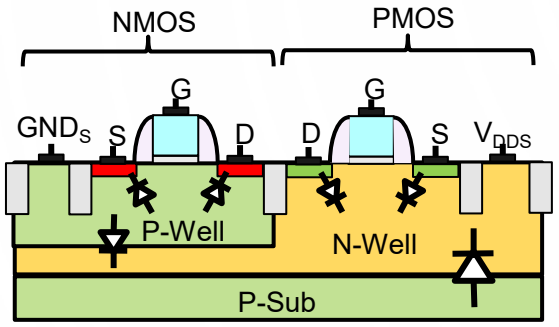
- Limiting transistor leakage
  - Multi-threshold designs
  - Transistor stacking
  - Sleep modes
  - Power gating

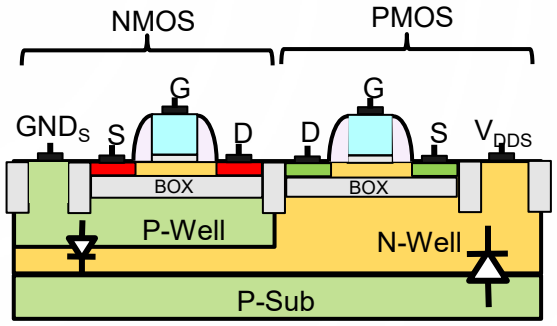
Dynamic Threshold Scaling

Dynamic Body Bias

- Similar concept to dynamic voltage scaling
- Control loop adjusts the substrate bias to meet the timing/leakage goal
  - Can be used just as runtime/sleep
- Limited range of threshold adjustments in bulk (<100mV)
  - Limited leakage reduction (<10x)
- Works well in FDSOI (80-85mV/V, with ~1.8V range)
- No delay penalty
  - Can increase speed by forward bias
- Energy cost of charging/discharging the substrate capacitance
  - but doesn't need a regulator

FDSOI and Bulk

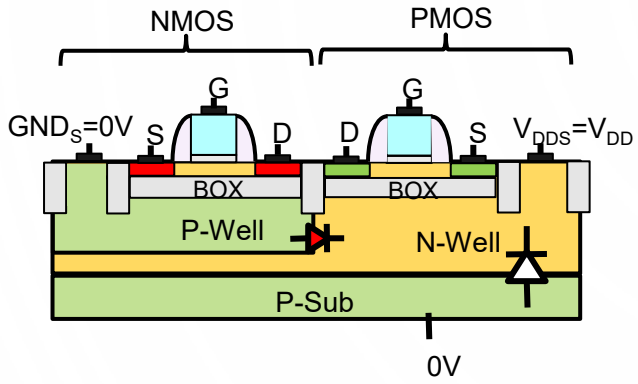




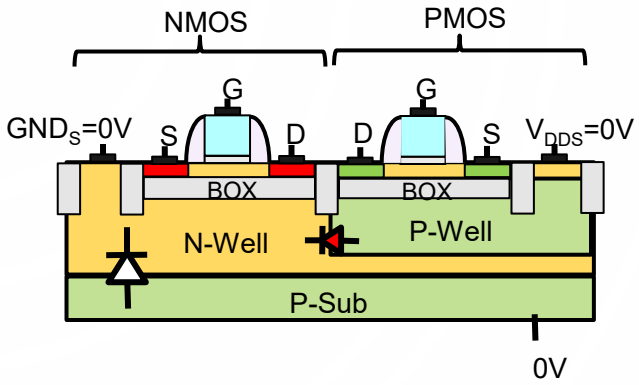
- Bulk CMOS
  - Leakage paths through bulk
  - RDF dominates local variability
  - Diodes and B2B tunneling limit back-bias range

- UTBB FD-SOI
  - Thin body for short-channel control
  - No doping – less RDF
  - Extended back-bias range

FDSOI Wells and Back Bias



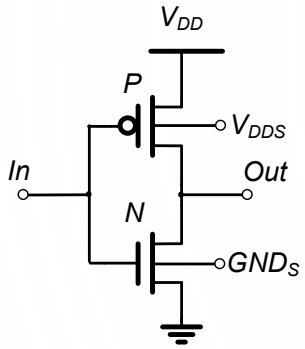
- Typical (RVT)
  - $GND_{S,nom}$ = 0V, $V_{DDS,\ nom}$ = V_{DD}
  - Reverse body bias, V_{BSN} < 0V
  - (-3V) < GND_S < V_{DD}/2+0.3V
    - Limit due to diodes, BOX
  - Can reverse bias 2-3V each

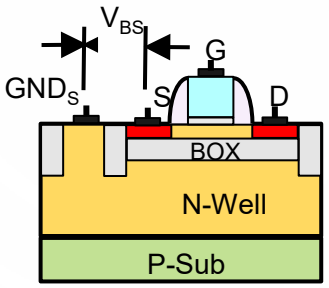


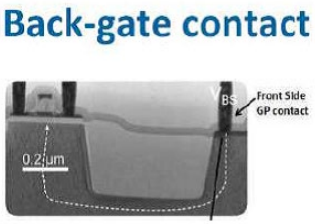
- Flip-well (LVT)
  - $V_{DDS,\ nom}$ = $GND_{S,nom}$ = 0V
  - Forward body bias V_{BSN} > 0V
  - 0.3V < GND_S < (3V)
    - Limit due to diodes, BOX
  - Can forward bias 2-3V each

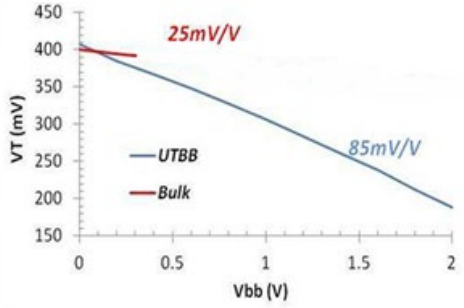
P. Flatresse, ISSCC'13

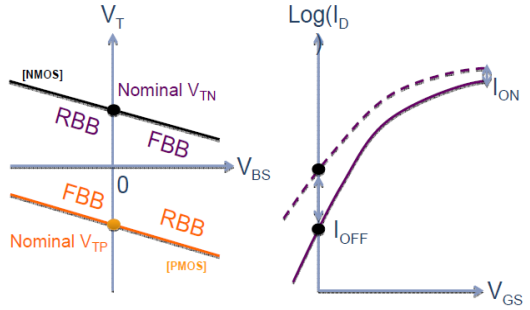
Back-Bias in FDSOI







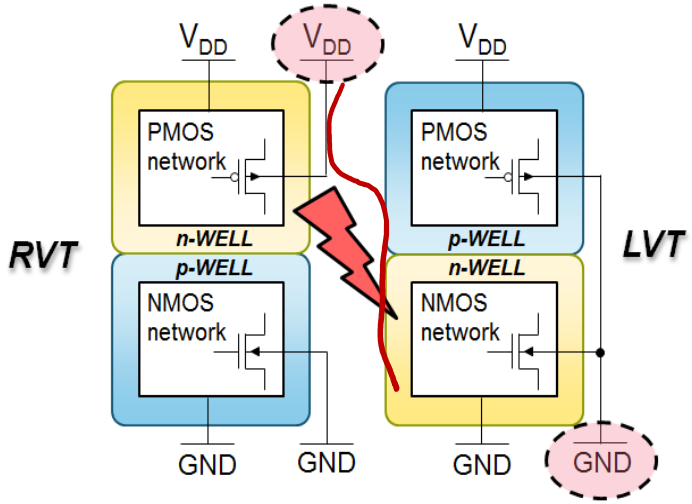




- γ = 85mV/V body coefficient, and extended voltage range
  - Lower coefficient and voltage range in bulk, finFET

D. Jacquet, JSSC 4/14

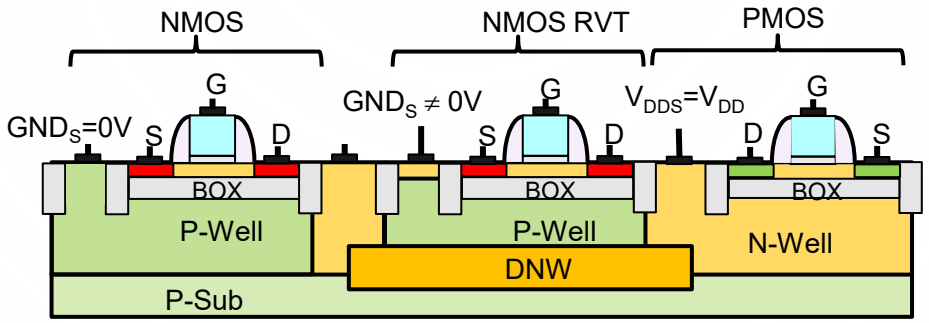
Multi V_{Th}



- No channel implant in 28FDSOI
  - No multi V_{Th}
- Can't abut wells
  - RVT and LVT require different well biases

D. Jacquet, JSSC 4/14

Back Bias in FDSOI



- Triple well (deep N-Well, DNW) allows for separate back bias
- Layout penalty; capacitance to drive

Digital Logic: UPF

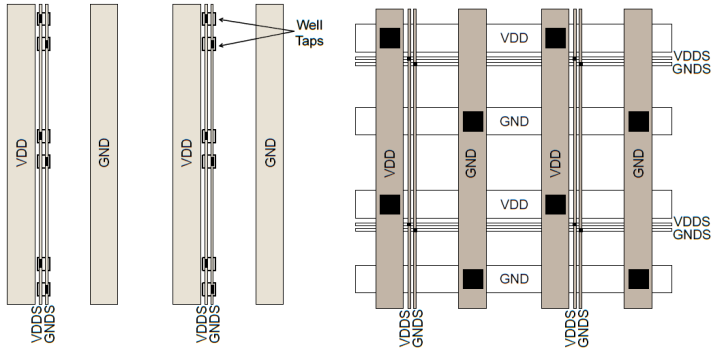
- Supply, back-bias defined in Unified Power Format (UPF)
  - Or Common Power Format (CPF)
- Handled by synthesis, place and route tools

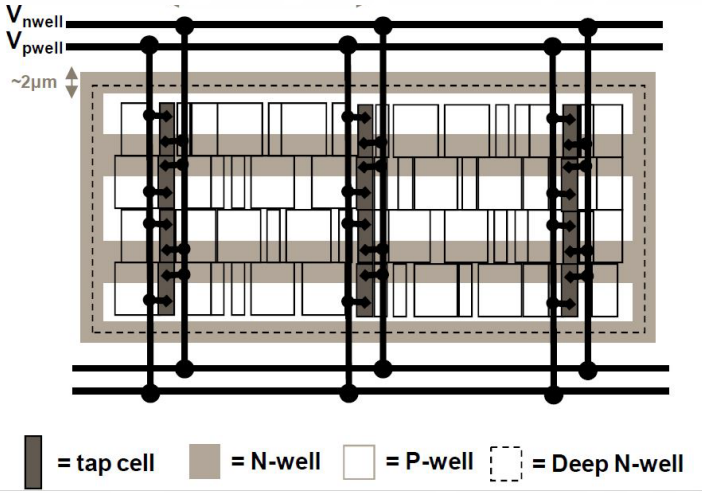
```
UPF description of PT_TOP with GND, VDD, GNDS and VDDS supplies.
create_power_domain PD_TOP

create_supply_port GND
create_supply_port VDD
create_supply_net  GND -domain PD_TOP
connect_supply_net GND -ports {GND}
create_supply_net  VDD -domain PD_TOP
connect_supply_net VDD -ports { VDD }

set_domain_supply_net PD_TOP -primary_power_net VDD -primary_ground_net GND

# Body-bias specification
create_supply_port VDDS
create_supply_port GNDS
create_supply_net  VDDS -domain PD_TOP
connect_supply_net VDDS -ports { VDDS vddgndvdds*/VDDSCORE }
create_supply_net  GNDS -domain PD_TOP
connect_supply_net GNDS -ports { GNDS gnds*/VDDCORE1V8 }

create_supply_set back_bias_set \
-function {nwell VDDS} \
-function {pwell GNDS} \
-reference_gnd {GND} \

create_power_domain PD_TOP -update -supply bias
associate_supply_set back_bias_set -handle PD_TOP.bias
```

M.Blagojevic, Ph.D. Dissertation, ISEP 2017

Digital Logic - Implementation

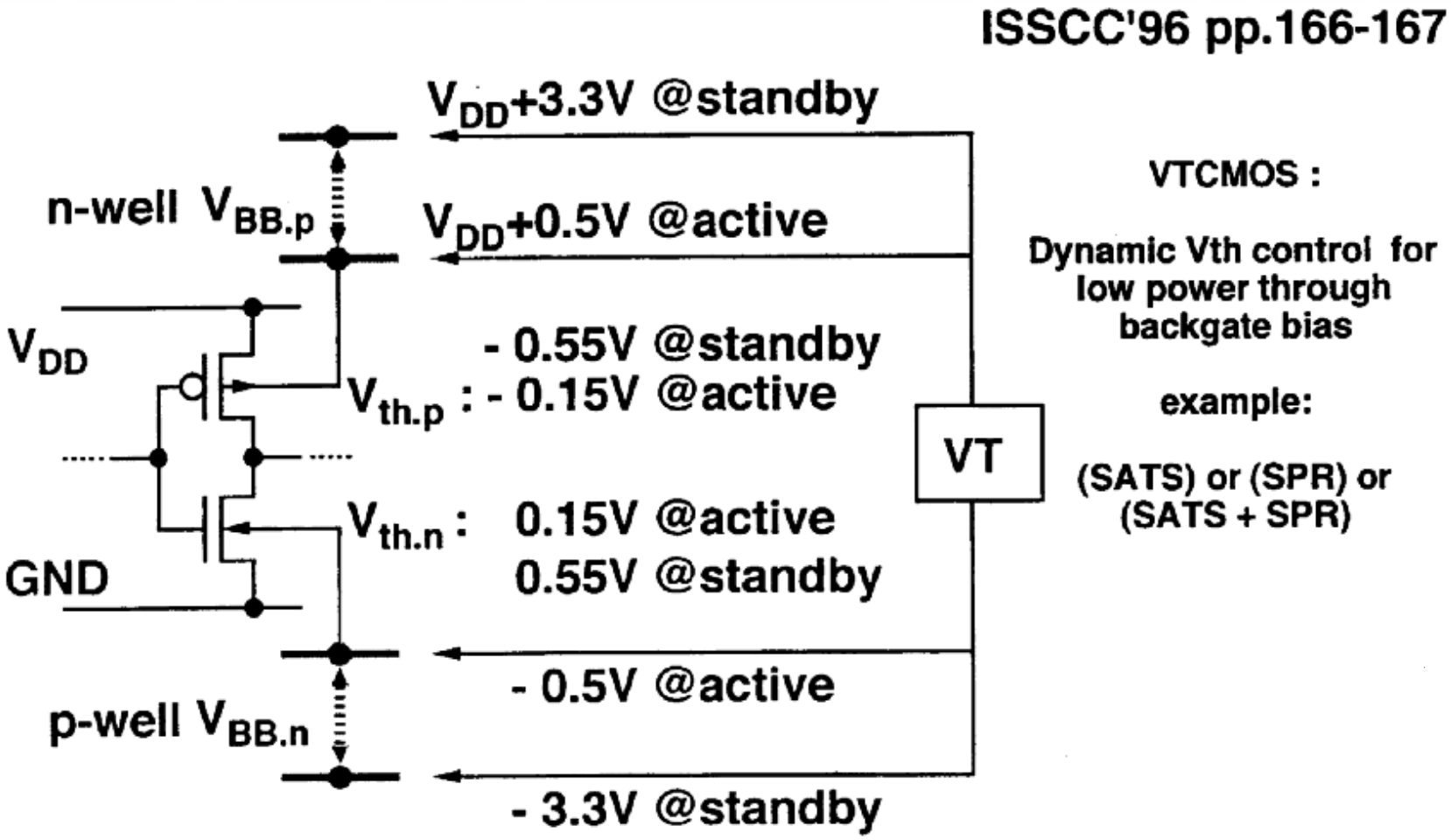
- Well taps added explicitly
  - Difference from bulk



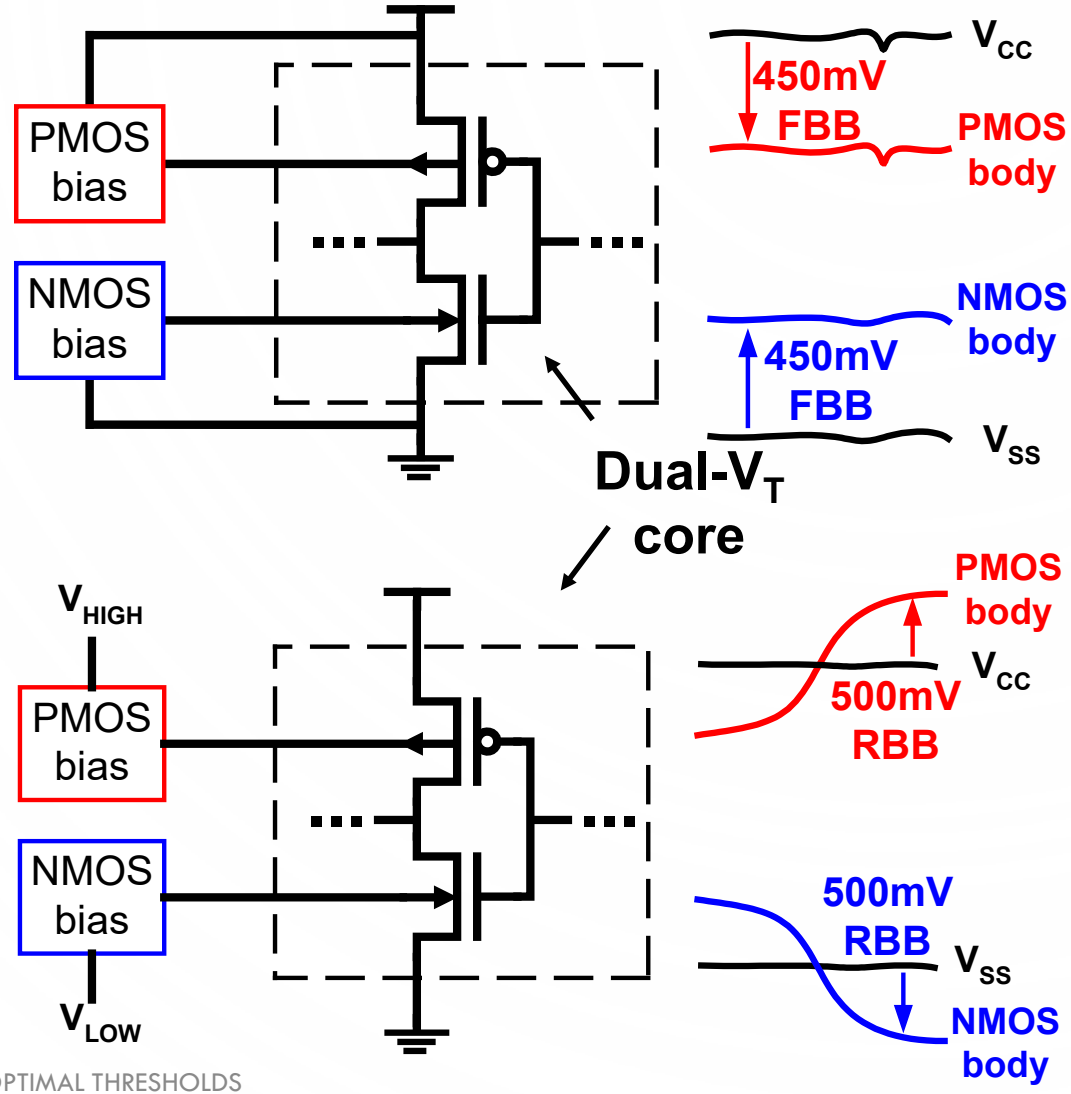


- **Back bias straps**
  - Low DC current
  - Except for very fast transitions

Dynamic Body Bias (Bulk)



Dynamic Body Bias (Bulk)



Active mode

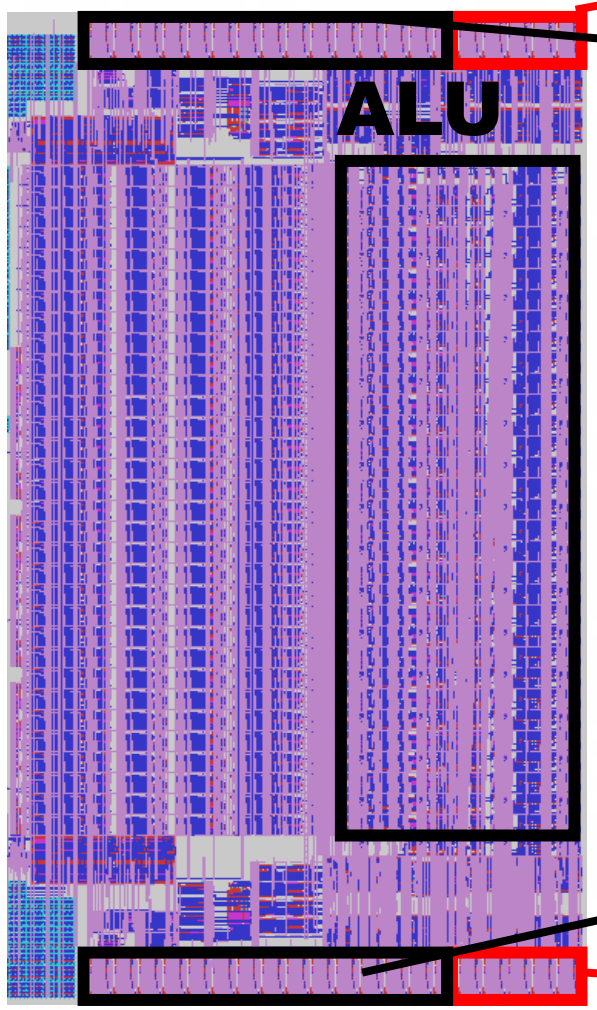
Forward body bias (FBB)
Local V_{CC} tracking

Idle mode

Reverse body bias (RBB)
Triple well needed

Tschanz, ISSCC'03

Body Bias Layout



Sleep transistor LBGs

ALU core LBGs

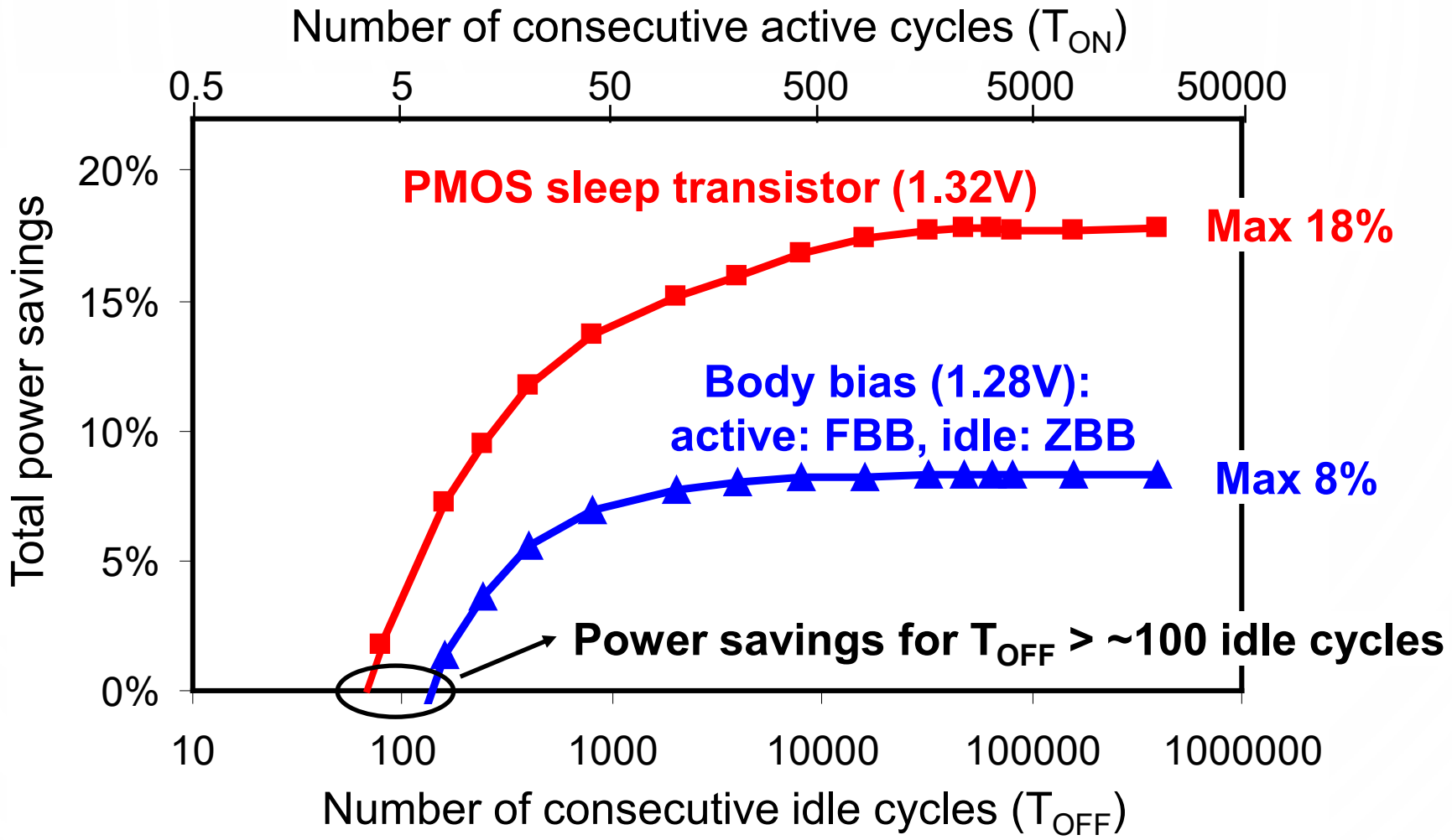
Number of ALU core LBGs	30
Number of sleep transistor LBGs	10
PMOS device width	13mm
Area overhead	8%

ALU core LBGs

Sleep transistor LBGs

Total Active Power Savings

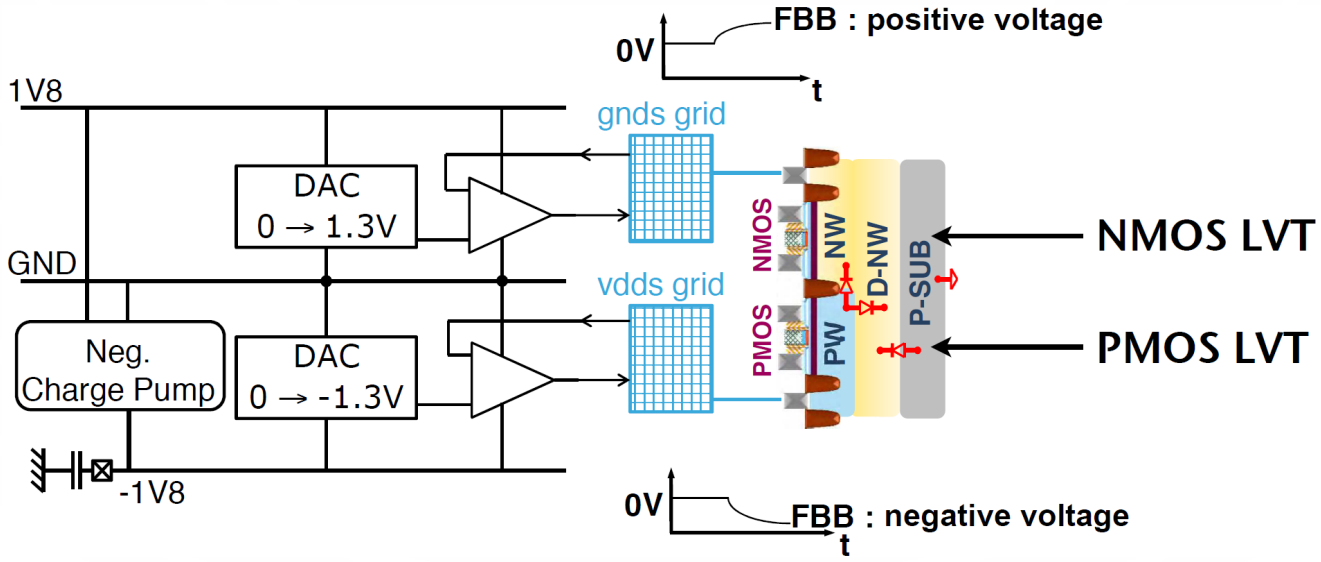
(Fixed activity: $\alpha = 0.05$)



Reference: 450mV FBB to core with clock gating, 1.28V, 4.05GHz, 75°C

Generating Back-Bias

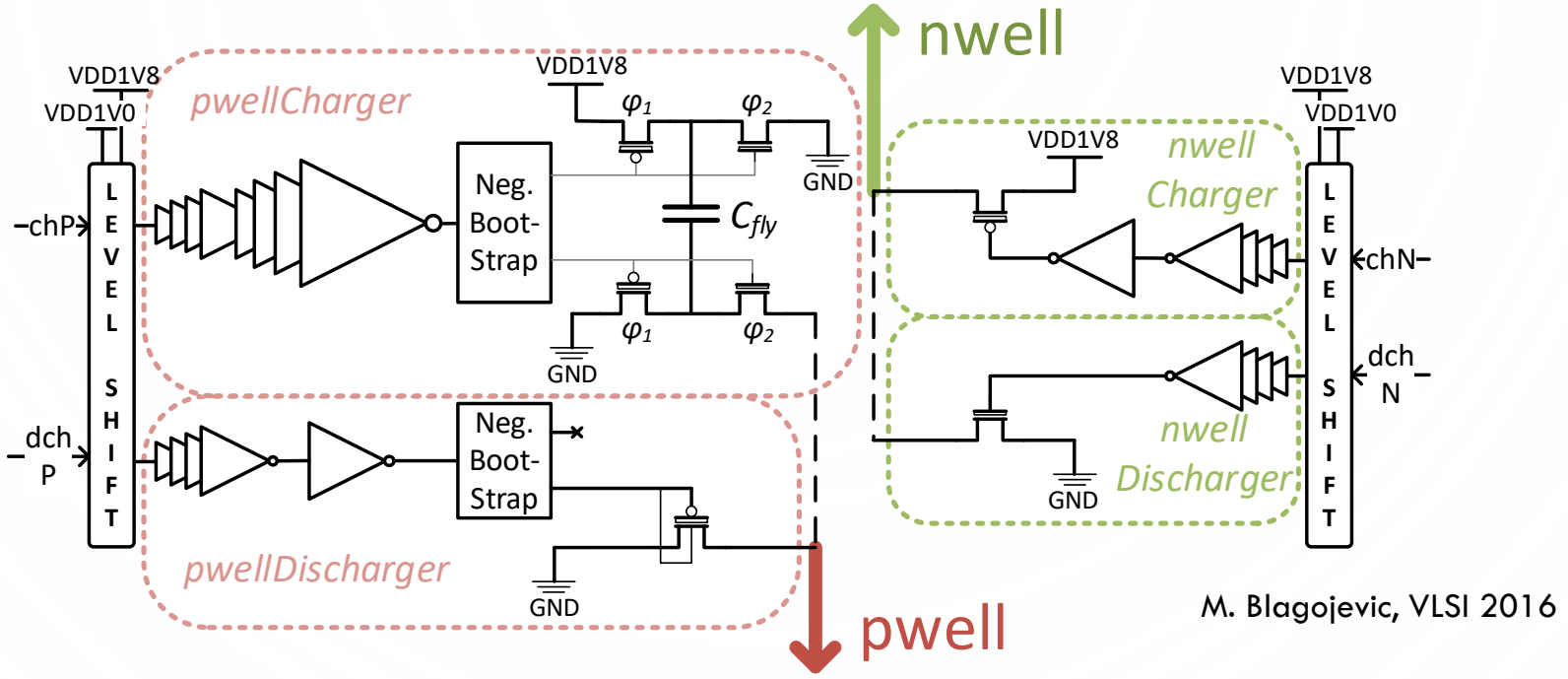
- Tradeoff – speed of charging and discharging well caps
- Often measure V_{BB} indirectly (leakage)
- Challenge: Generating $-V_{SS}$
- 28nm FDSOI implementation



D. Jacquet, VLSI 2013

Generating Back Bias

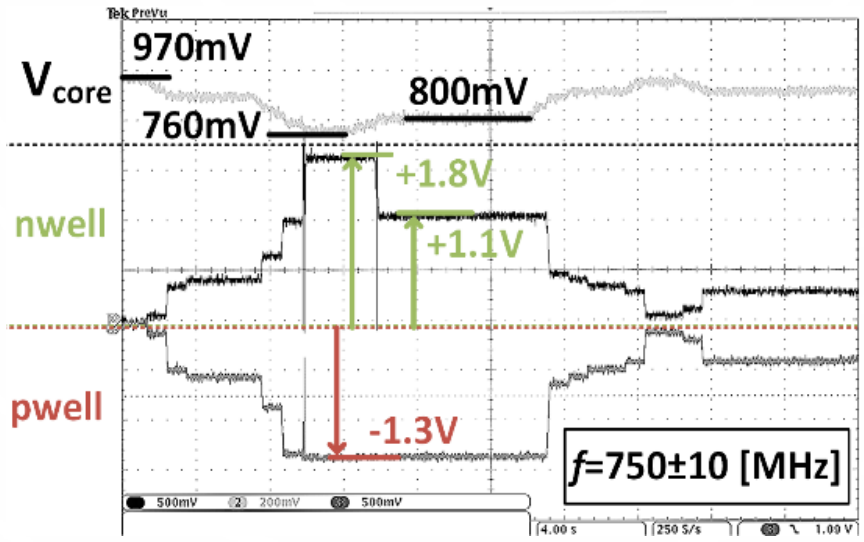
- Fast and wide voltage range back-bias in FDSOI



M. Blagojevic, VLSI 2016

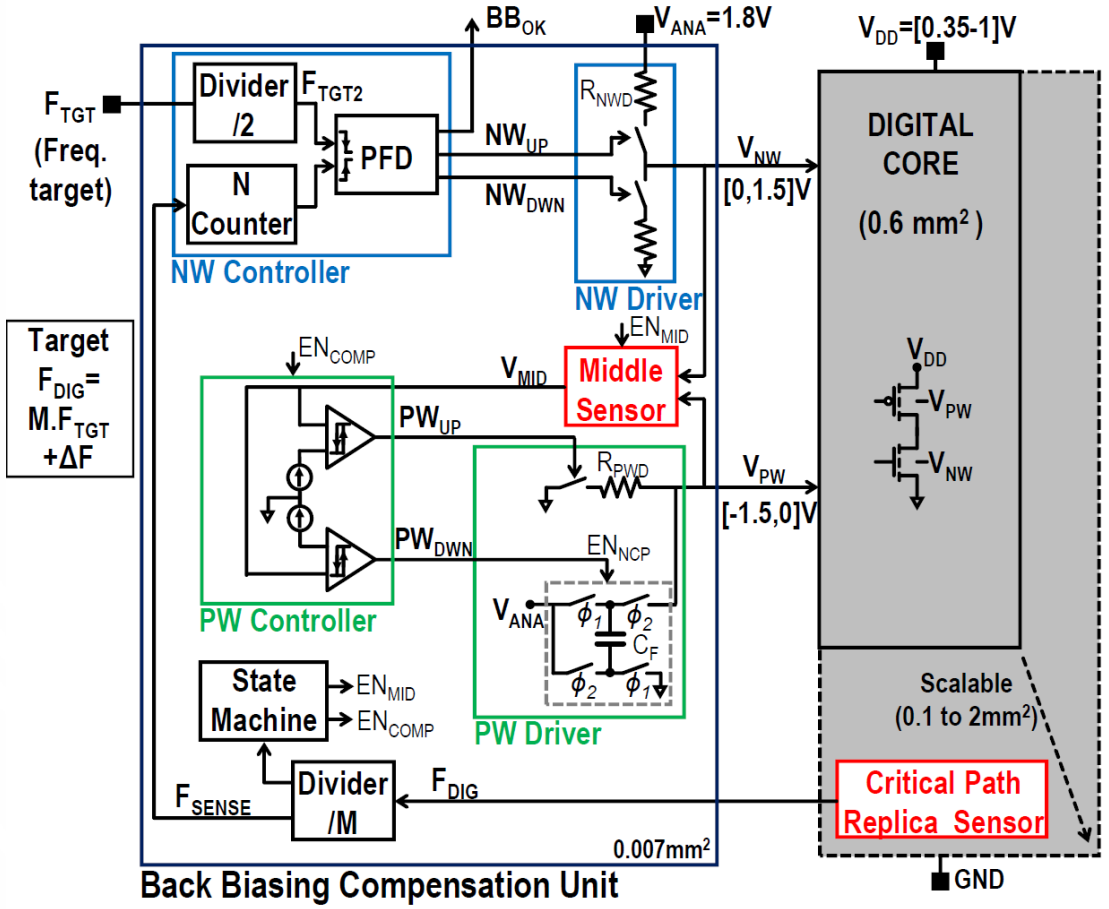
Switched capacitors generate negative bias and pump substrate

Supply/Process Compensation



- Able to track ~200mV supply droops and maintain constant frequency (measured by a replica) by back-bias adjustments

Dynamic Frequency Loop in FDSOI



Quelen, ISSCC'18

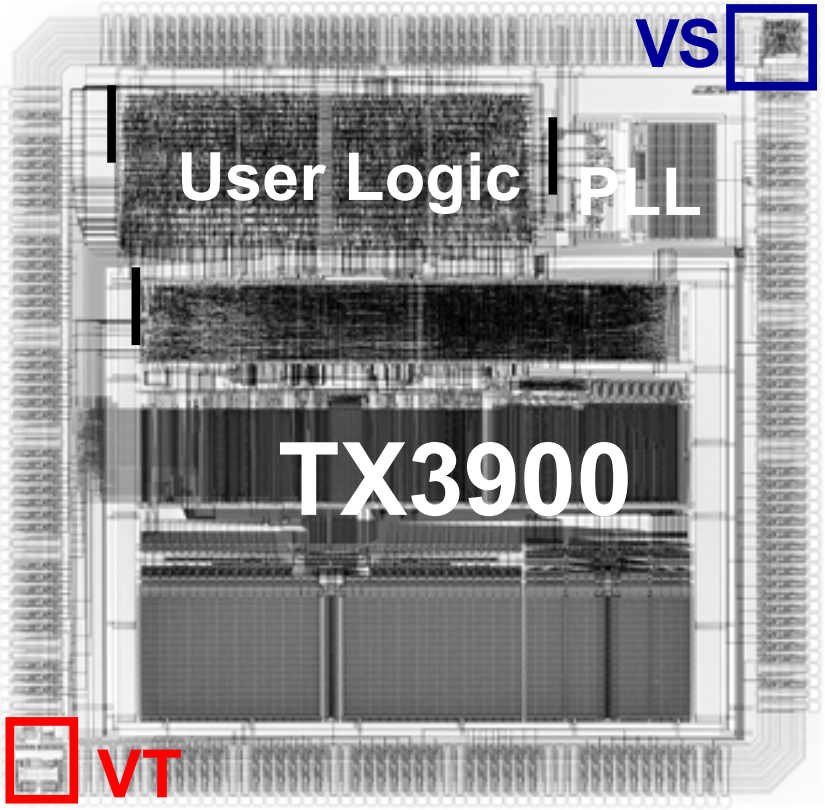
Announcements

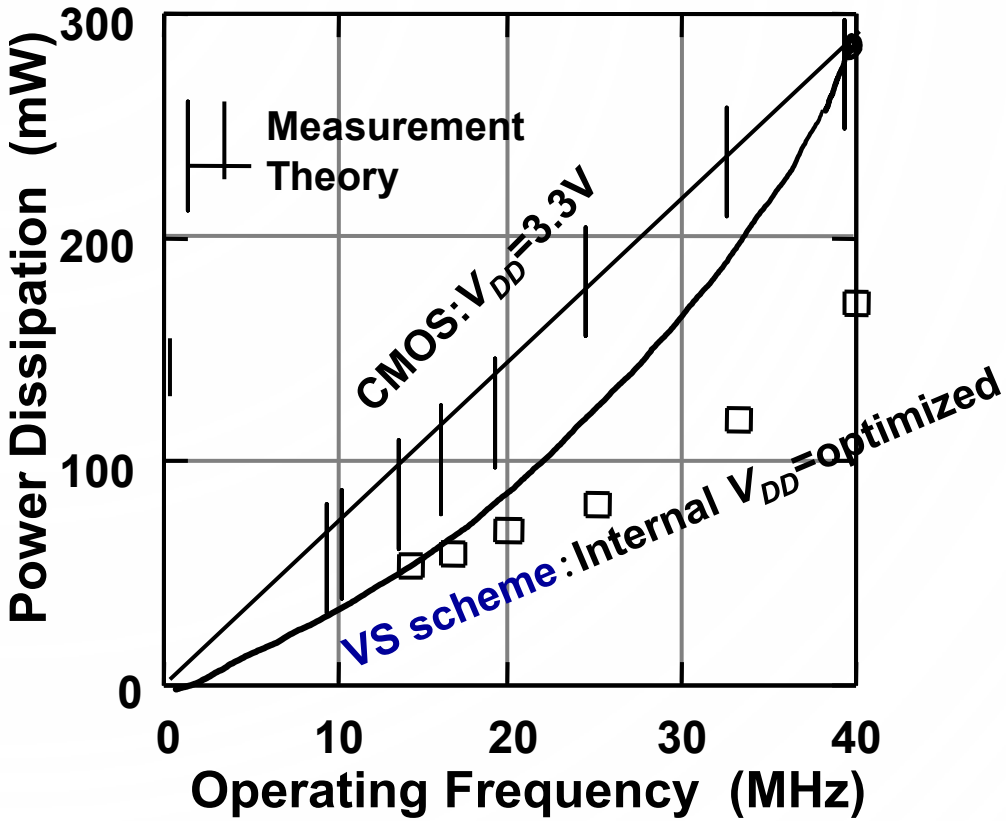
- Quiz 3 today
- Homework 4 due next week

5.0 Optimal V_{DD}, V_{Th}

Dynamic Voltage Scaled Microprocessor

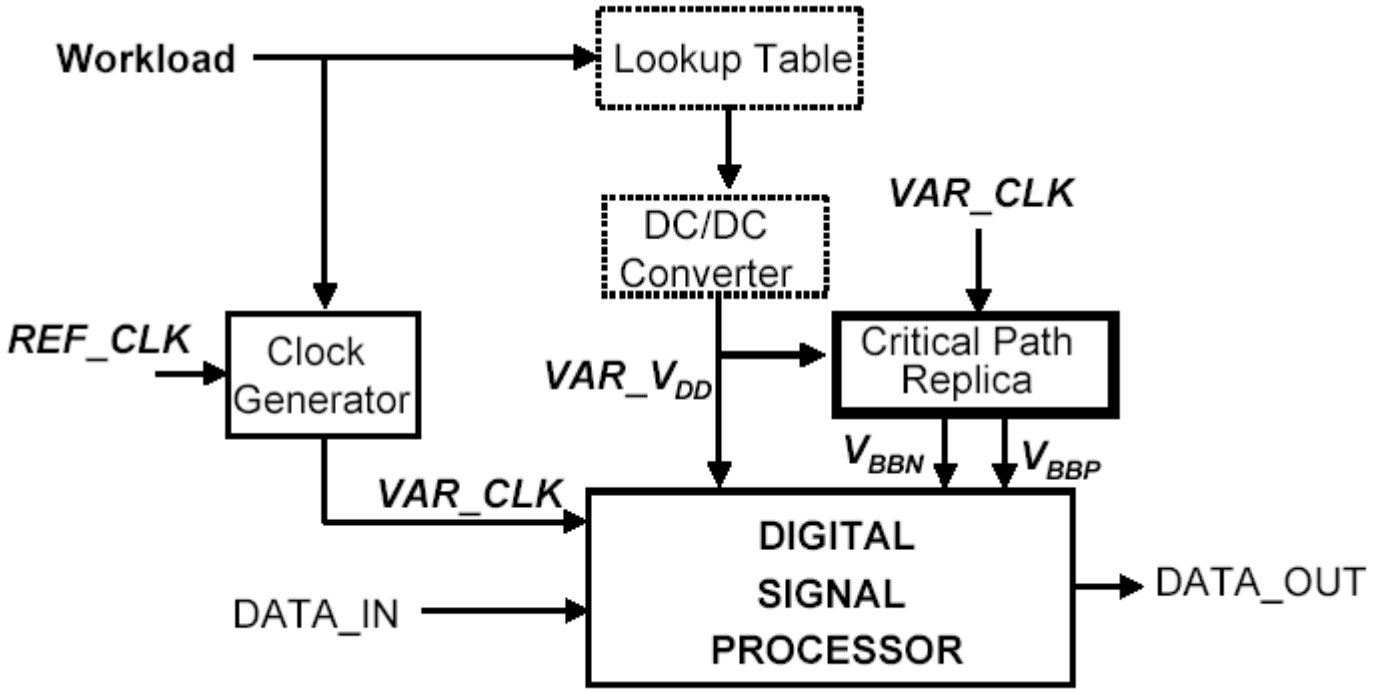
External V_{DD} 3.3V±10%
Internal V_{DDL} 0.8V~2.9V ±5%





Courtesy: Prof. Kuroda

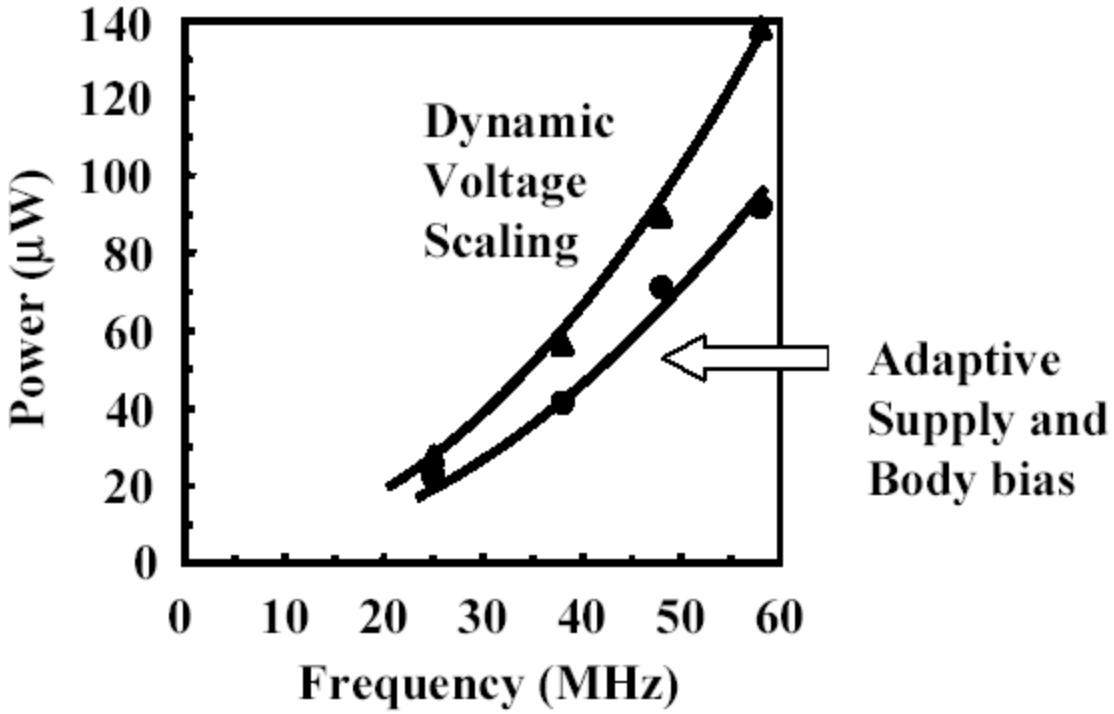
Adapting V_{DD} and V_{TH}



- Adapting both V_{DD} and V_{Th} during runtime
  - V_{Th} is much less sensitive

Miyazaki, ISSCC'02

Adapting V_{DD} and V_{TH}



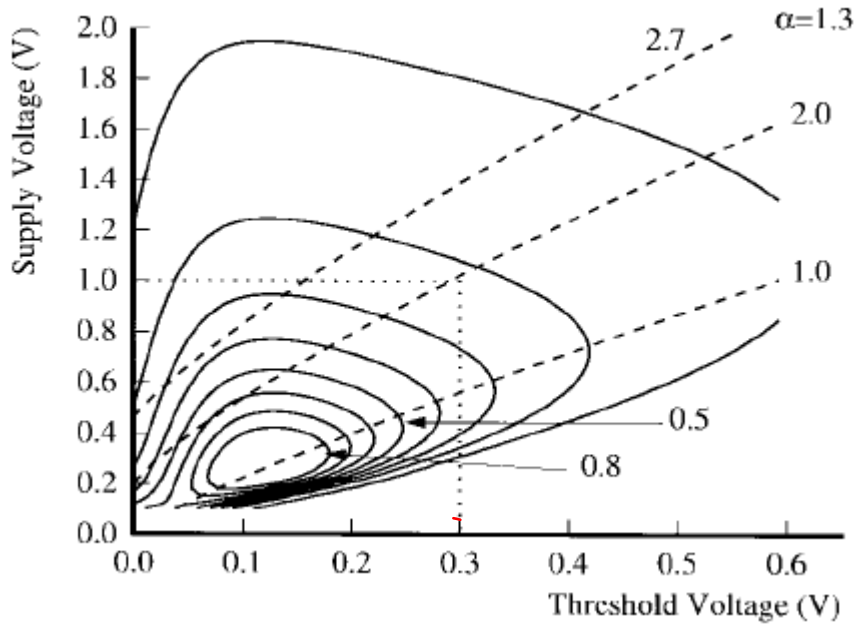
Miyazaki, ISSCC'02

Optimal V_{DD}, V_{Th}

- Adjusting V_{DD}, V_{Th} trades of energy and delay
- We studied energy-limited design
  - And alternate ways for optimizing energy and delay together
  - E.g. energy-delay product (EDP)
  - Or E^nD^m, $n,m > 1$

Optimal EDP Contours

- Plot of EDP curves in V_{DD}, V_{Th} plane



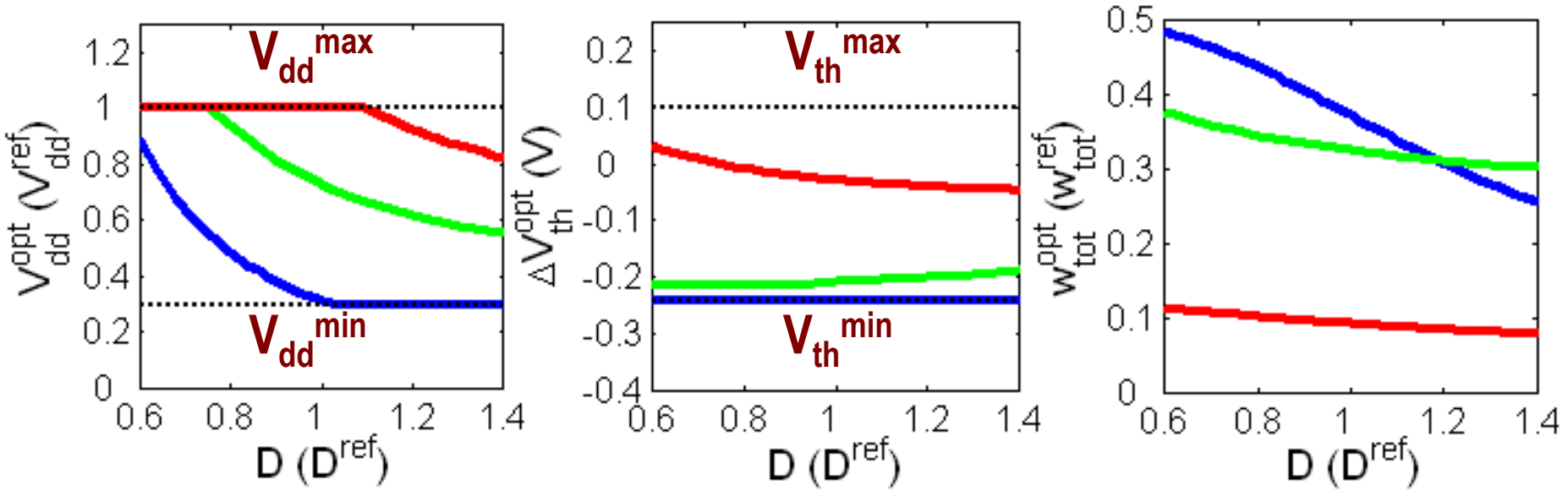
Gonzalez, JSSC 8/97

Sizing, Supply, Threshold Optimization

Reference Design:
D^{ref} (V_{dd}^{max},V_{th}^{ref})

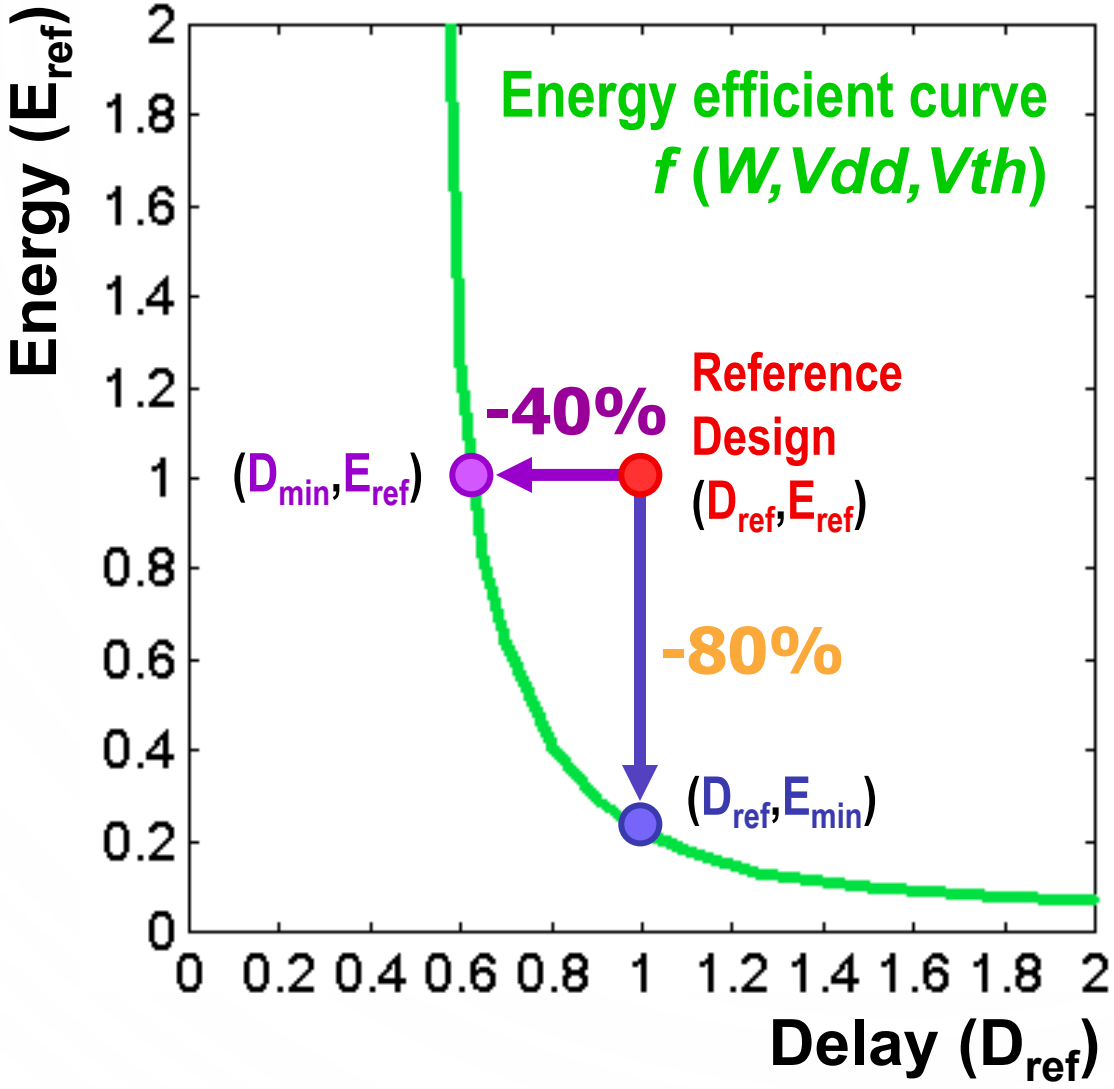
Topology	Inverter	Adder	Decoder
$(E_{Lk}/E_{Sw})^{ref}$	0.1%	1%	10%

Large variation in optimal circuit parameters V_{dd}^{opt}, V_{th}^{opt}, w^{opt}



Technology parameters (V_{dd}^{max}, V_{th}^{ref}) rarely optimal

Result: E-D Tradeoff in an Adder



Sensitivity	W	Vdd	Vth
(D_{ref},E_{ref})	∞	1.5	0.2
(D_{ref},E_{min})	1		
(D_{min},E_{ref})	22	16	22

80% of energy saved without delay penalty

40% delay improvement without energy penalty

Energy-constrained delay

- Active power

$$P_{act} = \alpha f C V_{DD}^{\ 2}$$

$$f = 1/L_D t_p$$

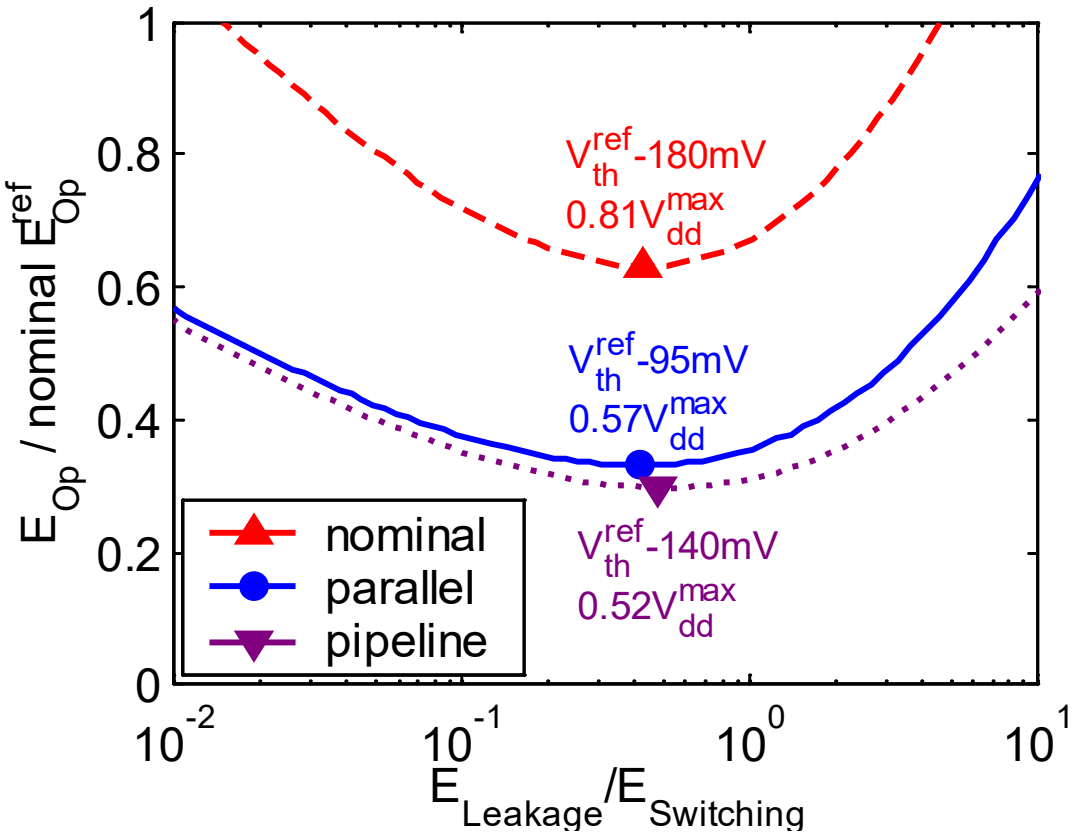
- Leakage power

$$P_{leak} = I_0 e^{\frac{-V_{Th} - \gamma V_{DD}}{S}} V_{DD}$$

- Eliminate one variable(V_{Th}) and find P_{min}(V_{DD})

Nose, ASP-DAC'00

Minimum energy: $E_{Sw} = 2_{ELk}$

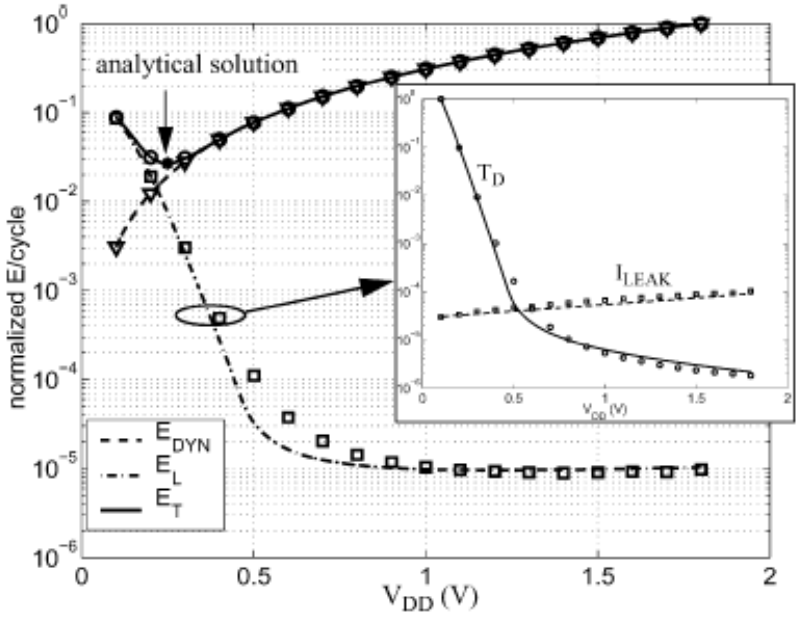


- Large $(E_{Lk}/E_{Sw})^{opt}$
- Flat E_{Op} minimum
- Topology dependent

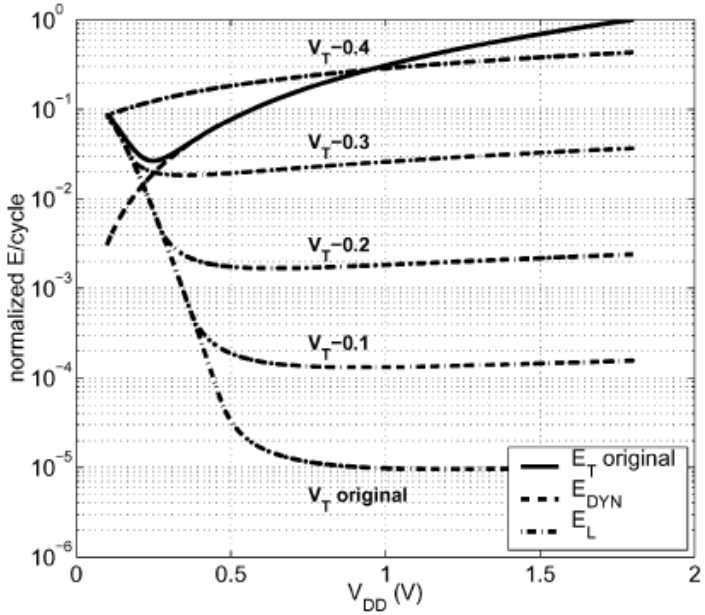
$$\left(E_{Lk}/E_{Sw}\right)_{opt} = \frac{2}{\ln\left(\frac{L_d}{\alpha_{avg}}\right) - K}$$

Optimal designs have high leakage ($E_{Lk}/E_{Sw} \approx 0.5$)

Subthreshold Optimum



f = 30kHz



Minimum is independent of V_T

Calhoun, JSSC 9/05

Summary

- Body effect weak in bulk CMOS
  - Strong in FDSOI
- Dynamic threshold scaling
  - Primarily for leakage control, process compensation
- Optimal thresholds
  - Total energy is minimized with 1/3 being leakage

Next Lecture

- Clock generation and distribution