

EECS251B : Advanced Digital Circuits and Systems

Lecture 13 – Timing

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Universal Chiplet Interconnect Express (UCle) Announced: Setting Standards For The Chiplet Ecosystem

March 2, 2022, AnandTech

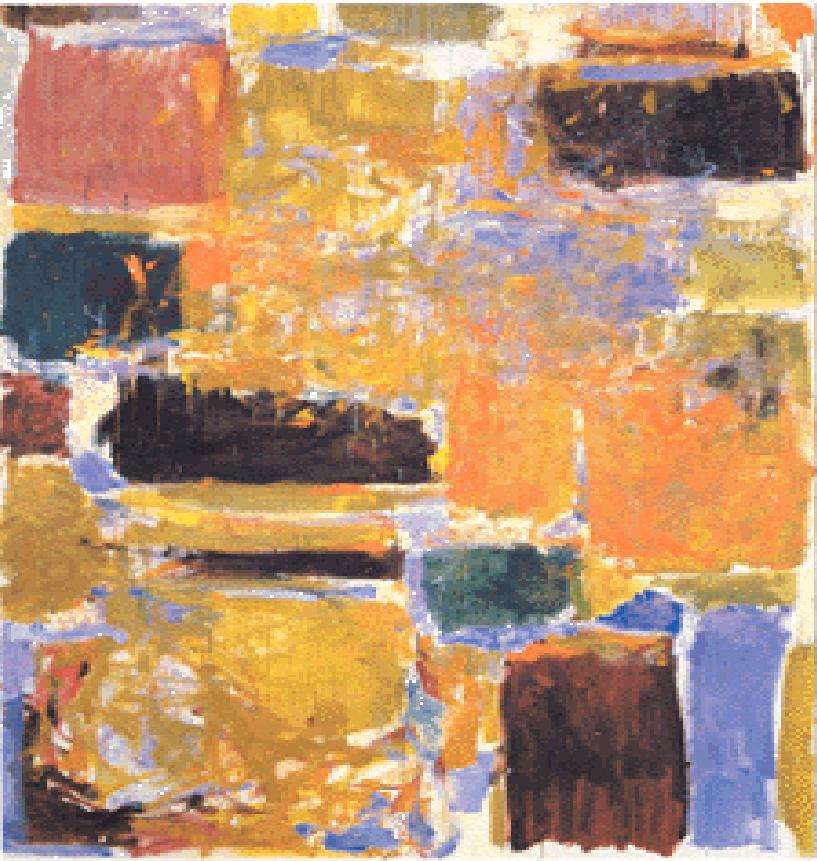
To that end, today Intel, AMD, Arm, and all three leading-edge foundries are coming together to announce that they are forming a new and open standard for chiplet interconnects, which is aptly being named **Universal Chiplet Interconnect Express**, or **UCle**.

www.uciexpress.org



Recap

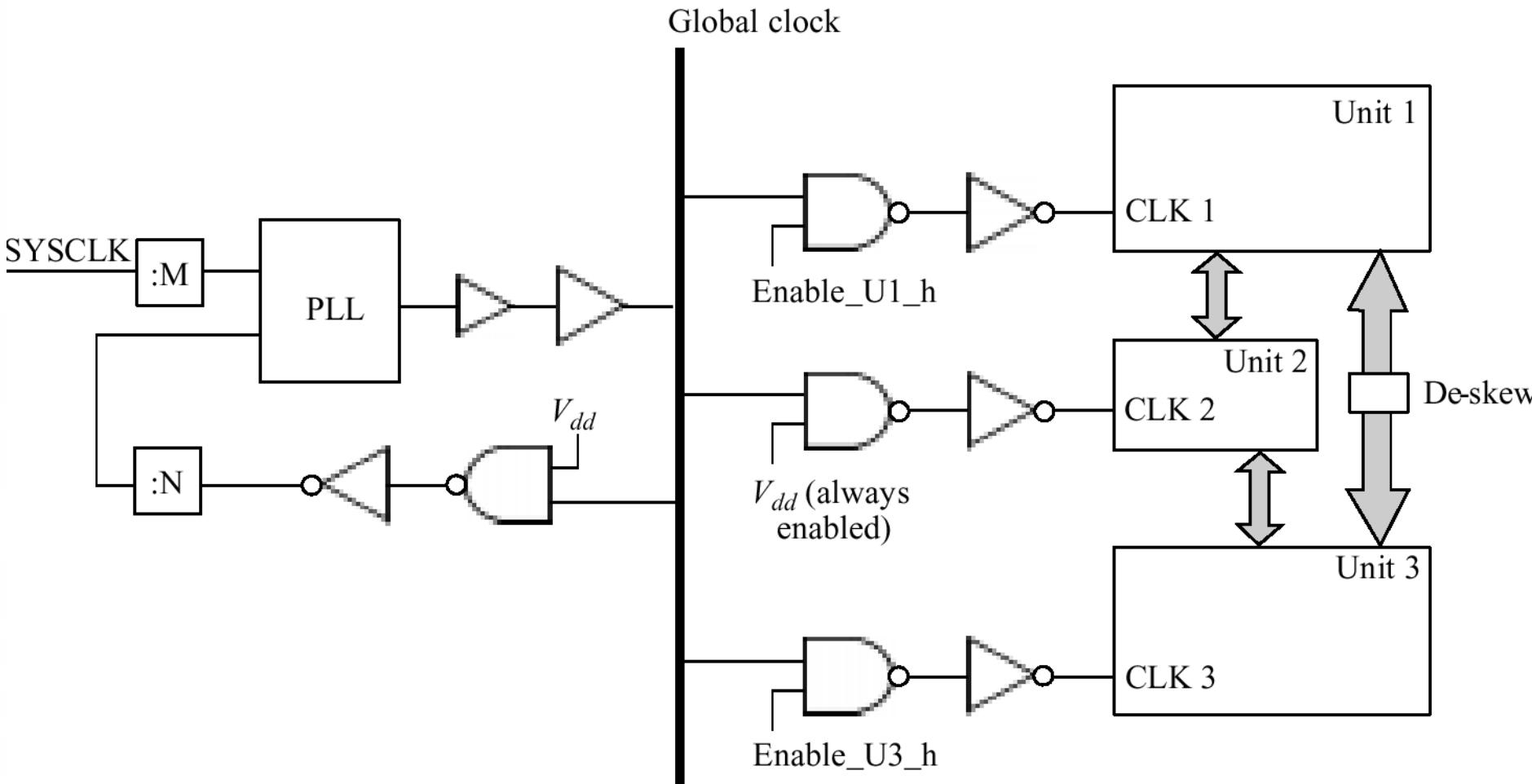
- Standard cell architectures depend on technology, maximize density-performance-power
- Standard cell library
 - Delay is tabulated, dependent on slope, load



Design for Performance

Flip-Flop-Based Timing

Example Clock System

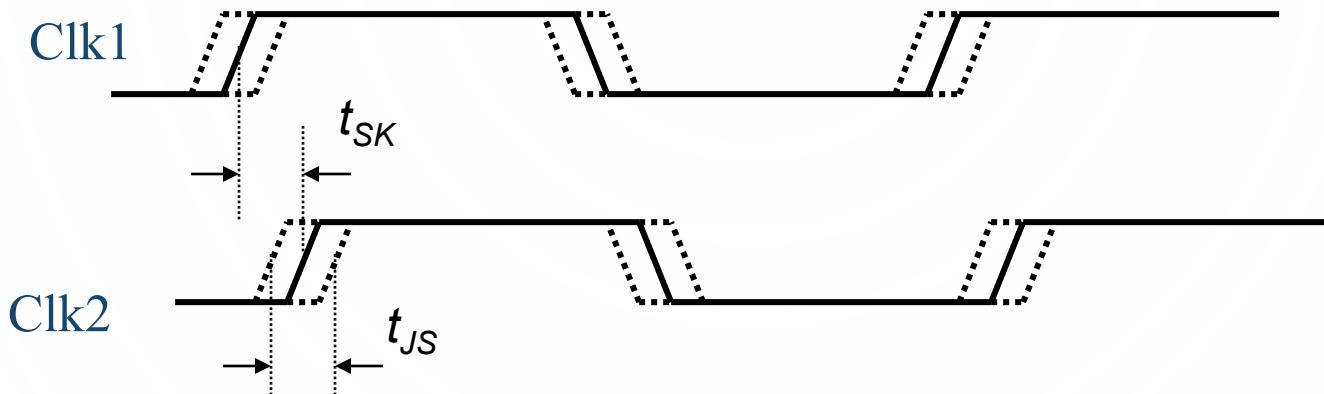


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Clock Nonidealities

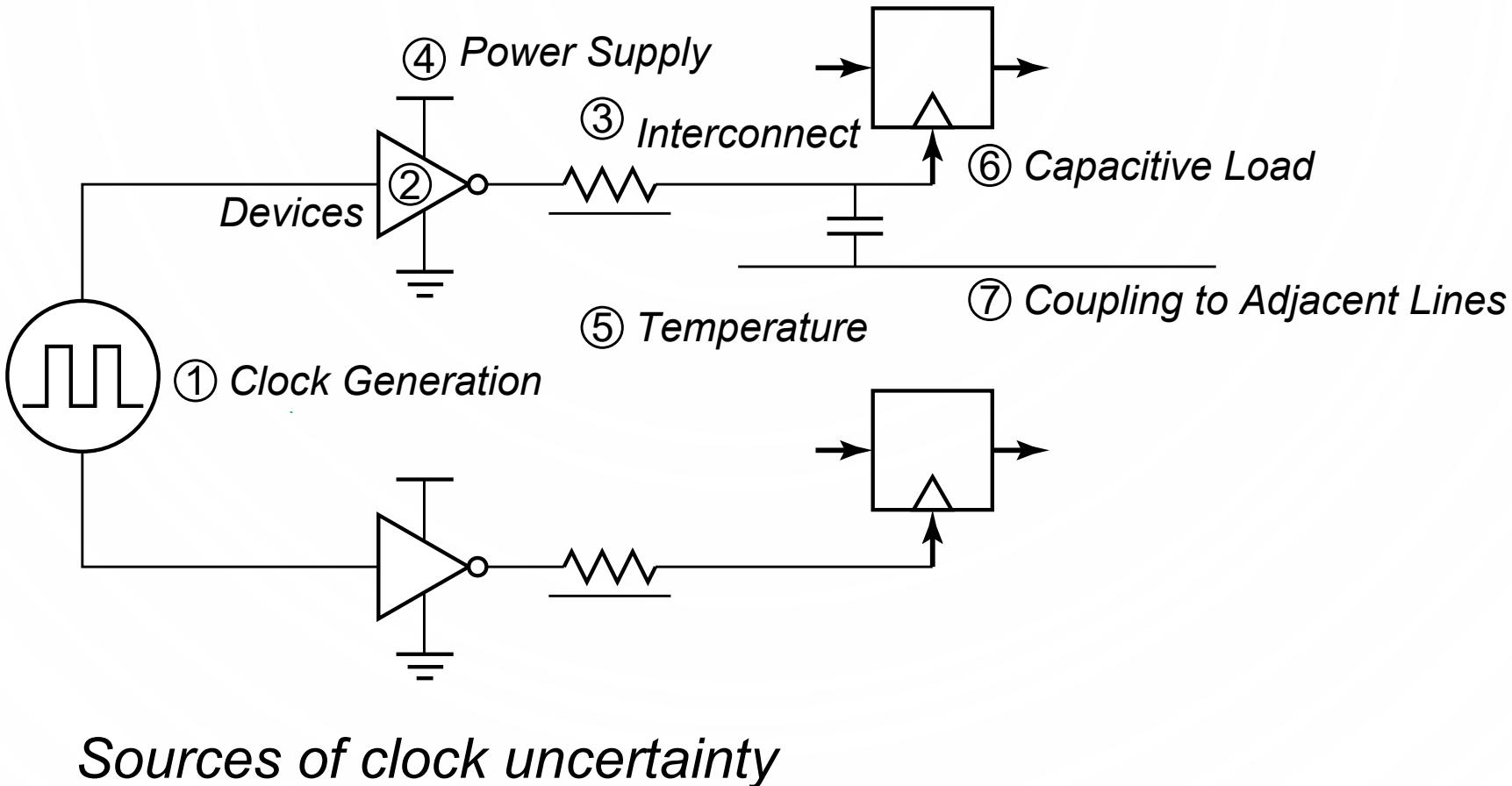
- Clock skew
 - Spatial variation in temporally equivalent clock edges; deterministic + random, t_{SK}
- Clock jitter
 - Temporal variations in consecutive edges of the clock signal; modulation + random noise
 - Cycle-to-cycle (short-term) - t_{JS}
 - Long-term - t_{JL}
- Variation of the pulse width
 - for level-sensitive clocking

Clock Skew and Jitter

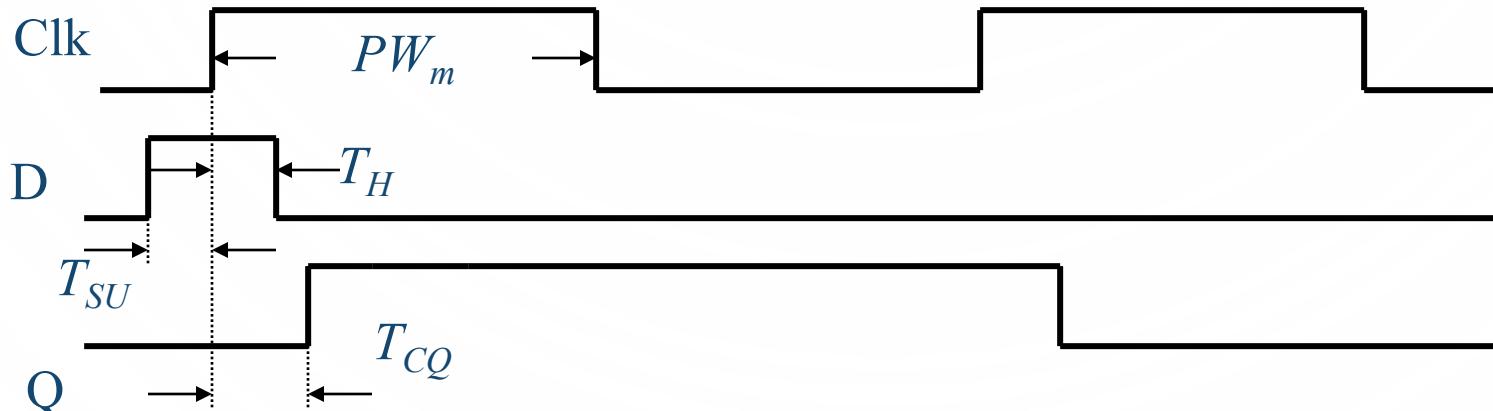
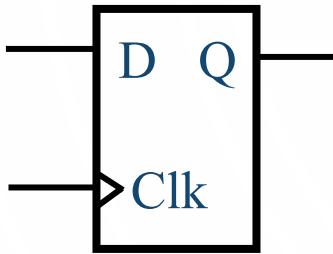


- Both skew and jitter affect the effective cycle time
- Only skew affects the race margin, if jitter is from the source
 - Distribution-induced jitter affects both

Clock Uncertainties

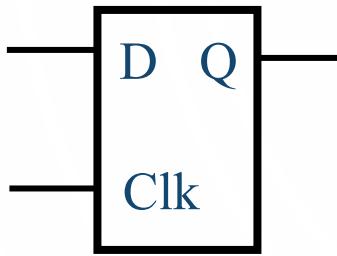


Flip-Flop Parameters

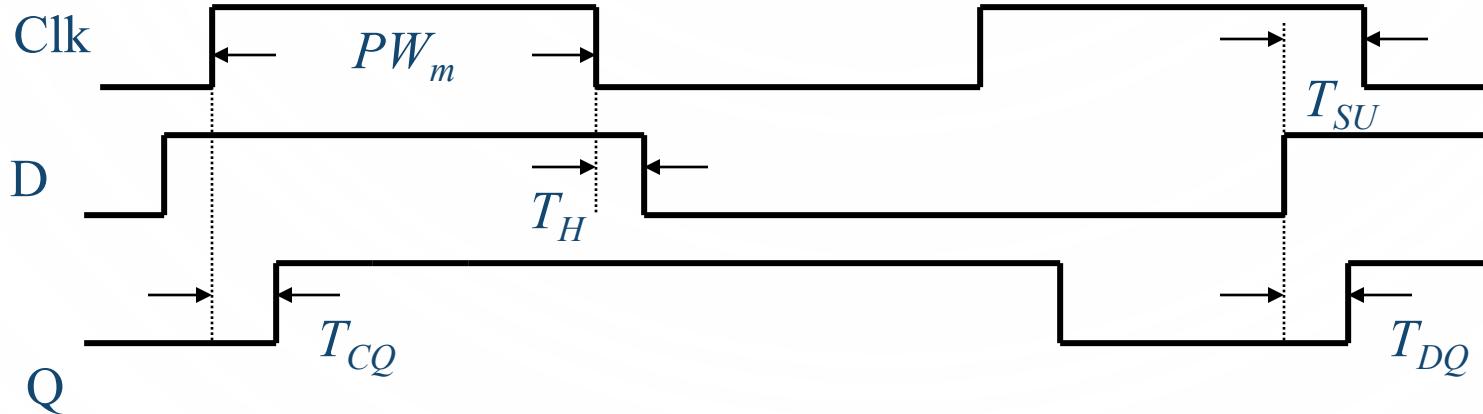


Delays can be different for rising and falling data transitions

Latch Parameters

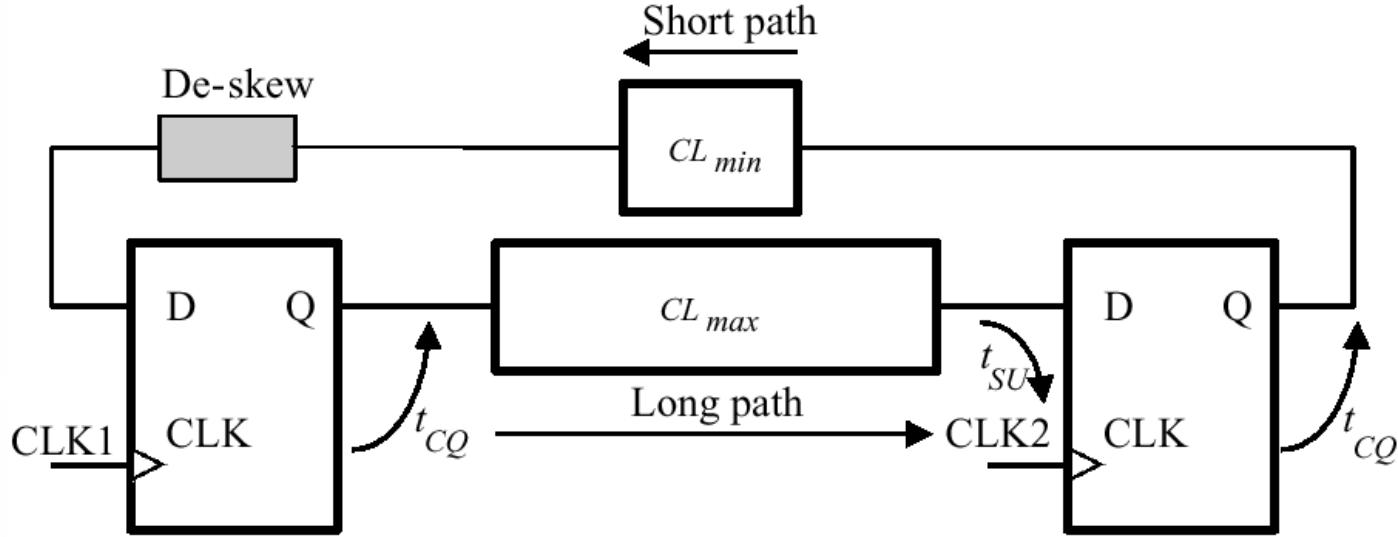


Unger and Tan
Trans. on Comp.
10/86



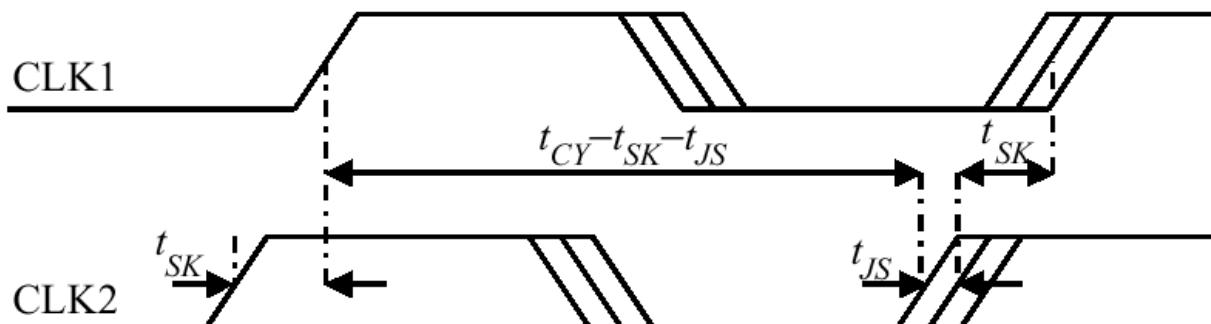
Delays can be different for rising and falling data transitions

Clock Constraints in Edge-Triggered Systems



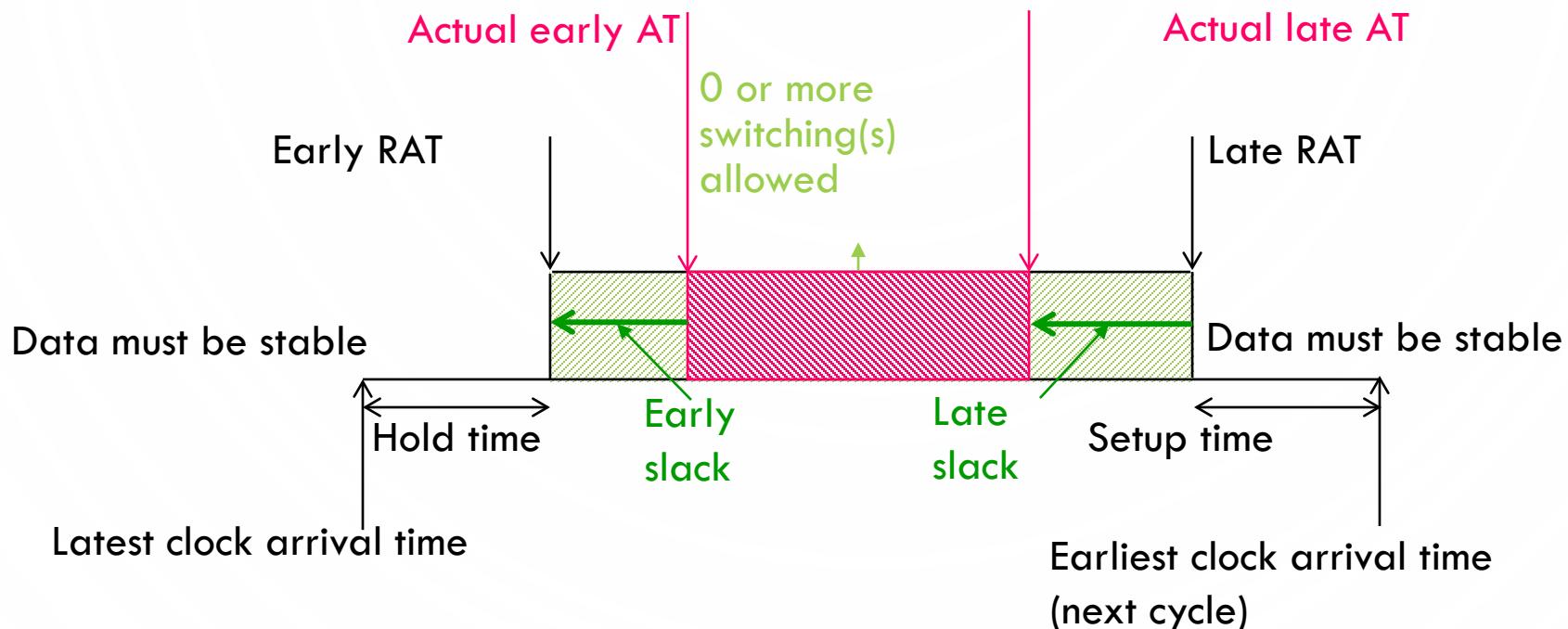
$$t_{CL} \leq (t_{CY} - t_{SK} - t_{JS}) - (t_{SU} + t_{CQ})$$

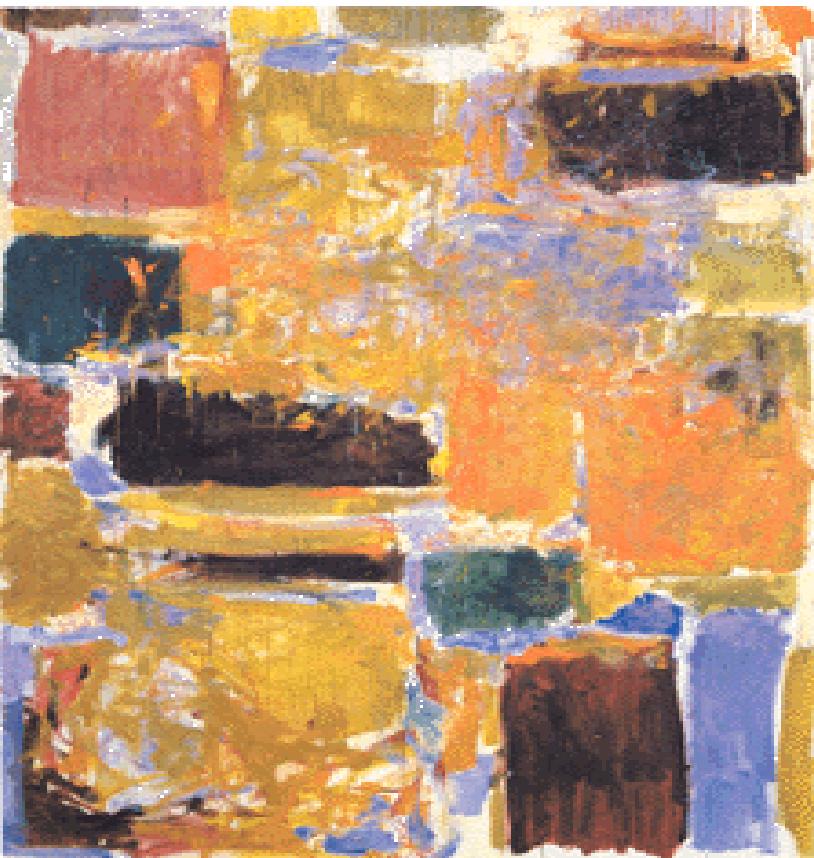
$$t_{CL} \geq t_{SK} + (t_H - t_{CQ})$$



Courtesy of IEEE Press, New York. © 2000

Pictorial View of Setup and Hold Tests



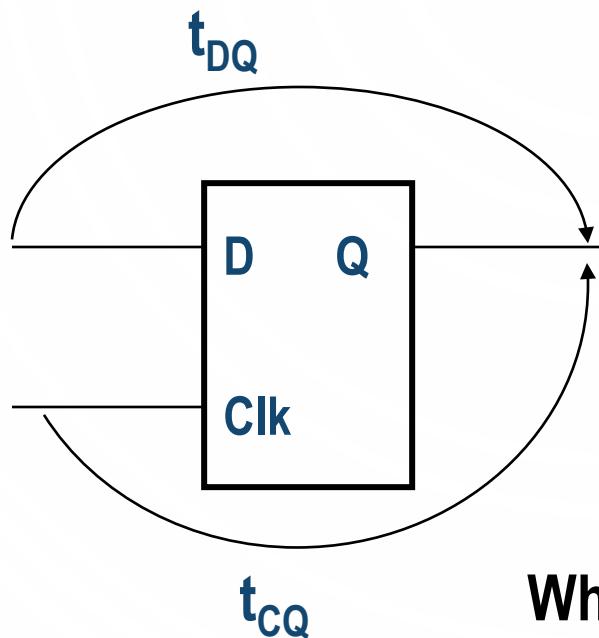


Latch Timing

Key Point

- Latch-based sequencing can improve performance, but is more complicated
 - Timing analysis not limited to a consecutive pair of latches

Latch Timing



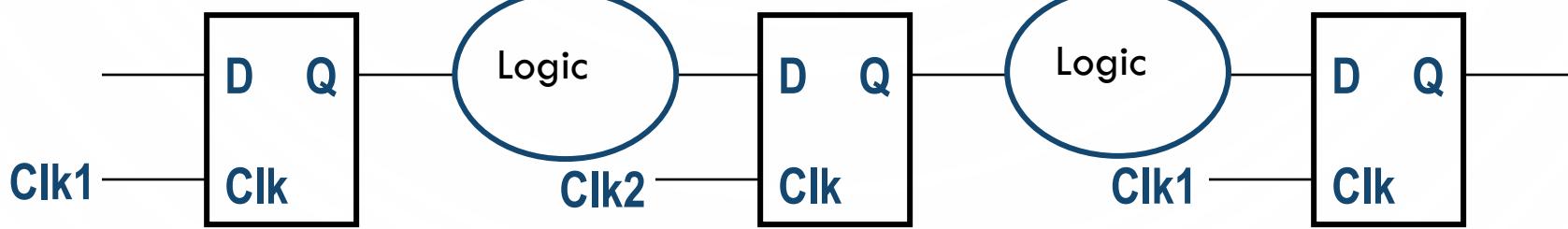
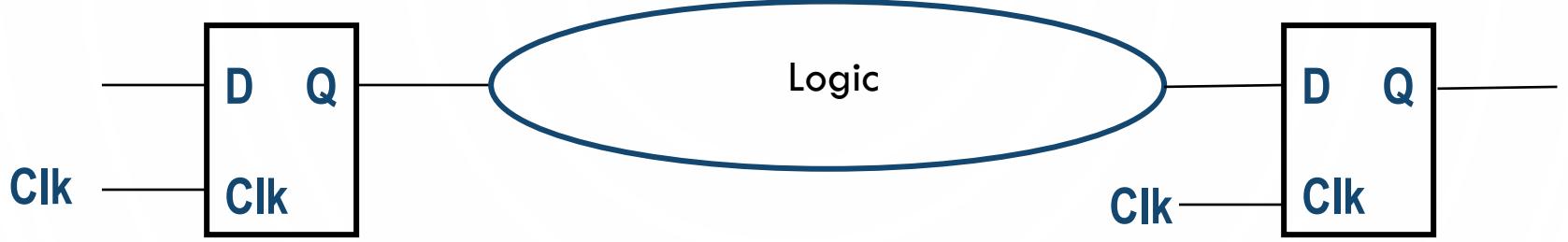
When data arrives
to transparent latch

Latch is a 'soft' barrier

When data arrives
to non-transparent latch

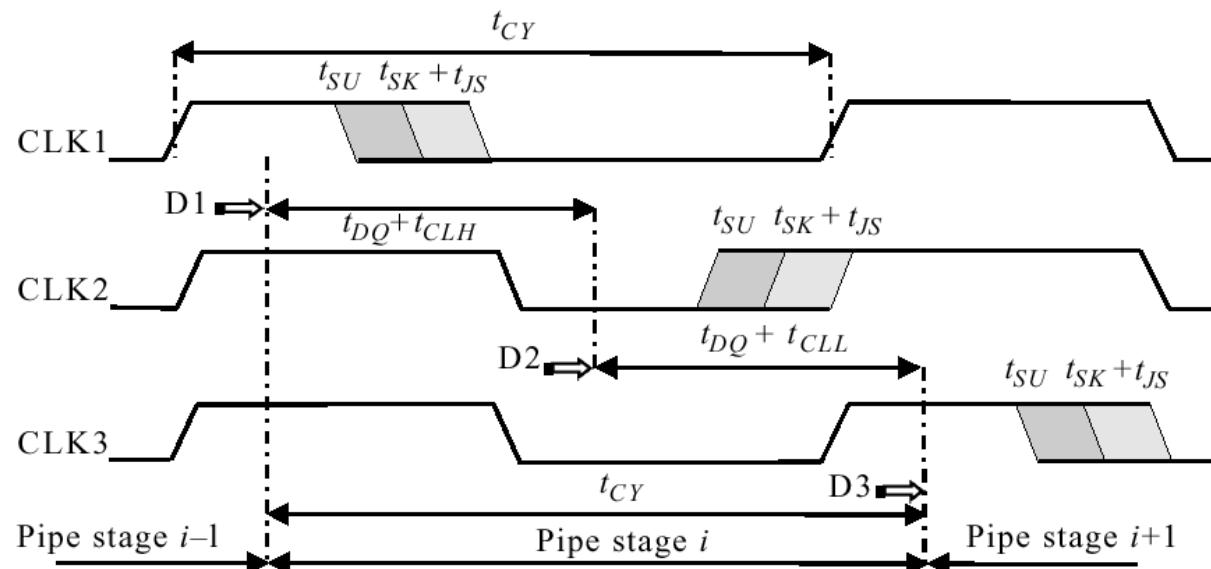
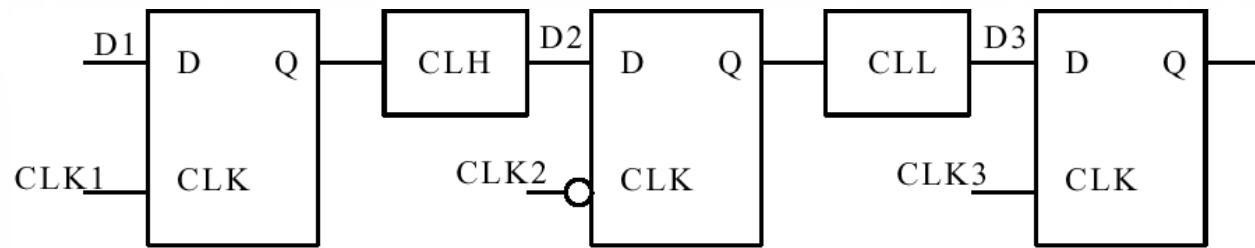
Data has to be 're-launched'

Latch Sequencing



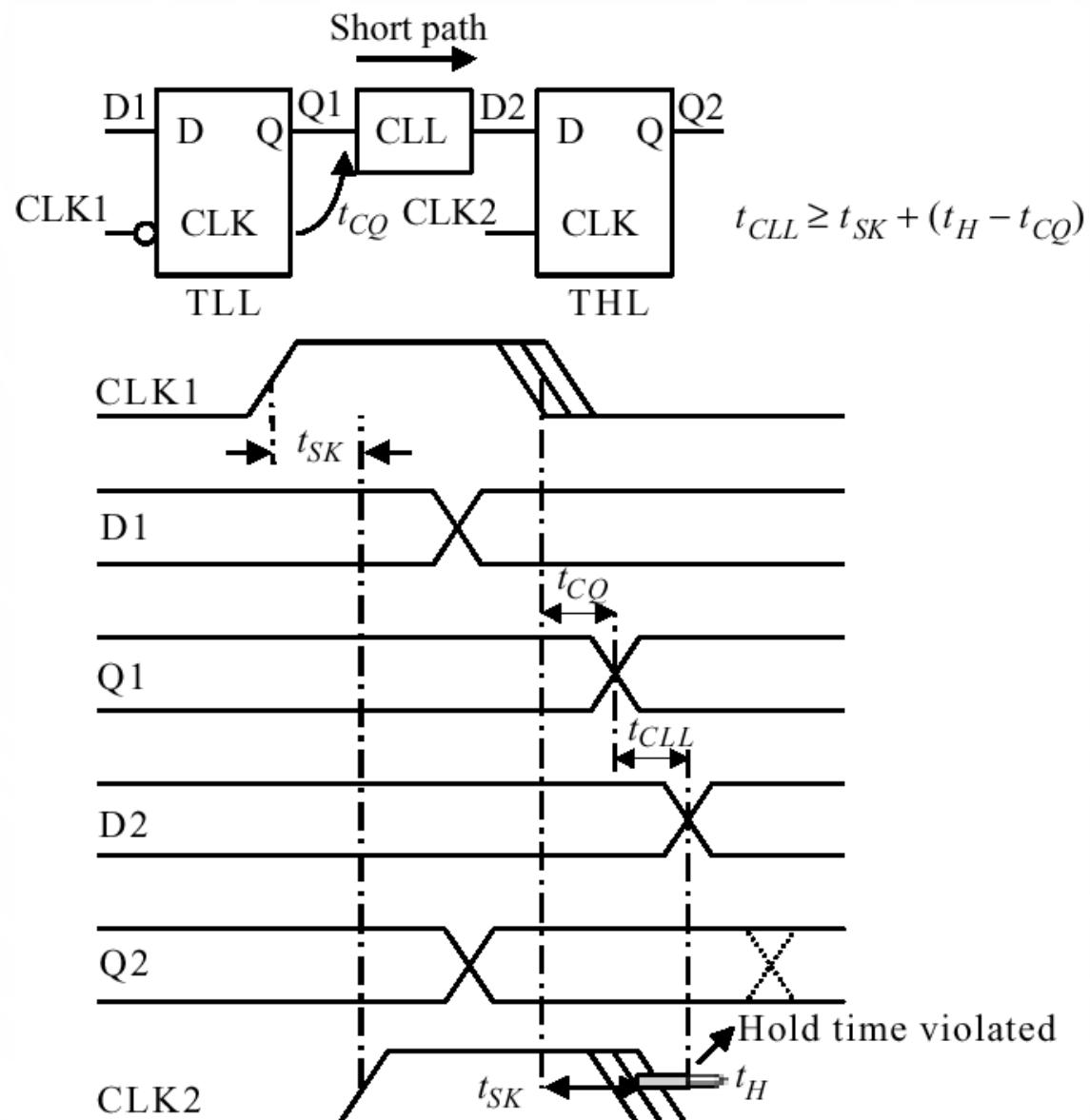
Latch-Based Timing

- Single-phase, two-latch



As long as transitions are within the assertion period of the latch, no impact of position of clock edges

Latch Design and Hold Times

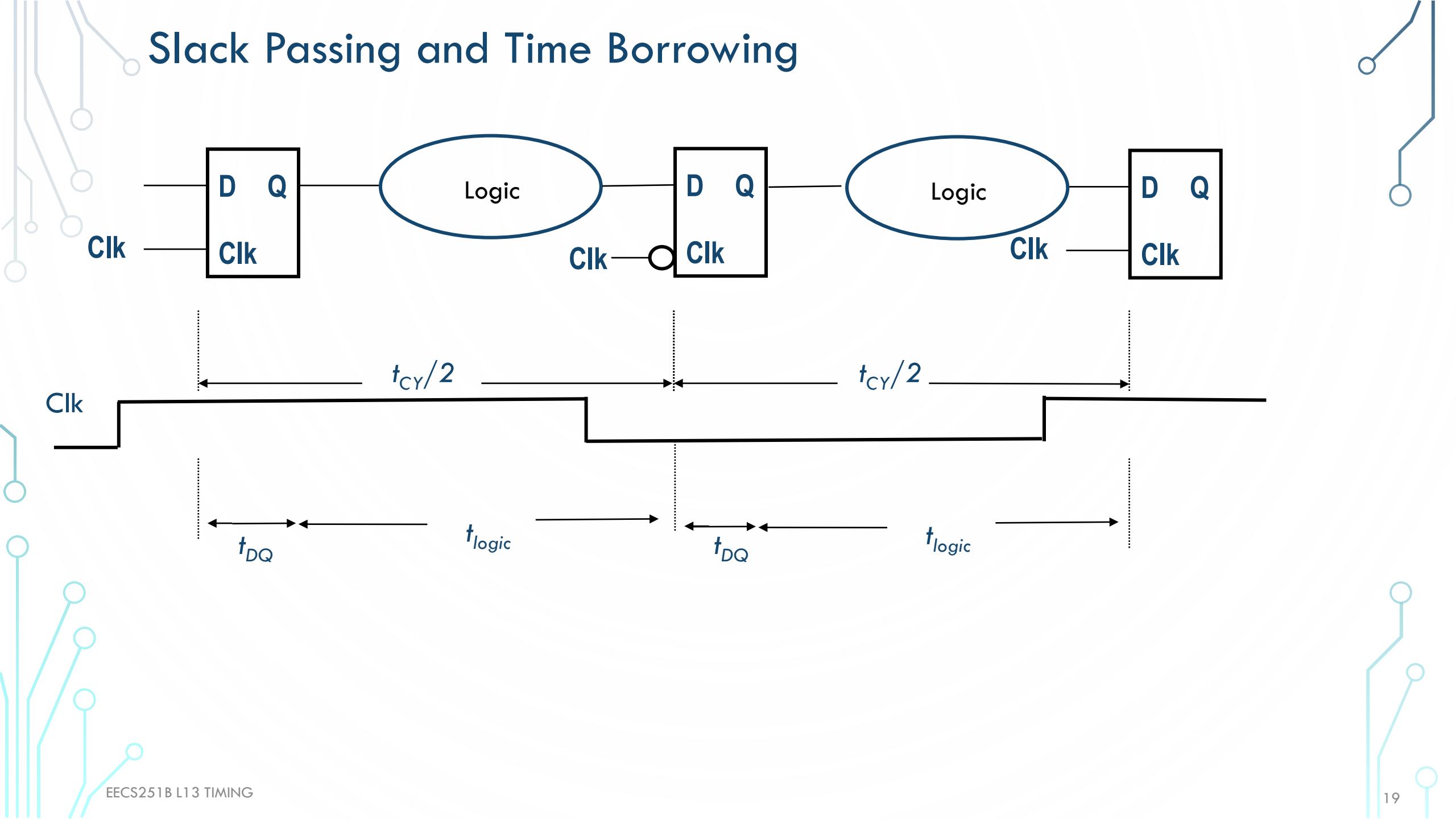


Soft-Edge Properties of Latches

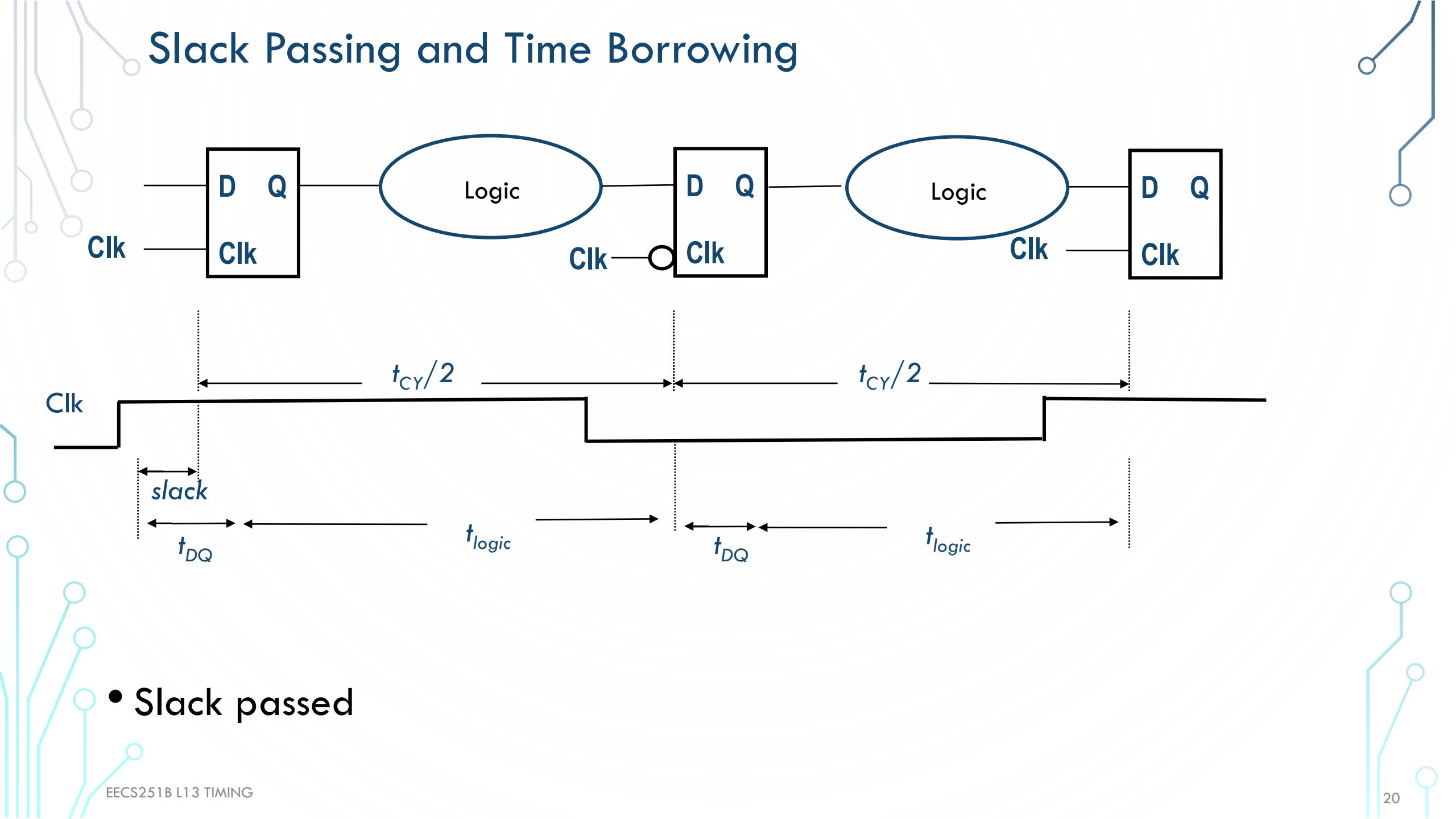
- **Slack passing** – logical partition uses left over time (slack) from the *previous partition*
- **Time borrowing** – logical partition utilizes a portion of time allotted to the *next partition*
- Makes most impact in unbalanced pipelines

Bernstein et al, Chapter 8, Chandrakasan, Chap 11 (by Partovi)

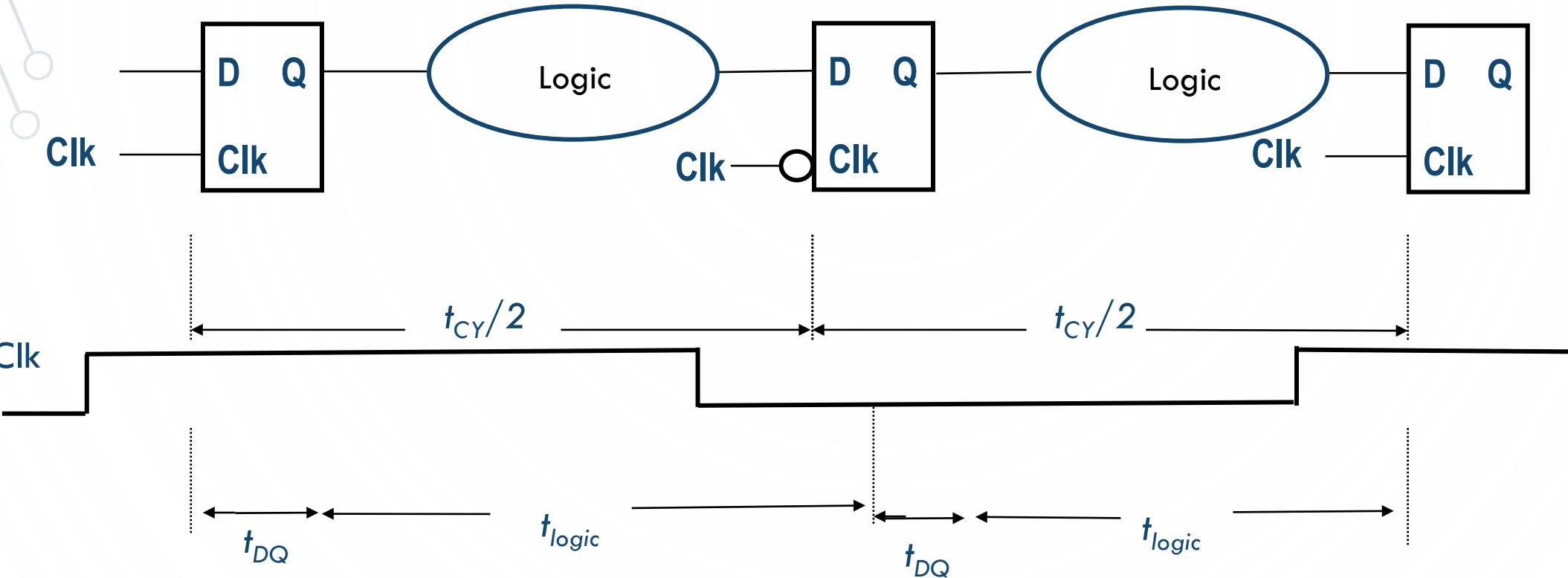
Slack Passing and Time Borrowing



Slack Passing and Time Borrowing

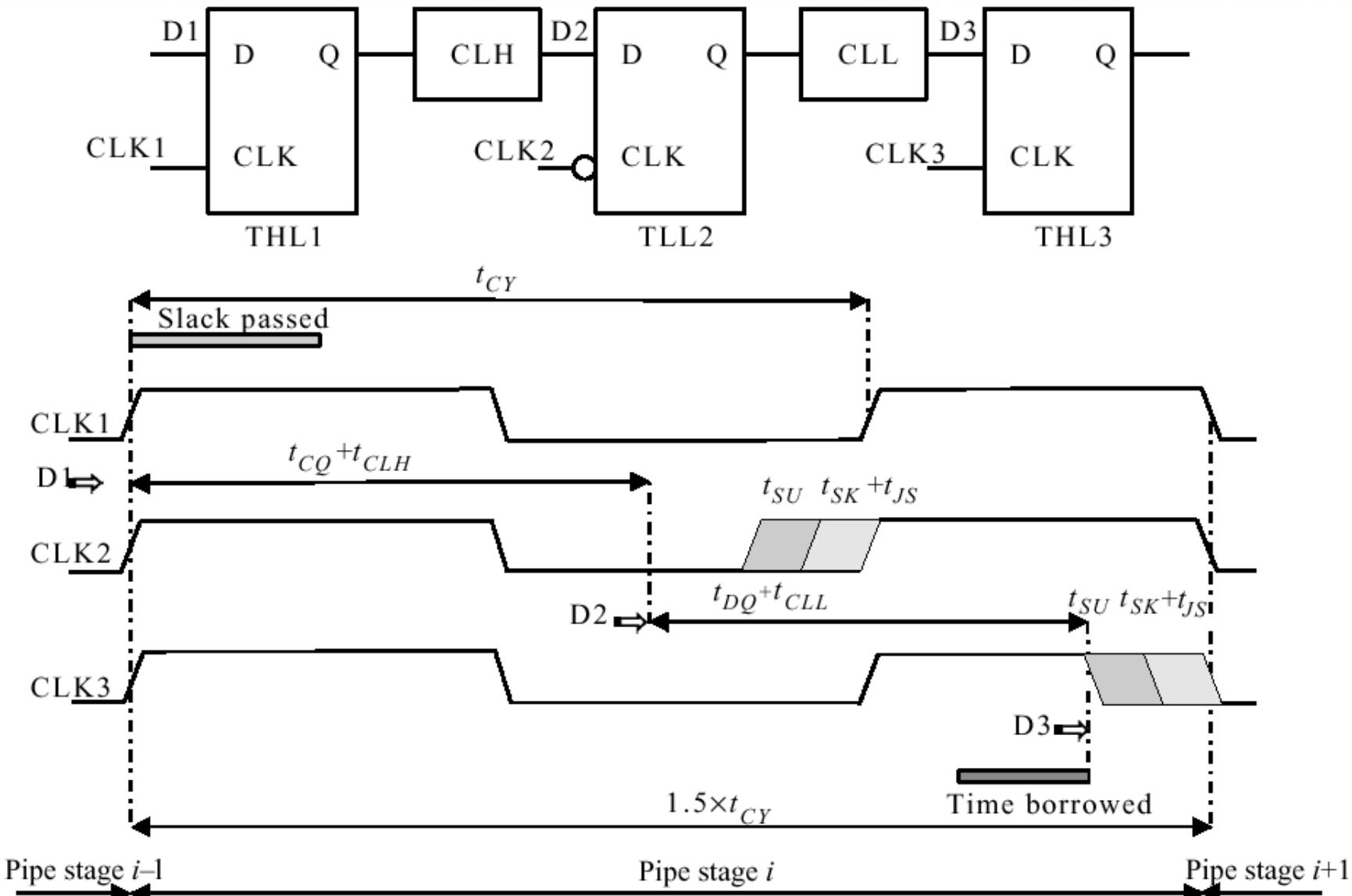


Slack Passing and Time Borrowing



• Time borrowed

Slack-Passing and Cycle Borrowing



For N stage pipeline, overall logic delay should be $< N \cdot T_{Cl}$

Announcements

- Assignment #1 due tomorrow
 - Quiz 1 next Tuesday, in lecture
- Lab 5 due next week

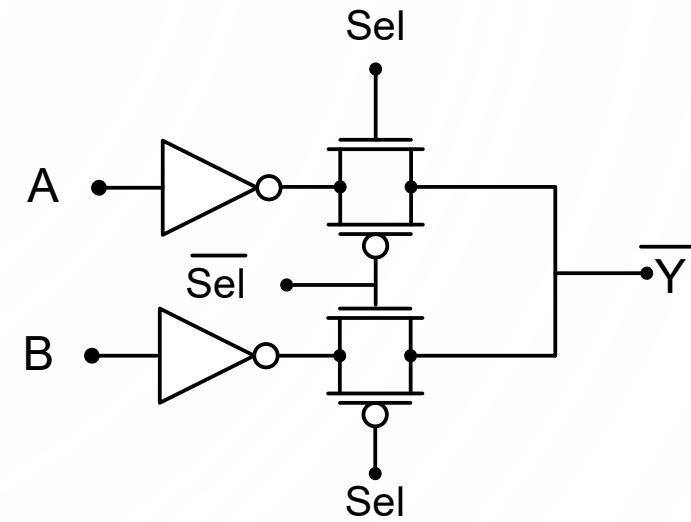
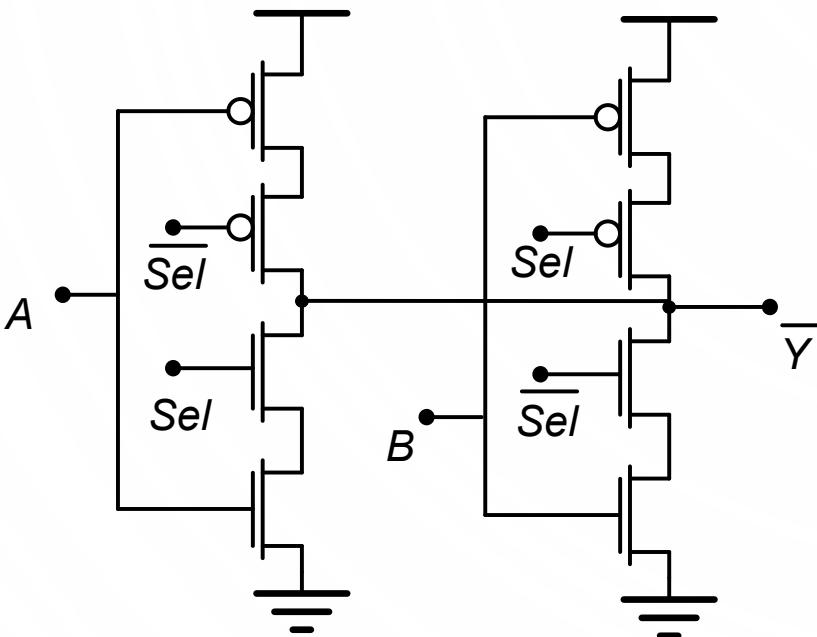
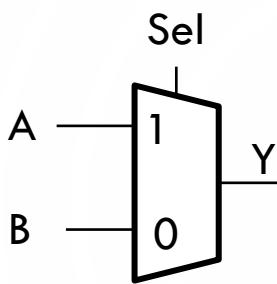


Design for Performance

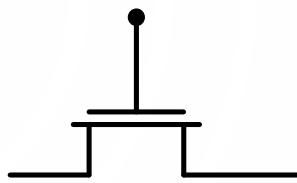
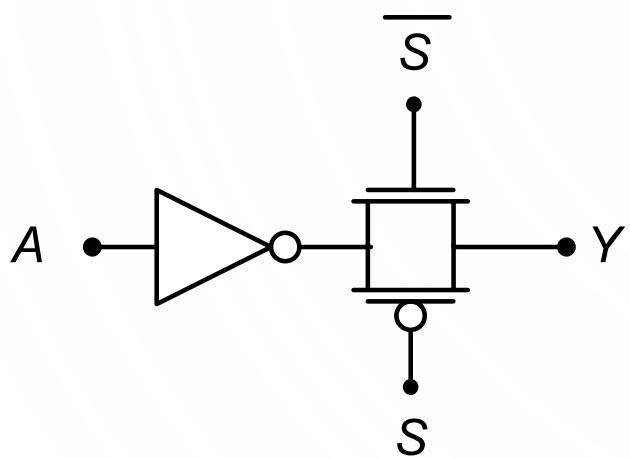
Latch Design

Review: MUX

- 2-input MUX

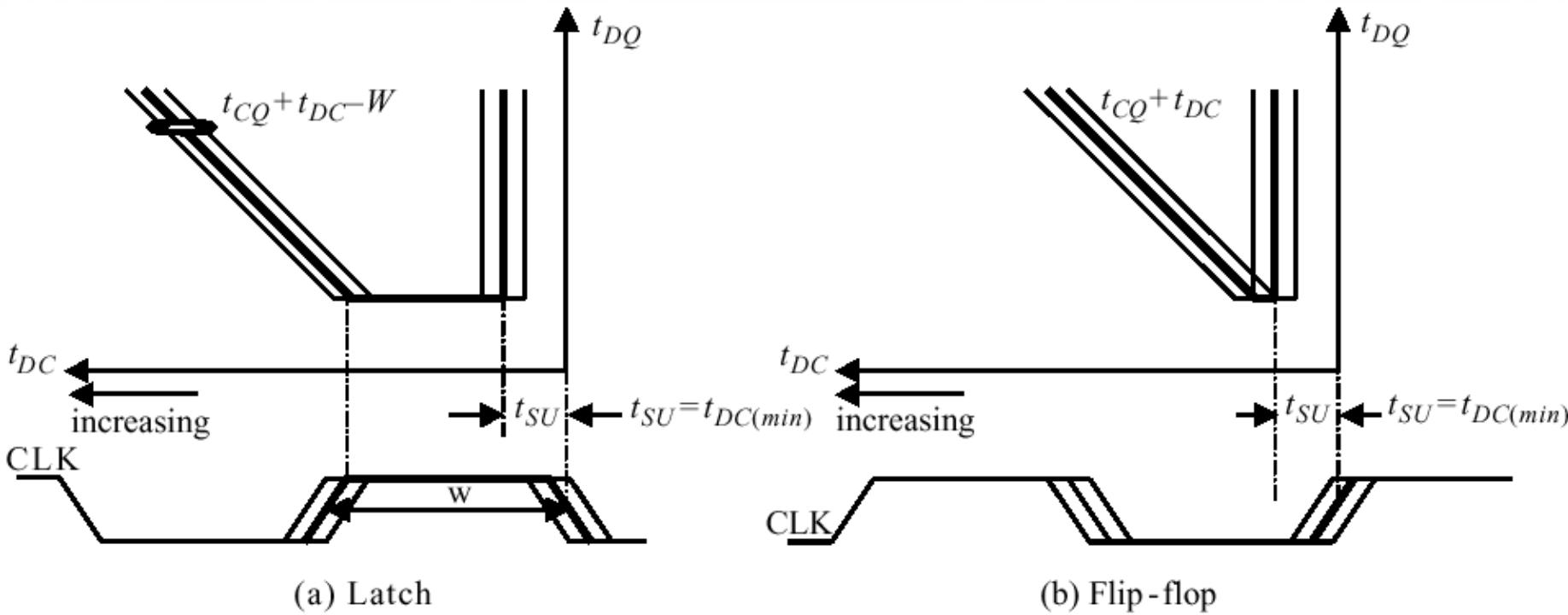


Review: Transmission Gates



Generating Complementary Clocks

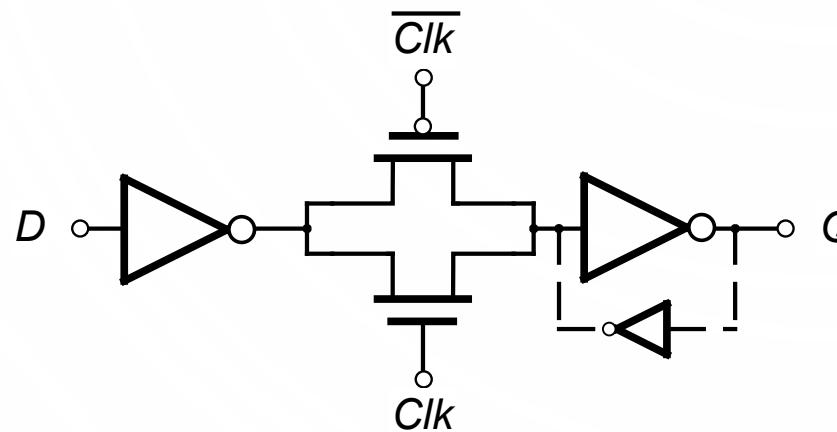
Latch vs. Flip-Flop



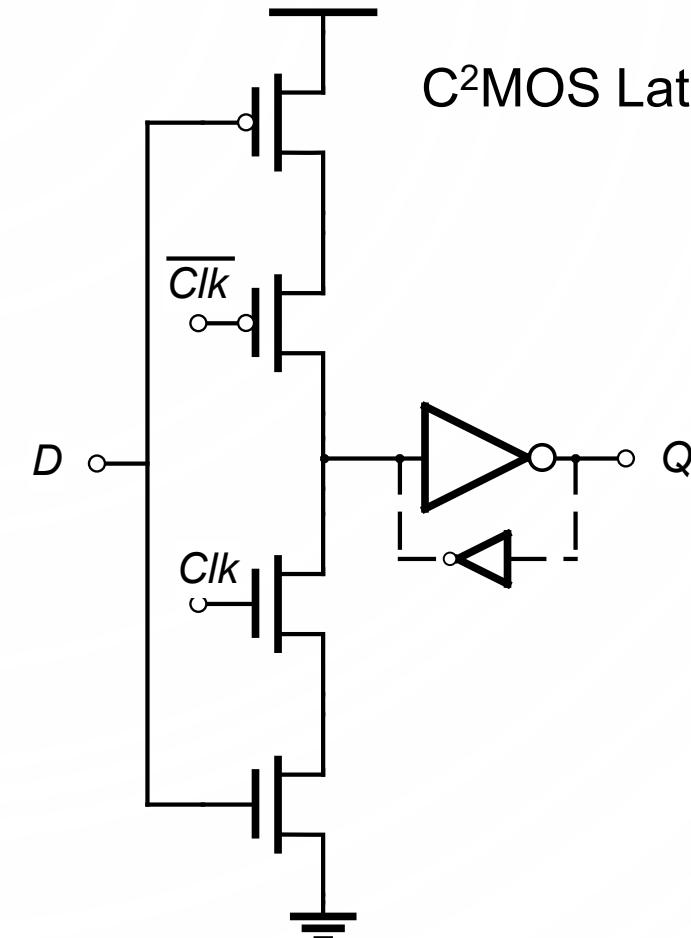
Courtesy of IEEE Press, New York. © 2000

Latches

Transmission-Gate Latch

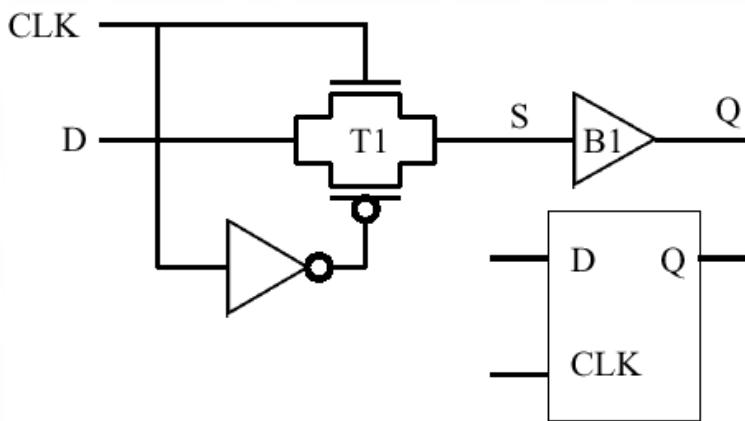


C²MOS Latch

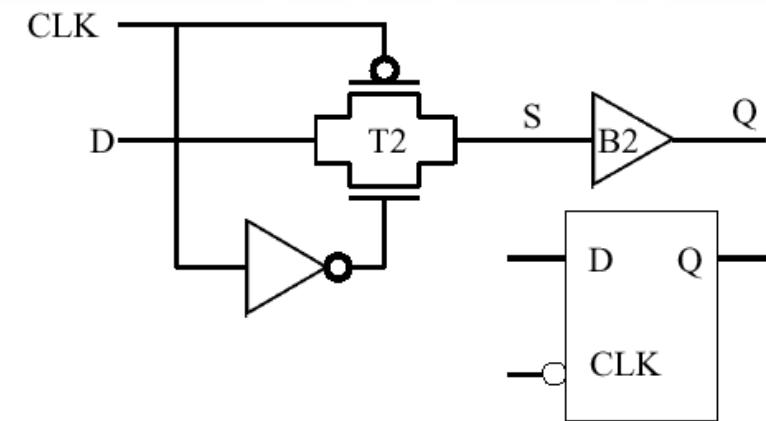


Usually without contention

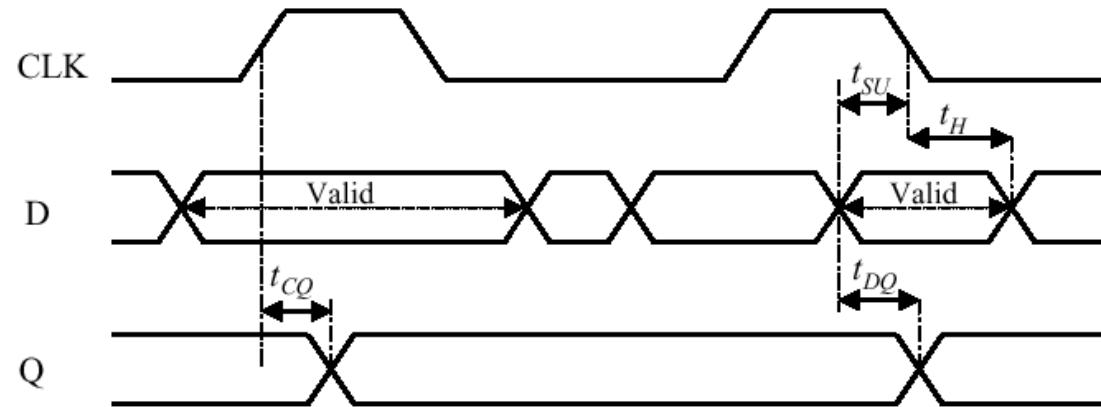
Latches



(a) The transparent high latch (THL)

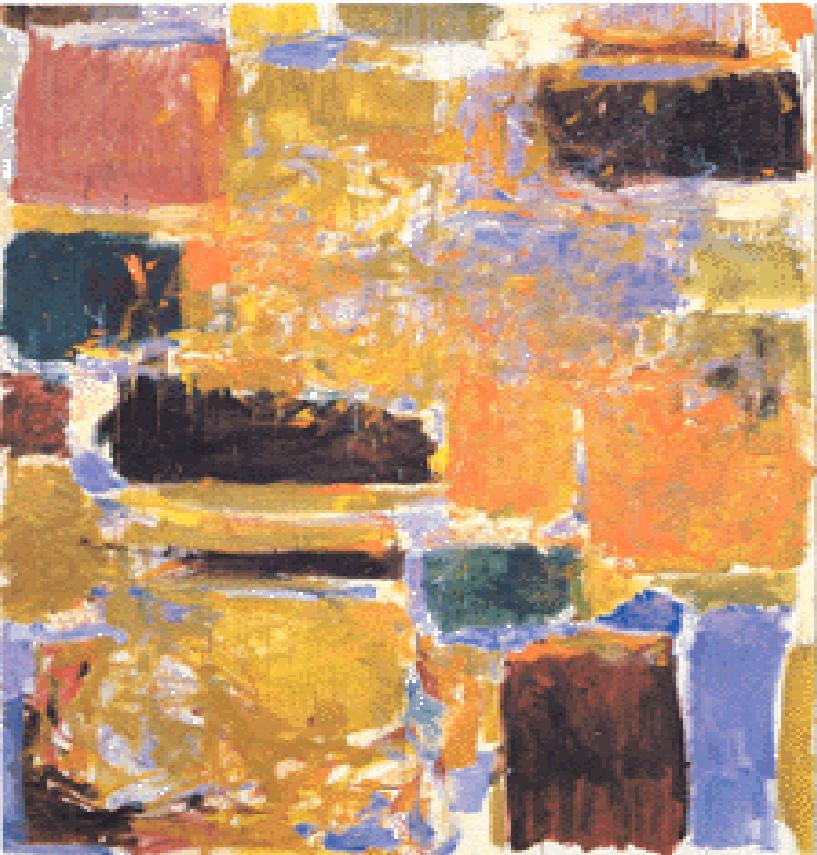


(b) The transparent low latch (TLL)



(c) Timing waveforms for the THL

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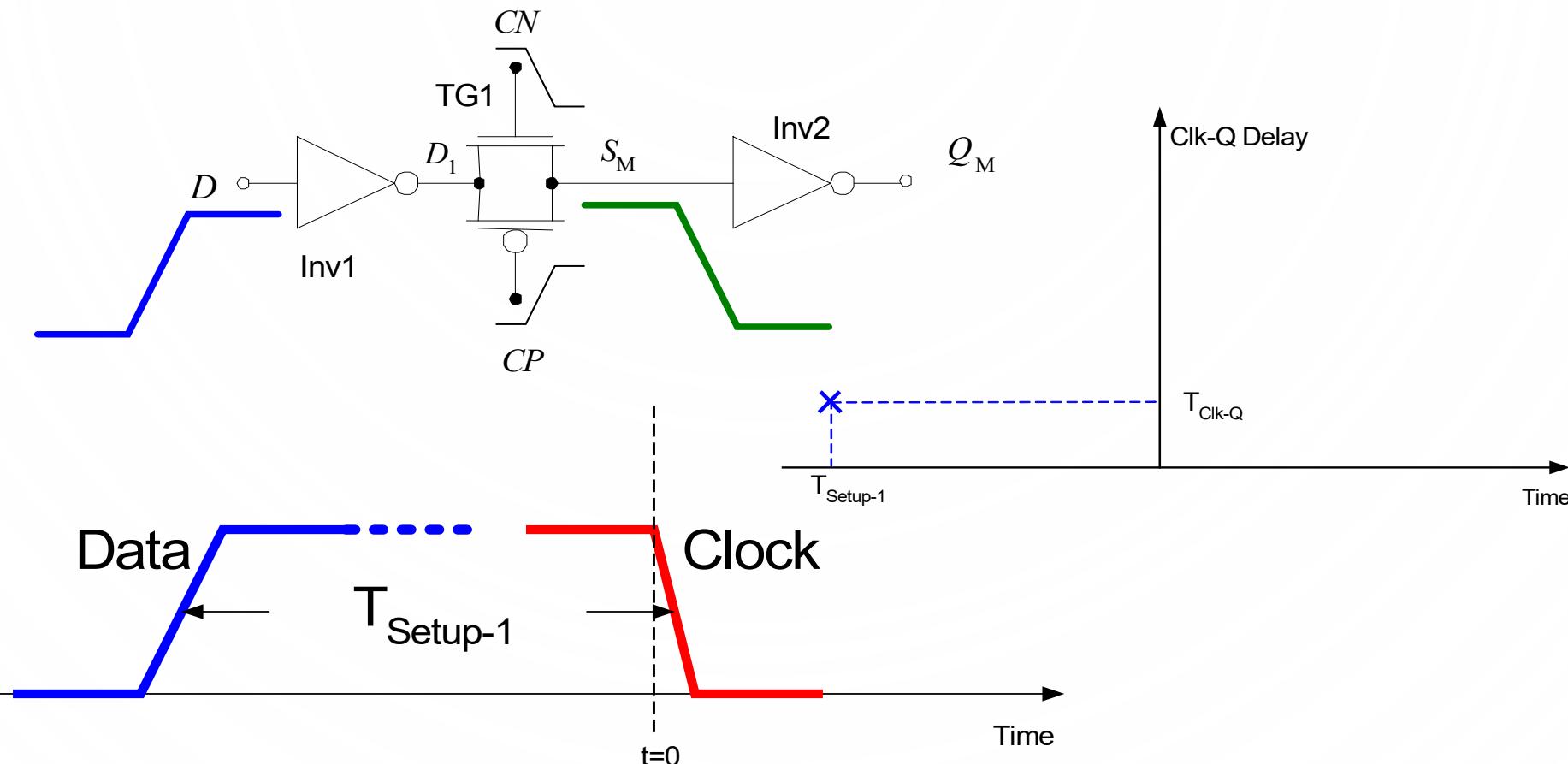


Design for Performance

Delay, Setup, Hold

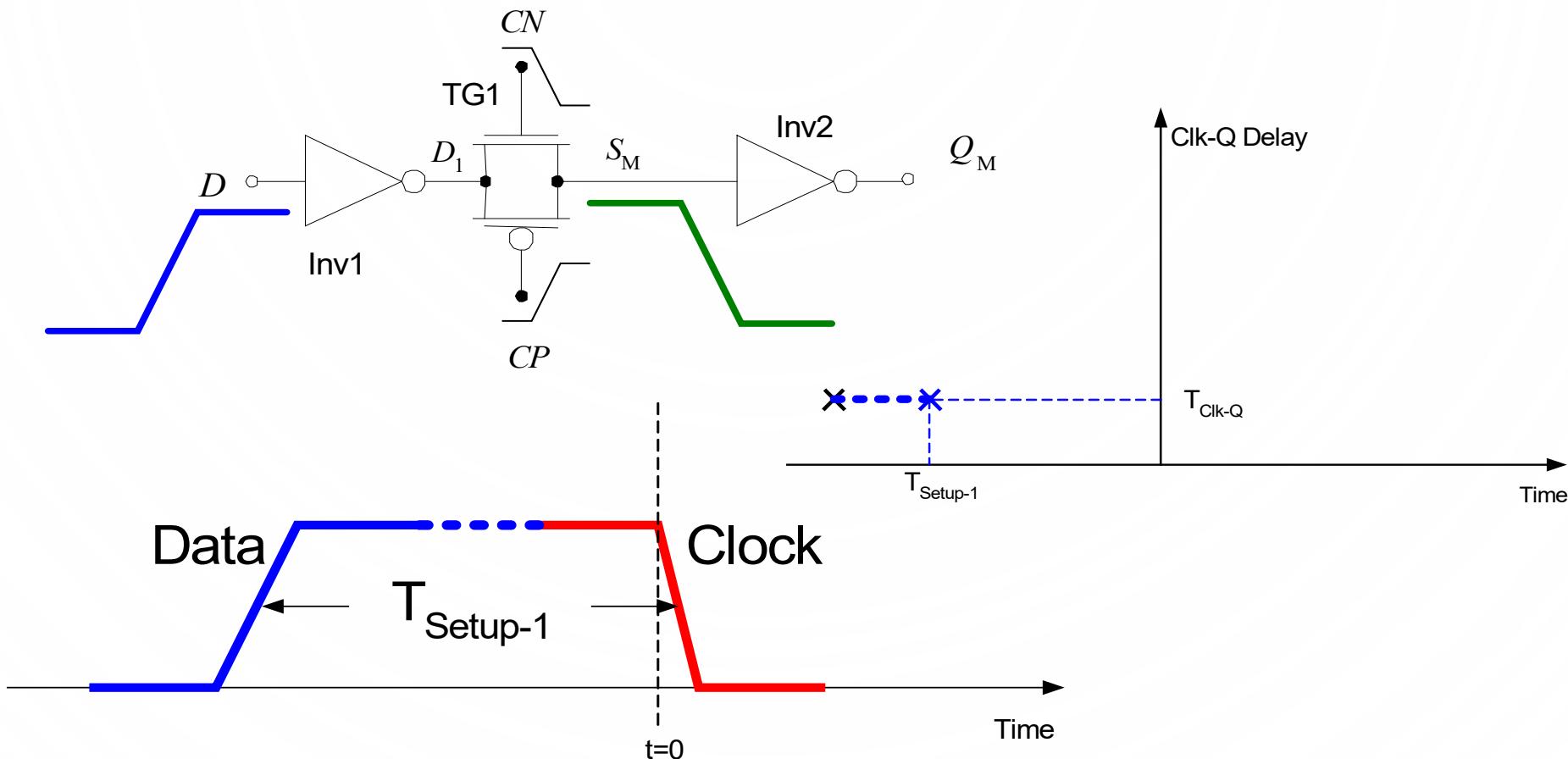
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



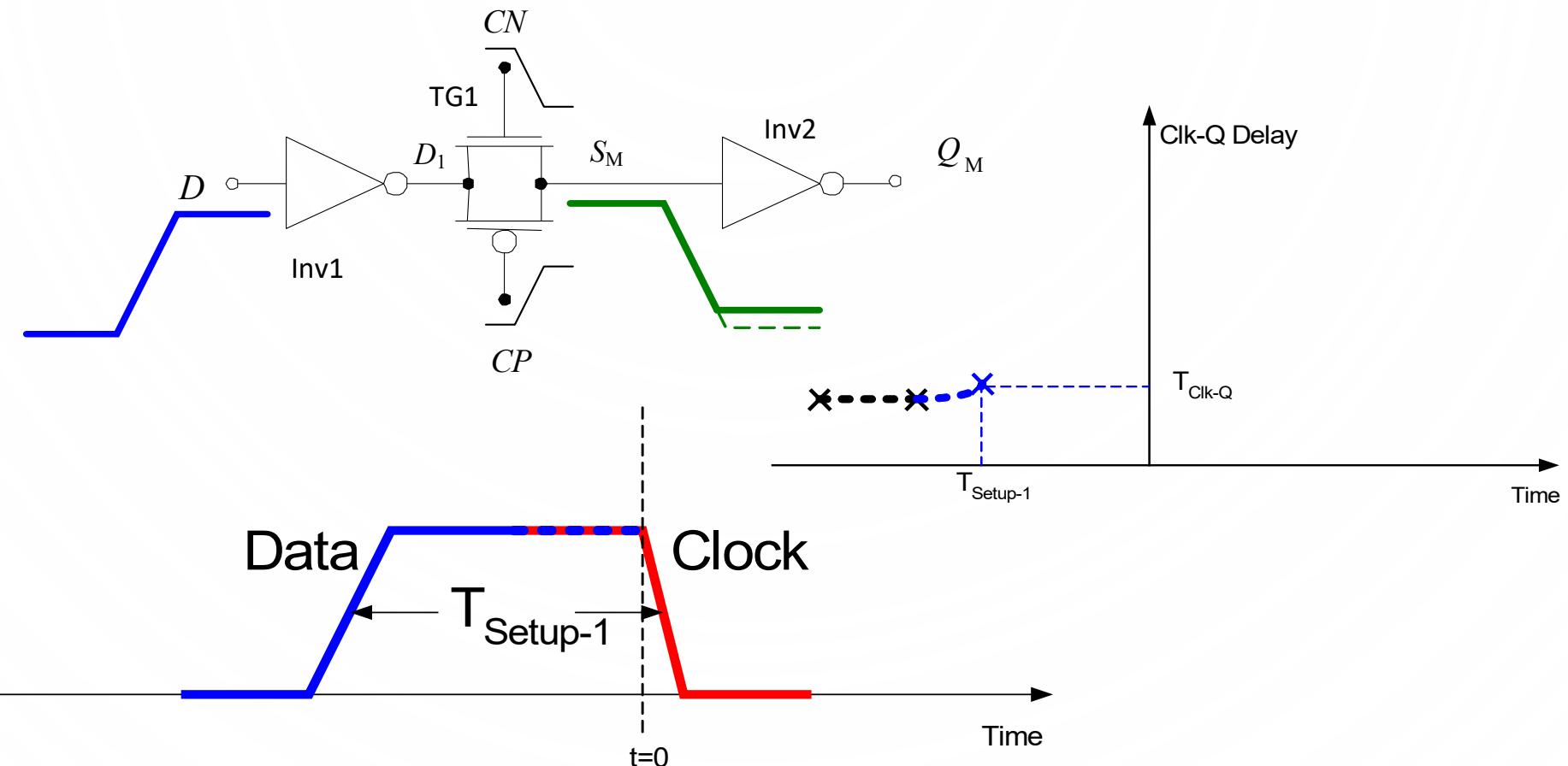
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



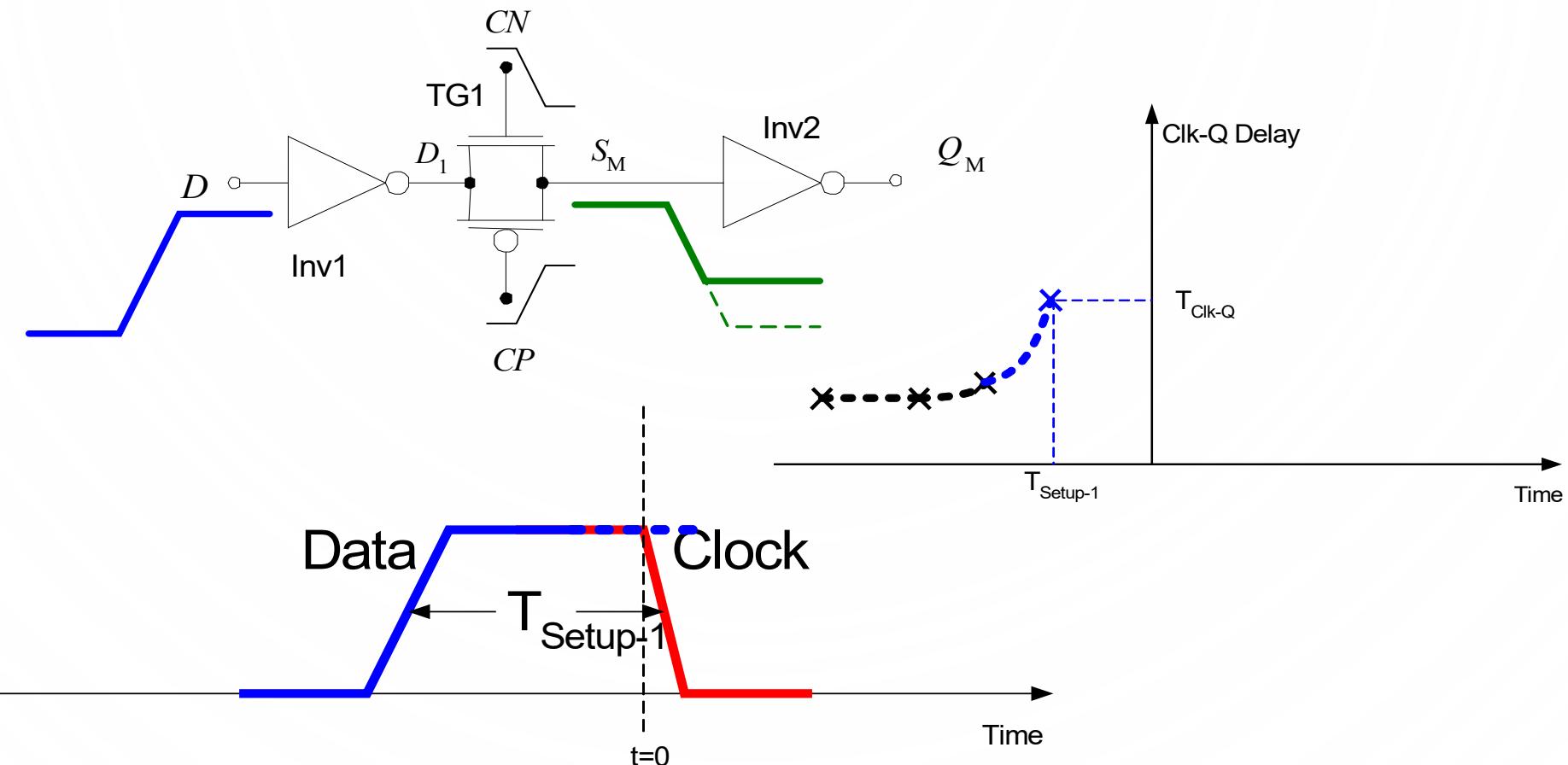
Setup-Hold Time Illustrations

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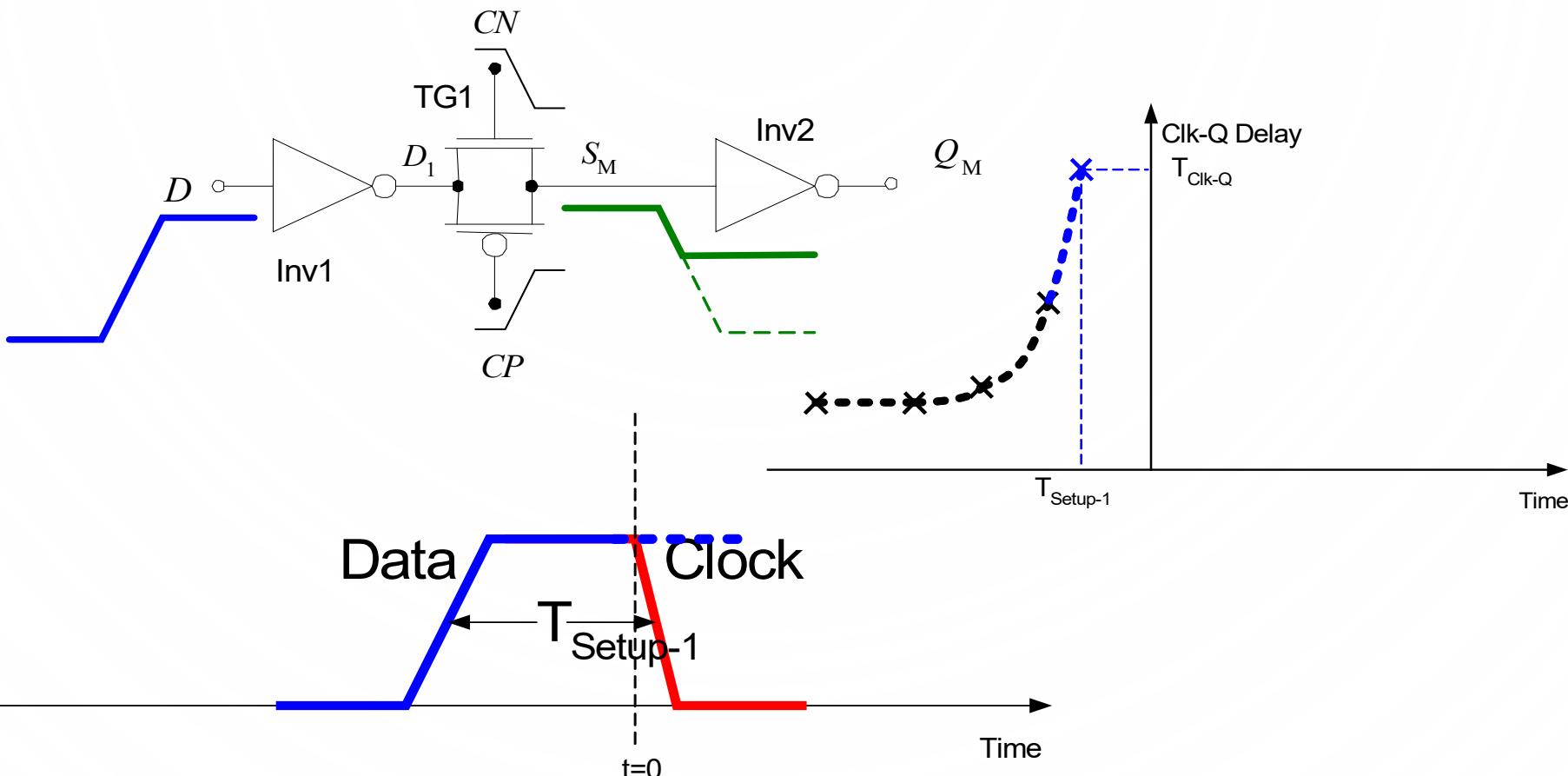
Setup-Hold Time Illustrations

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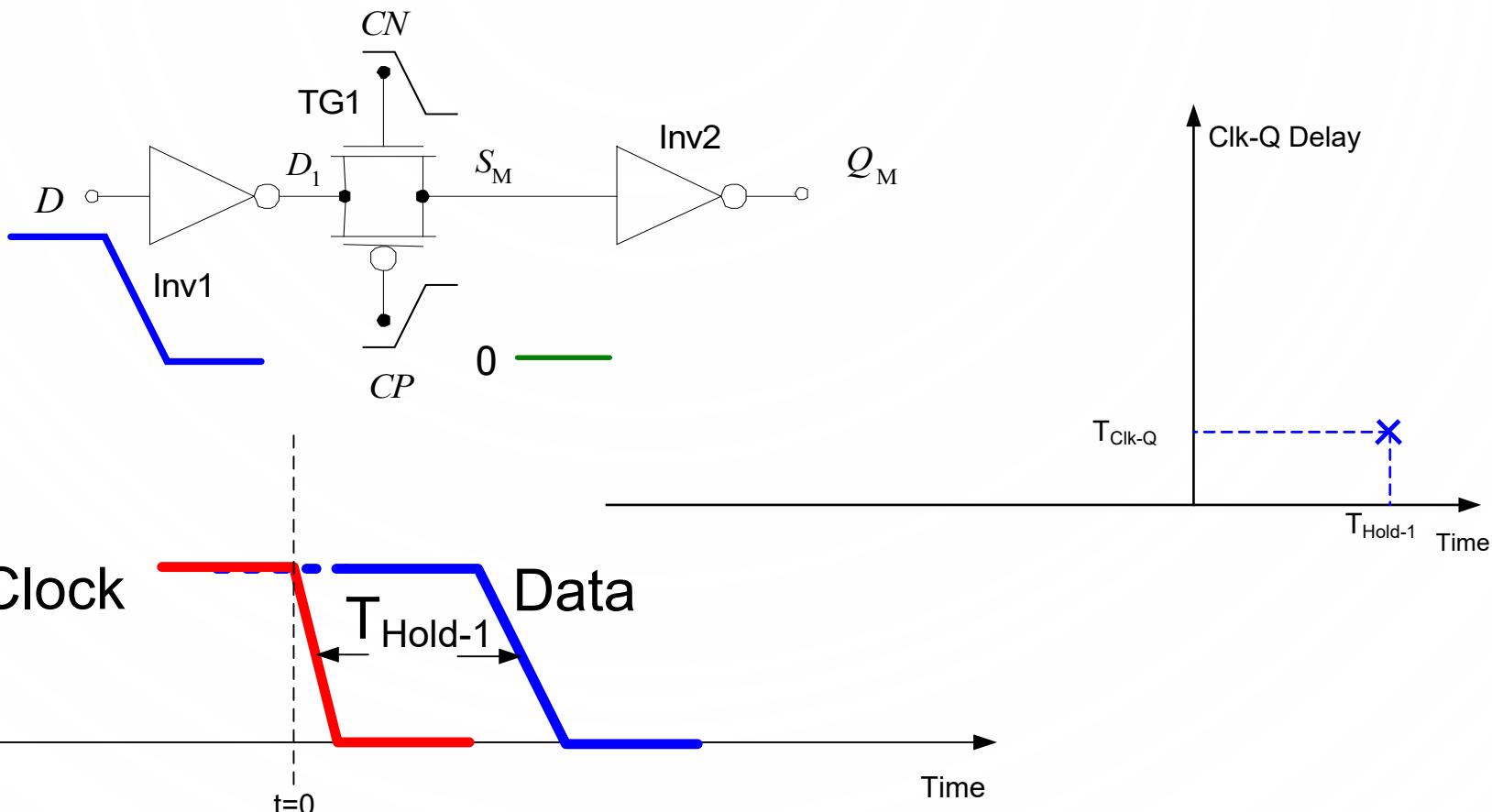
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



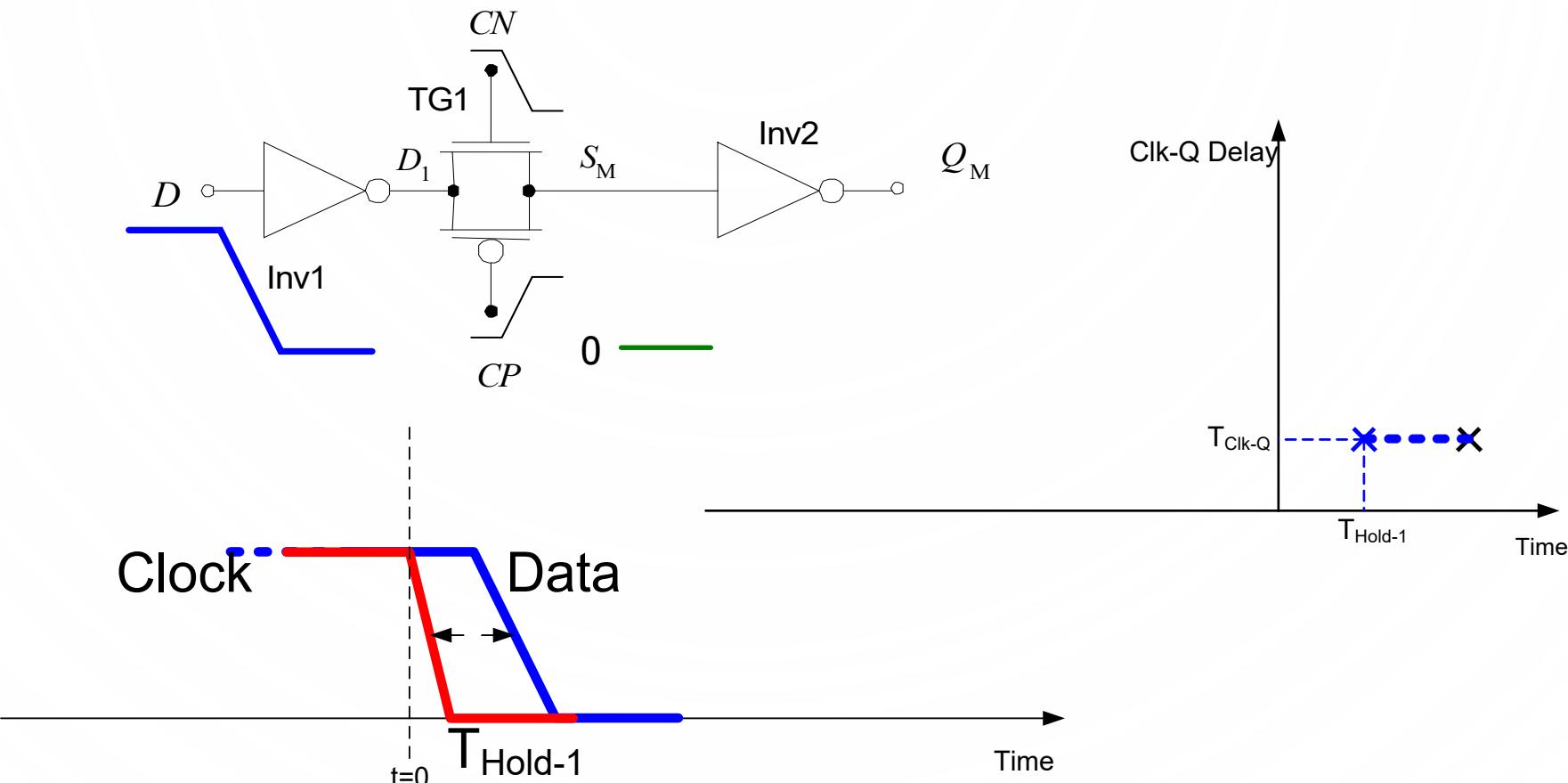
Setup-Hold Time Illustrations

Hold-1 case



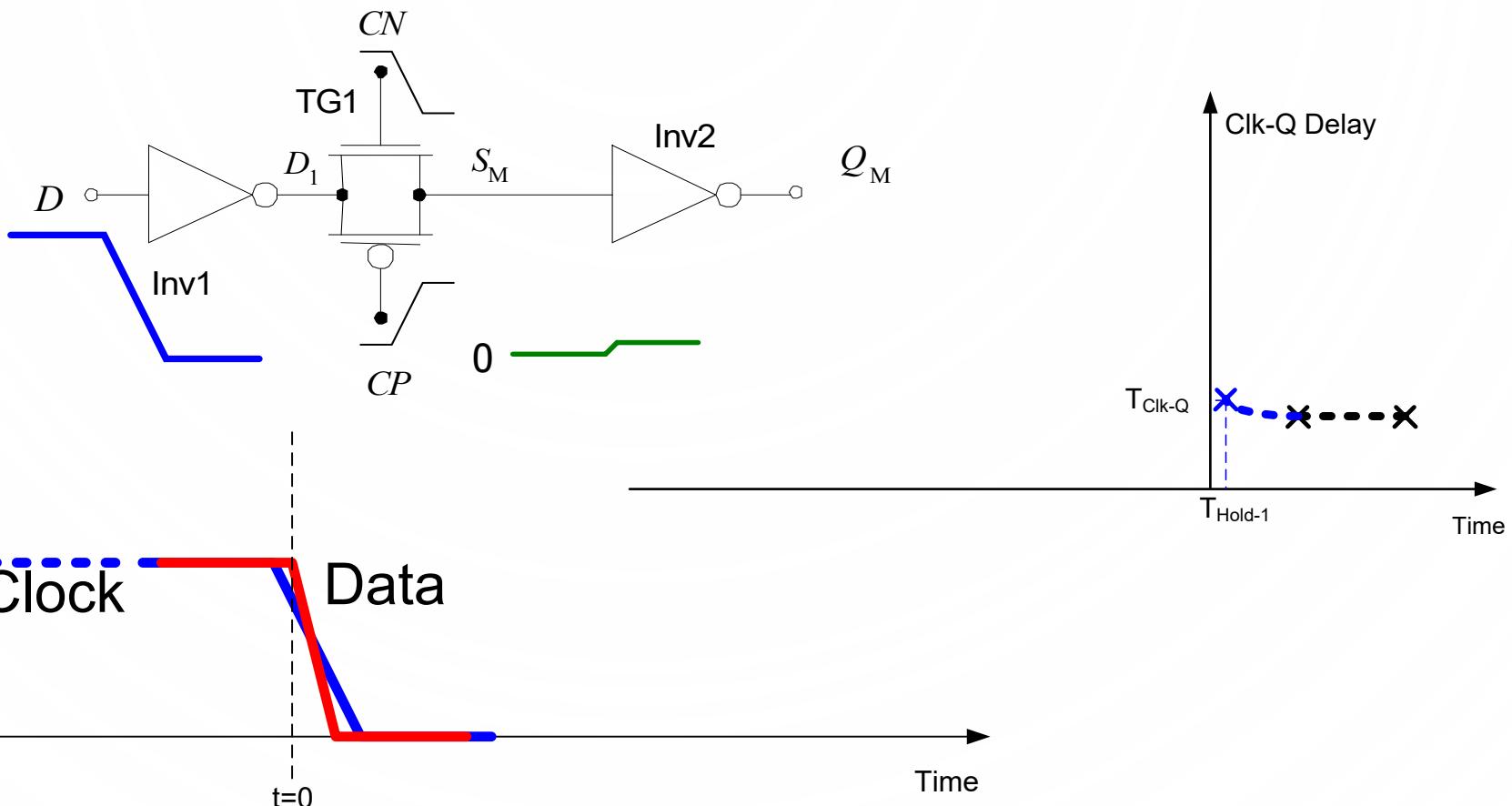
Setup-Hold Time Illustrations

Hold-1 case



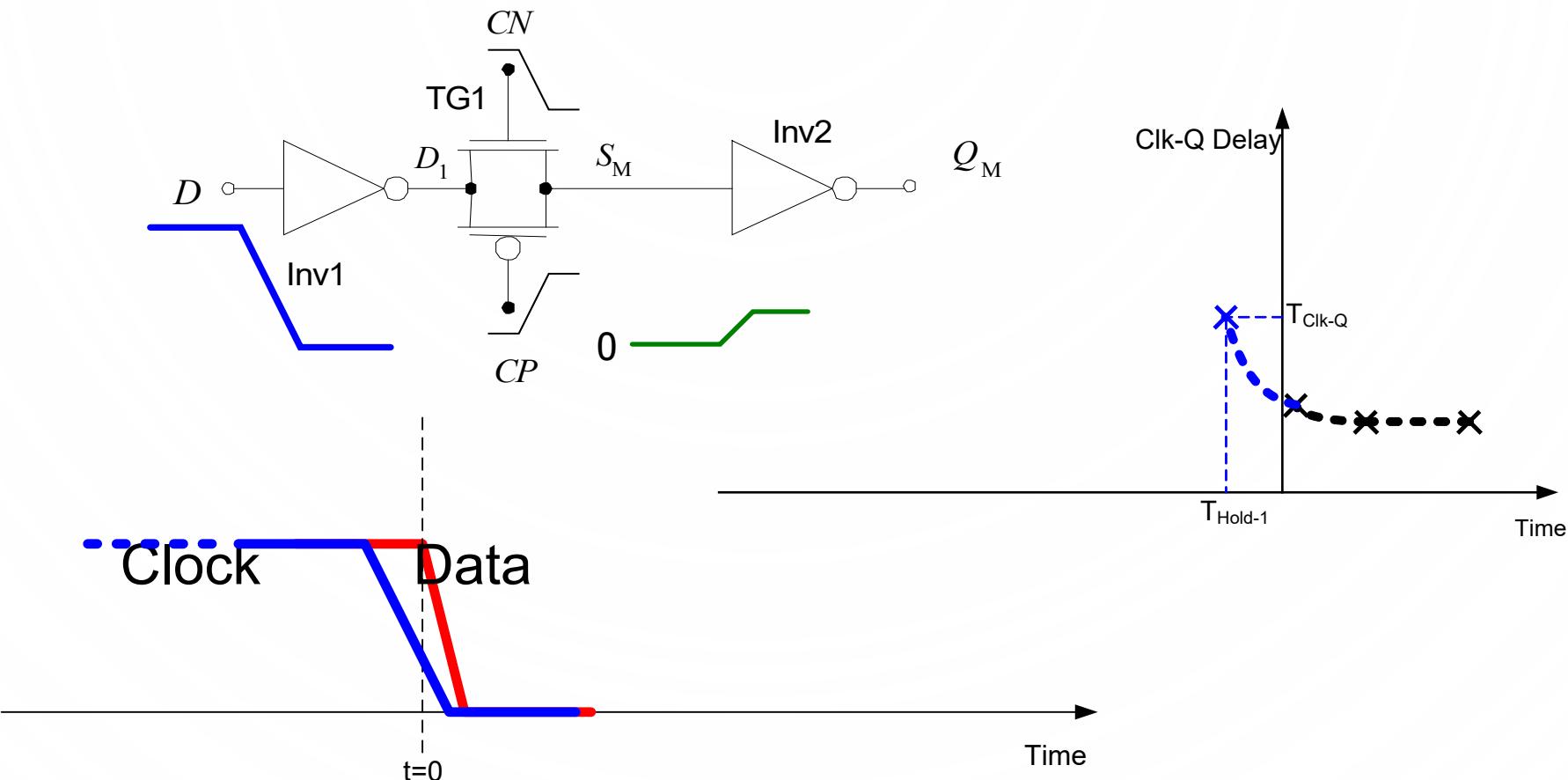
Setup-Hold Time Illustrations

Hold-1 case



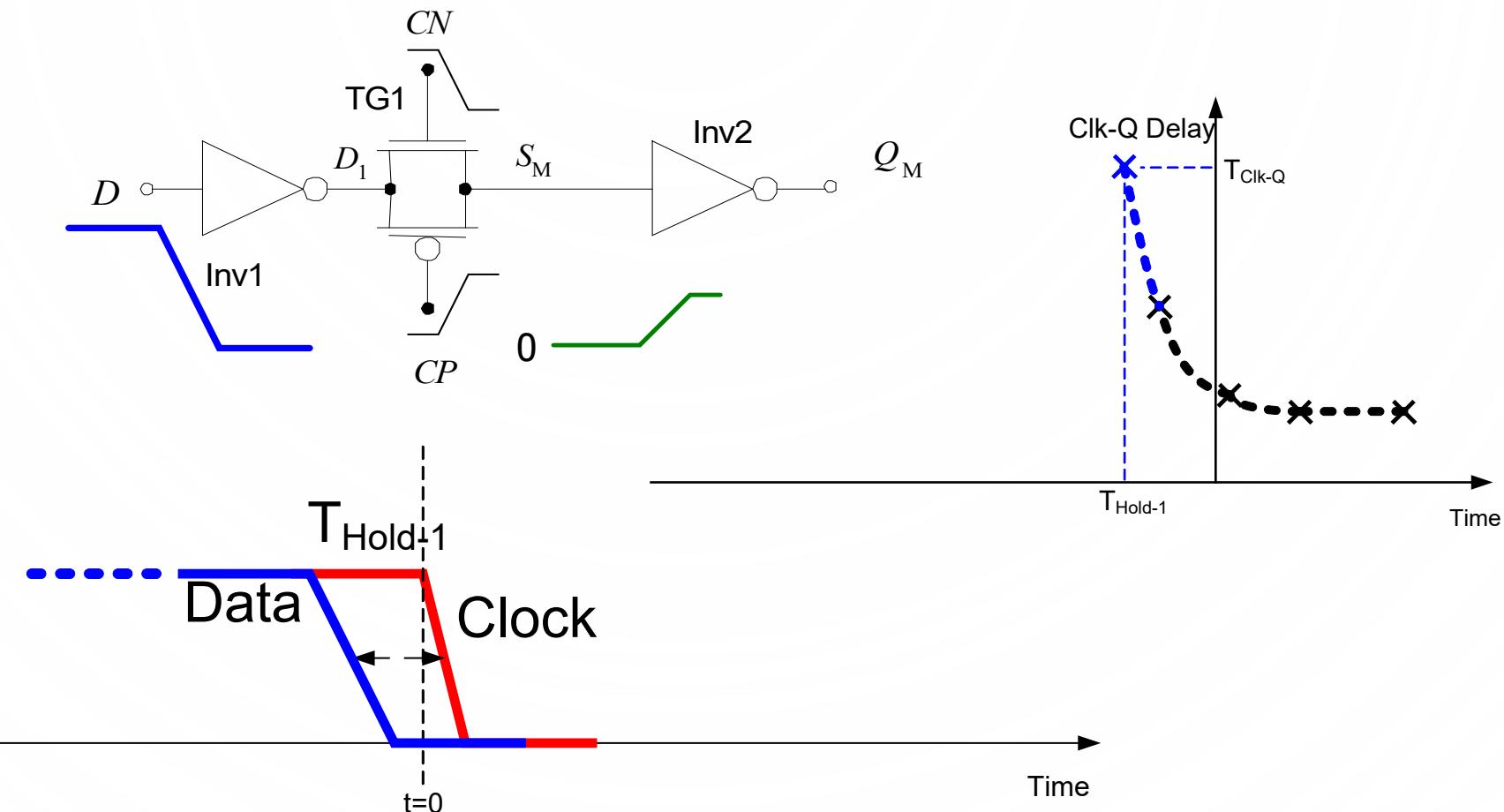
Setup-Hold Time Illustrations

Hold-1 case

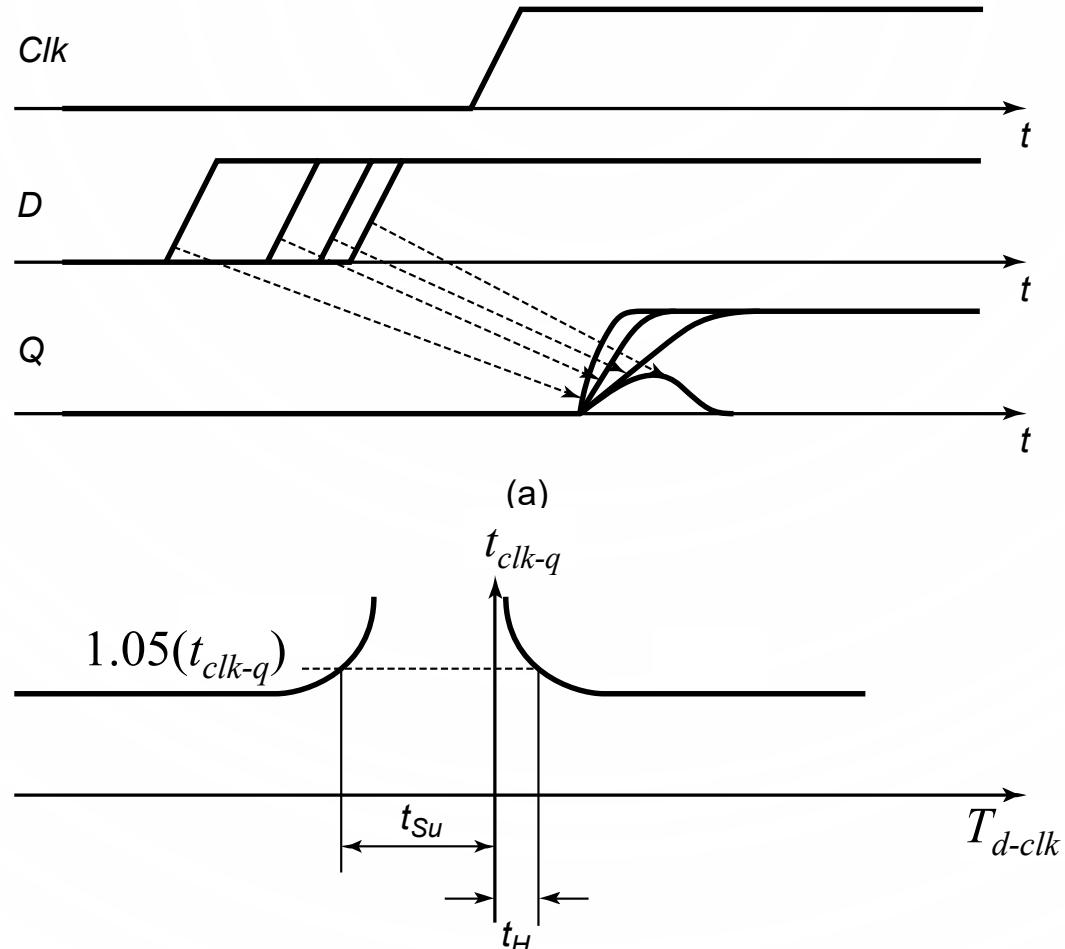


Setup-Hold Time Illustrations

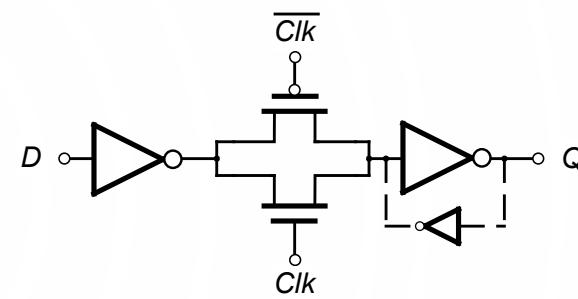
Hold-1 case

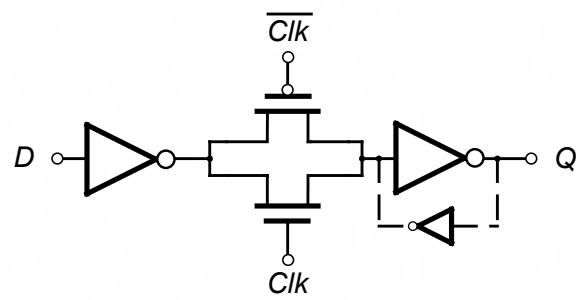


More Precise Setup Time



Latch t_{D-Q} and t_{Clk-Q}





Summary

- Flip-flop-based (edge-triggered) timing dominates today
- Latch-based timing can increase performance, but needs extra care
- There is also asynchronous design
- Logical effort can be used to analyze latch timing

Next Lecture

- Flip-flops
- Variability