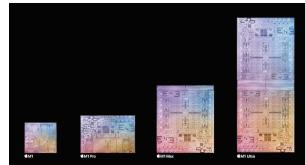


EECS251B : Advanced Digital Circuits and Systems



Borivoje Nikolić, Vladimir Stojanović, Sophia Shao

Apple Announces M1Ultra
March 8, 2022, AnandTech

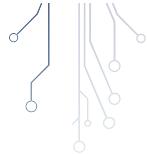
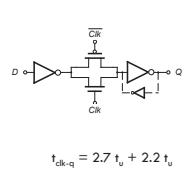


Recap

- Logical effort can be used to analyze latch timing
 - Clk-Q, D-Q delays are $\sim 1\text{FO4}$ delay (with F=1)

EECS251B L15 VARIABILITY

Berkeley EECS251B L15 VARIABILITY

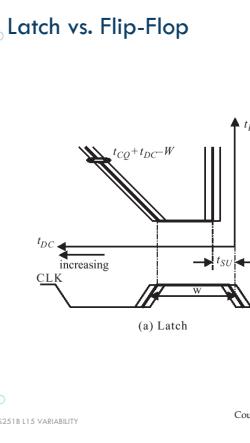


Flip-Flops



Key Point

- Two ways to design a flip-flop
 - Latch pair (large majority)
 - Pulsed latch



Courtesy of IEEE Press, New York, © 2000

Flip-Flops

- Performance metrics
- Delay metrics
 - Insertion delay
 - Inherent race immunity
 - 'Softness' (Clock skew absorption)
 - Inclusion of logic
 - Small (+constant) clock load
- Power/Energy Metrics
 - Power/energy
- Design robustness
 - Noise immunity

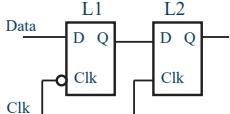


Scan Test

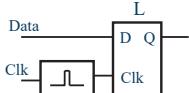


Types of Flip-Flops

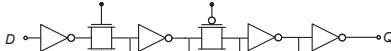
Latch Pair



Pulse-Triggered Latch



Flip-Flop (Latch Pair) Clk-Q, setup, hold



Flip-Flop Timing Characterization

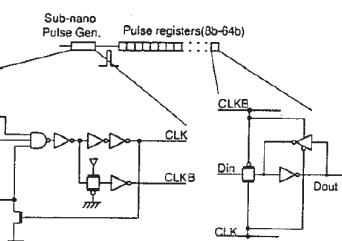
- Combinational logic delay is a function of output load and input slope
- Sequential timing (flip-flop):
 - t_{clk-q} is function of output load and clock rise time
 - $t_{S\&H}$, t_H are functions of D and Clk rise/fall times

Pulse-Triggered Latches

- First stage is a pulse generator
 - generates a pulse (glitch) on a rising edge of the clock
- Second stage is a latch
 - captures the pulse generated in the first stage
- Pulse generation results in a negative setup time
- Frequently exhibit a soft edge property
- Note: power is always consumed in the pulse generator
 - Often shared by a group (register)

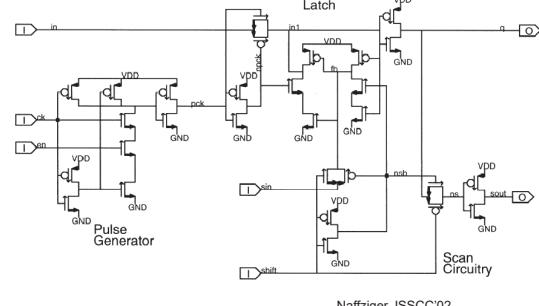
Pulsed Latch

Simple pulsed latch



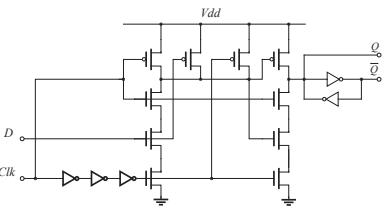
Kozu, ISSCC'96

Intel/HP Itanium 2



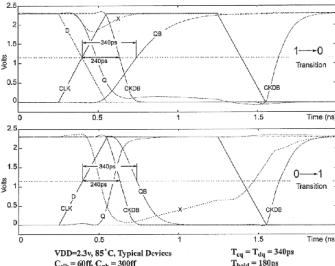
Pulsed Latches

Hybrid Latch Flip-Flop, AMD K-6
Partovi, ISSCC'96

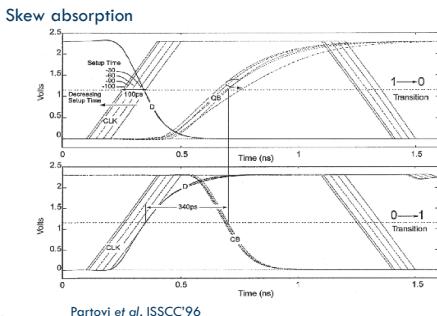


HLFF Operation

1-0 and 0-1 transitions at the input with 0ps setup time

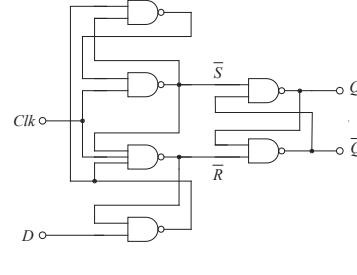


Hybrid Latch Flip-Flop



Pulsed Latches

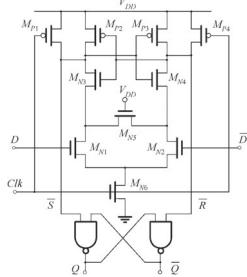
7474, from mid-1960's



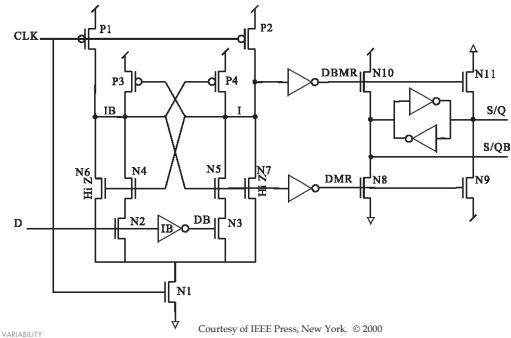
Pulsed Latches

Sense-amplifier-based flip-flop, Matsui 1992.
DEC Alpha 21264, StrongARM 110

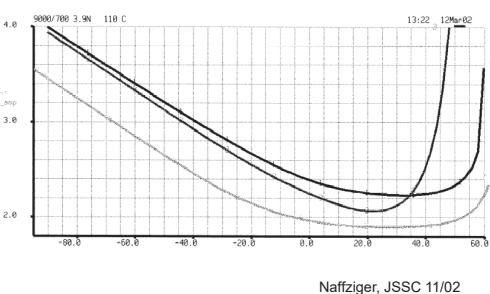
First stage is a sense amplifier, precharged to high, when $\text{Clk} = 0$.
After rising edge of the clock sense amplifier generates the pulse on S or R.
The pulse is captured in S-R latch.
Cross-coupled NAND has different propagation delays of rising and falling edges.



Sense Amplifier-Based Flip-Flop



Sampling Window Comparison



Announcements

- Lab 5 due this week
- Midterm reports due next week
 - 4 pages, conference format
- Assignment 2 posted this week

Variability Classification

- Nature of process variability
 - Within-die (WID), Die-to-die (D2D), Wafer-to-wafer (W2W), Lot-to-lot (L2L)
 - Systematic vs. random
 - Correlated vs. non-correlated
- Spatial variability/correlation
 - Device parameters (CD , t_{ox} , ...)
 - Supply voltage, temperature
- Temporal variability/correlation
 - Within-node scaling, Electromigration, Hot-electron effect, NBTI, self-heating, temperature, SOI history effect, supply voltage, crosstalk [Bernstein, IBM J. R&D, July/Sept 2006]
- Known vs. unknown
 - Goal of model-to-hw correlation is to reduce the unknowns

Design Variability Sources and Impact on Design



17

18

19

20

21

22

23

24

Sources of Variability

Technology

- Front-end (Devices)
 - Systematic and random variations in I_{on} , I_{off} , C , ...
- Back-end (Interconnect)
 - Systematic and random variations in R , C

Environment

- Supply (IR drop, noise)
- Temperature

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Temporal Variability

Technology

- Tech. node scaling
- Within-node scaling

Environment

- Temperature
- Data stream
- Electromigration
- NBTI
- Hot carrier effect
- Tooling changes
- Coupling
- Charge

After Rohrer
ISSCC'06 tutorial

Lot-to-lot

Charge

Temporal range [s]

$10^{12} \rightarrow 10^9 \rightarrow 10^6 \rightarrow 10^3 \rightarrow 10^0 \rightarrow 10^{-3} \rightarrow 10^{-6} \rightarrow 10^{-9} \rightarrow 10^{-12}$

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Systematic and Random Device Variations

Parameter	Random	Systematic
Channel Dopant Concentration Nch	Affects σ_{V_T} ^[1]	Non uniformity in the process of dopant implantation, dosage, diffusion
Gate Oxide Thickness Tox	Si/SiO ₂ & SiO ₂ /Poly-Si interface roughness ^[2]	Non uniformity in the process of oxide growth
Threshold Voltage V_T (non Nch related)	Random anneal temperature and strain effects	Non-uniform annealing temperature ^[3] (metal coverage over gate) Biaxial strain
Mobility μ	Random strain distributions	Systematic variation of strain in the Si due to STI, Si/D area, contacts, gate density, etc
Gate Length L	Line edge roughness (LER) ^[3]	Lithography and etching: Proximity effects, orientation ^[4]
Fin geometry/film thickness variations	Rounding, etc, σ_{V_T} , mobility	Systematic fin thickness Systematic Si film/BOX variations

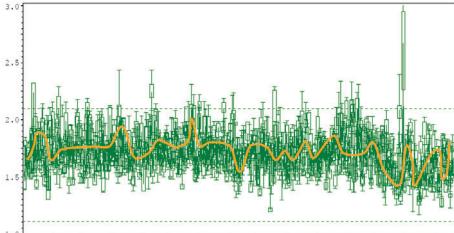
[1] P. Frank et al, VLSI Symposium, Jun. 1999. [2] A. Asenov et al, IEEE Trans on Electron Devices, Jan. 2002.

[3] P. Oldiges et al, SISPAD 2000, Sept. 2000. [4] M. Orshansky et al, IEEE Trans on CAD, May 2002. [5] Tuijnhout et al, IEDM, Dec 1996

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Systematic (?) Temporal Variability

Metal 3 resistance over 3 months



Spatial Variability

Global

Fab to fab

Deployed environment

Lot to lot

Across wafer

Across reticle

Across chip

Across block

Local

Temperature

Metal polishing

Transistor I_{on} , I_{off}

Line-edge roughness

Dopant fluctuation

Film thickness

EECS251B L15 VARIABILITY

After Rohrer
ISSCC'06 tutorial

$10^6 \rightarrow 10^3 \rightarrow 10^0 \rightarrow 10^{-3} \rightarrow 10^{-6} \rightarrow 10^{-9}$

Spatial range [m]

EECS251B L15 VARIABILITY

Systematic vs. Random Variations

Systematic

- A systematic pattern can be traced down to lot-to-lot, wafer-to-wafer, within reticle, within die, from layout to layout,...
- Within-die: usually spatially correlated

Random

- Random mismatch (dopant fluctuations, line edge roughness,...)
- Things that are systematic, but e.g. change with a very short time constant (for us to do anything about it). Or we don't understand it well enough to model it as systematic. Or we don't know it in advance ("How random is a coin toss?").

Unknown

EECS251B L15 VARIABILITY

Dealing with Systematic Variations

Model-to-hardware correlation classifies unknown sources

Systematic effect

Improve process

Limited options

Tighten a design rule

Density loss

Model/Design-in

Extraction/Compact modeling/Design techniques

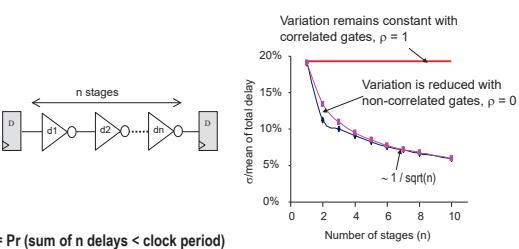
EECS251B L15 VARIABILITY

Impact of Correlations

EECS251B L15 VARIABILITY

EECS251B L15 VARIABILITY

Chip Yield Depends on Inter-Gate Correlation

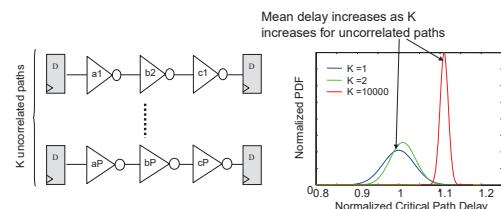


- Yield = $\Pr(\text{sum of } n \text{ delays} < \text{clock period})$
- $\rho = 0$ gives highest yield through averaging

Bowman et al, JSSC, Feb 2002.

EECS251B L15 VARIABILITY

Chip Yield Depends on Inter-Path Correlation



- Yield = $\Pr(\max \text{ delay of } K \text{ paths} < \text{clock period})$
- $K = 1$ gives highest yield

Correlated paths reduce impact of variation

Bowman et al, JSSC, Feb 2002.

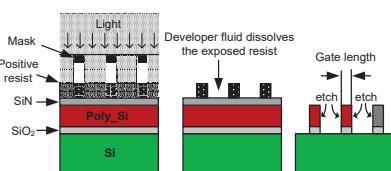
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Process Corners

EECS251B L15 VARIABILITY

Layout: Poly Proximity Effects

- Gate CD is a function of its neighborhood



Gate length depends on

- Light intensity profile falling on the resist
- Resist: application of developer fluid^[1], post exposure bake (PEB) temperature^[2]
- Dry etching: microscopic loading effects^[3]

[1] J.Colin, M.S. Thesis, UC Berkeley

[2] D. Steele et al, SPIE, vol.4689, July 2002.

[3] J.D. Plummer, M.D. Deal, P.B. Griffin, Silicon VLSI Technology, Prentice-Hall, 2000.

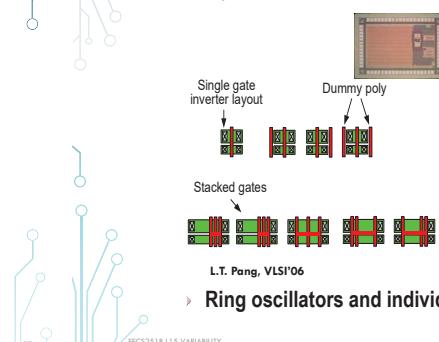
EECS251B L15 VARIABILITY

Design Variability Some Systematic Effects

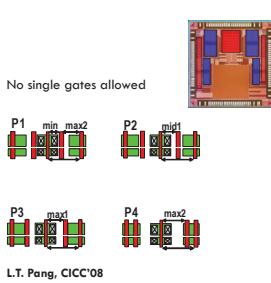


Layout: Proximity Test Structures

- 90nm experiments

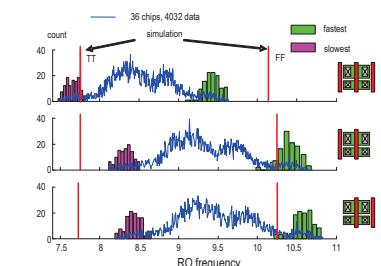


- 45nm experiments



Ring oscillators and individual transistor leakage currents

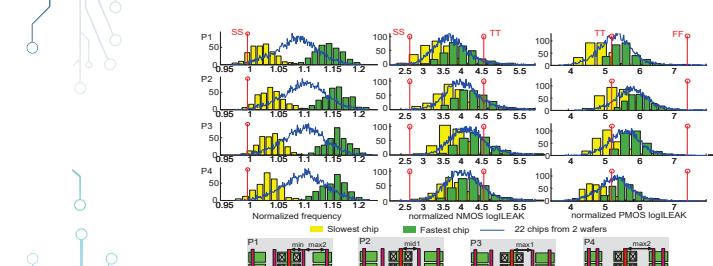
Results: Single Gates in 90nm



- Max ΔF between layouts $> 10\%$
- Within-die $3\sigma/\mu \sim 3.5\%$, weak dependency on density

EECS251B L15 VARIABILITY

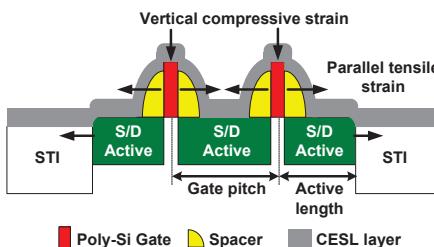
Results: Single Gates in 45nm



- Weak effect on performance, $\Delta F \sim 2\%$
- Small shifts in NMOS leakage and bigger shifts in PMOS leakage

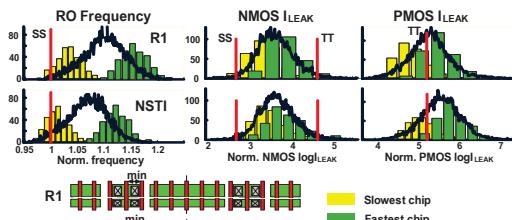
EECS251B L15 VARIABILITY

Impact of Stress



- > 45nm STM process: Wafer rotated <100> - higher PMOS mobility
- > NMOS strained through capping layer
- > Subatmospheric STI - weak tensile stress

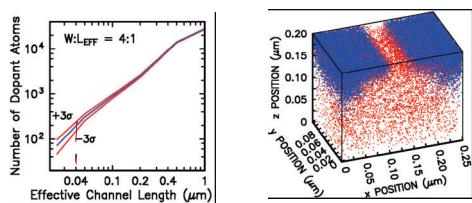
Impact of Shallow Trench Isolation (STI)



- $\Delta F \sim 3\%$, small changes in I_{LEAK}
- Due to STI-induced stress

Random Dopant Fluctuations

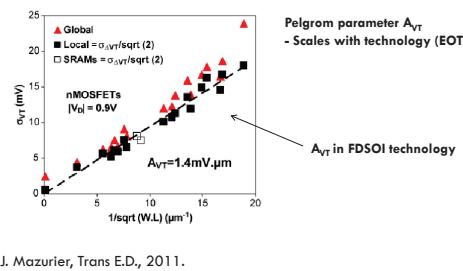
- Number of dopants is finite



Frank, IBM J R&D 2002

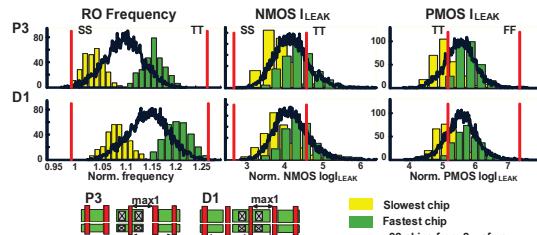
Transistor Matching

- V_{TH} matching of geometrically identical transistors varies with size $\sim \sqrt{WL}$ and distance



J. Mazurier, Trans E.D., 2011.

Impact of Longer Diffusion in 45nm

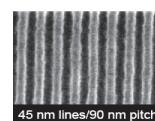


- Strongest effect measured in 45nm, $\Delta F \sim 5\%$
- No significant shift in I_{LEAK}

Design Variability Some Random Effects



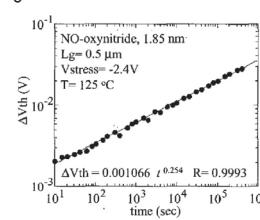
Processing: Line-Edge Roughness



- Sources of line-edge roughness:
 - Fluctuations in the total dose due to quantization
 - Resist composition
 - Absorption positions
- Effect:
 - Variation (random) in leakage and power

Negative Bias Temperature Instability

- PFET V_{TH} 's shift in time, at high negative bias and elevated temperatures
- The mechanism is thought to be the breaking of hydrogen-silicon bonds at the Si/SiO₂ interface, creating surface traps and injecting positive hydrogen-related species into the oxide.
- Also other charge trapping and hot-carrier defect generation
- Systematic + random shifts



Tsujikawa, IRPS'2003

Random Telegraph Signal (RTS)

- Trapping of a carrier in oxide traps modulates V_{th} or I_{ds}
 τ_e and τ_c are random and follow exponential distributions

N. Tega et al, IRPS 2008.

Summary

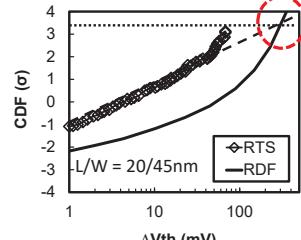
- Flip-flops:
 - Latch pairs
 - Pulse triggered
 - Variability
 - Systematic
 - Random

RTS and Technology Scaling

- RTS exceeds RDF at 3 sigma with 20nm gates

$$\Delta V_{th, RTS} \sim \frac{1}{WL}$$

$$\Delta V_{\text{th, RDF}} \sim \frac{1}{\sqrt{WL}}$$



Tega et. al, VLSI Tech. 09

Next Lecture

- Memories