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EECS251B : Advanced Digital Circuits and Systems

Lecture 9 – Modern Technologies

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2022 ISSCC: Feb. 19-26

(virtual)

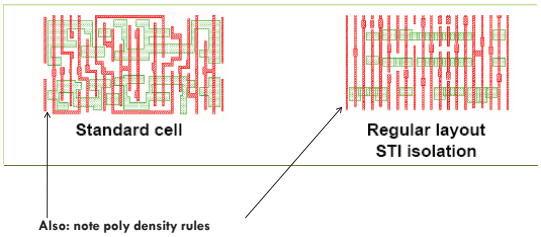
Main program, forums, tutorials, events

Recap

- Technology affects circuit design
  - Optimized for standard cell, SRAM density
  - Recent scaling not uniform per layer
- Lithography restricts layer orientation, length quantization
  - Favors layout regularity
  - Has implications on variability
- FinFETs add more restrictions (width quantization)

Lithography Implications

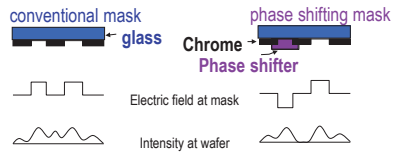
Litho (4): Restricted Design Rules (~45nm Node)



J.Hartmann, ISSCC'07

Litho (5): Phase-Shift Masks

- Phase Shifting Masks (PSM)
  - Creates interference fringes on the wafer →Interference effects boost contrast →Phase Masks can make extremely small lines

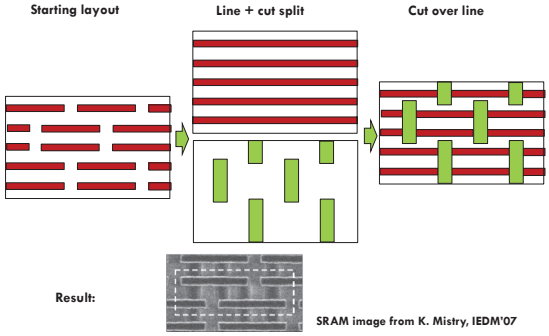


A. Kahng, ICCAD'03

Litho (6): Double Patterning

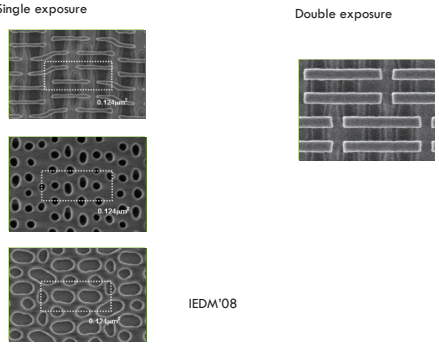
- Double exposure double etch
  - Double exposure double etch
  - Pitch split, litho-etch-litho-etch (LELE)
- Self-aligned methods
  - Self-aligned double patterning
  - Self-aligned quadruple patterning

Double-Exposure Double-Etch



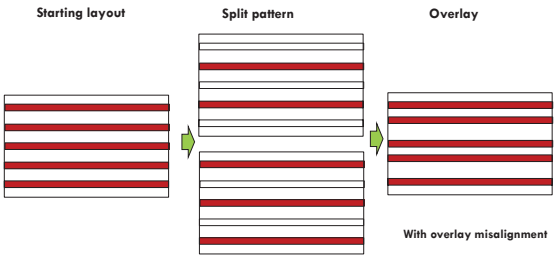
SRAM image from K. Mistry, IEDM'07

32nm Examples



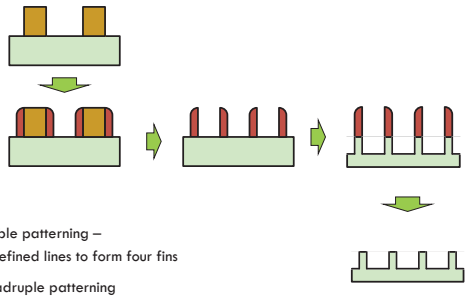
IEDM'08

Pitch-Split Double Exposure



Also called litho-etch-litho-etch (LELE)

Self-Aligned Double Patterning (SADP)



- SADP: Double patterning – Two litho-defined lines to form four fins
- SAQP: Quadruple patterning

Litho: Design Implications

- Forbidden directions
  - Depends on illumination type
  - Poly lines in other directions can exist but need to be thicker
- Forbidden pitches
  - Nulls in the interference pattern
  - Multiple patterning
- Forbidden shapes in PSM, multiple-patterning
- Assist features
  - If a transistor doesn't have a neighbor, let's add a dummy

Litho: Current Options (Beyond 10nm)

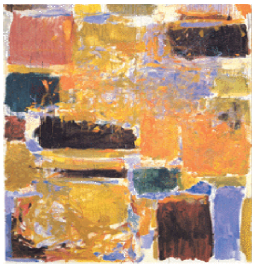
- Multiple patterning
  - NA ~ 1.2-1.35
- EUV lithography
  - λ = 13.5nm

Normalized wafer cost adder*	
SE	1
LELE	2.5
LELELE	3.5
SADP	2
SAQP	3
EUV SE	4
EUV SADP	6

*TEL™ Internal calculation

Cost adder reduced with increased power/throughput of EUV

A. Raley, SPIE'16



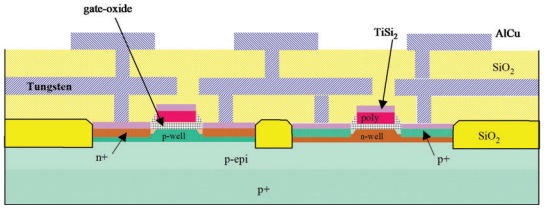
Modern Bulk/finFET/FDSOI processes

Some of the Process Features (Designer's Perspective)

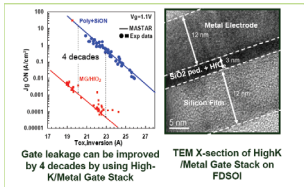
1. Shallow-trench isolation
2. High-k/Metal-gate technology
3. Strained silicon
4. Thin-body devices (28nm, and beyond)
5. Copper interconnects with low-k dielectrics

1. Shallow Trench Isolation

- Less space needed for isolation
- Some impact on stress

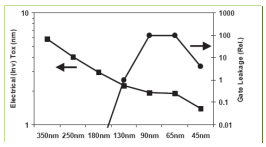


2. Hi-k/Metal gate



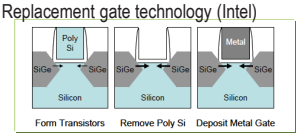
Gate leakage can be improved by 4 decades by using High-K/Metal Gate Stack

TEM X-section of HighK /Metal Gate Stack on FDSOI



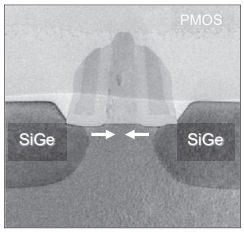
K. Mistry, IEDM'07

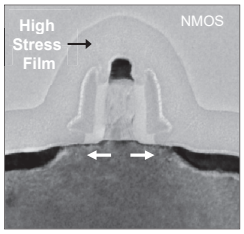
Replacement gate technology (Intel)



S. Natarajan, IEDM'08

3. Strained Silicon





Compressive channel strain 30% drive current increase in 90nm CMOS

Tensile channel strain 10% drive current increase in 90nm CMOS

Intel

Intel's Strained Si Numbers

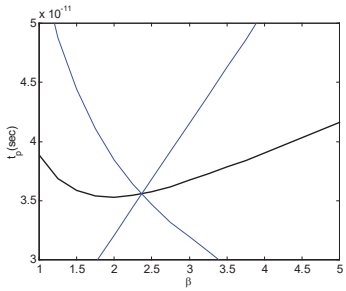
Performance gains:

	90 nm		65 nm	
	NMOS	PMOS	NMOS	PMOS
μ	20%	55%	35%	90%
IDSAT	10%	30%	18%	50%
IDLIN	10%	55%	18%	80%

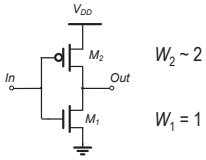
S. Thompson, VLSI'06 Tutorial

β-Ratio

- β=Wp/Wn

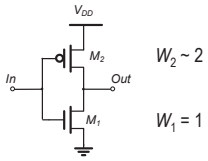


From Rabaey et al, DIC, 2nd ed, for 250nm CMOS

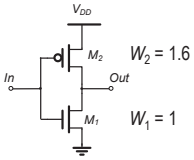


Strained Silicon: Implications on Sizing

- No strain

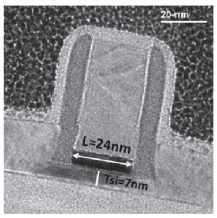


- Strained Si



5. Thin-Body Devices

- 28nm FDSOI



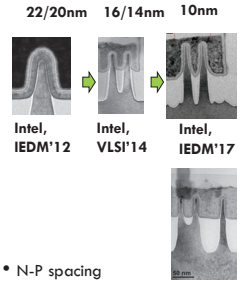
N. Planes, VLSI'2012

- 22/14nm finFET

C. Auth, VLSI'2012

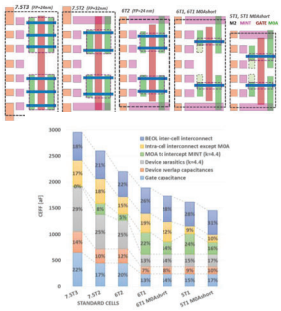
5. FinFETs

- FinFET scaling



- N-P spacing

- Track scaling

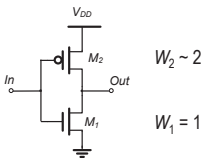


Garcia Bardon, IEDM'16

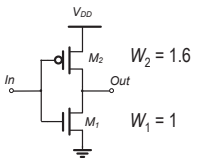
FinFETs and gate P/N sizing

- The use of strain closes the gap between N and P on currents to ~1:1

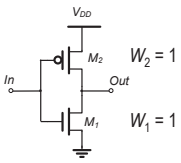
- No strain



- Strained planar Si



- FinFET



5. FDSOI

2012 2013 2014 2015 2016 2017

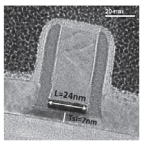
28FDSOI (STMicroelectronics)

28FD-SOI (Samsung)

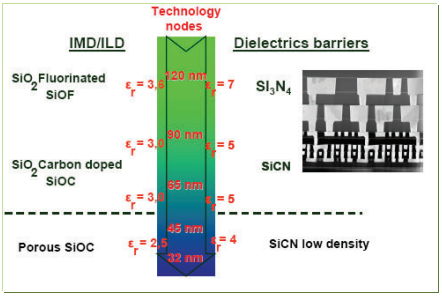
22FDX (GLOBALFOUNDRIES)

12FDX (GLOBALFOUNDRIES)

18FDS (Samsung)

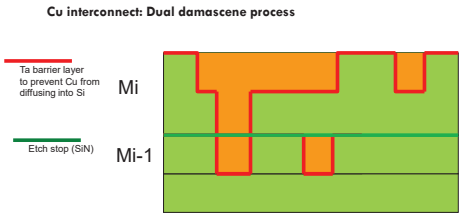


5. Interconnect



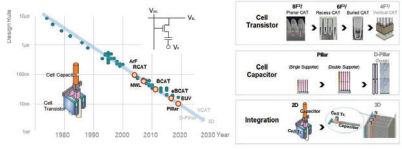
J. Hartmann, ISSCC'07

Interconnect: CMP



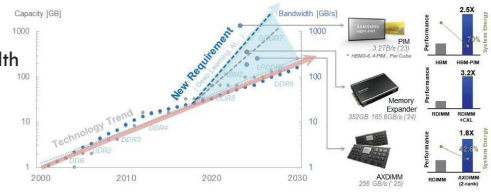
- Metal density rules (20%-80%)
- Slotting rules
- Also: Antenna rules

DRAM Scaling



- DRAM density scaling:
  - Transistor
  - Cap
  - Integration

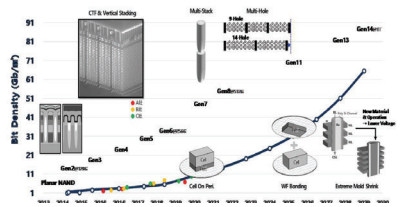
- DRAM capacity/bandwidth

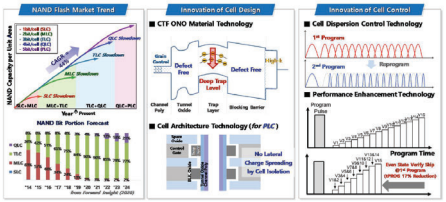


K.Kim, IEDM,'21

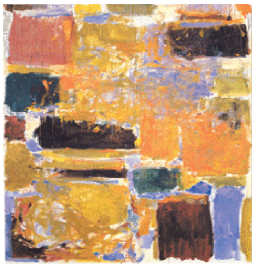
Flash Scaling

- Density and architecture scaling





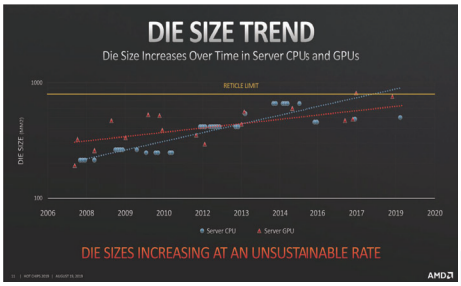
K.Kim, IEDM,'21



Chiplets

Die Size Trend

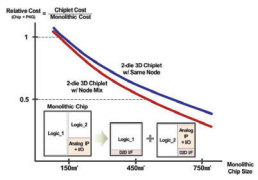
- To increase functionality and performance, die sizes have been increasing
  - Yield, cost tradeoffs



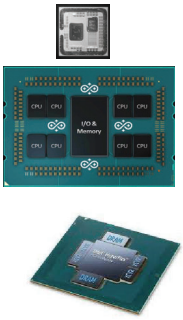
L. Su, HotChips'19 Keynote

Migration to Chiplets

- Split the product into multiple dies
  - Same or mixed technologies
- Increase functionality, performance @ lower cost
- Mix technologies

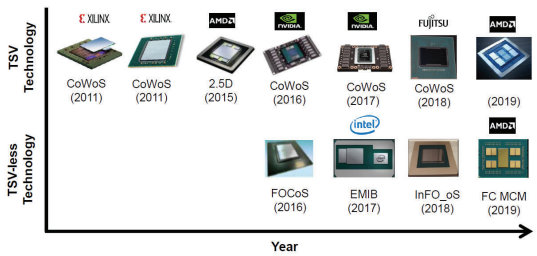


Plot from K.Kim, IEDM'21



2.D Chiplet Interfaces

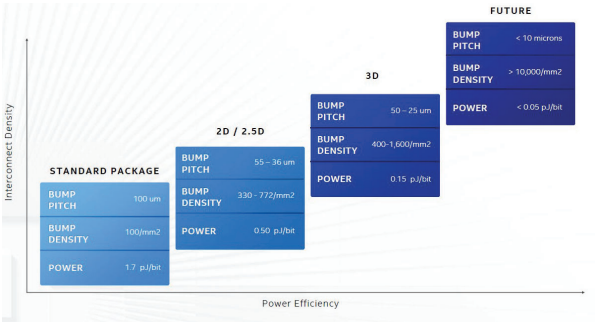
- High-denisity interfaces have been evolving over the past decade



K.C.Yee, D.Yu, IEDM'20 Short Course

Interconnect Density Scaling

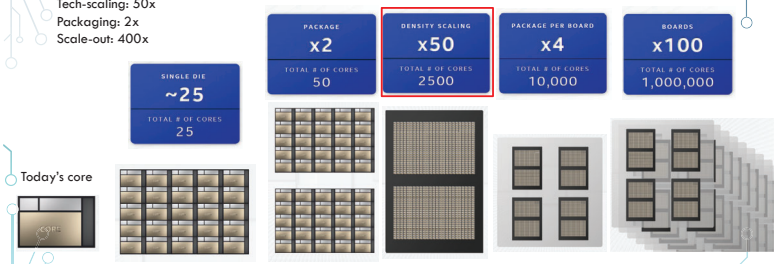
- Bump density and BW/edge or BW/area



Adapted from R. Koduri keynote, Hot Chips 2020

Scaling is scale-out ... Getting to 1M cores/system

On-chip integration: 25x
Tech-scaling: 50x
Packaging: 2x
Scale-out: 400x

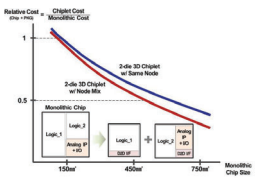


Today's core

Adapted from R. Koduri keynote, Hot Chips 2020

Some Open Issues

- High-value (e.g. hyperscale) products are driving the chiplet technology
  - What about sub-150mm2 dies?



Cost of disintegration:

- AIB 1.0: 12mm² in 16nm @ $0.1/mm² = $1.2 on each side (50k mm² on a $5k 12-in wafer; 5nm wafers are $15k – chiplet interface is 2 x $4)
- Substrate cost: >$10 (could be >$100)
- Test escape losses

Sum: $25+ (but can be >$100)

Chiplets are not for free

Can they offset the NRI costs?
Make medium volume ASICs affordable?

Summary

- FinFET and FDSOI processes deployed now
  - Expected to be replaced by nanosheets
- Lithography and manufacturing restrict design rules
  - Need to be aware of implications on design
  - EuV entering production
- More changes coming: forksheets, buried power rails, chiplets – 2.5D and 3D
  - Plurality of interconnect standards

Next Lecture

- Transistor models, gate sizing