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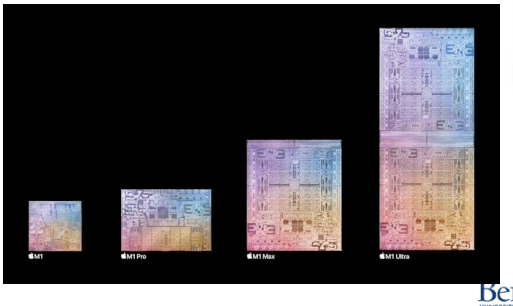
EECS251B : Advanced Digital Circuits and Systems

Lecture 15 – Variability

Borivoje Nikolić, Vladimir Stojanović, Sophia Shao

Apple Announces M1Ultra
March 8, 2022, AnandTech



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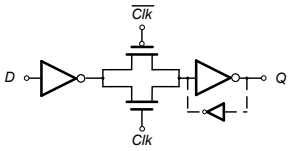
Recap

- Logical effort can be used to analyze latch timing
  - Clk-Q, D-Q delays are ~1FO4 delay (with F=1)

t_{setup}



$t_{clk\text{-}q} = 2.7\ t_u + 2.2\ t_u$

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Flip-Flops

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Key Point

- Two ways to design a flip-flop
  - Latch pair (large majority)
  - Pulsed latch

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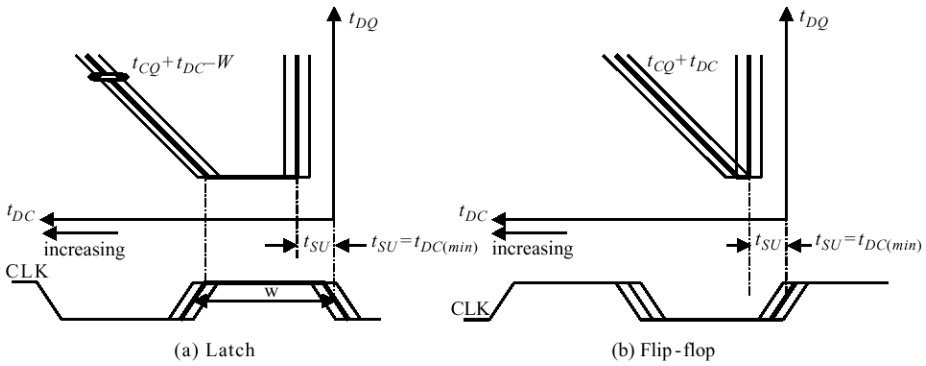
Latch vs. Flip-Flop



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Flip-Flops

- Performance metrics
- Delay metrics
  - Insertion delay
  - Inherent race immunity
  - 'Softness' (Clock skew absorption)
  - Inclusion of logic
  - Small (+constant) clock load
- Power/Energy Metrics
  - Power/energy
- Design robustness
  - Noise immunity

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Scan Test

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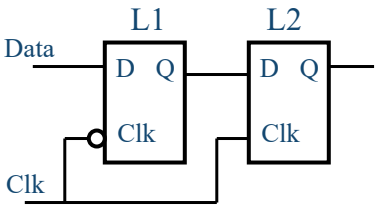
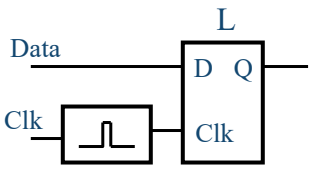
Types of Flip-Flops

Latch Pair



Pulse-Triggered Latch



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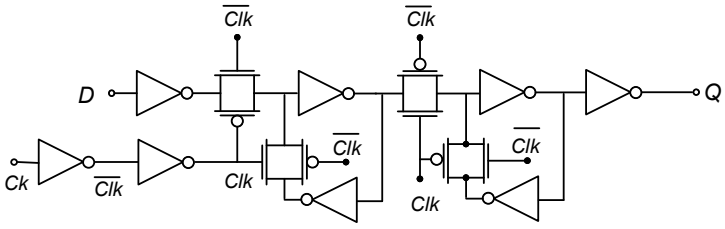
Flip-Flop (Latch Pair) Clk-Q, setup, hold



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Flip-Flop Timing Characterization

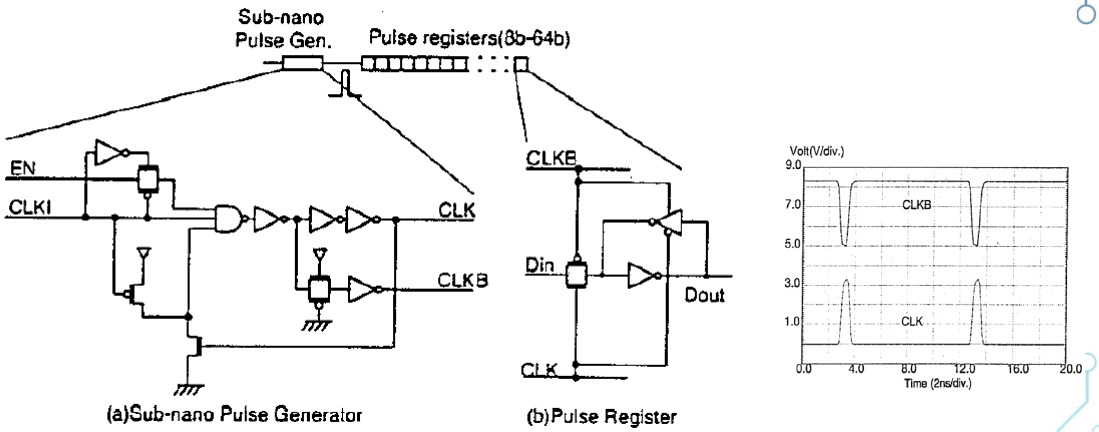
- Combinational logic delay is a function of output load and input slope
- Sequential timing (flip-flop):
  - t_{clk-q} is function of output load and clock rise time
  - t_{Su}, t_H are functions of D and Clk rise/fall times

Pulse-Triggered Latches

- First stage is a pulse generator
  - generates a pulse (glitch) on a rising edge of the clock
- Second stage is a latch
  - captures the pulse generated in the first stage
- Pulse generation results in a negative setup time
- Frequently exhibit a soft edge property
- Note: power is always consumed in the pulse generator
  - Often shared by a group (register)

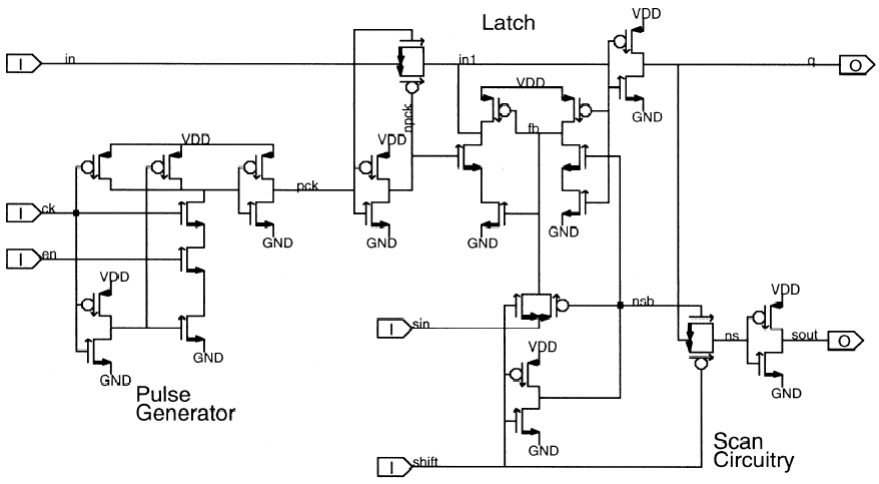
Pulsed Latch

Simple pulsed latch



Kozu, ISSCC'96

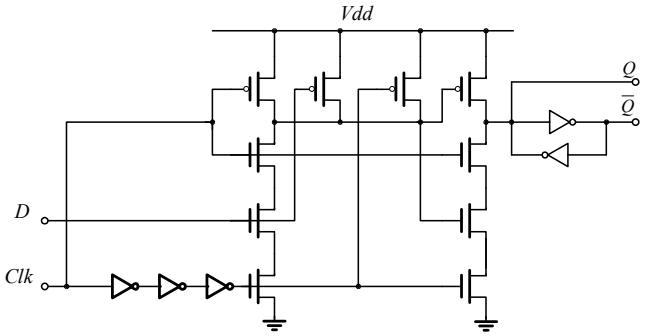
Intel/HP Itanium 2



Naffziger, ISSCC'02

Pulsed Latches

Hybrid Latch Flip-Flop, AMD K-6
Partovi, ISSCC'96



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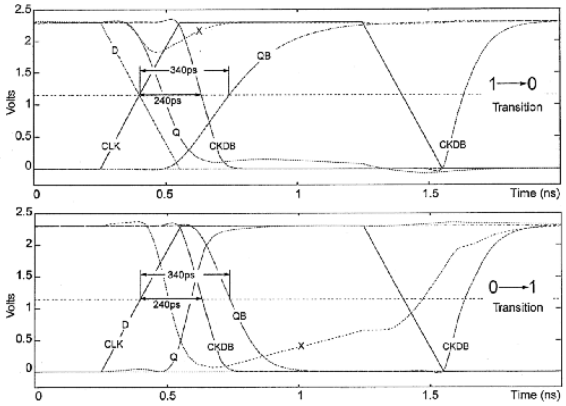
HLFF Operation

1-0 and 0-1 transitions at the input with 0ps setup time



VDD=2.3v, 85°C, Typical Devices
C_{clk} = 60ff, C_{qb} = 300ff

$T_{cq} = T_{dq}$ = 340ps
T_{hold} = 180ps
$T_{su(min)}$ = -90ps

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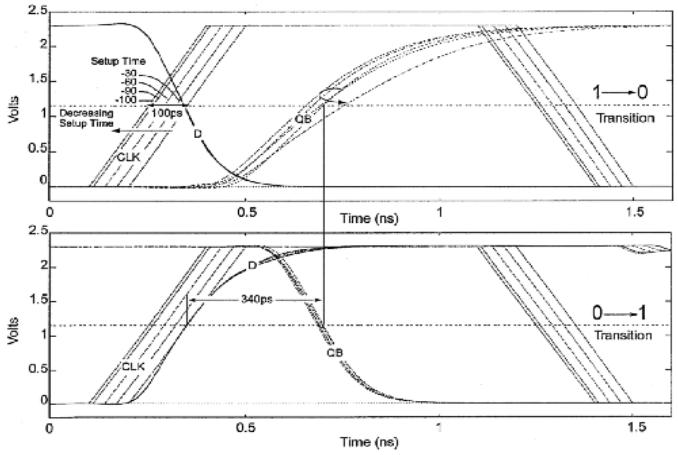
Hybrid Latch Flip-Flop

Skew absorption



Partovi *et al*, ISSCC'96

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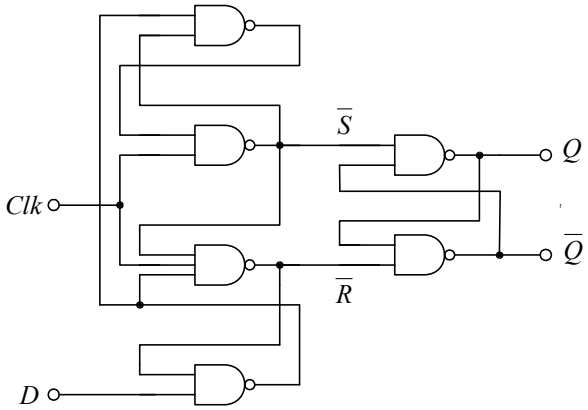
Pulsed Latches

7474, from mid-1960's



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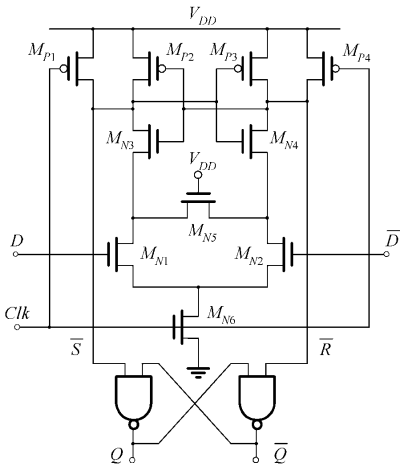
Pulsed Latches

Sense-amplifier-based flip-flop, Matsui 1992.
DEC Alpha 21264, StrongARM 110

First stage is a sense amplifier, precharged to high, when *Clk* = 0
After rising edge of the clock sense amplifier generates the pulse on
S or *R*
The pulse is captured in
S-R latch
Cross-coupled NAND has different propagation delays of rising and falling edges



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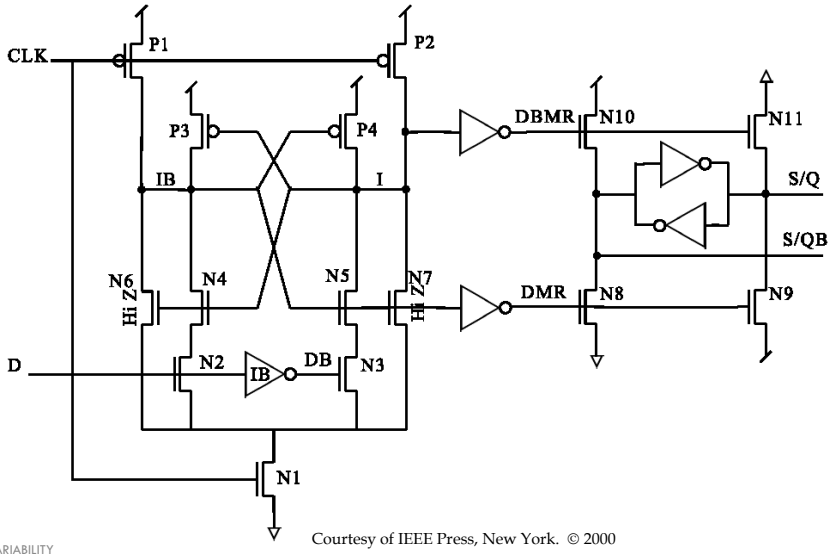
Sense Amplifier-Based Flip-Flop



Courtesy of IEEE Press, New York. © 2000

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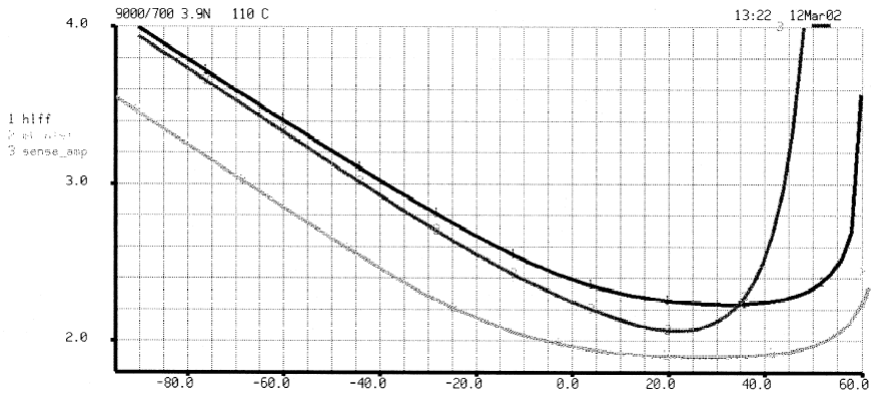
Sampling Window Comparison



Naffziger, JSSC 11/02

Announcements

- Lab 5 due this week
- Midterm reports due next week
  - 4 pages, conference format
- Assignment 2 posted this week

Design Variability Sources and Impact on Design

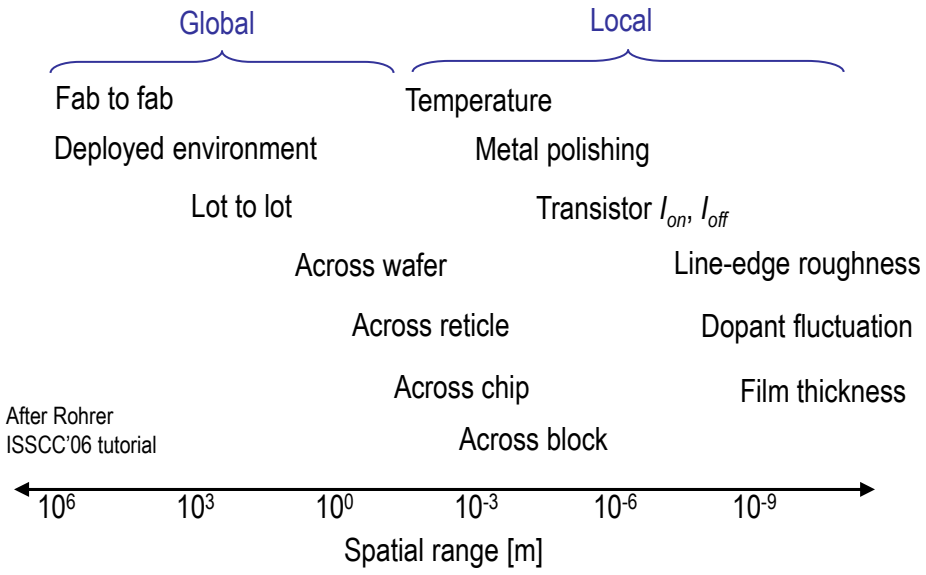
Variability Classification

- Nature of process variability
  - Within-die (WID), Die-to-die (D2D), Wafer-to-wafer (W2W), Lot-to-lot (L2L)
  - Systematic vs. random
  - Correlated vs. non-correlated
- Spatial variability/correlation
  - Device parameters (CD, t_{ox}, …)
  - Supply voltage, temperature
- Temporal variability/correlation
  - Within-node scaling, Electromigration, Hot-electron effect, NBTI, self-heating, temperature, SOI history effect, supply voltage, crosstalk
    [Bernstein, IBM J. R&D, July/Sept 2006]
- Known vs. unknown
  - Goal of model-to-hw correlation is to reduce the unknowns

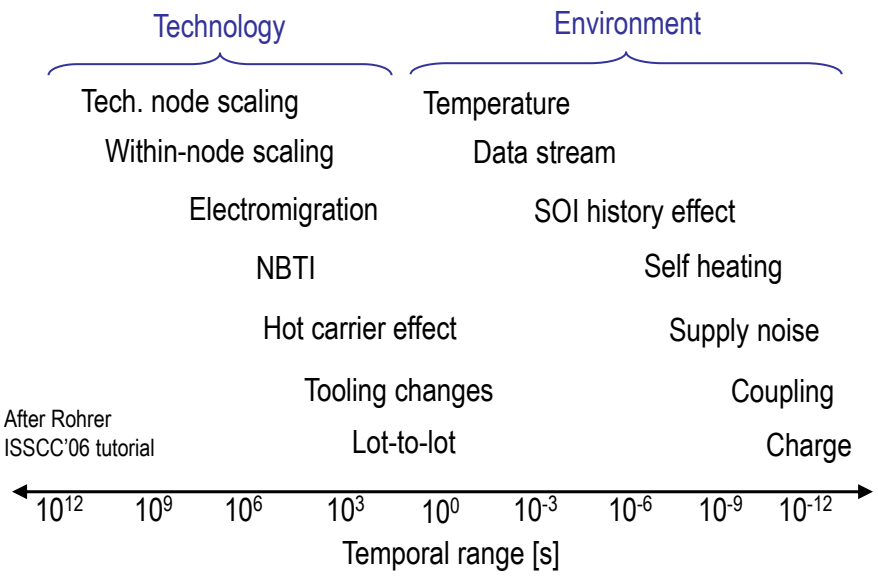
Sources of Variability

- Technology
  - Front-end (Devices)
    - Systematic and random variations in Ion, Ioff, C, …
  - Back-end (Interconnect)
    - Systematic and random variations in R, C
- Environment
  - Supply (IR drop, noise)
  - Temperature

Spatial Variability



Temporal Variability



Systematic vs. Random Variations

- Systematic
  - A systematic pattern can be traced down to lot-to-lot, wafer-to-wafer, within reticle, within die, from layout to layout,…
  - Within-die: usually spatially correlated
- Random
  - Random mismatch (dopant fluctuations, line edge roughness,…)
  - Things that are systematic, but e.g. change with a very short time constant (for us to do anything about it). Or we don't unedrstand it well enough to model it as systematic. Or we don't know it in advance ("How random is a coin toss?").
- Unknown

Systematic and Random Device Variations

Parameter	Random	Systematic
Channel Dopant Concentration Nch	Affects σ_{VT} [1] 	Non uniformity in the process of dopant implantation, dosage, diffusion
Gate Oxide Thickness Tox	Si/SiO_2 & SiO_2/Poly-Si interface roughness[2] 	Non uniformity in the process of oxide growth
Threshold Voltage V_T (non Nch related)	Random anneal temperature and strain effects	Non-uniform annealing temperature[5] (metal coverage over gate) Biaxial strain
Mobility μ	Random strain distributions	Systematic variation of strain in the Si due to STI, S/D area, contacts, gate density, etc
Gate Length L	Line edge roughness (LER)[3] 	Lithography and etching: Proximity effects, orientation[4]
Fin geometry/ film thickness variations	Rounding, etc, σ_{VT}, mobility.	Systematic fin thickness Systematic Si film/BOX variations

[1] D. Frank et al, *VLSI Symposium*, Jun. 1999 . [2] A. Asenov et al, *IEEE Trans on Electron Devices,* Jan. 2002.
[3] P. Oldiges et al, *SISPAD 2000,* Sept. 2000. [4] M. Orshansky et al, *IEEE Trans on CAD*, May 2002. [5] Tuinhout et al, *IEDM*, Dec 1996

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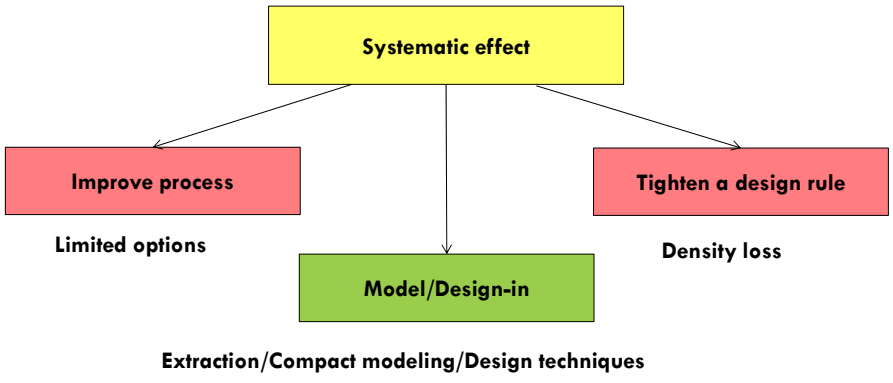
Dealing with Systematic Variations

- Model-to-hardware correlation classifies unknown sources



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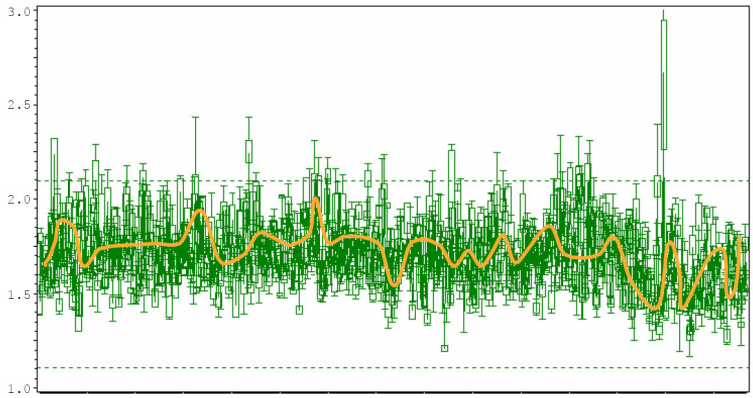
Systematic (?) Temporal Variability

Metal 3 resistance over 3 months



P. Habitz, DAC'06 tutorial

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Impact of Correlations

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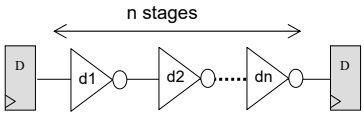
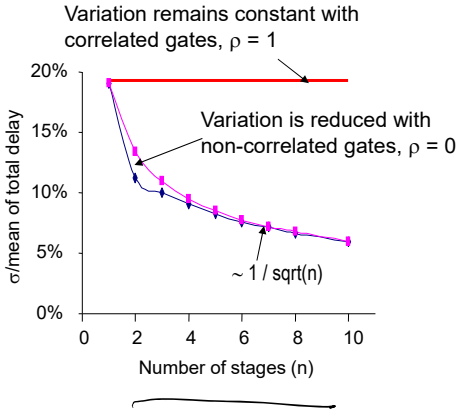
Chip Yield Depends on Inter-Gate Correlation



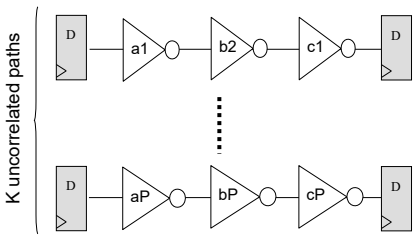


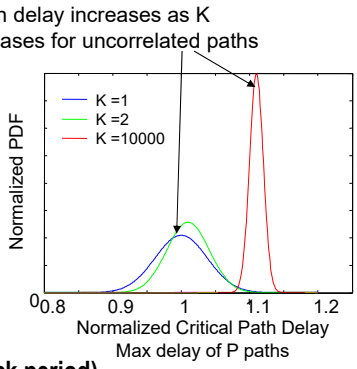
- **Yield = Pr (sum of n delays < clock period)**
- **ρ = 0 gives highest yield through averaging**

Non-correlated gates in a path reduce impact of variation

Bowman et al, *JSSC*, Feb 2002 .

Chip Yield Depends on Inter-Path Correlation





- **Yield = Pr (max delay of K paths < clock period)**
- **K = 1 gives highest yield**

Correlated paths reduce impact of variation

Bowman et al, *JSSC*, Feb 2002 .

Process Corners

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Design Variability
Some Systematic Effects

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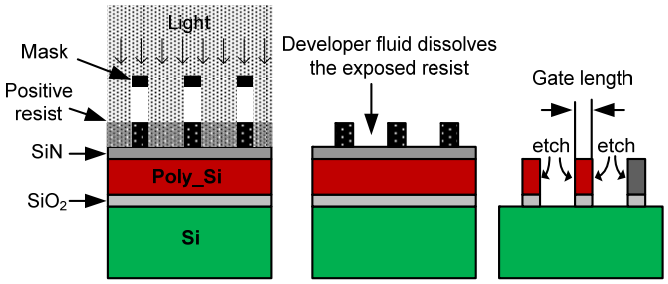
Layout: Poly Proximity Effects

- Gate CD is a function of its neighborhood



Gate length depends on

- **Light intensity profile falling on the resist**
- **Resist: application of developer fluid[1], post exposure bake (PEB) temperature[2]**
- **Dry etching: microscopic loading effects[3]**

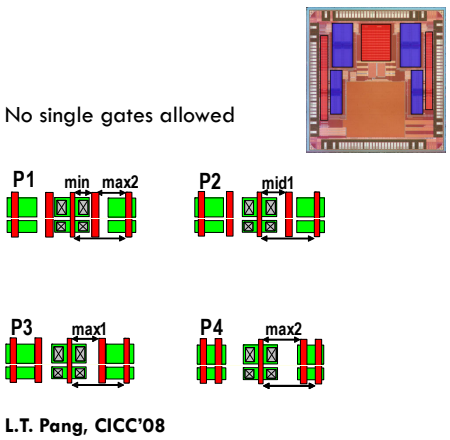
[1] J.Cain, M.S. Thesis, UC Berkeley
[2] D. Steele et al, *SPIE*, vol.4689, July 2002.
[3] J. D. Plummer, M.D. Deal, P.B. Griffin, Silicon VLSI Technology, Prentice-Hall, 2000.

Layout: Proximity Test Structures

- 90nm experiments

L.T. Pang, VLSI'06

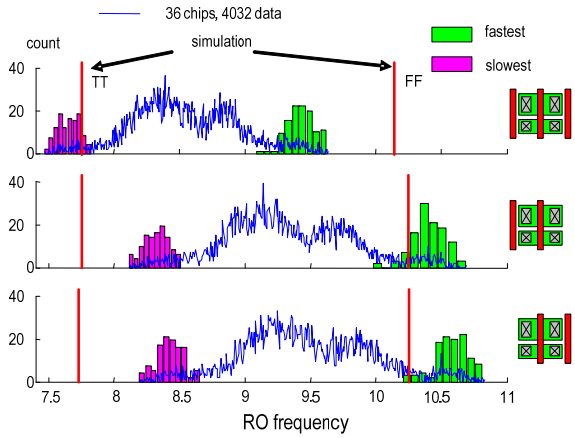
- 45nm experiments



L.T. Pang, CICC'08

- **Ring oscillators and individual transistor leakage currents**

Results: Single Gates in 90nm



- **Max ΔF between layouts > 10%**
- **Within-die 3σ/μ ~ 3.5%, weak dependency on density**

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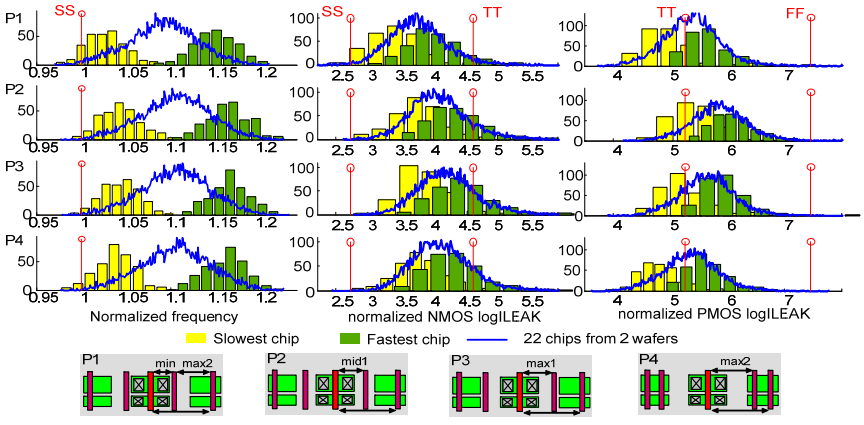
Results: Single Gates in 45nm



- **Weak effect on performance. ΔF ~ 2%**
- **Small shifts in NMOS leakage and bigger shifts in PMOS leakage**

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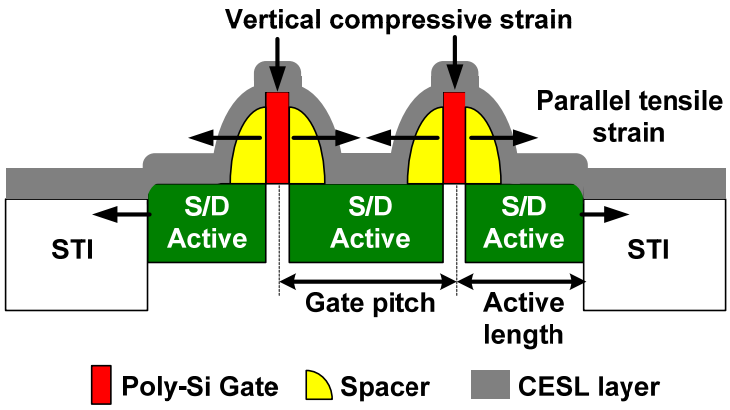
Impact of Stress



- 45nm STM process: Wafer rotated <100> - higher PMOS mobility
- NMOS strained through capping layer
- Subatmospheric STI – weak tensile stress

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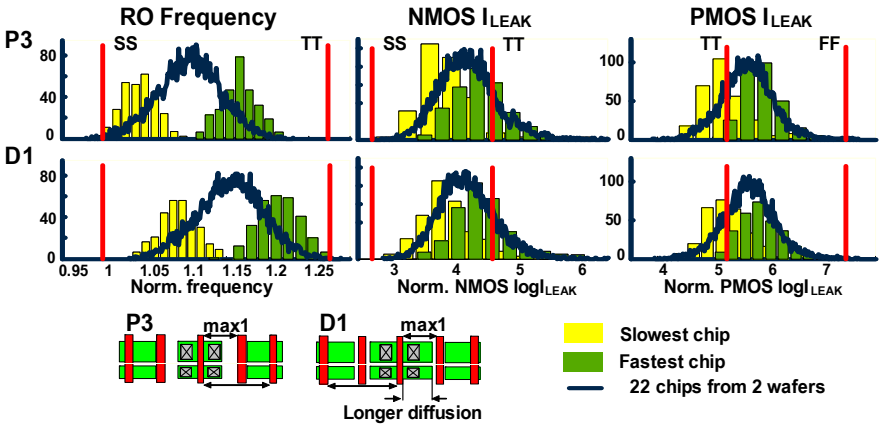
Impact of Longer Diffusion in 45nm



- Strongest effect measured in 45nm, ΔF ~ 5%
- No significant shift in I_{LEAK}

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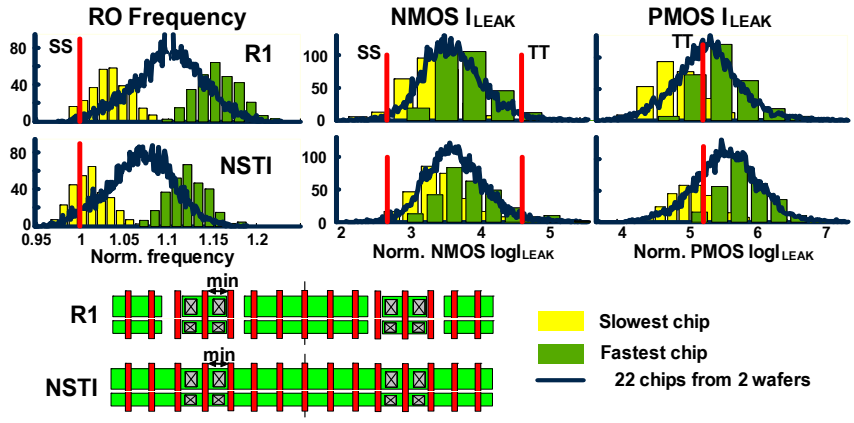
Impact of Shallow Trench Isolation (STI)



- ΔF ~ 3%, small changes in I_{LEAK}
- Due to STI-induced stress

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Design Variability
Some Random Effects

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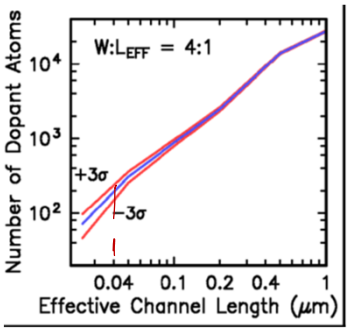
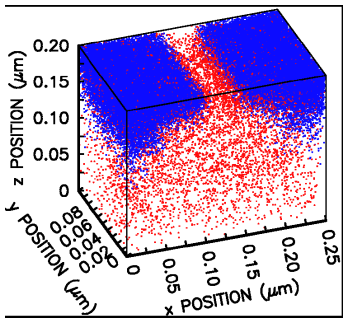
Random Dopant Fluctuations

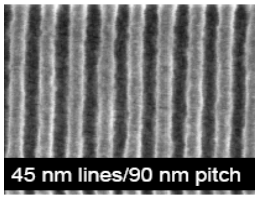
- Number of dopants is finite





Frank, IBM J R&D 2002

Processing: Line-Edge Roughness

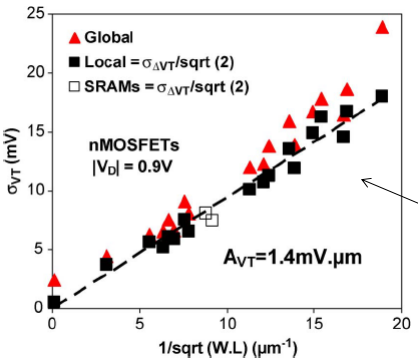


•Sources of line-edge roughness:
- Fluctuations in the total dose due to quantization
- Resist composition
- Absorption positions

Effect:
- Variation (random) in leakage and power

Transistor Matching

- V_{Th} matching of geometrically identical transistors varies with size $\sim\sqrt{WL}$ and distance



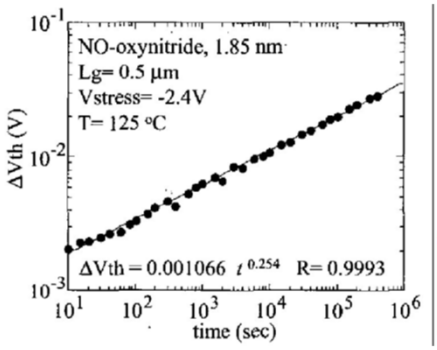
Pelgrom parameter A_{VT}
- Scales with technology (EOT)

A_{VT} in FDSOI technology

J. Mazurier, Trans E.D., 2011.

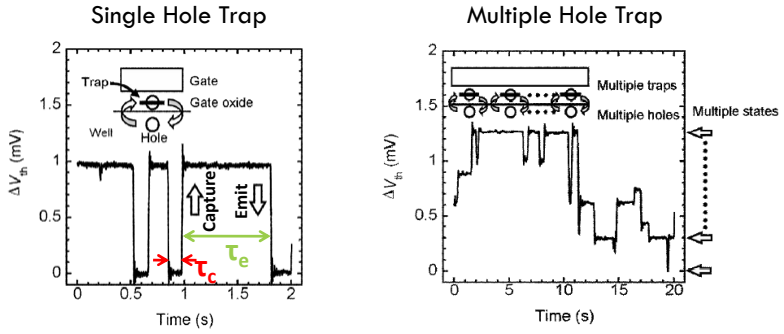
Negative Bias Temperature Instability

- PFET V_{Th}'s shift in time, at high negative bias and elevated temperatures
- The mechanism is thought to be the breaking of hydrogen-silicon bonds at the Si/SiO2 interface, creating surface traps and injecting positive hydrogen-related species into the oxide.
- Also other charge trapping and hot-carrier defect generation
- Systematic + random shifts



Tsujikawa, IRPS'2003

Random Telegraph Signal (RTS)



- Trapping of a carrier in oxide traps modulates V_{th} or I_{ds}
- τ_e and τ_c are random and follow exponential distributions

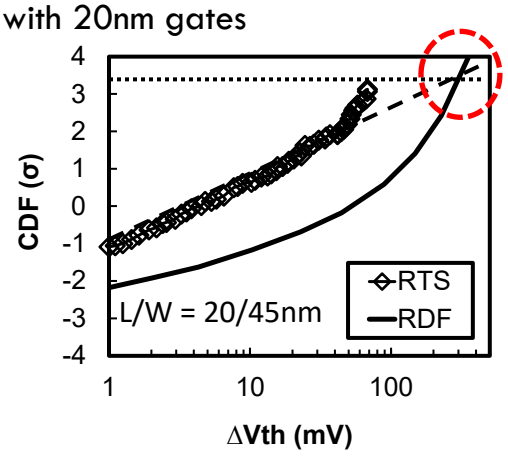
N. Tega et al, IRPS 2008.

RTS and Technology Scaling

- RTS exceeds RDF at 3 sigma with 20nm gates

$$\Delta V_{th,\,RTS} \sim \frac{1}{WL}$$

$$\Delta V_{th,\,RDF} \sim \frac{1}{\sqrt{WL}}$$



Tega *et. al*, VLSI Tech. 09

Summary

- Flip-flops:
  - Latch pairs
  - Pulse triggered
- Variability
  - Systematic
  - Random

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Next Lecture

- Memories

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