

EECS251B : Advanced Digital Circuits and Systems

Lecture 10 – Transistor Models



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Feb. 15, 2022, Reuters

Intel to acquire Tower Semiconductor in \$5.4 bln deal

Intel Corp agreed to acquire Tower Semiconductor Ltd (TSEM.TA) for an enterprise value of \$5.4 billion, the companies said on Tuesday.

Intel will acquire Tower for \$53 per share in cash, the statement added.

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Berkeley

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Recap

- FinFET and FDSOI processes deployed now
 - Expected to be replaced by nanosheets
- Lithography and manufacturing restrict design rules
 - Need to be aware of implications on design
 - EUV entering production
- More changes coming: forksheets, buried power rails, chiplets – 2.5D and 3D
 - Plurality of interconnect standards



MOS Transistor and Gate Delay Models

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Device Models

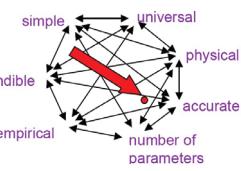
- Transistor models
 - I-V characteristics
 - C-V characteristics
- Interconnect models
 - R, C, L
 - Covered in EE240A

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Transistor Modeling

- DC
 - Accurate I-V equations
 - Well behaved conductance for convergence (not necessarily accurate)
- Transient
 - Accurate I-V and Q-V equations
 - Accurate first derivatives for convergence
 - Conductance, as in DC
- Physical vs. empirical

from BSIM group



Modeling Goals

- Models that traverse design hierarchy
- Start with transistor models
- Gate delay models
- Use models to time the design
- Modeling variability
- Based on 251A, approach
 - Start simple
 - Increase accuracy, when needed

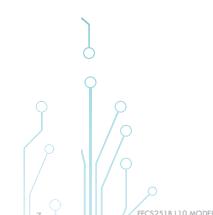
Transistor Modeling

- Different levels:
 - Hand analysis
 - Computer-aided analysis (e.g. Matlab, Python, Excel,...)
 - Switch-level simulation (some flavors of 'fast Spice')
 - Circuit simulation (Hspice)
- These levels have different requirements in complexity, accuracy and speed of computation
- We are primarily interested in delay and energy modeling, rather than current modeling
- But we have to start from the currents...

Goal for Today

- Develop velocity-saturated model for I_{on} and apply it to sizing and delay calculation
 - Similar approach as in 251A, just use an analytical model

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Transistor I-V Modeling

- BSIM
 - Superthreshold and subthreshold models
 - Need smoothening between two regions
- EKV/PSP
 - One continuous model based on channel surface potential

Project proposals

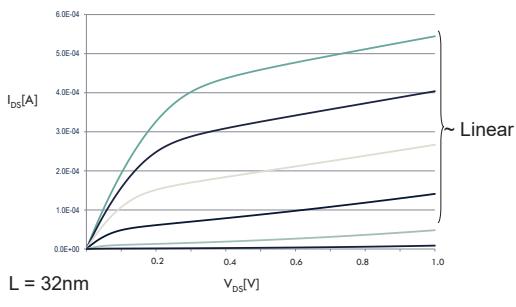
- Title: Pick a meaningful title
- Authors, contact e-mail
- 1/2-page abstract
- 5 references

MOS I-V (BSIM)

Start with the basics:

$$I_{DS} = W C_{ox} (V_{GS} - V_{Th} - V_c(x)) \mu E$$

Simulated 32nm Transistor



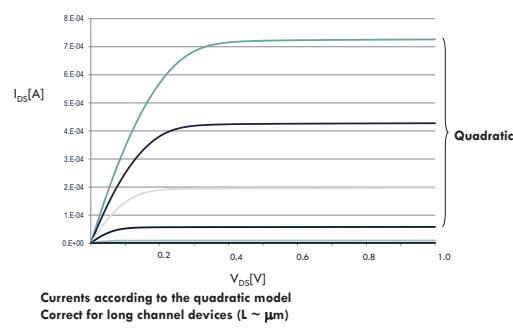
Announcements

- Assignment 1 posted this week
 - No new lab this week
- Project proposals due next Thursday
- No class on Tuesday

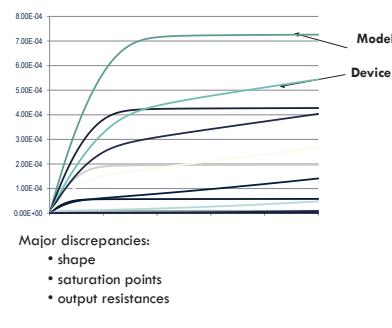
Long-Channel MOS On-Current



MOS Currents (32nm CMOS with $L >> 1\mu m$)



Simulation vs. Model

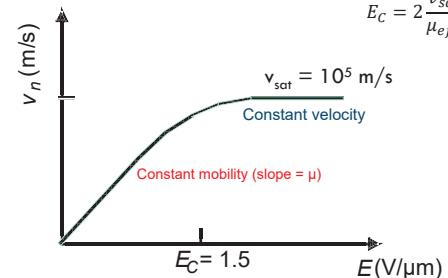




Velocity Saturation

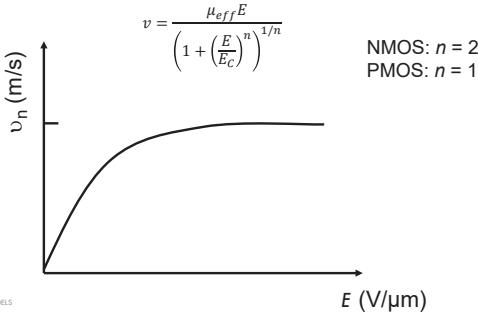
Velocity Saturation

$$E_C = 2 \frac{v_{sat}}{\mu_{eff}}$$



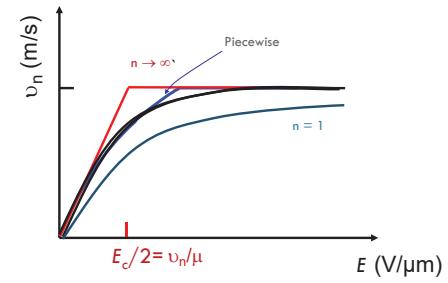
Modeling Velocity Saturation

- Fit the velocity-dependence curve



Modeling Velocity Saturation

- A few approximations: (a) $n \rightarrow \infty$, (b) $n = 1$, (c) piecewise



Short-Channel MOS On-Current

Approximation $n \rightarrow \infty$

$$I_{DS} = \mu C_{ox} \frac{W}{L} \left((V_{GS} - V_{Th}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

$$1) V = \mu_{eff} E, \quad E < E_c$$

$$I_{DS} = \mu C_{ox} \frac{W}{L} \left((V_{GS} - V_{Th}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

$$V_{DSat} = ?$$

Can be reduced to Rabaey DIC model by making $V_{DSat} = \text{const}$

Is this physically justified?

MOS Model from DIC, 2nd ed.

$$I_D = 0 \text{ for } V_{GT} \leq 0$$

$$I_D = k' \frac{W}{L} \left(V_{GT} V_{min} - \frac{V_{min}^2}{2} \right) (1 + \lambda V_{DS}) \text{ for } V_{GT} \geq 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$,

$$V_{GT} = V_{GS} - V_T$$

and $V_T = V_{TO} + \gamma (\sqrt{-2\phi_F + V_{SB}} - \sqrt{-2\phi_F})$

γ - body effect parameter

From Rabaey, 2nd ed.

Unified MOS Model

- Model presented is compact and suitable for hand analysis.
- Still have to keep in mind the main approximation: that V_{DSat} is constant . When is it going to cause largest errors?
 - When does E scale? – Transistor stacks.
- But the model still works fairly well.
 - Except for stacks

Approximation $n = 1$, piecewise

- $n = 1$ is solvable, piecewise closely approximates

$$\text{Velocity, } v: \quad v = \begin{cases} \frac{\mu_{eff}E}{1+E/E_c}, & E < E_c = \frac{2v_{sat}}{\mu_{eff}} \\ v_{sat}, & E > E_c \end{cases}$$

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Sodini, Ko, Moll, TED'84
Toh, Ko, Meyer, JSSC'88
BSIM model

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Drain Current in Velocity Saturation

- Solving for V_{Dsat}

$$V_{Dsat} = \frac{(V_{GS} - V_{Th})E_c L}{(V_{GS} - V_{Th}) + E_c L}$$

- And saturation current

$$I_{Dsat} = \frac{W \mu_{eff} C_{ox} E_c L}{2} \frac{(V_{GS} - V_{Th})^2}{(V_{GS} - V_{Th}) + E_c L}$$

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Velocity Saturation

- $E_c L$ is V_{GS} -dependent
- Can calculate V_{Dsat} ($V_{Th} \sim 0.4V$ in 28nm)

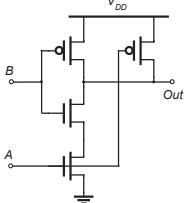
V_{GS} [V]	0.5	0.6	0.7	0.8	0.9	1.0
V_{Dsat} [V]	0	0.05	0.11	0.18	0.25	0.33

- For $V_{GS} - V_{Th} \ll E_c L$, V_{Dsat} is close to $V_{GS} - V_{Th}$
- For large V_{GS} , V_{Dsat} bends upwards toward $E_c L$
- Therefore, $E_c L$ can be sometimes approximated with a constant term
 - But also need to understand the limitation of the approximation

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Application of Models: NAND Gate

- 2-input NAND gate



Sizing for equal transitions:

- P/N ratio (β -ratio): 1 for $L < 20nm$, 1.6 for $20nm < L < 65nm$, 2 for $L > 90nm$
- Upsizing stacks by a factor proportional to the stack height

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Drain Current

- We can find the drain current by integrating I_{DS}

$$\text{Linear: } I_{DS} = \frac{\mu C_{ox}}{1 + (V_{DS}/E_c L)} \frac{W}{L} \left((V_{GS} - V_{Th})V_{DS} - \frac{V_{DS}^2}{2} \right)$$

In saturation:

$$I_{DSat} = C_{ox} W v_{sat} (V_{GS} - V_{Th} - V_{DSat})$$

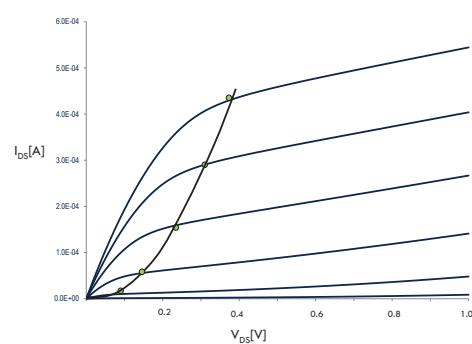
$$I_{DSat} = \frac{\mu C_{ox}}{1 + (V_{DSat}/E_c L)} \frac{W}{L} \left((V_{GS} - V_{Th})V_{DSat} - \frac{V_{DSat}^2}{2} \right)$$

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Velocity Saturation



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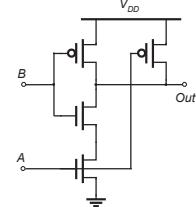
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Application of I-V Models



Transistor Stacks

- With transistor stacks, V_{DS} , V_{GS} reduce.
- Unified model assumes $V_{DSat} = \text{const.}$
- For a stack of two, appears that both have exactly double R_{eqv} of an inverter with the same width
- Therefore, doubling the size of each, should make the pull-down R equivalent to an inverter



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Velocity Saturation

- As $(V_{GS} - V_{Th})/E_C L$ changes, the depth of saturation changes

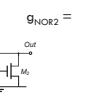
$$I_{DSat} = \frac{W}{L} \frac{\mu_{eff} C_{ox} E_C L}{2} \frac{(V_{GS} - V_{Th})^2}{(V_{GS} - V_{Th}) + E_C L}$$

- For $V_{GS}, V_{DS} = 1.0V$, $E_C L$ is $\sim 0.75V$
- With double length, $E_C L$ is $1.5V$ (in this model in 28nm)
- Stacked transistors are less saturated
- $V_{GS} - V_{Th} = 0.6V$, $I_{DSat} \sim 2/3$ of inverter I_{DSat} (64%)
- Therefore NAND2 should have pull-down sized 1.5X
- Check any library NAND2's
- Current halved in a stack of 3

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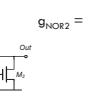
Example: Logical Effort

- Older CMOS ($>90nm$)

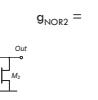


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- Planar CMOS ($\sim 28nm$, bulk, FDSOI)



- FinFET (7nm)



Note about FinFETs

- Widths are quantized



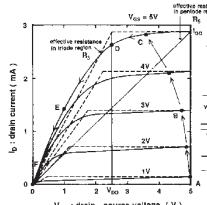
Other Velocity Saturation Models

Other Models: Alpha Power Law Model

- Simple model, sometimes useful for hand analysis

$$I_{DS} = \frac{W}{2L} \mu C_{ox} (V_{GS} - V_{Th})^\alpha$$

Parameter α is between 1 and 2.



Sakurai, Newton, JSSC 4/90

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Alpha Power Law Model

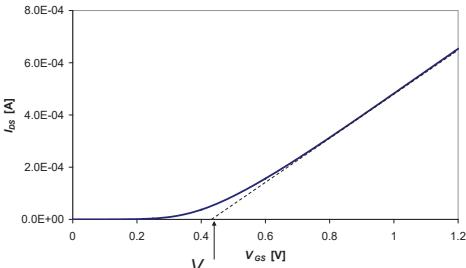
- This is not a physical model

- Simply empirical:

- Can fit (in minimum mean squares sense) to variety of α 's, V_{Th}
- Need to find one with minimum square error – fitted V_{Th} can be different from physical
- Can also fit to $\alpha = 1$
- What is V_{Th} ?

$K(V_{GS} - V_{Thz})$ Model ($\alpha = 1$)

Drain current vs. gate-source voltage



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Saturation Current Models

Model	Usage
$I_{DS} = K \frac{W}{L} (V_{GS} - V_{Thz})$	Delay estimates with $V_{DD} \gg V_{Th}$
$I_{DS} = \frac{W}{L} \frac{\mu C_{ox}}{2} (V_{GS} - V_{Th})^2$	Long channel devices (rare in digital)
$I_{DS} = \frac{W}{L} \frac{\mu C_{ox}}{2} (V_{GS} - V_{Th})^\alpha$	Delay estimates in a wider range of V_{DD} 's
$I_{DS} = \frac{W}{L} \frac{\mu C_{ox}}{2} (V_{GS} - V_{Th}) \frac{V_{DSat}^2}{2}$	Easy to remember, does not handle stacks correctly
$I_{DS} = \frac{W}{L} \frac{\mu C_{ox}}{2} \frac{E_C L (V_{GS} - V_{Th})^2}{(V_{GS} - V_{Th}) + E_C L}$	Handles stacks correctly, sizing

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Next Lecture

- Delay models

