**EE241B Advanced Digital Integrated Circuits** **Spring 2018.**

**HOMEWORK 4.** **Due: Thursday, April 19, 2018. in class.**

**This is an individual assignment!**

**Problem 1. Stack forcing and multi-$V_{Th}$ design.**

a) What is the sensitivity in the energy-delay space of stack forcing technique, applied to every inverter in an optimally sized (for minimum delay) inverter chain of length of 6? The input capacitance is 1fF, and the initial leakage is 25% of the total energy dissipated by the inverters. You can assume that the Cd = Cg = 2fF/μ, and a linear delay model used in this class. $V_{DD}$ = 1V and the stack of 2 reduces the leakage by a factor of 10.

b) Repeat the part a), but instead of using the stack effect on the transistor with nominal $V_{Th}$ of 300mV, use the transistor with a higher threshold of 380mV that reduces the leakage by a factor of 10. You can use the simplest I-V model for delay calculation.

**Problem 2. Delay replicas.**

Your design has a critical path of 30 FO4 inverter delays at the nominal supply voltage. Your friend has suggested a design of a replica circuit consisting of *N* FO1 inverters.

a) Design the actual replica made of N-1 identical stages with $N^{th}$ stage having an increased fanout to match the actual critical path. What is the fanout of the $N^{th}$ stage?

b) There are three nearly identical critical paths in the circuit, one consisting of 20 FO4 inverters, one consisting of all NAND2s and one consisting of all NOR2s. Simulate tracking of the replica form part a) from the nominal down to 0.5V with 50mV steps.

c) How would you design the replica to accurately track these critical paths across the supply voltage range. Just draw it, no need to simulate.

**Problem 3. Power-performance tradeoffs.**

a) Using the alpha-power law model, derive the analytical expression for the energy/delay sensitivity of a design to scaling of supply voltage. Evaluate this expression at the nominal supply voltage, using the results from Homework 1 ($K$ = 0.001, α = 1.5, $V_{TH}$ = 0.45V, for NMOS)

b) What is the energy/delay sensitivity of a design to the logic depth? You can define the logic depth as a number of FO4 inverters that fit into one clock period.

**Problem 4. Subthreshold design.**

a) From the lecture notes, it appears that for a design operating in subthreshold, the minimum energy point of a design does not depend on the threshold voltage, and only depends on the supply. Can you explain why (very briefly)?

b) If it doesn't matter for the energy consumption, why is it important to control the transistor threshold voltage in subthreshold design?