EE241B Advanced Digital Integrated Circuits **Spring 2019.**

HOMEWORK 3. **Due: Friday, April 5, 2019.**

This is an individual assignment!

1. Extracting and simulating the synthesized design.

In the first lab, we have created a design by using a strictly digital ('VLSI') design flow. Then in the second lab, we extracted and simulated the synthesized design using custom design tools. Let's now analyze the design we have.

To do this, please work through the tutorial entitled: *Using VLSI Design Flow Outputs, Part 2*, then turn in:

a) For the path A[2] rise to Z[15] rise, report the delay measured by SPICE simulated without extracted parasitics and SPICE simulated with parasitics, and compare to the result from ICC in HW2.

b) For the functional testbench that counts from A=0000 to A=1111, report the power measured by the SPICE simulation and the mixed-signal simulation. Compare this to the result from Primetime in HW2.

c) Run the mixed-mode simulation at 1.05V, 0.8V, 0.6V, and 0.4V and measure the average power at each point. Then convert average power to energy/op in terms of J/op and uW/Mhz. Compare these results from the theoretically predicted active energy savings for voltage scaling based on the 1.05V result and discuss possible reasons for the discrepency (Hint: think about leakage). Note that you will need to increase the clock period of the simulation for lower supply voltages. Make a reasonable assumption: you can either run a simulation to find the FO4 at different voltages to scale appropriately, or use trial and error to set a clock period that still yields correct results in the simulation output.

d) Post an Innovus screenshot of your decoder with pins, as well as a code snippet of the edit_pins hook you wrote to achieve this through HAMMER.

2. Timing

A timing path with a single register driving a latch-based system is shown in Figure 1. R0 is a rising-edge triggered register, while R1, R2, and R3 are level sensitive. There are two 50% duty cycle clock phases available, with clkb offset from clk by half a period. Both registers and latches have zero hold time, and there is no clock skew in the system. Registers have t_{clk-Q} = 100 ps. Latches have $t_{clk-Q} = t_{D-Q} = t_{su}$ = 100 ps.

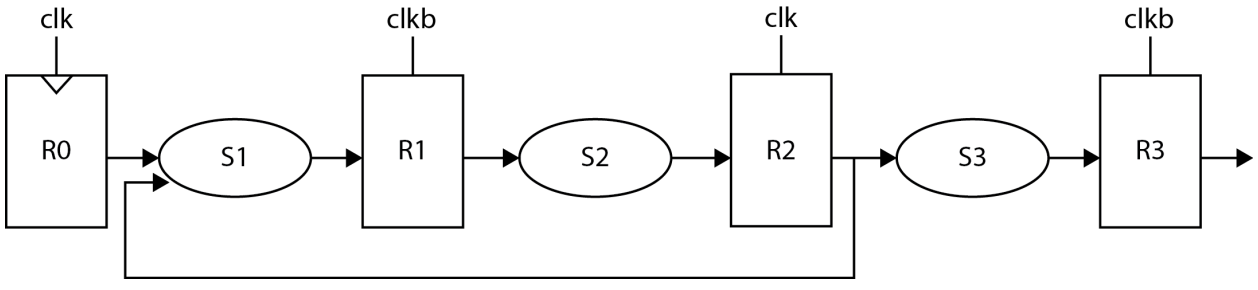

Figure 1.

a) The critical path of S1 is 400 ps, the critical path of S2 is 500 ps, and the critical path of S3 is 1.3 ns. Compute the minimum clock period.
b) Assume that we can model the on current with $I_{on} = K(V_{DD} - V_{thz})$, with K = 0.002, V_{DD} = 1 V, and V_{thz} = 0.25 V. There is a systematic variation on V_{thz}. What is the maximum value of V_{thz} that only leads to a 10% increase in delay?
c) The systematic variation of V_{thz} is normally distributed with σ = 0.03 V. What would be the yield in terms of timing if you are allowed a 10% margin on the clock period?

3. Flip-Flop

A flip-flop is shown in Figure 2.

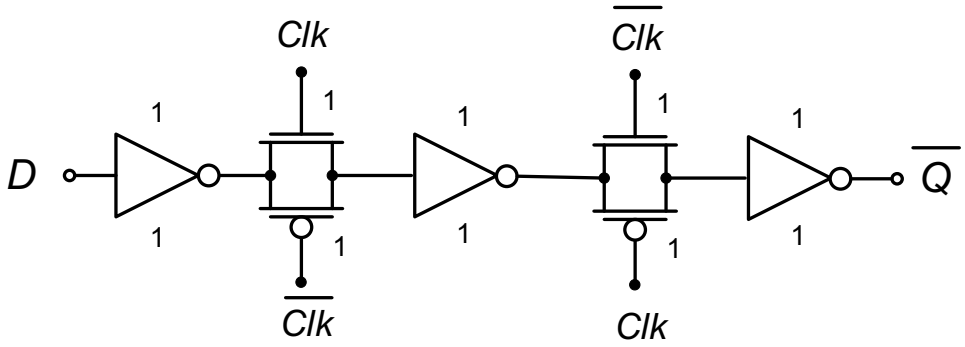

Figure 2.
In this process, a symmetrically-sized inverter has $W_p = W_n$, and a unit-sized transistor has gate and drain capacitances of 1fF and the on-resistance of 5kΩ. The resistance of a stack of two devices is 1.5x of the resistance of a single transistor with the same width. You can assume that the true and complementary clocks are ideal, and the logical effort of creating $\overline{Clk}$ from *Clk* is 1.

a) Is the flip-flop triggered by a rising or a falling edge of the *Clk*?
b) Calculate the $Clk - \overline{Q}$ delay for a 0→1 transition at the output and show your work.
c) Calculate the setup time for D = 1.