EE241B Advanced Digital Integrated Circuits **Spring 2019.**

HOMEWORK 2. **Due: Friday, March 8, 2019.**

This is an individual assignment!

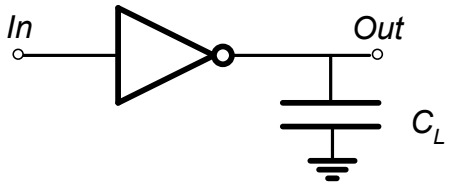
1. Extracting and simulating the synthesized design.

In the first lab, we have created a design by using a strictly digital ('VLSI') design flow. In this assignment, we will inspect the results of the static timing analysis.
To do this, please work through Lab 2, then turn in:

a) For the path A[2] rise to Z[15] rise, report the delay measured by IC Compiler.
b) A screenshot of the critical path highlighted in IC Compiler showing the wires that contribute to the path from a).
c) For the functional testbench that counts from A=0000 to A=1111, report the power measured by Primetime.
d) A screenshot of your decoder layout imported into Virtuoso after running it through the HAMMER flow.

2. Delays

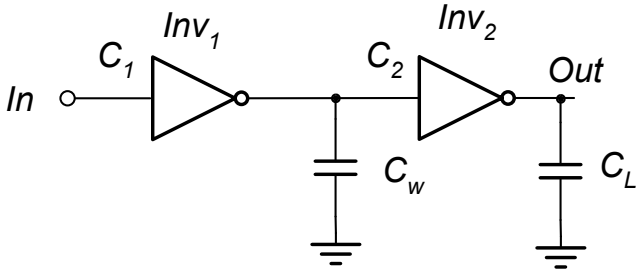
Consider an inverter driving a capacitive load in 28nm bulk-CMOS technology.



All transistors are minimum length and $W_n = 0.5\mu m$ $W_p = 1\mu m$, $V_{DD} = 1V$. In this technology, $C_g = C_d = 2fF/\mu m$, transistor thresholds are 0.25V and fanout-of-4 inverter delay is 15ps.

a) For what range of sizes of the load capacitor, C_L, adding another inverter to drive the load reduces the delay?

b) If the input capacitance of the first inverter in figure below is set to $C_1 = 3fF$, the wire capacitance C_w is 6fF, how would you size the second inverter that is driving 13.5fF load to minimize the overall delay from *In* to *Out*? Is this result intuitive?



3. Switching trajectories

In the IDS-VDS coordinates, plot simulated switching trajectories for the following transistors:

a) NMOS transistor in an inverter chain with a fanout of 1.
b) NMOS transistor in an inverter chain with a fanout of 4.
c) Top NMOS transistor in the 2-input NAND gate with a fanout of 3.
d) Bottom NMOS transistor in the 2-input NAND gate with a fanout of 3.