EE241B Advanced Digital Integrated Circuits **Spring 2018.**

HOMEWORK 2. **Due: Thursday, March 1, 2018.**

This is an individual assignment!

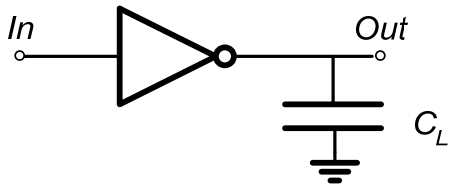
1. Extracting and simulating the synthesized design.

In the first lab, we have created a design by using a strictly digital ('VLSI') design flow. In this assignment, we will extract the synthesized and automatically placed and routed design to look under its hood. We will compare the results of dynamic simulation to the static timing analysis. To do this, please work through the tutorial entitled: Using VLSI Flow Outputs, then turn in:

a) For the path A[2] rise to Z[15] rise, report the delay measured by IC Compiler, SPICE simulated without extracted parasitics, and SPICE simulated with parasitics.
b) A screenshot of the critical path highlighted in IC Compiler showing the wires that contribute to the path from a).
c) For the functional testbench that counts from A=0000 to A=1111, report the power measured by Primetime, the SPICE simulation, and the mixed-signal simulation.
d) Run the mixed-mode simulation at 1.05V, 0.8V, 0.6V, and 0.4V and measure the average power at each point. Then convert average power to energy/op in terms of J/op and uW/Mhz. Compare these results from the theoretically predicted active energy savings for voltage scaling based on the 1.05V result and discuss possible reasons for the discrepency (Hint: think about leakage). Note that you will need to increase the clock period of the simulation for lower supply voltages. Make a reasonable assumption: you can either run a simulation to find the FO4 at different voltages to scale appropriately, or use trial and error to set a clock period that still yields correct results in the simulation output.

2. Delays

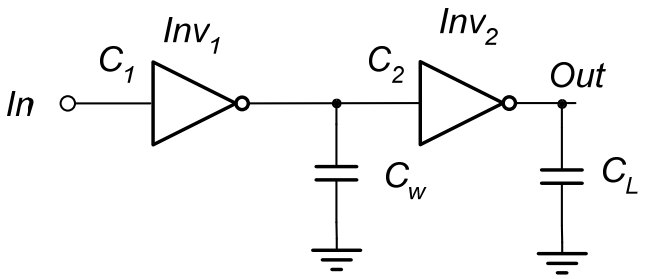
Consider an inverter driving a capacitive load in 28nm bulk-CMOS technology.



All transistors are minimum length and $W_n = 0.5\mu m$ $W_p = 1\mu m$, $V_{DD} = 1V$. In this technology, $C_g = C_d = 2fF/\mu m$, transistor thresholds are 0.25V and fanout-of-4 inverter delay is 15ps.

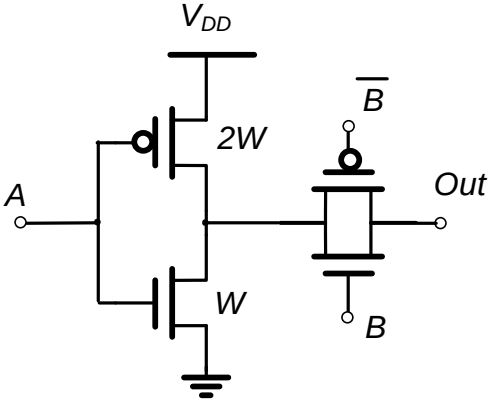
a) For what range of sizes of the load capacitor, C_L, adding another inverter to drive the load reduces the delay?

b) If the input capacitance of the first inverter in figure below is set to $C_1 = 3fF$, the wire capacitance C_w is 6fF, how would you size the second inverter that is driving 13.5fF load to minimize the overall delay from *In* to *Out*? Is this result intuitive?

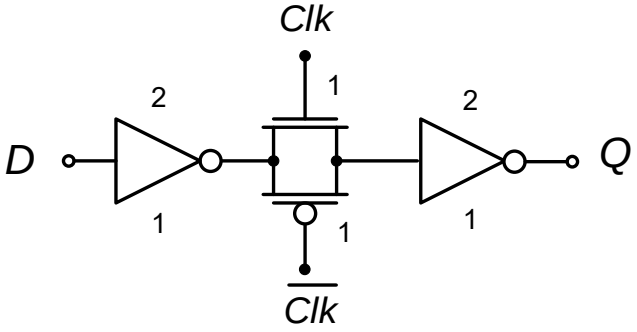


3. Flip-Flops

a) Calculate the logical effort for a transmission gate that consists of equally-sized NMOS and PMOS transistors, driven by a symmetrically-sized inverter, shown in figure. Assume that the equivalent resistance of the NMOS pulling up is twice that of it pulling down. Similarly, the equivalent resistance of the PMOS pulling down is twice that of it pulling up. Size the gate such that inputs A and B have the same logical efforts. $\overline{B}$ and B are perfectly complementary.

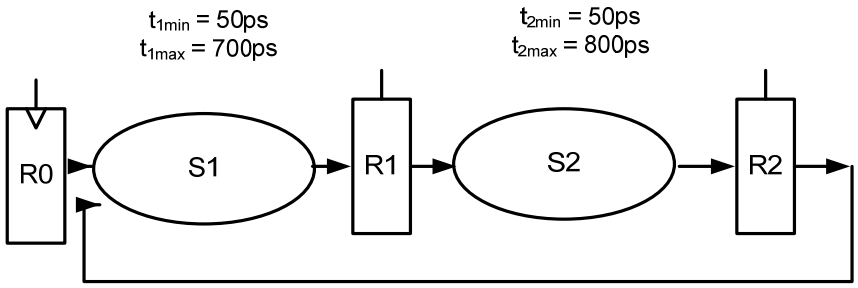


b) Find the setup time, hold time, and a clock-output delay, normalized to a fanout-of-4 inverter delay, of the latch in figure, driving a 2/1-sized inverter.



4. Timing

A logic path is shown in figure. Logic bubbles contain static logic with min and max delays.



a) If the registers R1 and R2 are positive edge triggered (t_{su} = 150ps t_h = 50ps, $t_{clk\text{-}Q}$ = 100ps), what is the minimum clock cycle that this system can operate at? Skew is zero.

b) If R1 and R2 are level –sensitive, label the clock phases so the system operates correctly.

c) What is the shortest clock cycle in a latch-based system ($t_{su} = t_h = t_{clk\text{-}Q} = t_{D\text{-}Q}$ = 100ps). Clock has a 50% duty cycle, and you can only use two phases for clocking. Skew is still zero.

d) Repeat c) with worst-case skew of 100ps.