How the voltage reference affects ADC performance, Part 1

By Bonnie Baker, *Senior Applications Engineer,*
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Introduction

When designing a mixed-signal system, many designers have a tendency to examine and optimize each component separately. This myopic approach can go only so far if the goal is to have a working design at the end of the day. Given the array of different components in a system, designers must have a complete understanding of not only the individual components but also their impact on the overall system performance. When a design has an analog-to-digital converter (ADC), it is critical to understand how this device interacts with the voltage reference and voltage-reference buffer.

This article is the first of a three-part series. Parts 2 and 3 will appear in future issues of the *Analog Applications Journal*. Part 1 looks at the fundamental operation of an ADC independently, exactly as many designers do, and then at the performance characteristics that have an impact on the accuracy and repeatability of the system. Part 2 will delve into the voltage-reference device, once again examining its fundamental operation and then the details of its impact on the performance of the ADC. Part 3 will investigate the impact of the voltage-reference buffer and the capacitors that follow it, and will discuss how to ensure that the amplifier is stable. Assumptions and conclusions will be compared to measurement results. The interplay between the driving amplifier, voltage reference, and converter will be briefly analyzed, followed by an investigation of the sources of error in the ADC's conversion results.

The fundamentals of ADCs

Figure 1 shows the voltage-reference system for the successive-approximation-register (SAR) ADC that will be examined in this three-part series. As the name suggests, the ADC converts an analog voltage to a digital code. The overall system accuracy and repeatability depend on how effectively the converter executes this process. The accuracy of this conversion can be defined with static specifications, and the repeatability with dynamic specifications. Generally, the ADC static specifications are offset-voltage error, gain error, and transition noise. The ADC dynamic specifications are signal-to-noise ratio (SNR), total harmonic distortion (THD), and spurious-free dynamic range (SFDR).

Static performance

Figure 2 shows an ideal and an actual (or non-ideal) transfer function of a 3-bit ADC. The actual transfer function has an offset-voltage error and a gain error. In the example application circuit, only the ADC gain error, transition noise, and SNR are of concern.

Figure 1. Voltage-reference system for SAR ADC

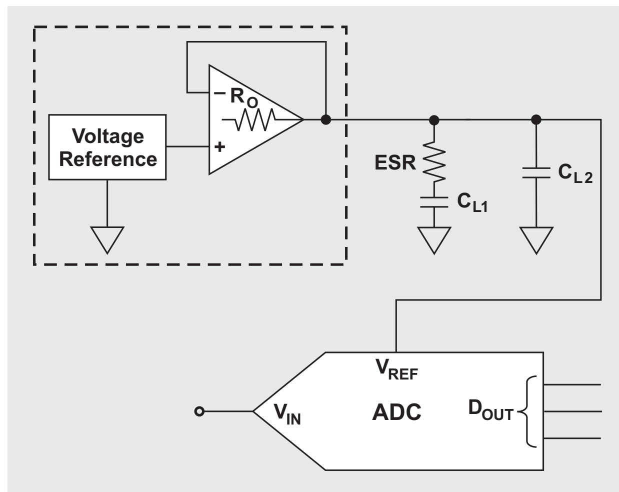


Figure 2. Ideal and actual ADC transfer functions with offset and gain errors

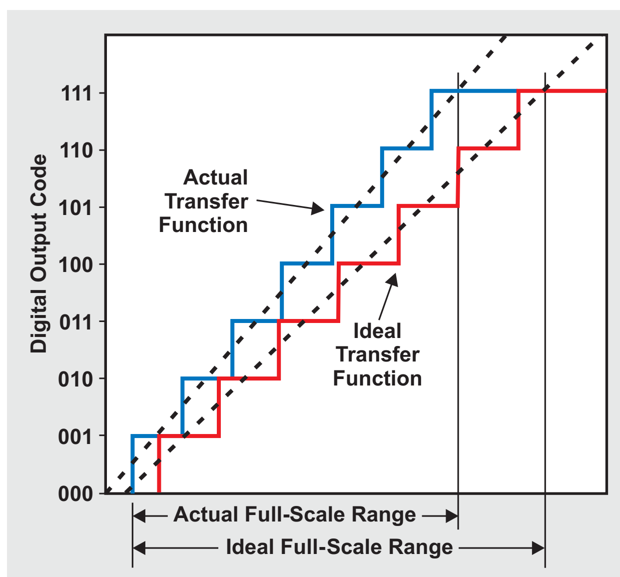
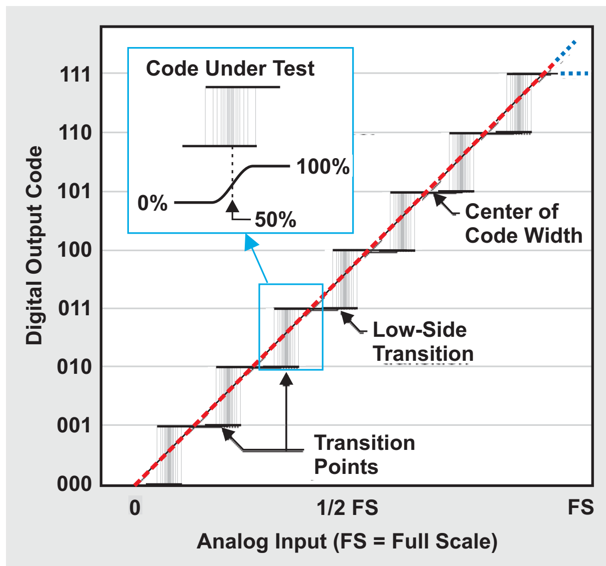


Figure 3. Transition noise with a 3-bit ADC



Equation 1 describes the typical transfer function of the ideal (error-free) ADC:

$$\text{Code} = V_{IN} \times \frac{2^n}{V_{REF}}, \qquad \textbf{(1)}$$

where "Code" is the ADC output code in decimal form, V_{IN} is the analog input voltage (in volts), n is the resolution of the ADC (or number of output-code bits), and V_{REF} is the analog value of the voltage reference (in volts). This equation demonstrates that the ADC output code is directly proportional to the analog input voltage and inversely proportional to the voltage reference. Equation 1 also shows that the output code depends on the number of bits (the converter resolution).

The DC errors of non-ideal ADCs are offset-voltage error and gain error. If the offset-voltage error is introduced into the transfer function, Equation 1 can be rewritten as

$$\text{Code} = \left(V_{IN} - V_{OS\_ADC}\right) \times \frac{2^n}{V_{REF}}, \qquad \textbf{(2)}$$

where V_{OS_ADC} is the input offset voltage of the ADC. Gain error is equal to the difference between the ideal slope from zero to full scale and the actual slope from zero to full scale. The notation for gain error is a decimal or percentage. If the impact of only the gain error (no offset-voltage error) on an ADC is considered, Equation 1 can be rewritten as

$$\text{Code} = V_{IN} \times \frac{2^n}{V_{REF}\left(1 - GE_{ADC}\right)}, \qquad \textbf{(3)}$$

where GE_{ADC} is the gain error in decimal form, expressed as

$$GE_{ADC} = \frac{\text{Actual Gain} - \text{Ideal Gain}}{\text{Actual Gain}}.$$

From Equation 3 it can be seen that the gain-error factor adds to the initial accuracy of V_{REF}. The output code is inversely proportional to the combination of the voltage reference plus the gain error. The DC error caused by noise from the voltage-reference chip inversely impacts the gain accuracy of the ADC. Part 2 of this series will specifically show the impact of the voltage reference's errors.

Equations 2 and 3 can be combined to show the final transfer function:

$$\text{Code} = \left(V_{IN} - V_{OS\_ADC}\right) \times \frac{2^n}{V_{REF}\left(1 - GE_{ADC}\right)} \qquad \textbf{(4)}$$

To analyze ADC transition noise, the code transition points in the ADC's transfer curve can be examined. These are the points where the digital output switches from one code to the next as a result of a changing analog input voltage. The transition point from code to code is not a single threshold but a small region of uncertainty. Figure 3 shows the uncertainty at these transitions that results from internal converter noise. The region of uncertainty is defined by measuring repetitive code transitions from code to code.

An ADC's transition noise has a direct effect on the signal-to-noise ratio (SNR) of the converter. Since it is important to understand this phenomenon, Part 2 of this series will look more closely at voltage-reference noise characteristics.

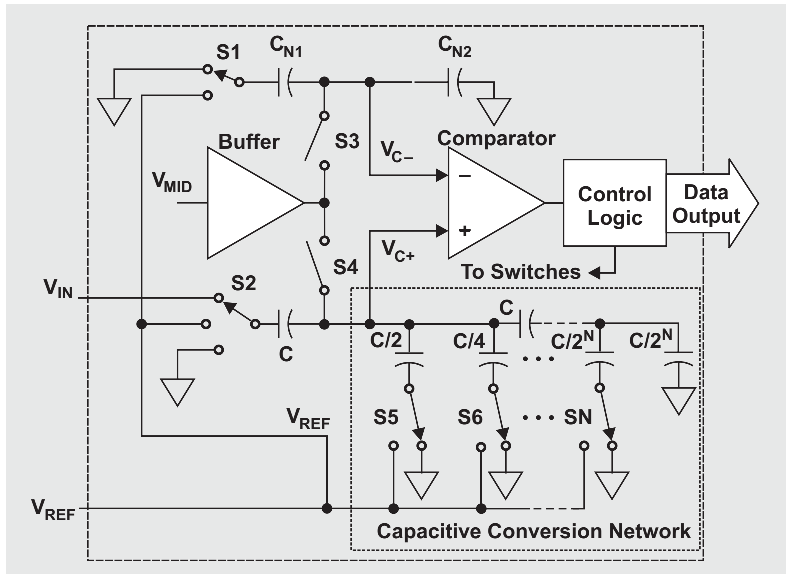
Dynamic performance

The total system noise from the circuit in Figure 1 is a combination of the inherent ADC noise, the noise from the analog input-buffer circuitry, and the reference input-voltage noise. Figure 4 shows a simplified internal circuit of a SAR ADC.

To determine the dynamic performance of an ADC, a fast Fourier transform (FFT) plot of the converter's output data can be used. An FFT plot can be calculated from a consistent clocked series of converter outputs. The FFT plot provides the SNR, the noise-floor level, and the spurious-free dynamic range (SFDR). In the example application circuit, only the SNR specification is of interest. Figure 5 provides an FFT plot of these specifications.

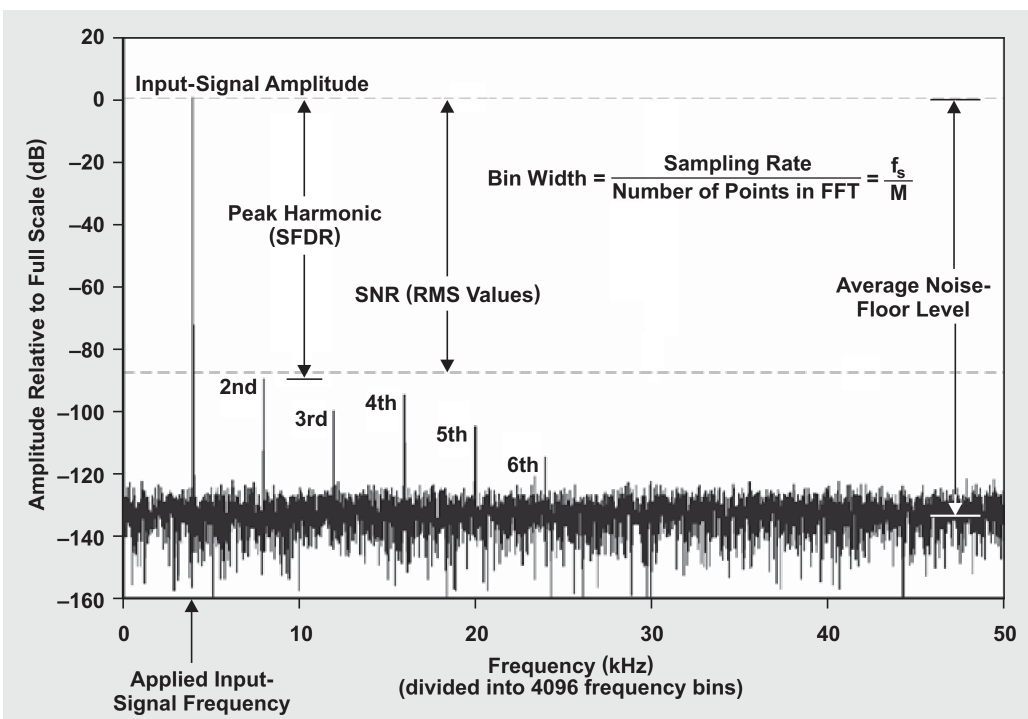
A useful way of determining noise in an ADC circuit is to examine the SNR (see Figure 5). The SNR is the ratio of the root mean square (RMS) of the signal power to the RMS of the noise power. The SNR of the FFT calculation is a combination of several noise sources, which may include the ADC quantization error and the ADC internal noise. Externally, the voltage reference and the reference driving amplifier contribute to the overall system noise. The theoretical limit of the SNR is equal to 6.02n + 1.76 dB, where n is the number of ADC bits.

Figure 4. Simplified topology of a SAR ADC



The total harmonic distortion (THD) quantifies the amount of distortion in the system. THD is the ratio of the root sum square (RSS) of the powers of the harmonic components (spurs) to the input-signal power. For example, in Figure 5, the harmonic components are labeled "2nd" through "6th." An RSS calculation is also known as the

Figure 5. FFT plot with 8192 data samples from a 16-bit converter



square root of the sum of the squares of several values. Spurs resulting from the nonlinearity of the ADC appear at whole-number multiples of the input signal's frequency (the fundamental frequency). Most manufacturers use the first six to nine harmonic components in their THD calculations.

If the ADC creates spikes in the FFT plot, it is probable that the converter has some integral nonlinearity errors. Additionally, spurs can come from the input signal through the signal source or from the reference driving amplifier. If the driving amplifier is the culprit, the amplifier may have crossover distortion; or it may be marginally stable, slew-rate-limited, bandwidth-limited, or unable to drive the ADC. Injected noise from other places in the circuit, such as digital-clock sources or the frequency of the mains, can also contribute spurs to the FFT result.

The combination of the converter's SNR and THD can be used to determine the signal to noise and distortion (SINAD) of the device. Many engineers refer to SINAD as "THD plus noise" or "total distortion." SINAD is an RSS calculation of the SNR and THD; i.e., it is the ratio of the fundamental input signal's RMS amplitude to the RMS sum of all other spectral components below half the sampling frequency (excluding DC). While the SAR converter's theoretical minimum for SINAD is equal to the ideal SNR, or 6.02n + 1.76 dB, the working SINAD is

$$\text{SINAD (dB)} = -20\log\sqrt{10^{-\text{SNR}/10} + 10^{\text{THD}/10}}. \quad \textbf{(5)}$$

SINAD is an important figure of merit because it provides the effective number of bits (ENOB) with a simple calculation:

$$\text{ENOB} = \frac{\text{SINAD} - 1.76\text{ dB}}{6.02} \quad \textbf{(6)}$$

In an FFT representation of converter data, the average noise floor (see Figure 5) is an RSS combination of all the bins within the FFT plot, excluding the input signal and signal harmonics. The number of samples versus the number of ADC bits can be chosen so that the noise floor is below any spurs of interest. With these considerations, the theoretical average FFT noise floor (in decibels) is

$$\text{FFT Noise Floor} = 6.02\text{n} + 10\ \log\left(\frac{3\text{M}}{\pi \times \text{ENBW}}\right),$$

where M is the number of data points in the FFT, and ENBW is the equivalent noise bandwidth of the FFT window function. A reasonable number of samples for the FFT of a 12-bit converter is 4096, which will result in a theoretical noise floor of –107 dB.

Conclusion

The ADC specifications that impact the application circuit in Figure 1 are gain error, transition noise, and SNR. Part 2 will examine the voltage reference's DC accuracy and noise contribution to the system performance.

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How the voltage reference affects ADC performance, Part 2

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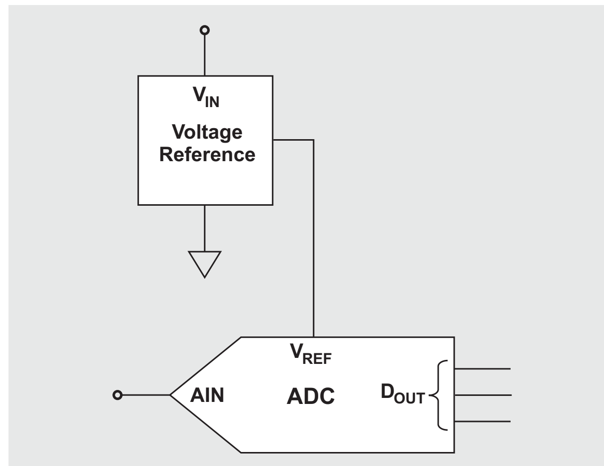
Introduction

This article is Part 2 of a three-part series that investigates the design and performance of a voltage-reference system for a successive-approximation register (SAR) analog-to-digital converter (ADC). A simplified version of this system is shown in Figure 1. When a design uses an ADC in this system, it is critical to understand the voltage-reference path to the converter. Part 1 (see Reference 1) examined the fundamental operation of an ADC independent of the voltage reference, and then analyzed the performance characteristics that have an impact on the accuracy and repeatability of the system. Part 2 looks at the key characteristics of the voltage-reference block in Figure 1 and the reference's possible impact on the ADC's performance. Part 2 also shows how to design an appropriate external reference for 8- to 14-bit ADCs. Part 3, which will appear in a future issue of the *Analog Applications Journal*, will investigate the impact of the voltage-reference buffer and the capacitors that follow it, discuss how to ensure that the amplifier is stable, and provide a reference design that is appropriate for ADCs with 16+ bits.

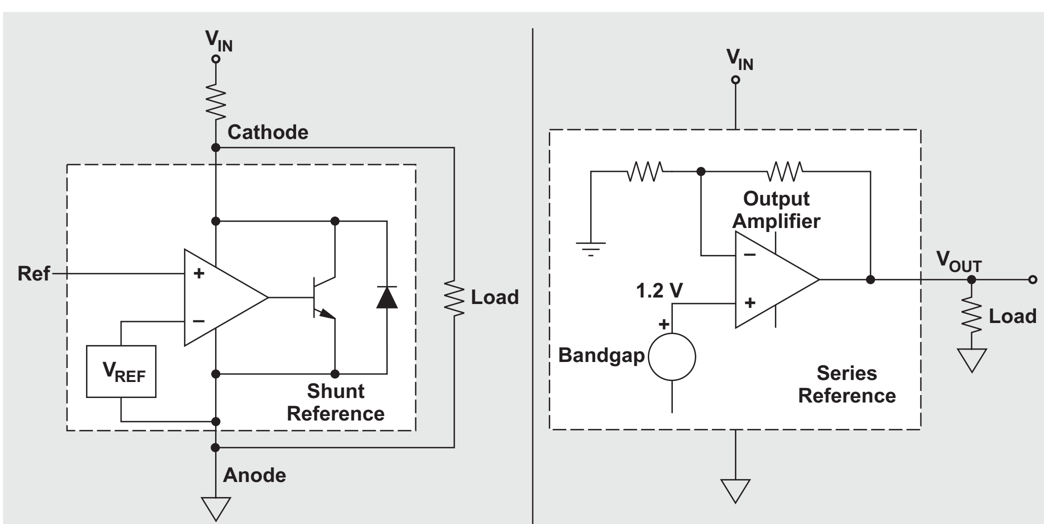
Figure 1. Voltage-reference system for SAR ADC



Choosing the correct V_{REF} topology

Voltage references are available in two-terminal shunt or three-terminal series configurations (see Figure 2). Figure 2a shows a two-terminal shunt voltage reference, in which the entire IC chip of the shunt reference operates in parallel to its load. With a shunt voltage reference, an input voltage is applied to the resistor that is connected to the cathode. The typical initial voltage accuracy of this device can be as low as 0.5% or range up to 5%, with a temperature coefficient of approximately 50 to 100 µV/°C. The shunt voltage reference can be used to create positive, negative, or floating reference voltages.

Figure 2. Voltage-reference configurations



(a) Two-terminal shunt

(b) Three-terminal series

The three-terminal series voltage reference (Figure 2b) operates in series with its load. An internal bandgap voltage, in combination with an internal amplifier, creates the output voltage of this reference. The series voltage reference produces an output voltage between the output and ground while providing the appropriate output current to the external load. As the load current increases or decreases, the series reference maintains the voltage at V_{OUT}.

The typical initial voltage accuracy of a series-reference device can be as low as 0.05% or range up to 0.5%, with temperature coefficients as low as 2.5 ppm/°C. Because of the series reference's superior initial output voltage and overtemperature performance, this type of device would be used to drive the reference pins of precision ADCs. Beyond 8 or 14 resolution bits, where the size of the least significant bit (LSB) is respectively 0.4% and 0.006%, an external series voltage reference ensures that the intended precision of the converter can be achieved.

Another common application for series voltage references is sensor conditioning. In particular, a series voltage reference is useful in bridge-sensor applications as well as applications that have thermocouples, thermopiles, and pH sensors.

The initial accuracy of the series voltage reference in an ADC application (as in Figure 1) provides the general reference for the conversion process. Any initial inaccuracy of the output voltage can be calibrated in hardware or software. Additionally, changes in the accuracy of the voltage-reference output can be a consequence of the temperature coefficient, the line regulation, the load regulation, or long-term drift. The series voltage reference provides better performance in all of these categories.

Figure 3. An ideal, 3-bit ADC transfer function

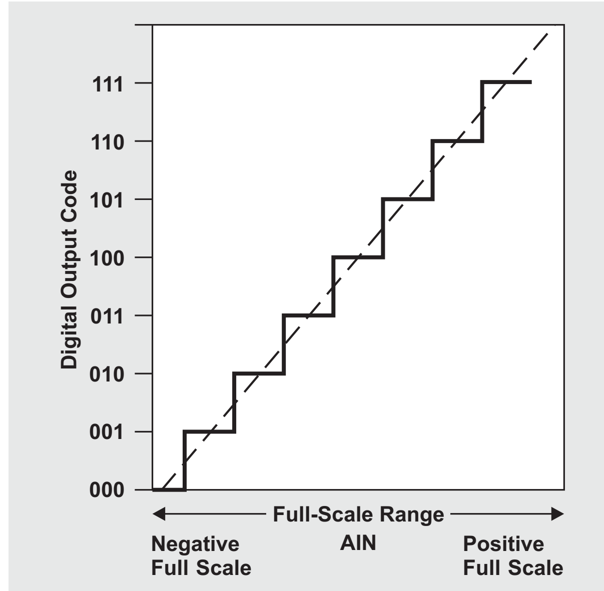
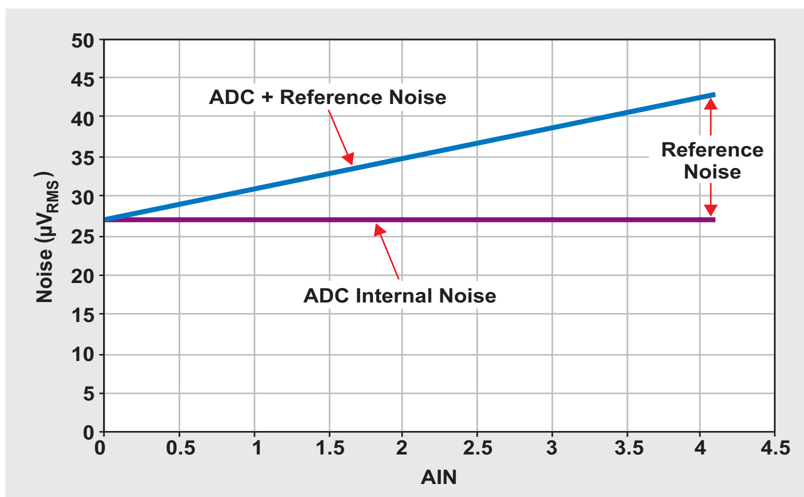


Figure 4. Total noise at ADC output as a function of ADC input voltage



Understanding reference-voltage noise

From Part 1 of this series it can be concluded that the ADC has only one function. That function is to compare an input voltage to a reference voltage, or to create an output code based on an input signal and reference voltage. Part 1 presented diagrams and formulas that describe the basic transfer function of the ADC along with the device's noise characteristics. The typical transfer function of an ideal ADC, shown here in Figure 3, was described as

$$\text{Code} = V_{IN} \times \frac{2^n}{V_{REF}}, \qquad (1)$$

where "Code" is the ADC output code in decimal form, V_{IN} is the analog input voltage to the ADC, n is the number of ADC output bits, and V_{REF} is the analog value of the reference voltage to the ADC. This formula shows that any initial error or noise in the reference voltage translates to a gain error in the code output of the ADC.

If several points from the ADC's negative full-scale input to its positive full-scale input are measured, it becomes clear that the contribution of the reference noise is a function of the ADC input voltage. To evaluate the voltage-reference noise as well as the overall noise, it is necessary to measure the noise close to both the negative full scale and the positive full scale. Figure 4 shows the results of measuring the reference noise and the ADC noise in a system. These results show that the overall noise is not constant but linearly dependent on the ADC's analog input voltage. When this type of system is designed, it is important to keep the reference noise lower than the ADC's internal noise.

Both reference topologies in Figure 2 generate comparable noise over frequency. The voltage noise in series voltage references comes mainly from the bandgap and the output amplifier. Both of these elements generate noise in the 1/f region and the broadband region (see Figure 5).

Noise in the voltage reference's 1/f region

In the data sheets of most series-reference devices, the specification for output-voltage noise is over the frequency range of 0.1 to 10 Hz, which encompasses the 1/f region in Figure 5. Noise in the 1/f region, often called "pink noise," is replaced in the higher frequency domain by the broadband noise.

Noise in the voltage reference's broadband region

Some manufacturers include specifications for the voltage reference's output noise density. This type of specification is usually for noise in the broadband region, such as the noise density at 10 kHz. Broadband noise, which is present over the higher wide-band frequencies, is also known as "white noise" or "thermal noise."

An added low-pass filter with an extremely low corner frequency will reduce the broadband noise at the output of the reference. This filter is designed with a capacitor, the equivalent series resistance (ESR) of the capacitor, and the open-loop output impedance of the reference output amplifier (see Figure 6).

Table 1 shows the noise measured from the Texas Instruments REF5040 for different frequency bandwidths as well as for different external-capacitor values and types. These measurements demonstrate that ceramic capacitors with a low ESR of about 0.1 Ω have a tendency to increase noise compared to tantalum capacitors with a standard ESR of about 1.5 Ω. This tendency is the result of stability problems and the gain peaking of the reference's output amplifier.

As mentioned earlier, the two sources of noise in the reference voltage are the internal output amplifier and the bandgap. The internal schematic of the REF5040 in Figure 7 shows that the TRIM pin provides direct access to the bandgap. An external capacitor can be added to the TRIM pin to create a low-pass filter. This filter provides a

Figure 5. Example voltage-noise regions in the frequency domain

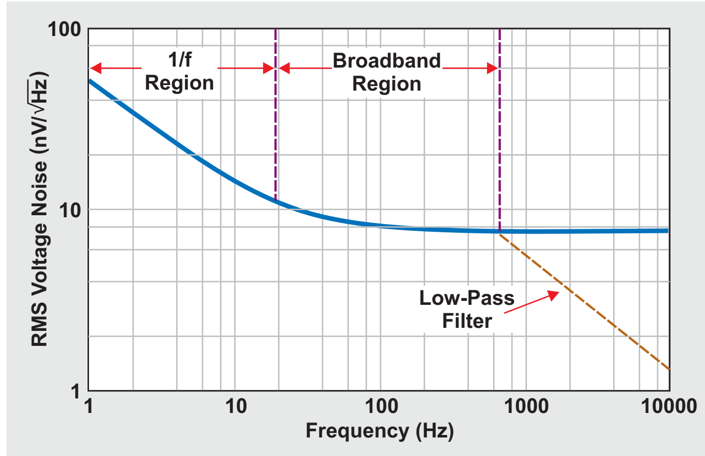


Figure 6. Low-pass filter between series voltage reference and ADC

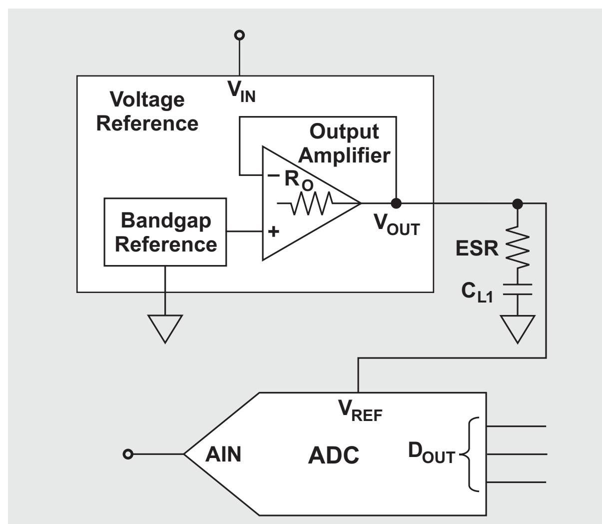


Figure 7. Using TRIM pin to filter REF5040 bandgap noise

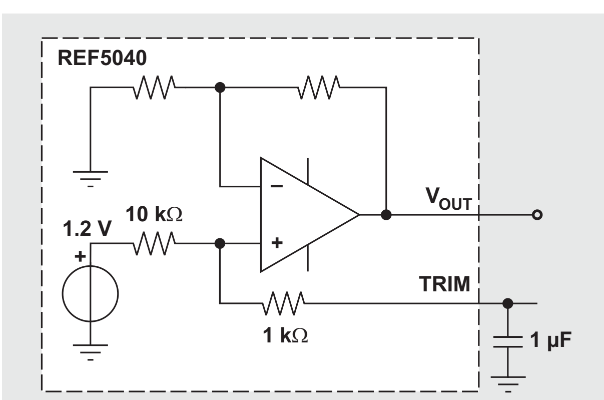


Table 1. Noise measured from REF5040 for different bandwidths and capacitor values and types

CAPACITOR	MEASURED NOISE (μV_{RMS}) FOR FOUR BANDWIDTHS			
	22 kHz (Low-Pass 5-Pole)	30 kHz (Low-Pass 3-Pole)	80 kHz (Low-Pass 3-Pole)	>500 kHz
GND	0.8	1	1.8	4.9
1 µF (tantalum)	37.8	41.7	53.7	9017
2.2 µF (ceramic)	41.7	46.2	55.1	60.8
10 µF (tantalum)	33.4	33.4	35.2	38.5
10 µF (ceramic)	37.1	37.2	37.8	39.1
20 µF (ceramic)	33.1	33.1	33.2	34.5
47 µF (tantalum)	23.2	23.8	24.1	26.5

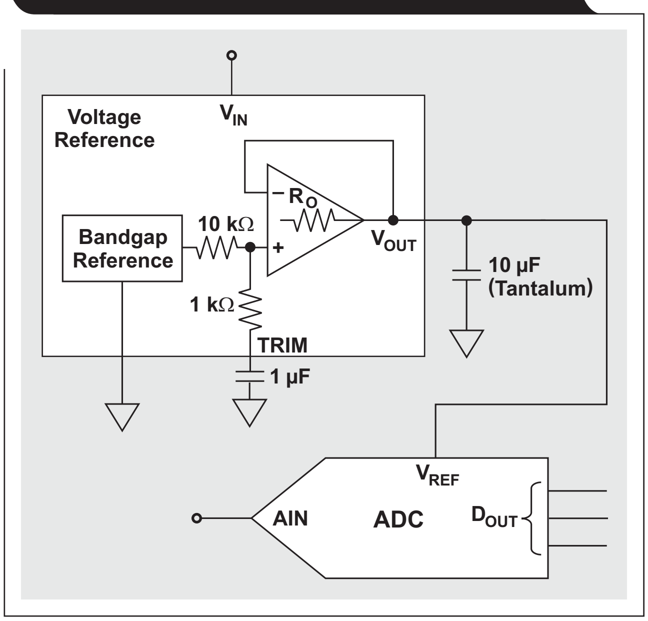
bandgap broadband attenuation of approximately –21 dB. For example, a small 1-µF capacitor adds a pole at 14.5 Hz and a zero at 160 Hz. If more filtering is needed, a larger-value capacitor can be used in place of the 1-µF capacitor. For instance, a 10-µF capacitor will generate a 3-dB corner frequency of 1.45 Hz. This low-pass filter will lower the bandgap noise. Attaching a 1-µF capacitor to the TRIM pin of the REF5040 will lower the total output RMS noise by a factor of 2.5.

Conclusion

Figure 8 shows a complete circuit diagram for a reference system configured with an 8- to 14-bit converter. The accuracy of the voltage reference in this system is important; however, any initial inaccuracy can be calibrated with hardware or software. On the other hand, eliminating or reducing reference noise will require a degree of characterization and hardware-filtering techniques. Part 3 of this article series will explore the proper filtering for the broadband region.

Part 3 will also investigate and explain how to design a reference circuit that is appropriate for converters with 16+ bits. The impact of the voltage-reference buffer and its following amplifier/resistor/capacitor network will be analyzed. With the measurements that follow the final system tuning, the assumptions and conclusions of this article series will be compared to the real world.

Figure 8. Voltage-reference circuit for 8- to 14-bit converters



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2. Bonnie Baker, "A Glossary of Analog-to-Digital Specifications and Performance Characteristics," Application Report	sbaa147
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How the voltage reference affects ADC performance, Part 3

By Bonnie Baker, *Senior Applications Engineer,*
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This article is Part 3 of a three-part series that investigates the design and performance of a voltage-reference system for a successive-approximation-register (SAR) analog-to-digital converter (ADC). Part 1 (see Reference 1) examined the ADC characteristics and specifications, with a particular interest in the gain error and signal-to-noise ratio, while assessing how the voltage reference impacts the ADC transfer function and DC accuracy. Part 2 (see Reference 2) examined the voltage-reference characteristics, focusing on how the voltage-reference noise produces the most error at the converter's full-scale range. Part 2 concluded by presenting a design for a voltage-reference circuit that is appropriate for 8- to 14-bit converters. This article, Part 3, tackles the challenge of designing a voltage-reference circuit that is appropriate for converters with 16+ bits. Part 3 examines methods of improving noise filtering and of compensating for losses caused by the improved filters.

Basics of reducing voltage-reference noise

As discussed in Part 2, the two sources of noise in the reference voltage are the internal output amplifier and the bandgap. The voltage-reference circuit from Part 2 that was configured with an 8- to 14-bit ADC can be used as a starting point to continue the discussion. The size of the least significant bit (LSB) of any converter in a 5-V system is equal to 5 V/2^N, where N is the number of converter bits. The 8-bit LSB size in this environment is 19.5 mV, and the 14-bit LSB size is 305 µV. The target value for voltage-reference noise should be less than these LSB values. The bandgap noise of the circuit from Part 2 was reduced by adding an external capacitor to the output to create a low-pass filter. This circuit's output noise can be further reduced by adding another capacitor as a passive low-pass filter. Figure 1 shows an example of such a design, which uses a voltage reference from the Texas Instruments (TI) REF50xx family. In this design, the 1-µF capacitor (C_1) provides a minimal 21-dB noise reduction at the internal bandgap reference. C_2, in combination with the open-loop output resistance (R_O) of the voltage reference's internal amplifier (see Reference 4), further reduces the output noise of the reference at the V_{REF_OUT} pin. In this case, the equivalent series resistance (ESR) of the 10-µF ceramic capacitor (C_2) is equal to 200 mΩ.

Figure 1. Voltage-reference design appropriate for 8- to 14-bit converter

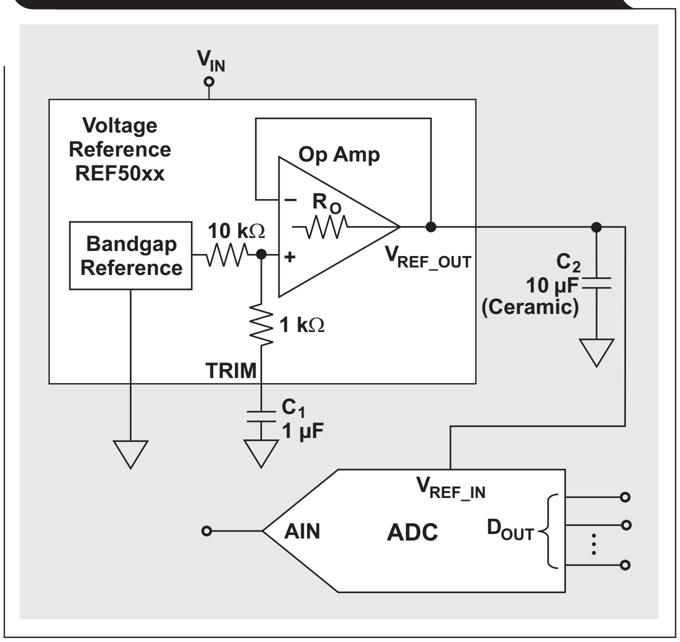


Figure 2 shows a fast-Fourier-transform (FFT) plot of the output signal of the circuit in Figure 1. Note that the output-noise level peaks at around 9 kHz because of the response of the circuit's internal amplifier to the capacitive load (C_2). This peaking is the main contributor to the overall measured noise. This output noise, measured with an analog meter over a frequency range of up to 80 kHz, is approximately 16.5 μV_{RMS}. If the voltage-reference circuit was connected to the input of an ADC, the measured noise across a 65-kHz frequency range would be 138 μV_{PP}. This noise level makes the solution in Figure 1 adequate for 8- to 14-bit converters.

Reducing voltage-reference noise for an ADC with 16+ bits

Since the voltage-reference circuit in Figure 1 would introduce too much noise into a converter with 16+ bits, another low-pass filter can be added to further reduce the reference's output noise. This filter consists of a 10-kΩ resistor (R_1) and an additional capacitor (C_3) as shown in Figure 3. The corner frequency of this added RC filter, 1.59 Hz, will reduce broadband noise as well as noise at extremely low frequencies.

Figure 2. FFT plot of V_{REF_OUT} signal of circuit in Figure 1

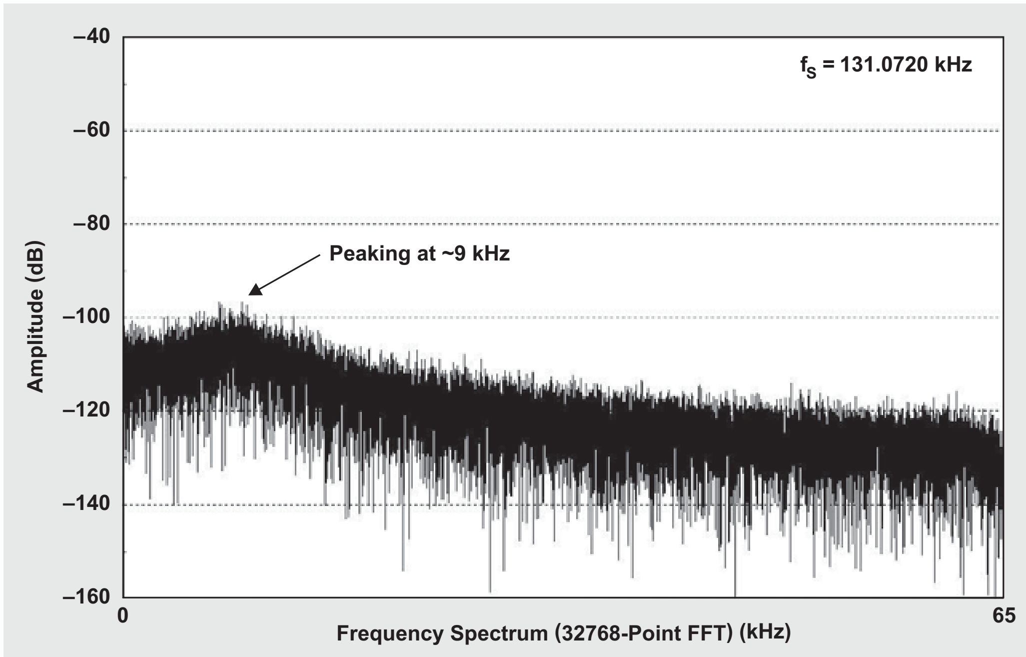


Figure 3. Voltage-reference circuit with R_1 and C_3 added as filters

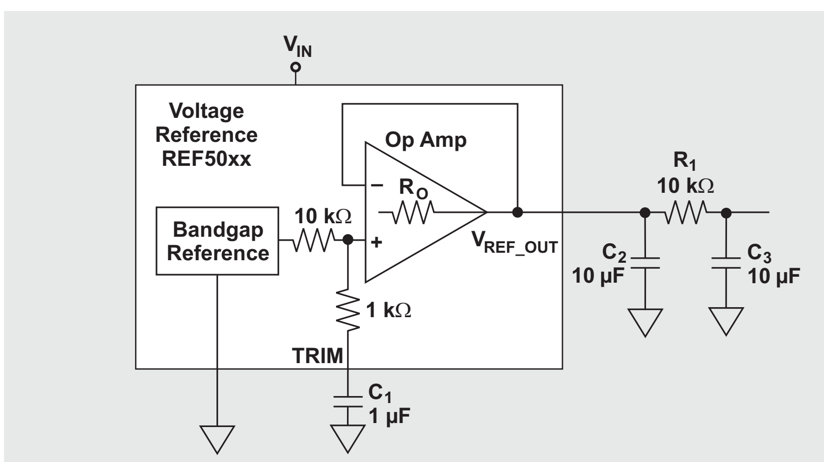


Figure 4. FFT plot of V_{REF_OUT} signal of circuit with RC filter added

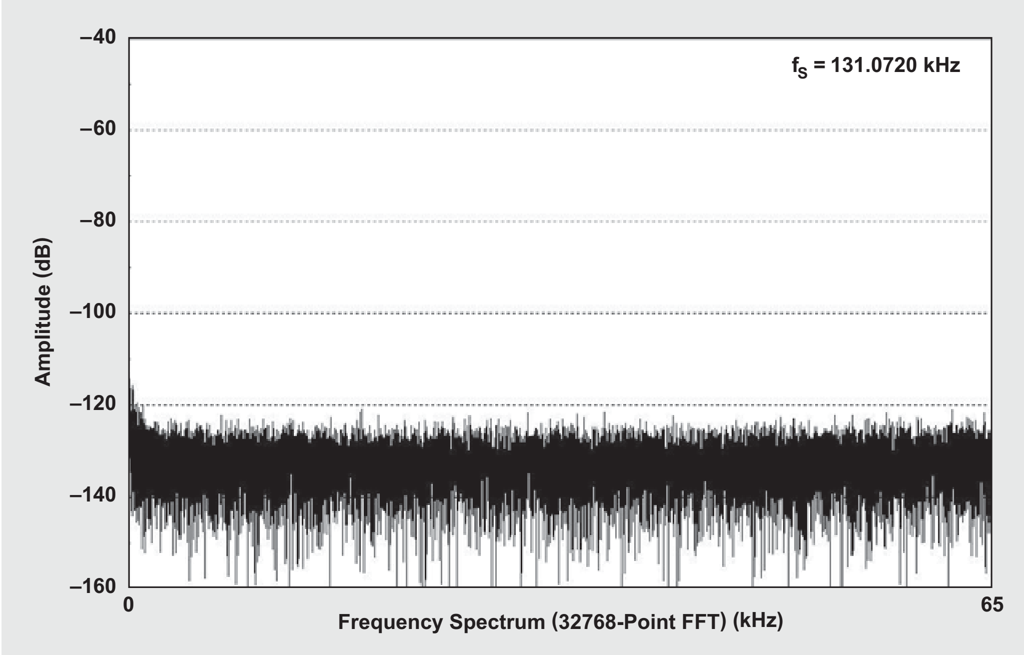


Figure 4 shows that the addition of R_1 and C_3 has a significant effect on the output noise for this system. The 9-kHz noise peak is gone. With this signal response, the output noise of the reference circuit in Figure 3 becomes 2.2 μV_{RMS} or 15 μV_{PP}, a reduction of nearly 90%. This improvement brings the noise level so well under control that the voltage-reference circuit is now appropriate for ADC resolutions of up to 20 bits.

This is encouraging; however, pulling current through R_1 from the ADC reference pin will corrupt the conversion by introducing a voltage drop equivalent to the average charge level from the reference pin of the ADC. Consequently, the output of this new circuit will not be able to adequately drive the ADC's voltage-reference input. To accomplish this, a buffer will need to be added to the low-pass filters.

Adding a buffer to the voltage-reference circuit

Figure 5 shows an example of the fluctuations in ADC reference drive current that can occur during a conversion. The signal was captured with a low-capacitance probe to show the voltage drop across the 10-kΩ resistor (R_1) between the input of the ADC voltage-reference pin and V_{REF_OUT}. The top trace in Figure 5 shows the trigger signal that the converter receives to initiate a new conversion. The ADC's voltage-reference circuit demands different amounts of current (bottom trace) for the initiation of the conversion and for each code decision. Therefore, the voltage-reference analog circuitry connected to the ADC must be able to accommodate these high-frequency fluctuations efficiently while maintaining a strong voltage reference for the converter.

Figure 5. Drive current required by ADC's reference input

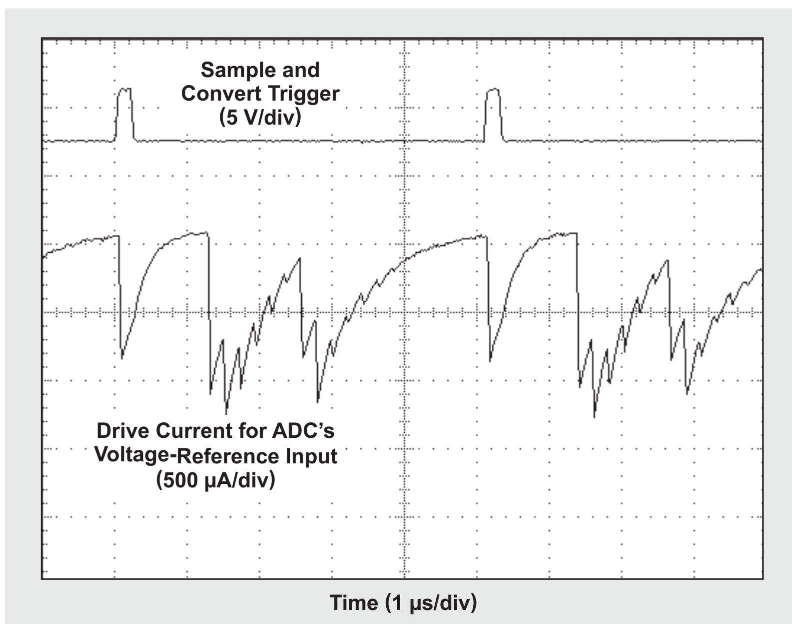


Figure 6. Voltage-reference circuit with added buffer and output filter

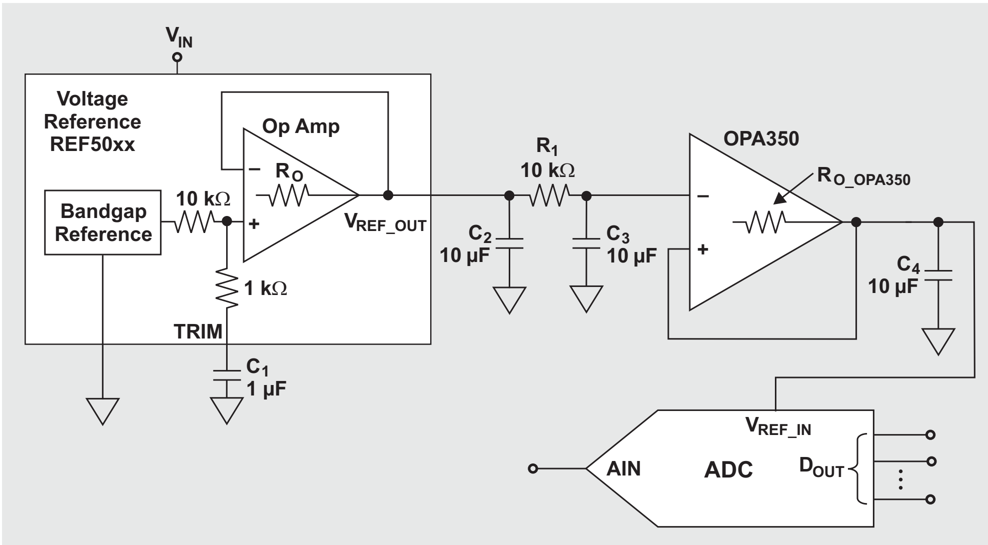


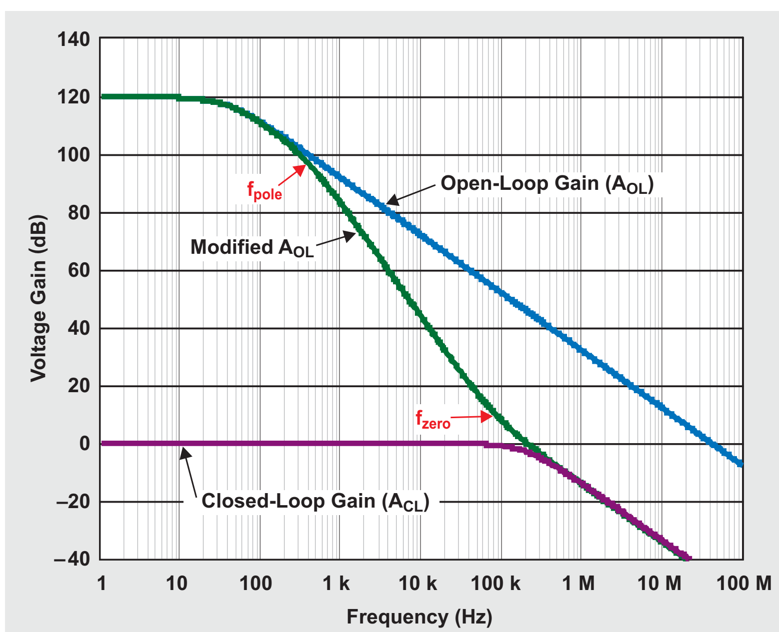
Figure 6 shows a voltage-reference circuit that will adequately drive a high-resolution ADC. In this circuit, the TI OPA350 is placed as a buffer after the low-pass filter that was constructed with R_1 and C_3 for the circuit in Figure 3. The OPA350 drives a 10-µF filter capacitor (C_4) and the voltage-reference input pin of the ADC. The noise measured at the output of the OPA350 in Figure 6 is 4.5 μV_{RMS} or 42 μV_{PP}. The input bias current of the OPA350 is 10 pA at 25°C. This current, in combination with the current through R_1, generates a 100-nV, constant-DC drop. Note that this voltage drop does not change with the ADC's bit decisions. It is true that the input bias current of the OPA350 changes over temperature, but a maximum current that is no more than 10 nA at 125°C can be expected. This value generates a change of 100 µV over a temperature range of 100°C.

It is useful to put the voltage drop across R_1 into perspective. This voltage drop is added to the errors contributed by the REF50xx and the OPA350. The initial error of the REF50xx output is ±0.05%, with an error over temperature of 3 ppm/°C. With a 4.096-V reference (REF5040), the initial reference error is equal to 2.05 mV at room temperature and an additional 1.23 mV at 125°C. Therefore, the reference output error is significantly larger than the errors produced by R_1 and variations in the OPA350's offset and input bias current.

Amplifier stability

There is a final word of caution about the circuit in Figure 6. The stability of the OPA350 can be compromised if C_4 and the OPA350's open-loop output resistance (R_{O_OPA350}) modify the open-loop voltage-gain (A_{OL}) curve to create a marginally stable state. To illustrate this phenomenon, Figure 7 shows how the output capacitor (C_4), with a 0.2-Ω ESR and the OPA350's open-loop output resistance (43 Ω), modifies the OPA350's A_{OL} curve. These curves can be used to quickly determine the stability of the circuit. A circuit with good stability would basically be one where the rate of closure of the operational amplifier's modified A_{OL} curve and closed-loop voltage-gain (A_{CL}) curve is

Figure 7. Frequency response of buffer with an RC load



20 dB/decade. This rule of thumb is presented in Reference 4. The open-loop output resistance of the OPA350 is 43 Ω, and the ESR of C_4 (R_{ESR_C4}) is 200 mΩ. The frequency locations of the pole and zero that are created by these values are

$$f_{pole} = \frac{1}{2 \times \pi \times (R_{O\_OPA350} + R_{ESR\_C4}) \times C_4} = 368 \text{ Hz and}$$

$$f_{zero} = \frac{1}{2 \times \pi \times R_{ESR\_C4} \times C_4} = 79.6 \text{ kHz.}$$

Per Figure 7, the circuit in Figure 6 is stable.

Thinking ahead

Unfortunately, the voltage-reference designs in this article can degrade ADC performance by adding unwanted temperature drift and initial gain error. Higher-performance systems with 21+ bits may require a voltage-reference design that addresses these issues. Future articles will explore a new approach with auto-zero amplifiers that will compensate for these errors.

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