A 200-GHz Triple-Push Oscillator in 65-nm CMOS with Design Techniques for Enhancing DC-to-RF Efficiency

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***Abstract* — In this paper, new design techniques for improving the DC-to-RF efficiency for sub-THz triple-push oscillators in CMOS technology is presented. We investigate the effect of the bias of transistors and the impedance seen by each transistor on the overall performance of triple-push CMOS oscillators in terms of DC-to-RF efficiency. By optimizing the harmonic generation and harmonic extraction in a triple-push oscillator fabricated in 65-nm CMOS, output power of −8.75 dBm is achieved at 200-GHz while 28.8-mW of DC power is consumed. This translates into a DC-to-RF efficiency of 0.46%.**

Index Terms —sub-THz, oscillator, CMOS, efficiency.

I. Introduction

Interesting and undiscovered properties of materials at terahertz (THz) band as well as unique characteristics of THz signals have led to the emergence of unique and significant applications in health, security and spectroscopy industry. Today, however, THz systems are realized using expensive and bulky devices such as gas lasers. If compact and on-chip THz systems are realized the numerous related applications will thrive. The bottleneck for design of on-chip THz systems is design of an integrated THz source.

Existing works on THz and sub-THz oscillators and synthesizers have focused on achieving higher frequency and higher output power [1-5]. For some applications, such as the newly proposed silicon waveguide chip-to-chip interconnect [6], power efficiency becomes a more important metric and the requirement on generating high output power can be relieved by the relatively low loss of the interconnect channel. Given the limited f_{max} of today's silicon technologies, N-push structures which extract the harmonics of oscillation have been used to achieve oscillation frequencies as high as (or higher than) f_{max} of the transistors [1].

In general there are two main challenges in the design of N-push oscillators: 1) harmonic generation, 2) harmonic extraction. In this paper, we propose design techniques for increasing efficiency of harmonic generation in the transistors through providing an optimum operating condition for them. At the same time, by tuning the impedance of the output combining networks with respect to the fundamental oscillation network, the extraction of the generated harmonics to the load is enhanced. Based on the proposed techniques, a triple-push 200-GHz oscillator prototype is designed and fabricated in a 65-nm CMOS technology. Based on the measurement results of the proof-of-concept prototype, the oscillator achieves −8.75-dBm output power while consuming 28.8-mW DC power. This translates to a DC-to-RF efficiency of 0.46%.

The paper is organized as follows: in Section II, the optimization of harmonic generation in a triple-push CMOS oscillator is discussed. Section III explains about optimized extraction of the generated harmonics from the transistors into the load. Section IV provides details about the implementation and is followed by measurement results of the fabricated prototype in Section V. Conclusions, performance summary and comparison to the state-of-the-art is provided in Section VI.

II. Harmonic Generation

Generally, in an N-push oscillator, harmonics are generated due to existence of circuit nonlinearities. In the case of MOS transistors, nonlinearities can be categorized into nonlinearity in the input and output terminals of the transistors, i.e. nonlinearity of drain current (i_D) versus gate-source voltage (v_{GS}) and nonlinearity of drain current versus drain-source voltage (v_{DS}). When MOS transistor is biased in saturation region, the i_D-v_{DS} nonlinearity is weaker in terms of generating harmonics as the drain current is almost independent of the v_{DS} voltage. Thus harmonic generation is a stronger function of i_D-v_{GS} nonlinearity which is almost always responsible for a large percentage of harmonic generation in an N-push CMOS oscillator.

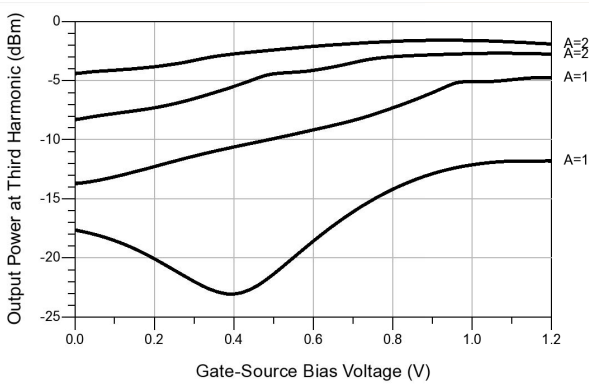


Fig. 1: The simulated dependency of third harmonic generation on gate-source voltage amplitude A (in Volt) and gate-source bias voltage.

When large signal oscillation is present, along with the oscillation amplitude, the bias point is also a defining parameter in the amount of harmonic generation in the circuit. As already reported in the context of multipliers in [7], if gate-source voltage is biased close to the threshold voltage such that given the oscillation amplitude at its gate, the transistor momentarily goes to the cut-off region, more harmonics can be generated comparing to the case that instantaneous gate-source voltage is always large than threshold voltage. Fig. 1 shows the dependency of harmonic generation to the gate-source bias as well as gate voltage drive amplitude for a single transistor at f_0 of 67-GHz when loaded by a fixed impedance in the 65-nm CMOS technology. As can be observed from this figure, for moderate gate-source voltage amplitudes, a larger gate-source bias results in significantly higher harmonic power generation in the transistor. However, if the gate-source voltage amplitude becomes large enough this dependency weakens. This is of particular importance as it

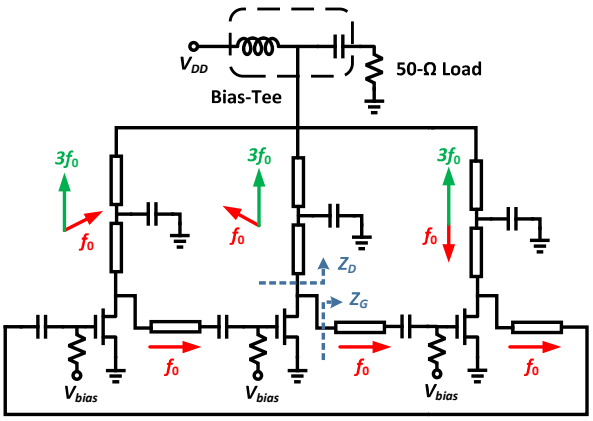


Fig. 2: Schematic of the proposed triple-push oscillator

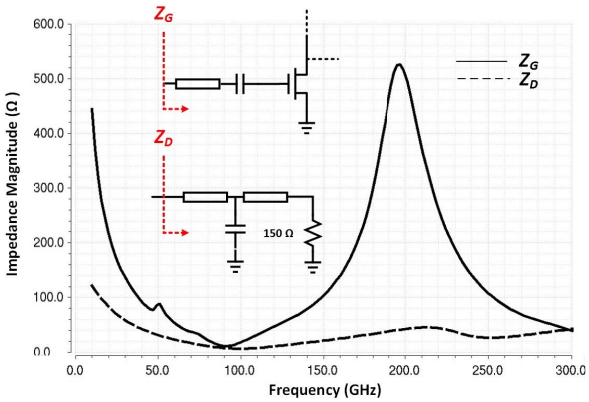


Fig. 3: Plot of magnitude of impedance looking into the drain (Z_D) and gate of the next transistor in the loop (Z_G).

suggests that if the gate-source voltage amplitude is large enough, the gate-source bias voltage can be lowered (i.e., lower DC power consumption) while almost the same amount of harmonic is generated out of transistors.

Thus in this design as shown in Fig. 2, we decouple the bias of transistors from V_{DD} by use of a series capacitor. Based on Fig. 1, we choose to work with gate-source bias voltage of about 0.7-V which for large enough gate-source voltage amplitudes results in the optimum efficiency in terms of harmonic generation.

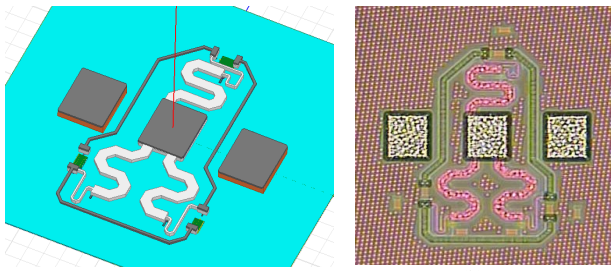
III. Harmonic Extraction

As mentioned in the introduction, the harmonics generated in an N-push oscillator need to be efficiently transferred to the load. This is a challenging task as, for example in the oscillators of Fig. 2, the third harmonic current generated by each transistor is divided between the drain network of that transistor and the network connected to the gate of the next transistor in the loop. Assuming the transistor as a current-source, in order to achieve the maximum extraction of the generated harmonics, the impedance of the drain network must be much smaller than the impedance that transistor sees looking into the gate of the next transistor in the loop. Another constraint is that for maximum power transfer at $3f_0$, each transistor should see the conjugate of its own output impedance. At the same time, to sustain the oscillation, the parallel combination of the drain network and the gate network, must meet the oscillation criteria (the necessary 120 degree phase shift) at the fundamental frequency.

TABLE I. PERFORMANCE SUMMARY AND COMPARISON

References	[1]	[2]	[3]	[4]	[5]	This Work
Extracted Harmonic	3rd	2nd	3rd	2nd	2nd	3rd
f_0 (GHz)	482/256	320/290	288	260	256	200
P_{out} (dBm)	−7.9/−17	−3.3/−1.2	−1.5	0.5*	4.1	−8.75
DC Power (mW)	61/71	339/325	275	800	227	28.8
Efficiency (%)	0.26/0.03	0.14/0.23	0.26	0.14	1.14	0.46
Technology	65nm/0.13µm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS

*Radiated power.



(a) (b)

Fig. 4. (a) The 3D model of the passive networks used for EM simulations. (b) Chip micrograph of the fabricated prototype.

To meet these three conditions, there is a need for more degrees of freedom in designing the gate and drain networks. Therefore, instead of a single inductor, a T-network is used in implementing the drain network. By proper choice of the inductors (implemented as transmission lines) and capacitors, the three conditions, i.e., 120° phase shift per section in the loop at fundamental frequency, conjugate matched impedance seen by each transistor and a drain network with significantly smaller impedance magnitude at the third harmonic, are simultaneously achieved.

Fig. 3 shows the plot of magnitude of impedance looking into the drain network (Z_D) and into the gate of the next transistor in the loop (Z_G). Here the loop is opened to obtain Z_G. It can be seen form the figure that by proper choice of the length of transmission line connected to the gate of transistor, the magnitude of Z_G is approximately ten times larger than that of Z_D at the third harmonic of 200 GHz.

IV. IMPLEMENTATION

Based on the approach described above, we have designed a triple-push 200-GHz oscillator (Fig. 2) in 65-nm CMOS technology with one top aluminum metal layer (AP) and six copper metal layers including one ultra-thick-metal (UTM) layer. All the inductors are implemented by microstrip transmission lines on either the UTM or the AP layer while a plane made out of M_1 and M_2 serves as the ground plane. For decoupling capacitors, Metal-Oxide-Metal (MoM) capacitors are custom

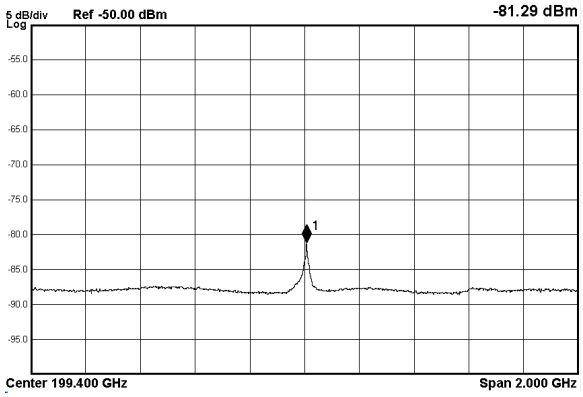


Fig. 5: The output spectrum of the oscillator.

designed. All the transmission lines and capacitors are electromagnetically simulated in Ansys HFSS (Fig. 4 (a)).

V. MEASUREMENT RESULTS

Fig. 4 (b) shows the chip micrograph of the fabricated prototype in 65-nm CMOS technology. The oscillator draws 24-mA from a 1.2-V supply. Two different approaches are used for measurement of the RF signal. In one setup, a WR-5 OML harmonic mixer (N9029AE05) is used in conjunction with a N9030A Agilent PXA to down-convert the output spectrum of the oscillator. In the second approach a Virginia Diodes Erickson PM4 power meter is used to measure the power generated by the oscillator given the assumption that all the output power is at $3f_0$.

Fig. 5 shows the output spectrum derived by the first measurement approach. As can be seen from this figure, the oscillation frequency of the oscillator is 199.4-GHz. Due to the inaccuracies of calibrating the loss of equipment and especially the conversion loss of the harmonic mixer, an Erickson PM4 power meter is used to accurately measure the output power of the oscillator. The best dc-to-RF efficiency of 0.46% is achieved for an output RF power of −8.75 dBm at 0.7-V bias for v_{GS}. Table. I summarizes the performance and compares the measurement results of this work with some of the best reported works in CMOS.

VI. Conclusion

In this paper, we have presented new design techniques for the optimum generation and extraction of harmonics in N-push oscillators for high efficiency signal generation at sub-millimeter-wave and THz frequencies. A 200-GHz oscillator with RF-to-DC efficiency of 0.46% is designed and fabricated in 65-nm CMOS technology as a proof of concept device.

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