A 100nW CMOS Wake-Up Receiver with -60dBm Sensitivity Using AlN High-*Q* Piezoelectric Resonators

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***Abstract* — In the paper, a new CMOS wake-up receiver is presented which is capable of detecting RF signals as weak as -60dBm while consuming only 100nW power. In order to achieve such sensitivity, a passive voltage-boosting network is incorporated into the design which increases the level of the signal that reaches to the input of the first block of the receiver, i.e. the CMOS rectifier. To enhance the effectiveness of the voltage-boosting technique, a high quality factor piezoelectric microelectromechanical transformer is utilized to implement the required inductor in the voltage-boosting network. The trade-offs in designing the voltage boosting network is explained and the optimum number of rectifier stages is derived. The output of the rectifier is applied to a low-power comparator which generates a pulse as the indicator for detection of the RF input signal. A proof-of-concept wake-up receiver is designed and laid-out in a 0.13µm CMOS process.**

Index Terms — CMOS, wake-up receiver, rectifier, voltage boosting.

I. Introduction

Wake-up receivers are essential parts of wireless sensor networks which are used for applications such as Internet of Things, ambient intelligence (AmI) and personal area networks (PANs) [1-4]. One of the most important challenges in design of wake-up receivers is to lower the power consumption to extend the battery life. While heavy duty-cycling is commonly used to lower the power consumption of the receiver, such a receiver suffers from limited functionality. CMOS rectifiers can be used in radio frequency (RF) wake-up receivers to convert the weak signal picked up by the antenna to a DC voltage that can be further processed by the subsequent blocks such as comparators which can flip a bit as an indicator for detection of the RF signal. However, the sensitivity of these rectifiers is limited and as the level of the input signal goes to µW or even nW range, it becomes more difficult to activate a CMOS rectifier stage. Conventionally, the interface between the antenna and the rectifier stage is a power matching network that maximizes the power that is transferred from the antenna to the rectifier. However, a power matching network may not generate the maximum possible voltage at the gate of the MOS transistors. This in turn significantly limits the minimum detectable power of the input RF signal. Alternatively, a passive voltage boosting network can be incorporated as the interface between the antenna and the CMOS rectifier circuit [5]. While this approach can improve the sensitivity of the CMOS rectifier, its effectiveness is strongly dependent on the quality factor of the passive components which are employed which is relatively low in most CMOS processes. To tackle this performance limiting factor, there is a need for high quality factor inductors. In this work, a high-Q piezoelectric resonators fabricated on an AlN MEMS process which can be integrated with CMOS process, is used to implement the inductor required in the voltage-boosting which improves the level signal which reaches to the input of the CMOS rectifier circuit.

In this paper, the application of voltage boosting network for increasing the sensitivity of the rectifier circuit is discussed in Section II. Section III is about the fabrication and modeling of piezoelectric resonators utilized to implement the inductor in the voltage boosting network. The trade-off between the voltage boosting and number of rectification stages is explained in Section IV. In Section V, the operation of the low-power comparator circuit is discussed. Section VI provides the simulation results of the prototype circuit laid-out in a 0.13um CMOS process. Conclusion and comparison with the state-of-the-art can be found in Section VII.

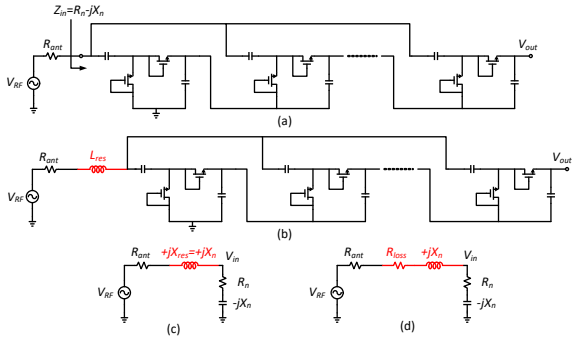

Fig. 1: (a) N-stage MOS rectifier connected to the antenna, (b) Incorporation of a series inductor as a voltage boosting network to increase the level of signal applied to the MOS rectifier, (c) series RLC circuit for voltage boosting, (d) inclusion of the loss of the series inductor

II. Voltage-Boosting

CMOS rectifiers are usually constructed using diode-connected MOS transistors as shown in Fig. 1 (a). The input impedance of this circuit is capacitive and can be shown by $Z_{in} = R_n - jX_n$ in which $R_n = R_1 \div n$, $X_n = n \times X_1$ and R_1 and X_1 are the resistance and reactance of each of the stages in an n-stage rectifier. An important limiting factor in performance of CMOS rectifiers is the large mismatch between the level of the impedance at their input and the impedance of the antenna (R_{ant}). Conventionally, the interface between the antenna and the rectifier stage is a power matching network that maximizes the power that is transferred from the antenna to the rectifier. If the rectifier is modeled by a parallel RC circuit, the parallel resistance value is given by $R_p = \frac{R_n^2+X_n^2}{R_n}$ which is usually significantly larger than 50Ω. This in turn makes it very difficult to implement a power matching network with finite-Q components. This in turn significantly limits the minimum detectable power of the input RF signal.

Alternatively, if we insert a single inductor as the voltage booting network between the antenna and the rectifier which resonates with the capacitive part of the input impedance of the rectifier, the magnitude of the phasor of current in the loop is maximized and therefore the voltage at the input of the rectifier is boosted. The equation for the phasor of voltage at the input of rectifier can be written as:

$$V_{in} = \frac{\sqrt{X_n^2+R_n^2}}{R_n+R_{ant}} V_{RF} \approx \frac{X_n}{R_n+R_{ant}} V_{RF}\,, \qquad (1)$$

From equation (1), the higher the value of the reactance of the input impedance of the rectifier comparing to ($R_n + R_{ant}$), the higher will be the voltage boosting that can be obtained. While this approach can improve the sensitivity of the CMOS rectifier, its effectiveness is strongly dependent on the quality factor of the passive components which are employed which is relatively low in most CMOS processes. Note that while a large value for X_n results in a large voltage boost factor, it also implies large impedance value for the series inductor. If the loss of the inductor is modeled by a series resistor, the equation for voltage boost factor can be revised to:

$$V_{in} \approx \frac{X_n}{R_n+R_{loss}+R_{ant}} V_{RF}\,, \qquad (2)$$

where $R_{loss} = \frac{X_n}{Q}$ and Q is the quality factor of the inductor. Given, the relatively large value of the reactance of the inductor (X_n), the value of R_{loss} can be comparable or larger than ($R_{rect} + R_{ant}$) and this in turn can significantly drop the voltage boost factor.

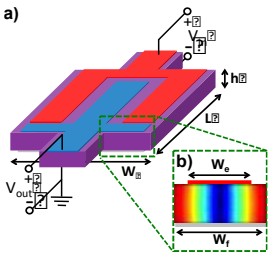

Fig. 2: a) 3D view of a 2-port piezoelectric laterally-vibrating MEMS resonator and b) cross section representation of one finger exhibiting a width-extensional mode of vibration

III. High-Q MEMS Resonator

MEMS resonators with high quality factors are good candidates to replace the series inductor needed for voltage boosting technique mentioned above considering that they can be integrated with CMOS electronics. The principle of operation of 2-port piezoelectric laterally-vibrating MEMS resonators has been described in literature [6], [7]. Essentially, the device is based on a piezoelectric plate sandwiched between two patterned metal layers that are employed to create an electric field across the thickness of the piezoelectric film (h). The top metal is formed by an array of interdigitated (IDT) electrodes that are alternatively connected to input (V_{in}) and output (V_{out}) ports while the bottom metal works as a common ground plate (Fig. 2 (a)).

The 2-port piezoelectric MEMS resonator vibrating in its width-extensional mode can be modeled as a one-degree-of-freedom system in the electrical domain. The equivalent stiffness, damping, and mass of each resonator finger are respectively represented by the motional capacitance (C_m), resistance (R_m), and inductance (L_m). This circuit is known as the modified Butterworth Van-Dike (mBVD) model as it also includes the parasitic capacitance that accounts for the dielectric polarization of the piezoelectric layer (C_0). Fig. 3 shows the electrical representation of a 2-port piezoelectric transducer with 2 input fingers (n_{in}=2) and 1 output finger (n_{out}=1), Replacing the inductor in Fig. 1 (b). In spite of the adverse effect of C_0 on the performance of the voltage boost circuit, the overall performance is significantly better comparing to the case that on-chip or off-chip inductors are used.

IV. Rectifier Circuit Design

As mentioned before, the voltage conversion gain of the rectifier can be increased linearly with increasing the number of stages (N) [5]:

$$V_{out,DC} = \frac{N.V_{in}^2}{2V_T} \qquad (3)$$

However, this comes at the price of increasing the input capacitance of the rectifier (C_n) as the additional stages can

be considered to be effectively in parallel. It can be shown that increasing the value C_n results in lowering of the voltage boost ($\frac{V_{in}}{V_{RF}}$) that can be obtained:

$$\frac{V_{in}}{V_{RF}} = \frac{1}{j\omega(C_0+C_n)(R_{ant}+R'_m)} V_{RF} \,. \quad (4)$$

By replacing (4) in (3), we get to the following equation for $V_{out,DC}$

$$V_{out,DC} = \frac{N.V_{RF}^2}{2\omega^2(R_{ant}+R'_m)^2(C_0+NC_1)^2} \,. \quad (5)$$

To find the optimum number of stages, we need to take the derivative of (5) and set it to zero:

$$\frac{\partial V_{out,DC}}{\partial N} = 0 \Rightarrow \frac{1}{(C_0+NC_1)^2} - \frac{2NC_1}{(C_0+NC_1)^3} = 0 \,. \quad (6)$$

Which results in optimum N given by

$$N_{opt} = \frac{C_0}{C_1} \,. \quad (7)$$

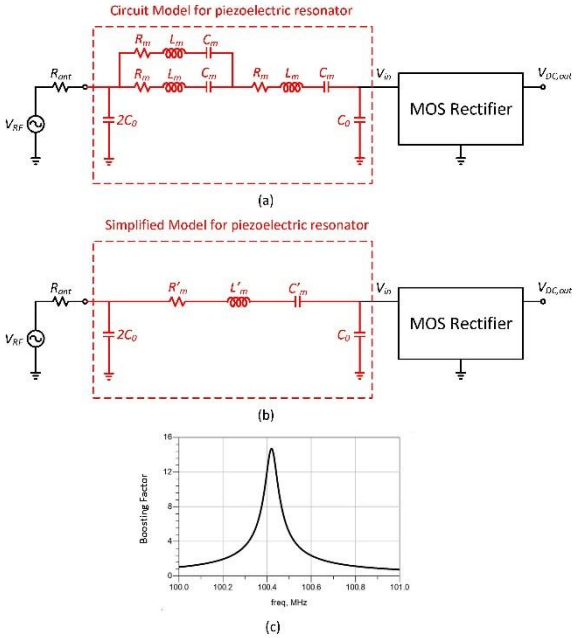

Fig. 3: (a) The circuit model for the piezoelectric resonators as a high-Q series inductor, (b) a simplified model for the piezoelectric resonators, (c) typical voltage boosting factor versus frequency.

V. Low-Power Comparator

A nano-watt comparator using a StrongARM latch [8] (Fig. 4) has been designed to sense the DC signal at the output of the rectifier. The performance of this comparator is based on the fact that the positive-feedback in the cross-coupled PMOS transistors of the StrongARM latch shown in Fig. 5 have ideally infinite gain overtime. Logical decisions, barring any imperfection, are influenced by the difference between the inputs by changing the impedance in the differential structure of the latch (Fig. 5). This circuit looks for slopes that are steeper than the responding reference slope of the integrator. If the signal is slower or no signal is applied then the resulting output oscillates closer in frequency to that of the clock due to noise. The latch resets both outputs high when clock is low; so the outputs are connected through a set of an inverters to an SR-Latch to hold the current decision of the comparator value during rest. The SR-Latch result is passed into a level-shifter; which is used to generate both positive and negative voltage. The level-shifter is loaded with a capacitor to make an integrator in negative feedback to minimize the offset of the StrongARM latch due to mismatch (Fig. 4).

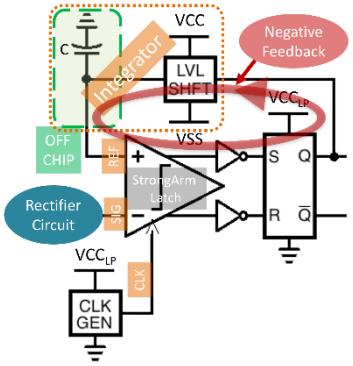

Fig. 4: The block diagram of the low-power comparator including the StrongARM latch, SR latch, level shifter and integrator.

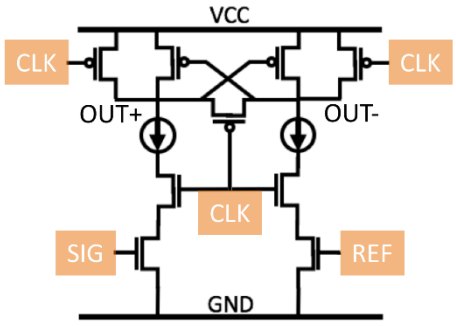

Fig. 5: Schematic view of StrongARM latch used in this work. The current mirrors are used to limit sort-circuit current when sampling

The use of an integrator in the negative feedback path feeds the average of the decisions to one of the inputs and pushes the choice of the comparator to have a 50-50% chance of choosing a zero or one. In other words, this setup can detect changes in signal such that the frequency of the signal is bounded in the range $I/(2\pi CA) < f_{SIG} < f_{CLK}/2$, where I/C is the slope of the voltage on the integrator capacitor found from slamming input, and A the amplitude of received sinusoid signal.

In case that a DC signal (output of the rectifier) is applied to the comparator, the criteria on the frequency of input signal can be translated into the slope of the rising exponential. If the slope is higher than a limit, then the integrator catches the variations in the input signal and the comparator generates a high signal at the output. Eventually as the DC signal reaches a steady-state value, the slope of its variation goes below the minimum slope required by the comparator and thus the output signal goes back to a 50-50% chance of being zero or one. If the signal at the output of the comparator is low-pass filtered, a pulse which is an indicator for detection of RF signal can be obtained.

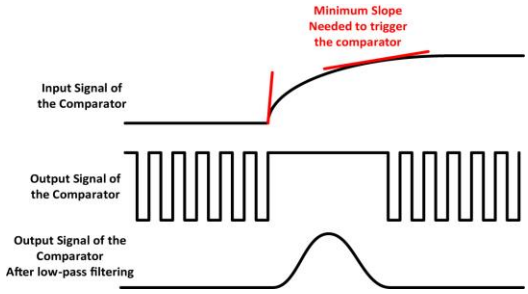

Fig. 6: Schematic view of StrongARM latch used in this work. The current mirrors are used to limit sort-circuit current when sampling

A low-power voltage-boosted wake-up receiver is designed and laid-out in a 0.13µm CMOS process using the technique explained above. A piezoelectric transformer with Q of 500 was designed in an AlN process that can be integrated with the CMOS circuits at the wafer level. The equivalent circuit model of Fig. 3 (a) with parameters $R_m = 640\Omega$, $C_m = 5fF$, $L_m = 490\mu H$ and $C_0 = 430fF$ is used to find the optimum number of stages for the rectifier circuit which leads to an optimum number of stages of $N_{opt} = 8$. Fig. 7 shows the simulation result for the output signal of the rectifier. As it can be observed from this figure, the initial slope of the output signal of the rectifier is larger than

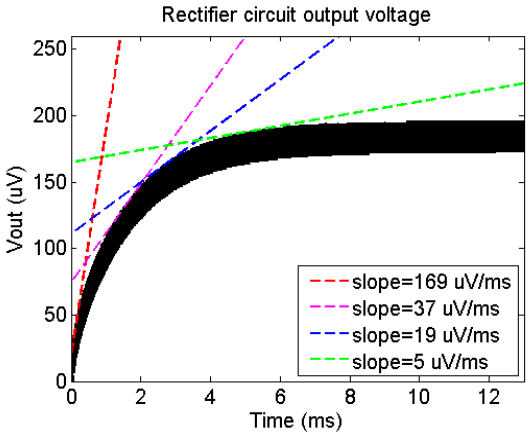

Fig. 7: The output voltage of the CMOS rectifier.

TABLE I. PERFORMANCE SUMMARY AND COMPARISON

References	[1]	[2]	[3]	[4]	This Work
Freq. (GHz)	0.9	0.08	2	1.9	0.1
Power (µW)	16.4	45	52	65	0.1*
Supply (V)	0.5	0.7	0.5	0.5	1
Technology	130nm	180nm	90nm	90nm	130nm

*Simulated power.

45µV/ms which is the minimum slope needed to trigger the comparator circuit.

VI. CONCLUSION

A novel architecture for low-power wake-up receivers is presented. Table. I compares the post-layout simulation results of the proof-of-concept prototype circuit with some of the reported low-power wake-up receivers in the literature.

REFERENCES

[1] S. Moazzeni, M. Sawan, and G. E. R. Cowan, "An ultra-low-power energy-efficient dual-mode wake-up receiver," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 2, pp. 517–526, Feb 2015.

[2] J. Bae and H. J. Yoo, "A 45 µw injection-locked fsk wake-up receiver for crystal-less wireless body-area-network," in *2012 IEEE Asian Solid State Circuits Conference (A-SSCC)*, Nov 2012, pp.333–336.

[3] N. M. Pletcher, S. Gambini, and J. Rabaey, "A 52 µw wake-up receiver with - 72 dbm sensitivity using an uncertain-if architecture," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 1, pp. 269–280, Jan 2009.

[4] N. Pletcher, S. Gambini, and J. Rabaey, "A 65 µw, 1.9 GHz RF to digital baseband wakeup receiver for wireless sensor nodes," in *2007 IEEE Custom Integrated Circuits Conference*, Sept 2007, pp. 539–542.

[5] S. Oh, and D. D. Wentzloff, "A -32dBm Sensitivity RF Power Harvester in 130nm CMOS," in *Proceeding of IEEE Radio Frequency Integrated Circuits Symposium*, pp. 483-486, June 2012.

[6] G. Piazza, "One and two port piezoelectric higher order contour-mode MEMS resonators for mechanical signal processing," *Solid-State Electron.*, pp. 1596–1608, 2007.

[7] M. Rinaldi, C. Zuniga, C. Zuo, and G. Piazza, "Super-high-frequency two-port AlN contour-mode resonators for RF applications," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 57, no. 1, pp. 38–45, Jan. 2010.

[8] B. Razavi, "The strongarm latch [a circuit for all seasons]," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 12–17, Spring 2015.