High Energy-Efficiency High Bandwidth-Density Sub-THz Interconnect for the Last-Centimeter Chip-to-Chip Communications

Bo Yu, Yu Ye, Xuan Ding, Xiaoguang "Leo" Liu, Jane Gu

Abstract — This paper presents a high energy-efficiency high bandwidth-density dielectric waveguide based sub-THz interconnect, including a near-field coupled low-loss, wide-bandwidth sub-THz channel and a high energy-efficiency transceiver. The channel loss is 4.0 dB with 59 GHz 3-dB bandwidth. The transmitter output power is -1.7 dBm with 6.7 mW of DC power consumption, and the receiver DC power consumption is 7.5 mW. The energy efficiency is 2.8 pJ/b, and the bandwidth density is 33.3 Gbps/mm^2.

***Index Terms* — Channel, communication, interconnect, micromachined, sub-THz, sub-THz interconnect, THz.**

I. Introduction

As rapid growth of demands of scientific workloads and commercial applications, the I/O bandwidth requirement increases with the rate about twice per two years [1]. However the I/O pin number increases slowly due to physical limitations, such as pad size, cross talk issue. Besides, the energy efficiency needs to be improved with the similar rate of data increasing to sustain sustainability. Therefore, to ultimately solve the problem of intra-/inter- chip interconnect, which is called last centimeter dilemma [2], both bandwidth density and energy efficiency should be boosted.

Some works have already been published to achieve high energy efficiency. They are majorly based on electrical [3]–[6] and optical interconnect [7]. Electrical schemes are compatible with existing planar silicon processes. However, it has limited bandwidth and large loss at high frequencies in both wired and wireless methods. For optical schemes, the fiber provides high bandwidth and low loss. However, they face the challenges to be integrated with planar CMOS processes. To fill the interconnect gap with sub-THz/THz interconnect illustrated in Fig. 1 holds high potentials by leveraging advantages of both optical and electrical interconnect approaches: low loss quasi-optical channels as well as advanced high speed semiconductor devices. Also a figure-of-merit (FoM) is introduced as energy efficiency multiplying the cross section area of the channel to quantify to interconnect performance.

As the first investigation of a waveguide based sub-THz interconnect system, this paper presents a high energy-efficiency and high bandwidth-density interconnect, which includes a near-field coupled low-loss, wide-bandwidth dielectric waveguide (DWG) based sub-THz channel and a high energy-efficiency transceiver in a 65nm CMOS technology. The energy efficiency of 2.8 pJ/b, the bandwidth density of 33.3 Gbps/mm^2 and a FoM of 0.4 pJ/bit·mm^2 are achieved.

II. Design of Sub-THz Interconnect

The top block diagram of the DWG based sub-THz interconnect is shown in Fig. 2. It consists of an oscillator, a switch based modulator, a DWG based sub-THz channel, and an envelope detector (ED) based demodulator to generate

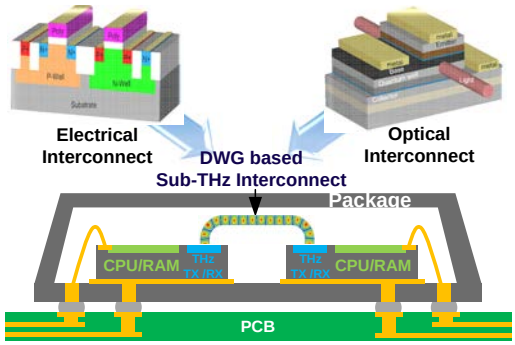

Fig. 1. Proposed sub-THz interconnect by leveraging the advantages of optical interconnect and electrical interconnect advantages.

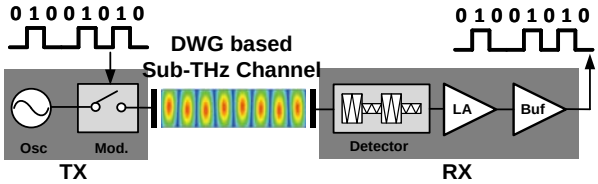

Fig. 2. Top block diagram of the DWG based sub-THz interconnect.

binary signals for the following digital signal processing. To driver the off-chip 50-Ω loads, a limiting amplifier (LA) and an output buffer are utilized. Thanks to the low-loss channel, the power amplifier is removed from this architecture to boost the energy efficiency. Input data generated from a Pseudo Random Bit Sequence (PRBS) generator is modulated by using an on-off keying (OOK) modulator.

To enable high energy-efficiency and high bandwidth-density communication, the key component is the low-loss and high bandwidth-density channel. A near-field coupling structure based channel [8] is employed. The complete channel structure is illustrated in Fig. 3(a). It includes a straight DWG channel, two microstrip lines (MSLs), and two back-to-back MSL-to-DWG transitions. Each transition consists of a tapered DWG and a tapered MSL, which overlaps with each other. With the taper-shape transition, the electromagnetic (EM) waves is transitioned smoothly since the EM mode is gradually changed from the quasi-TEM in the MSL to the hybrid mode in the transition and then to the E_{y11} mode in the DWG. The 50-Ω MSL is designed on a 100-μm thick quartz substrate with the metal width of 218 μm. The magnitude of the E-Field distribution is drawn in Fig. 3(b). The simulated insertion loss, which is plotted in Fig. 3(c), is 0.7 dB with bandwidth of 107 GHz for a 10 mm DWG with back-to-back transitions.

To achieve the high energy efficiency for sub-THz/THz interconnect, an ultra-high efficiency transmitter with passive modulation scheme is presented. Fig. 4 shows the schematic of the transmitter, which consists of a transformer based fundamental signal generator and a single-pole and single-

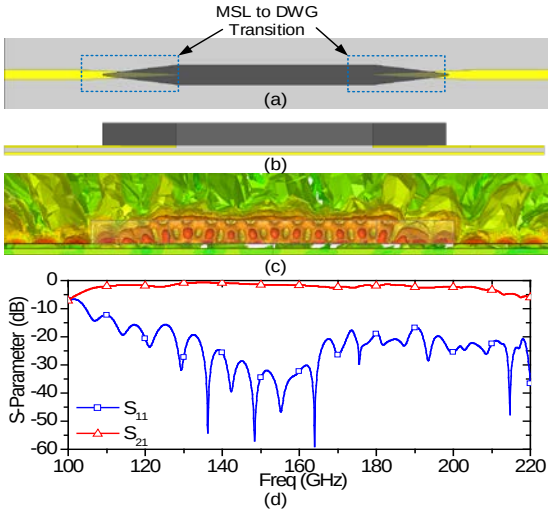

Fig. 3. (a) Top view of the sub-THz interconnect channel with two back-to-back MSL to DWG transitions. (b) Side view of the sub-THz interconnect channel. (c) Side view of the magnitude of E-Field distribution. (d) Simulated S-Parameters.

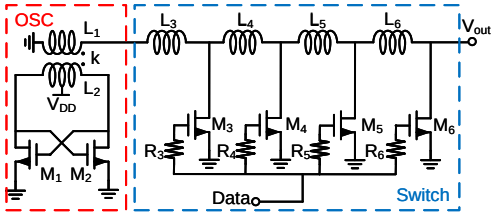

Fig. 4. Schematic of the transmitter, including the transformer based signal generator, and the SPST switch based OOK modulator.

throw (SPST) switch based modulator. The signal source is based on a fundamental cross-coupled oscillator with a transformer output network. The transformer is introduced as an output network with two advantages. First, the transformer based network achieves an impedance converting ratio proportional to $1/k^2$, where k is coupling factor of the transformer [9]. This behavior helps the optimization of the oscillator, especially when the output impedance of the core transistor-pair is much higher than the load. Meanwhile, the well matched transformer exhibits a minimum insertion loss only proportional to $1/k$. The insertion loss increases $1/k$ slower than the impedance converting effect. Second, the transformer can play the role as the inductor in the *LC* tank to save the chip area. The core transistor of 9.6 µm in width and 65 nm in length is used. A transformer with outer diameters of 28/40 µm for the primary/secondary coil and width of 4 µm is used, which corresponds to k = 0.45, is selected in the transmitter design.

As shown in Fig. 4, a passive cascaded SPST switch based OOK modulator is designed to achieve low insertion loss and high on-off ratio. When the input data is "0", the transistors are turned off to represent parasitic capacitors to cooperate with the series inductors and transit the signal. When the input data is "1", the transistors are turned on to represent small resistors to bypass the signal to ground and provide isolation between port 1 and port 2. With the tradeoff between the insertion loss and the isolation, the 24.48 µm (C_{off} = 21 fF and R_{on} = 13.47 Ω)

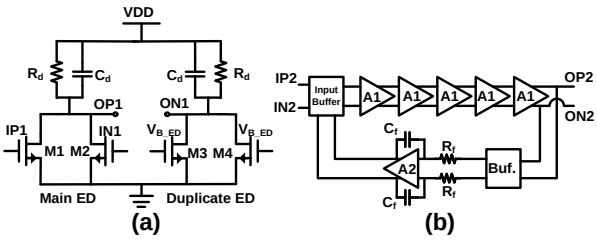

Fig. 5. Schematics of (a) ED based demodulator and (b) LA.

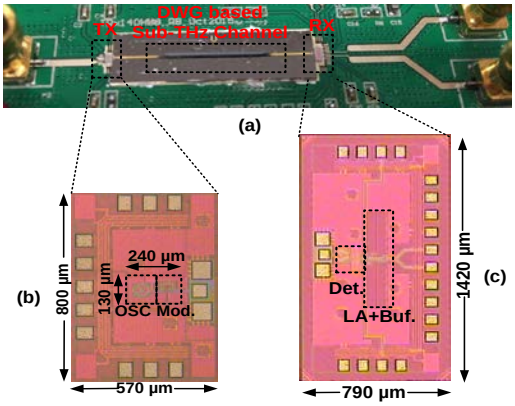

Fig. 6. (a) Test board of the DWG based sub-THz interconnect. (b) Die photo of the transmitter. (c) Die photo of the receiver.

transistors are employed. The series inductor of 27.5 pH is implemented. The simulated rising and falling time for the proposed switch are only 24 ps and 19 ps, respectively.

The LNA-free architecture is used in this receiver to boost the energy efficiency. The envelop detector (ED), illustrated in Fig. 5(a), utilizes the square law feature of MOS transistors. The differential inputs are used to suppress the odd mode signals and realized by input transformer of the ED. This transformer also serves as the impedance matching with the diameters of 26 µm and 38 µm for primary and secondary windings, respectively. To suppress the common mode and improve the noise rejection, the duplicated ED is employed and the four inputs of ED are biased by the center tap of second coil of the ED input transformer. To maximize the responsivity, the ED is biased at class AB, that is, $V_{B\_ED} \approx V_{TH}$. The low pass filter formed by C_d and R_d is used to filter the carrier and the higher order harmonics. The power consumption of the demodulator is only 7.5 mW. The 5-stage LA, which is shown in Fig. 5 (b), and output buffer consume 21.8 mW, which is excluded from FoM calculations, and are optimized to drive the off-chip 50-Ω loads.

III. Experimental Demonstration

The channel fabrication includes two parts: DWG and coupling structure. For the DWG, it is based on lithography and deep reactive ion etching (DRIE). For the coupling structure, it is based on gold deposition and electroplating. The straight DWG length l=10 mm, width w=300 µm, and height h=500 µm. The MSL-to-DWG transition length is 2 mm. Fig. 6(a) shows the test board, which is built with FR4 substrate.

TABLE I Comparison with the state-of-the-art interconnects

	[3]	[4]	[5]	[6]	[7]	This work
Electrical (E)/ Optical (O)	E	E	E	E	O	E
Technology	40 nm CMOS	40 nm CMOS	65 nm CMOS	28 nm CMOS	28 nm SOI CMOS	65 nm CMOS
f_c (Hz)	135G	120G	107G	0	194T	165G
Modulation	ASK	CPFSK	OOK	N/A	OOK	OOK
Channel	Wireless	Wireline	Wireless	Wireline	Wireline	Wireline
Distance (mm)	100	1000	300	5000	N/A	22.6
Channel Loss (dB)	N/A	N/A	N/A	51	N/A	4.0
Chip Area (mm^2)	2	0.48	0.68	25.3	N/A	1.75
Power Consumption (mW)	98	52	34	403	123	14.2
Data Rate (Gb/s)	10	12.7	10	25.8	25	5
Channel Area (mm^2)	> 1.4*	3.14	> 3.23*	103.36**	N/A	0.15
Energy Efficiency (pJ/b)	9.8	4.8	3.4	15.6	4.9	2.8
Bandwidth Density (Gbps/mm^2)	7.09	4	3.1	0.25	N/A	33.3
FoM*** (pJ/bit*mm^2)	13.7	15.1	11.0	1612	N/A	0.4

* At least larger than waveguide size ** A QSFP connector is used. The minimum size of QSFP is 103.36 mm^2

*** FoM (pJ*mm^2/bit) = Energy Efficiency / Channel cross-section Area

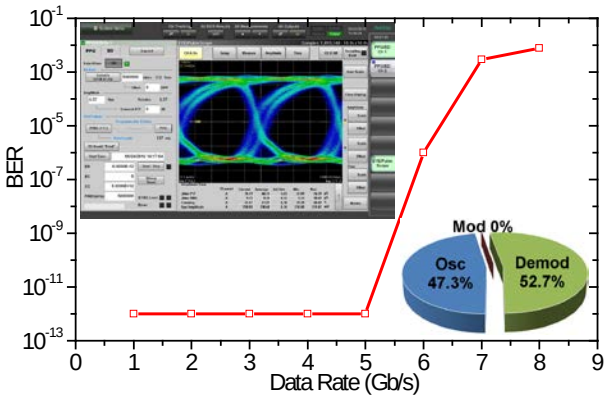

Fig. 7. BER versus data rate with the insets of the eye diagram at PRBS 2^7-1, 5 Gb/s and BER < 1×10^{-12}, and the pie chart of DC

The transceiver chips are implemented in a 65nm bulk CMOS technology and die photos are shown in Fig. 6(b) and (c). The chip areas of transmitter and receiver are 570 µm × 800 µm and 790 µm × 1420 µm, respectively.

The measured insertion loss of the channel is 4.0 dB with 59-GHz 3-dB bandwidth for a 10 mm DWG with MSL-to-DWG transitions. The measured output power and DC-to-RF efficiency with the various power supply at 165 GHz. The maximal output power is 0.63 dBm with 1-V power supply and 12 mA DC current. The best efficiency is 10.6% with 0.8 V.

The measured bit-error rate (BER) versus data rate with an inset of the eye diagram is drawn in Fig. 7. The 2^7-1 PRBS pattern is generated from Anritsu MP2011B. The data rate is up to 5 Gb/s for the total communication distance of 22.6 mm. The power consumptions of the transmitter and the receiver are 6.7 mW and 7.5 mW, respectively. As tabulated in Table I, comparing with the other state-of-the-art interconnects, this work has achieved the best energy efficiency, bandwidth density, and FoM.

IV. Conclusion

This paper for the first time presents the design and demonstrates the silicon DWG based sub-THz interconnect system for high energy-efficiency and high bandwidth-density communications. This technique can be readily scaled up to THz frequencies for a better bandwidth density and possibly better energy efficiency by leveraging the wider bandwidth feature. Therefore, the authors envision that THz interconnect has the potential to eventually solve the long-standing interconnect problems of chip-to-chip communications.

References

[1] X. Zheng and A. V. Krishnamoorthy, "Si photonics technology for future optical interconnection," in *Communications and Photonics Conference and Exhibition, 2011. ACP. Asia*, 2011, pp. 1–11.

[2] Q. J. Gu, "THz interconnect: the last centimeter communication," *IEEE Commun. Mag.*, vol. 53, no. 4, pp. 206–215, Apr. 2015.

[3] M. Fujishima, M. Motoyoshi, K. Katayama, K. Takano, N. Ono, and R. Fujimoto, "98 mW 10 Gbps Wireless Transceiver Chipset With D-Band CMOS Circuits," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2273–2284, Oct. 2013.

[4] W. Volkaerts, N. Van Thienen, and P. Reynaert, "An FSK plastic waveguide communication link in 40nm CMOS," in *Solid-State Circuits Conference - (ISSCC), 2015 IEEE International*, 2015, pp. 1–3.

[5] N. Weissman, S. Jameson, and E. Socher, "A packaged 106-110 GHz bi-directional 10Gbps 0.11 pJ/bit/cm CMOS transceiver," in *Microwave Symposium (IMS), 2015 IEEE MTT-S International*, 2015, pp. 1–4.

[6] T. Norimatsu *et al.*, "3.3 A 25Gb/s multistandard serial link transceiver for 50dB-loss copper cable in 28nm CMOS," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, 2016, pp. 60–61.

[7] Y. Chen *et al.*, "A 25Gb/s hybrid integrated silicon photonic transceiver in 28nm CMOS and SOI," in *Solid-State Circuits Conference - (ISSCC), 2015 IEEE International*, 2015, pp. 1–3.

[8] B. Yu, Y. Liu, Y. Ye, X. Liu, and Q. J. Gu, "Low-loss and Broadband G-Band Dielectric Interconnect for Chip-to-Chip Communication," *IEEE Microw. Wirel. Compon. Lett.*, to be published.

[9] Y. Ye, B. Yu, and Q. J. Gu, "A 165-GHz Transmitter With 10% Peak DC-to-RF Efficiency and 0.68-pJ/b Energy Efficiency in 65-nm Bulk CMOS," *IEEE Trans. Microw. Theory Tech.*, vol. PP, no. 99, pp. 1–12, 2016.