

Summer School

FULL STACK OPEN-SOURCE ECOSYSTEM

FOR PROCESSOR BASED CHIP DESIGN



23, 24 September 2023

FOSS Compact/SPICE Modeling and its Verilog-A Standardization Technology - Devices - Applications

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PAKISTAN
SUPERCOMPUTING™



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Center*

Centro Nacional de Supercomputación



FOSS TCAD/EDA Tools for Compact Modeling

Outline

- The Transistor Turns 75
- Moore's Law
- History and Evolution towards FOSS TCAD/EDA
 - <www.mos-ak.org/books/CAD_CM_Book.php>
 - 2/3D Numerical TCAD Device Simulations
 - Schematic entry and circuit simulation
 - Device Level Parameter Extraction
 - Standardized Data Exchange Format For Device Modeling
- Outlook:
 - A call for Building Talent and Skills
- 2023 MOS-AK Compact/SPICE Modeling Events



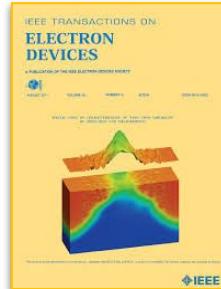
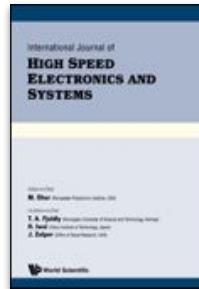
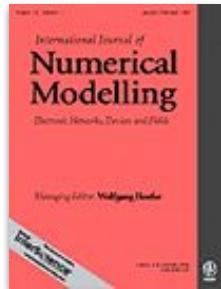
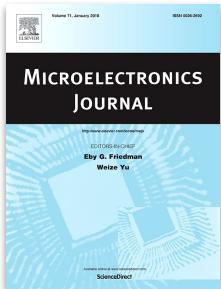
Over two decades of MOS-AK in brief

- 20 subsequent MOS-AK modeling workshops and
- 6 consecutive TRACKs: Compact Modeling
at ESSDERC/ESSCIRC Conferences
- 30+ international MOS-AK modeling workshops
in Europe, USA, Latin America, India, China
- 20+ Special compact modeling sessions
at MIXDES Conference
- 50+ active sponsors and technical program promoters
- 450+ MOS-AK technical CM papers and posters
(available online www.mos-ak.org)
- 5 modeling MOS-AK modeling books
<http://www.mos-ak.org/books/>

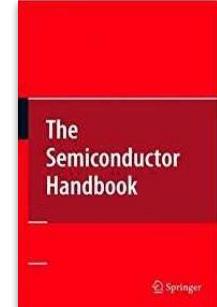
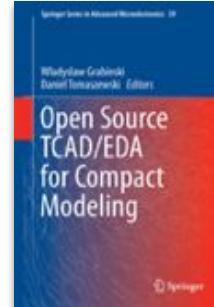
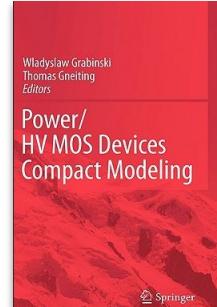
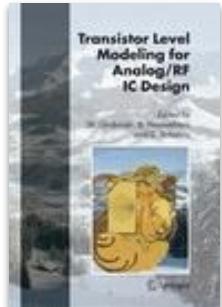
Arbeitskreis Modellierung von Systemen und Parameterextraktion Modeling of Systems and Parameter Extraction Working Group



MOS-AK Scientific Publications



Special Compact Modeling Issues



Compact/SPICE Modeling Books

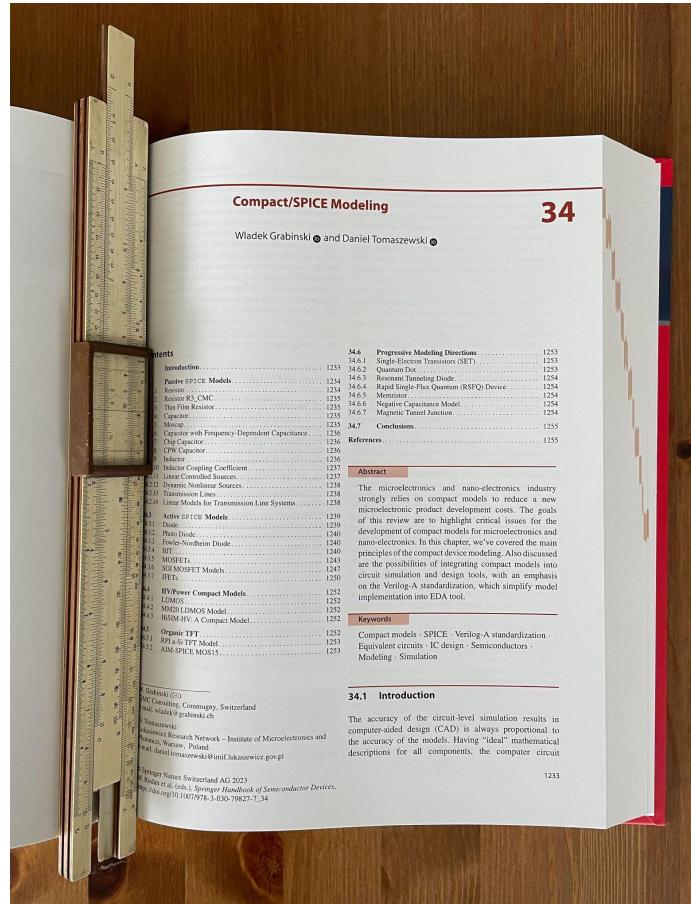
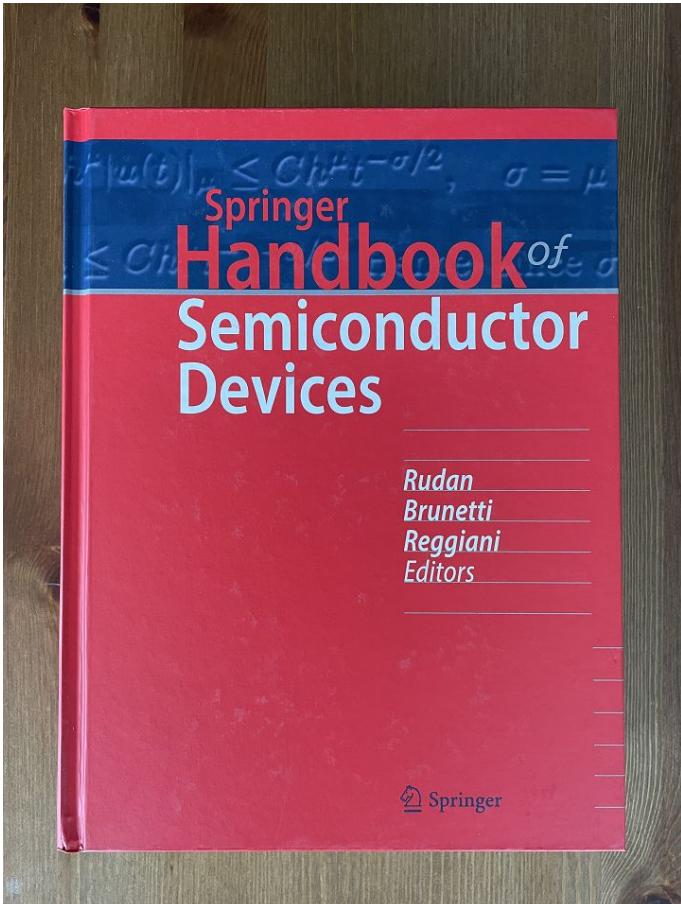


TRACK3: Compact Modeling and Process/Device Simulation (Lisbon 2023)

Arbeitskreis Modellierung von Systemen und Parameterextraktion Modeling of Systems and Parameter Extraction Working Group



The Semiconductor Handbook

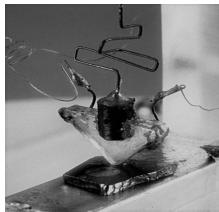




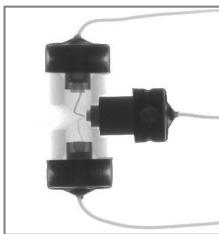
William Shockley and his Slide Rule



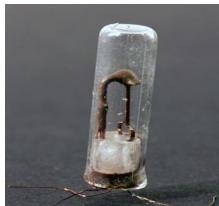
The Transistor Turns 75



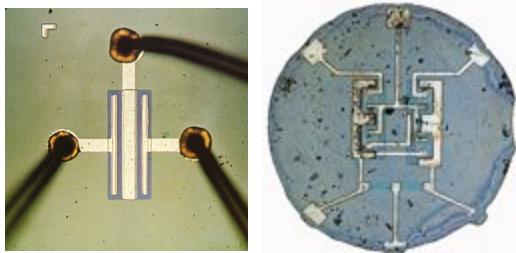
December 23, 1947, John Bardeen and Walter Brattain at AT&T's Bell Labs in Murray Hill, New Jersey, performed experiments and observed that when **two gold point contacts were applied to a Ge** crystal, a signal was produced with the output power greater than the input.



The '**transistron**' invented by two German physicists: Dr. Herbert F. Mataré and Heinrich Welker, working at the Compagnie des Fréins & Signaux, Westinghouse in Aulnay-sous-Bois near Paris. French minister Eugene Thomas presented the "Transistron" in Paris on May 19, 1949



TP-1 Ge Point-contact Transistor; First Polish Bipolar Transistor
W. Rosiński, J. Groszkowski, "Doświadczalne tranzystory punktowe model TP" Arch. Elektrot. 4, 1955, p. 381

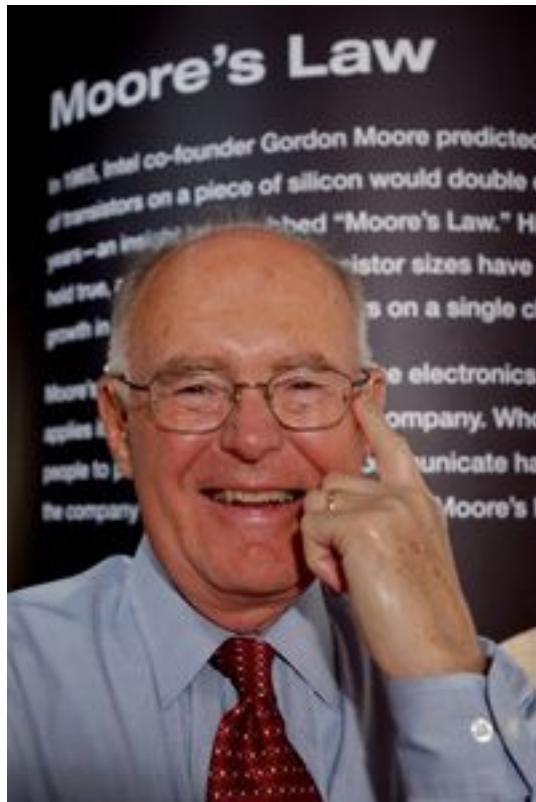


C.T. Sah of Fairchild built an MOS-controlled tetrode (1960)
The first working monolithic devices (IC) presented by Fairchild Semiconductor on May 26, 1960



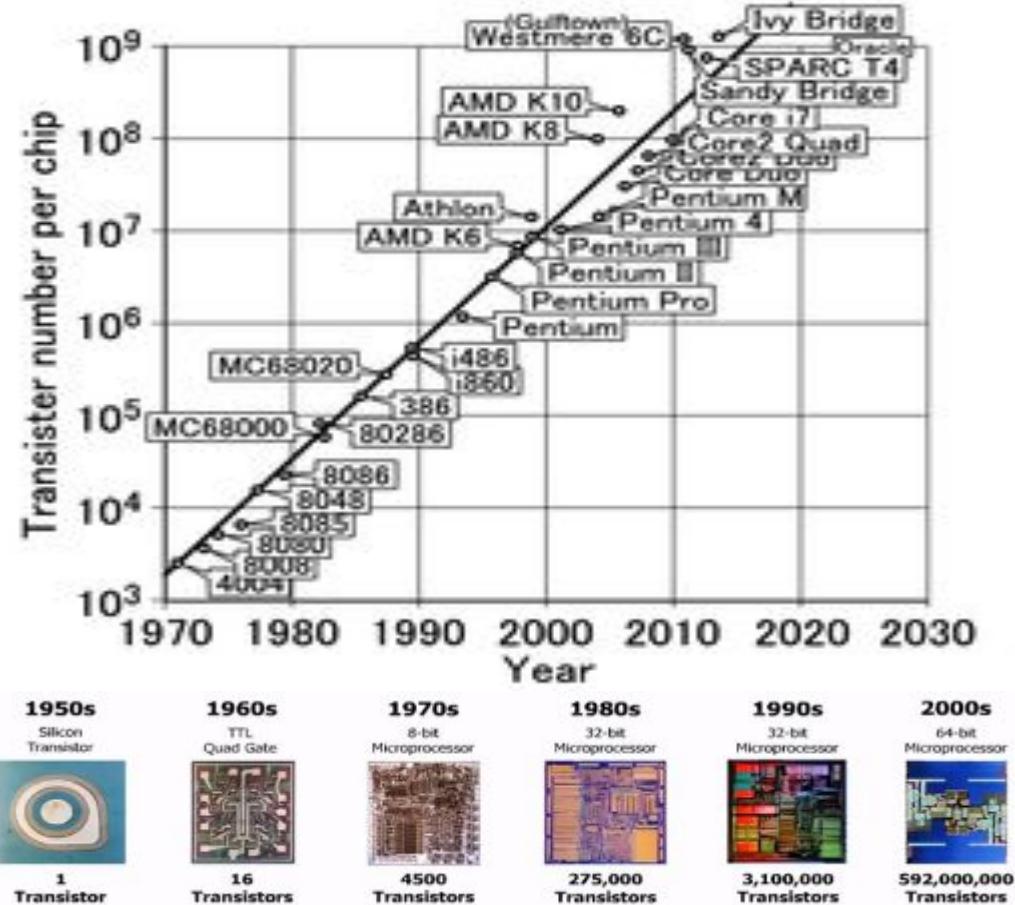
The Raspberry Pi Zero is half the size of a Model A+, with twice the utility. A tiny Raspberry Pi that's affordable enough for any project! \$5 or even free as early 2016; Raspberry Pi Zero 2 W: 15\$
www.raspberrypi.org/products/pi-zero

Moore's Law



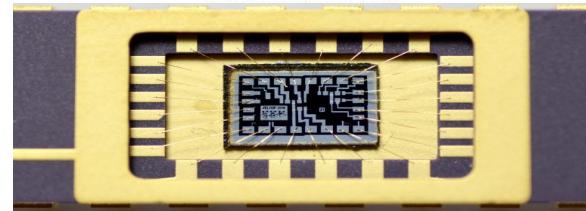
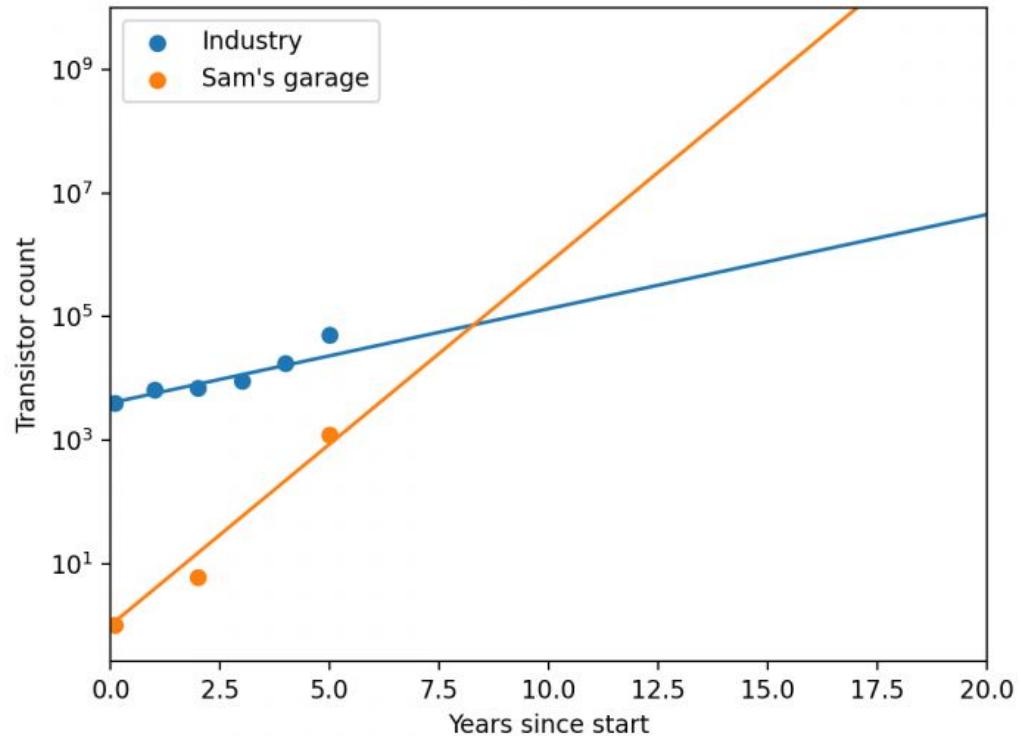
Gordon E. Moore

*Jan. 3, 1929 +Mar. 24, 2023



Moore's Law is the fundamental driver of the semiconductor industry, what's even more important is what it delivers to the end user.

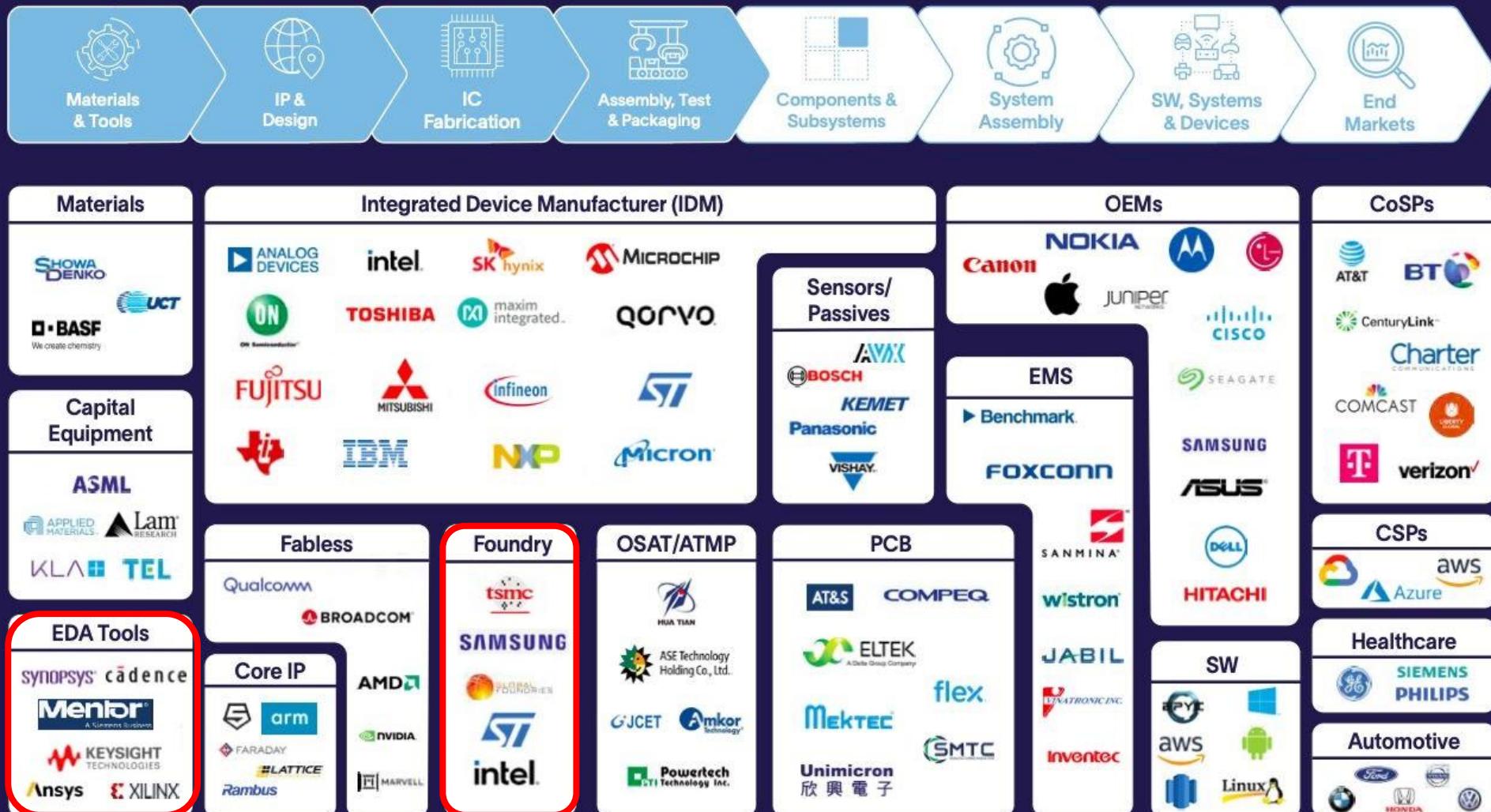
Sam Garage's Law



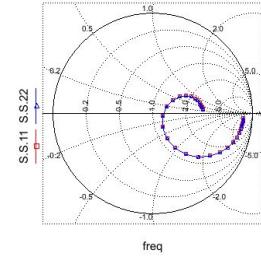
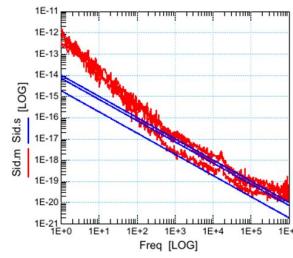
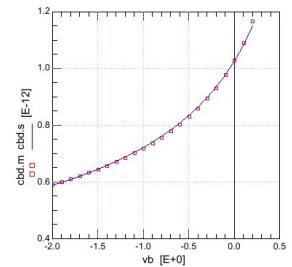
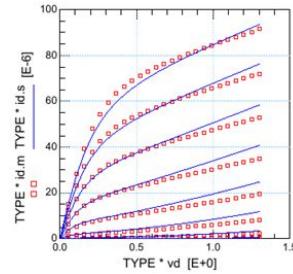
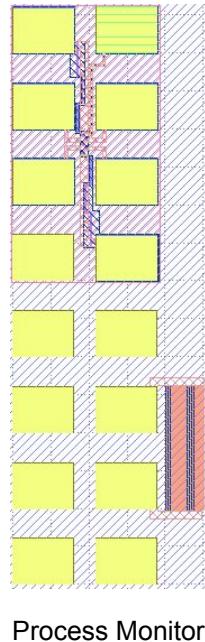
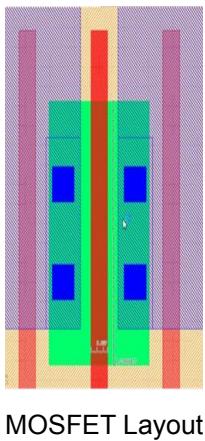
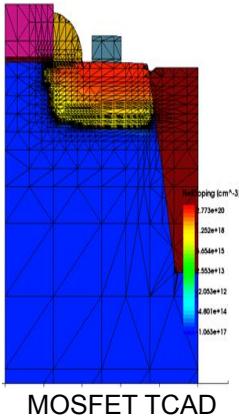
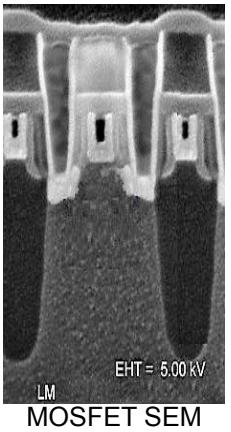
The Z1 by Sam Zeloof had 6 transistors and was a great test chip to develop all the processes and equipment. The Z2 has 100 transistors on a $10\mu\text{m}$ polysilicon gate process - same technology as Intel's first processor. [REF: <http://sam.zeloof.xyz/>]

Moore's Law Or Sam Garage's Law

Or....



CMOS Technology Abstract Views



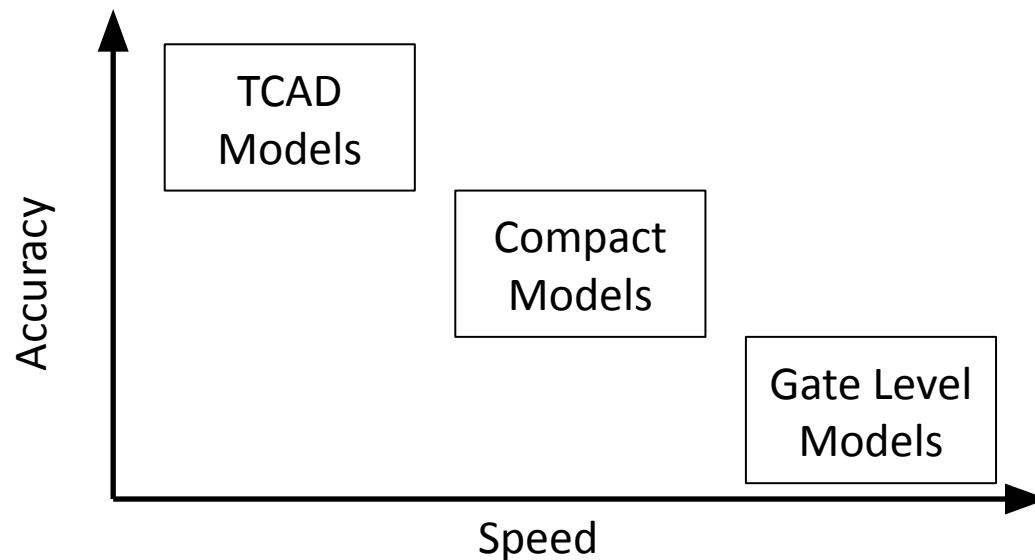
Technology **TCAD**

Electrical **SPICE**

Dennard **MOSFET Scaling**

Compact/SPICE Modeling

- A model of semiconductor device charges, currents and voltages
- Built from physically-motivated equations
- Intended for use in an analog circuit simulator



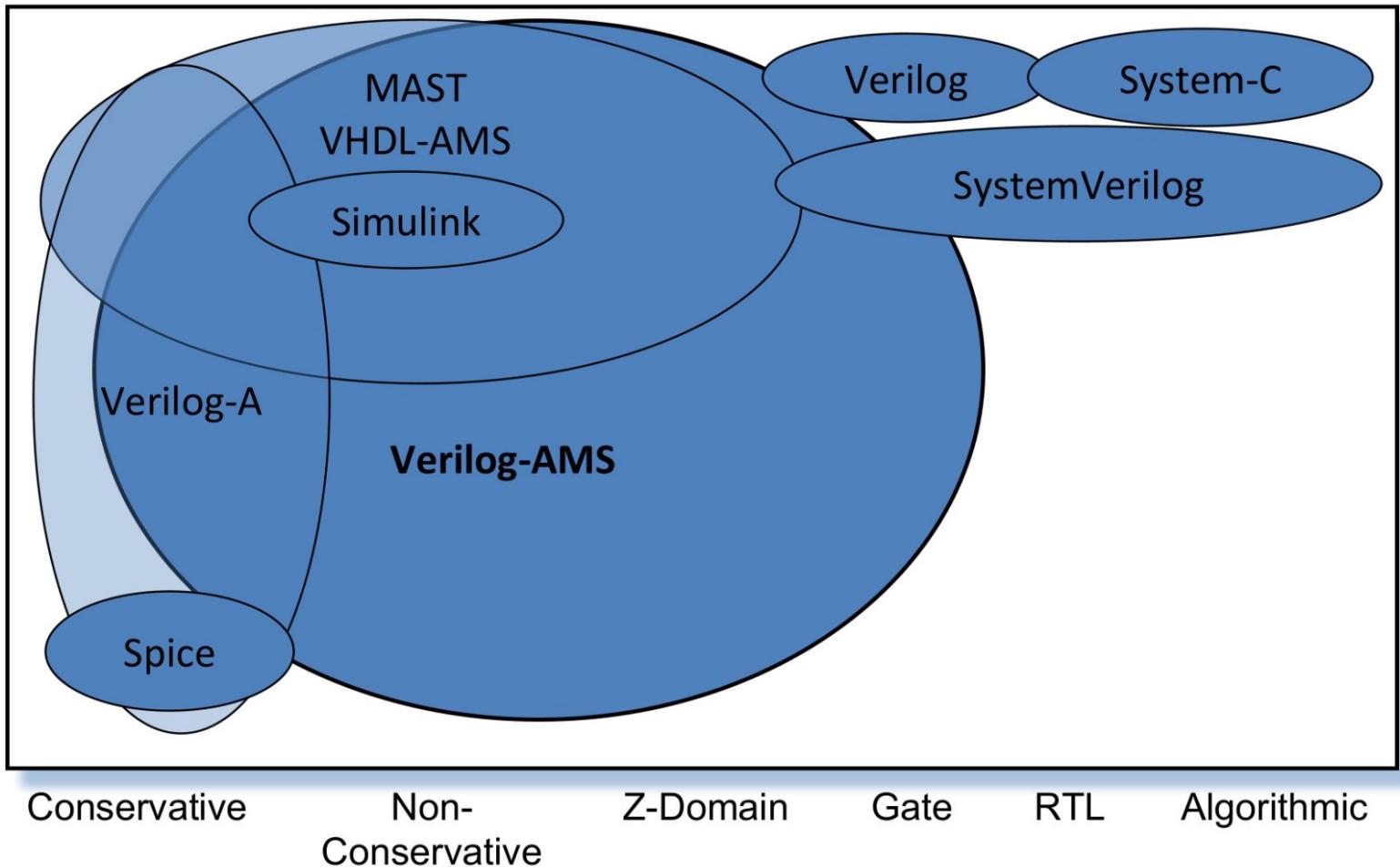
Ranges of AMS Modeling

Primitives

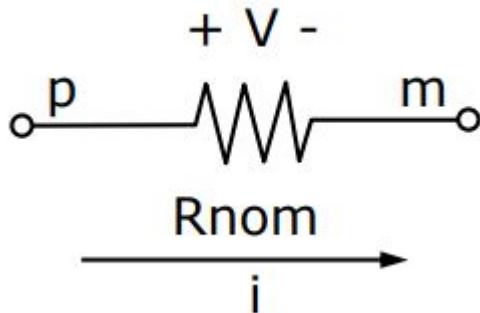
Equations

Table Driven

Predefined



Behavioral Languages



The **MAST** is Analog and Mixed-Signal Hardware Description Language (HDL) for SABER

```
template resistor p m =  
Rnom electrical p, m  
number Rnom  
  
{  
branch  
    v=v(p, m),  
    i=i(p->m)  
  
equations { i = v / Rnom  
}  
}
```

The voltage across this device is determined by the simulator. The current through it is defined by the device characteristic equation:

$$i = \frac{v}{R_{nom}}$$

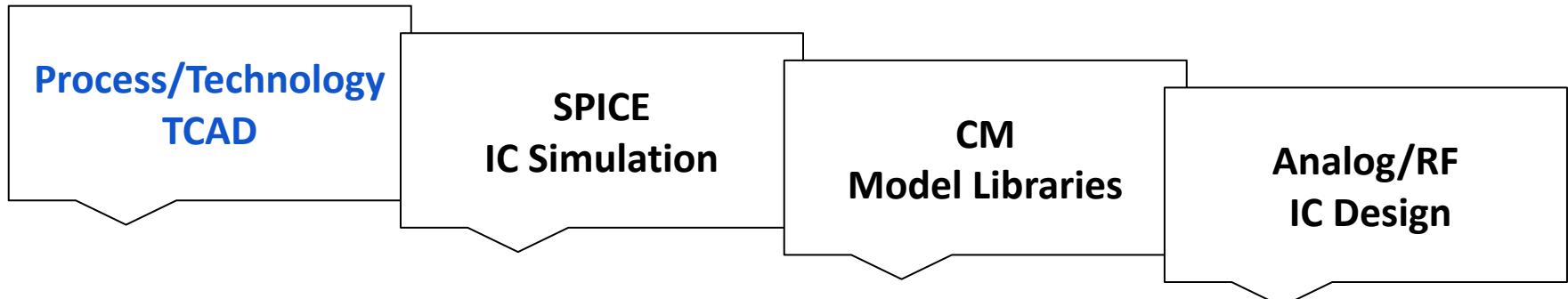
VHDL-AMS is the IEEE 1076.1 a HDL for the description/ simulation of analog, digital, and mixed-signal systems

```
use work.electrical_systems.all;  
  
entity resistor is generic  
(  
Rnom : real :=1  
);  
port ( terminal p, m :  
electrical);  
architecture behavior of  
resistor is  
begin  
    i == (p-m) / Rnom;  
end architecture simple
```

Verilog-A(AMS) HDL of analog, digital, and mixed-signal systems is derived from IEEE Std 1364-200

```
`include "std.vah"  
  
module resistor (p, m);  
parameter real Rnom=1  
inout p,m;  
electrical p, m;  
  
analog  
    I(p,m) <+ V(p,m) / Rnom;  
end // analog  
endmodule
```

FOSS TCAD/EDA Tools



- Cogenda TCAD
- DevSim TCAD
- Stanford TCAD
- TU Wien TCAD
- IIS ETHZ TCAD
- Uni Glasgow NESS
- Nextnano
- QUANTUM ESPRESSO
- EM Simulators
- MEMS Simulators
- other

- Ngspice
- Qucs
- Xyce
- GnuCap
- FOSSEE eSim
- other

- Verilog-A Standardization
 - ADMS
 - OpenVAF
 - MAPP
- measurements
 - SweepMe!
- parameterization
 - TRADICA
 - DMT
- other

- IC Schematic
- IC Layout Editors
- DRC, LVS
- other

Stanford TCAD Software

Professor **Robert W. Dutton** and his group has developed industry-standard modeling codes such as SUPREM (process modeling in 1D and 2D) and PISCES (2D device modeling). He was a co-founder of Technology Modeling Associates (TMA), acquired by Avant!, specializing in advanced semiconductor TCAD modeling codes. Prof. Dutton has held a number of industrial visits and summer appointments: Fairchild, Palo Alto (1967); AT&T, Holmdel (1973); HP Labs, Palo Alto (1975); IBM, Yorktown Heights (1977); Matsushita Electric Industrial, Japan (1988-89)

Device Modeling	Process Modeling	Framework/Utilities
PROPHET	SUPREM3	ET3D
Monet	SUPREM IV	FOREST
PISCES	SUPREM IV GS	HDFVset
PISCES 2ET	SUPREM ALAMOD	VIP3D
PISCES 2H-B	SPEEDIE	Mixed Mode
SEDAN III		
STRIDE		

Stanford TCAD

[REF] <http://www-tcad.stanford.edu/>

TU Wien TCAD Software

O.Univ.Prof. Dipl.-Ing. Dr.techn. Dr.h.c. **Siegfried Selberherr** has been holding the venia docendi on Computer-Aided Design since 1984. From 1988 to 1999 he was the Head of the Institute for Microelectronics. From 1998 to 2005 he served as Dean of the Faculty of Electrical Engineering and Information Technology. His current research topics are modeling and simulation of problems for microelectronics engineering.

Open Source Software

ViennaCL

ViennaData

ViennaFEM

ViennaGrid

ViennaIPD

ViennaMag

ViennaMath

ViennaMesh

ViennaProfiler

ViennaSHE

ViennaSiSpin

ViennaTS

ViennaWD

ViennaX

No Longer Supported

deLink 1.0

Promis

SIESTA

ViennaMOS

VMC

VSP

Minimos-NT



INSTITUTE FOR
MICROELECTRONICS

Early History of Device Physics & TCAD at IIS, ETH Zurich

- 1985** Wolfgang Fichtner appointed as Professor at Electronics, Department of Electrical Engineering, ETH Zürich
- 1986** “Integrated Systems Laboratory” (IIS) founded by merging of the research groups of Prof. Wolfgang Fichtner (Department of Electrical Engineering) and Prof. Martin Morf (Department of Computer Science)
- 1988** Microelectronics Design Center founded as part of the IIS
- 1991** Federal Priority R&D LESSIT Project (TCAD simulation support for ABB, EMM Marin)
- 1991** Andreas Schenk, Scientific Adjoint, joins the IIS of ETH Zurich
- 1993** Integrated Systems Engineering AG (ISE) Founded
(Acquired in 2004 by Synopsys Inc.)
- 2011** Mathieu Luisier joins IIS
as SNF Assistant Professor for Computational Nanoelectronics
- 2022** Mathieu Luisier has been appointed
as Full Professor of Computational Nanoelectronics at D-ITET

Early History of Device Physics & TCAD at ISS ETH Zurich

Device Physics

- rudimentary physics for DD (1990)
- standard models for mobility, recombination, impact ionization, band gap narrowing, carrier-carrier scattering, contacts (1991)
- Device simulation for smart integrated systems (**DESSIS**) ESPRIT 6075 (1992-95)
- bulk and contact tunneling models, optical carrier generation (1992)
- generation by alpha-particles, full-band MC bulk, FN tunneling & hot-electron injection (1993)
- energy-balance model, 2D hybrid MC-EB simulator (1994)
- 1D Schrödinger-Poisson solver (1995)
- gate tunneling, full-RPA BGN, FEMFETs (1996)
- 3D hybrid MC-EB (1997)
- high-Temperature models, models for QW lasers, electrothermal MC (1998)
- prototype SET simulator SIMNAD, QDD equations in DESSIS, HF and 1/f noise modeling with direct IFM in DESSIS, 3D QW laser diodes (1999)

Process Simulation

- basic process steps 1D, 2D (1990)
- 2D analytical doping profiles, 3D solid modeler PROSIT started (1991)
- **TESIM-4** (1D) and **DIOS** (2D) interfaces, models for oxidation, non-isotropic deposition & etching (1992)
- point-defect based models in DIOS, non-equilibrium dopant transport (1993)
- 3D device models from 1D, 2D (PROMPT), 1D MC for implantation Crystal-TRIM (1994)
- arsenic channeling in crystalline Si (1995)
- stress-dependent oxidation & silicidation in DIOS (1995)
- transient-enhanced diffusion modeling in DIOS (1996)
- Crystal-TRIM implementation in DIOS for non-planar 2D structures (1996)
- basic algorithms for full 3D process simulation (1998)

Early History of Device Physics & TCAD at IIS ETH Zurich

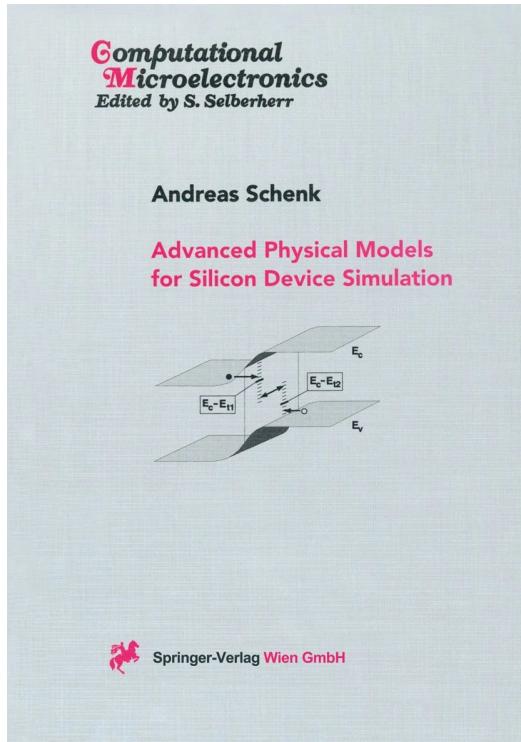
Mesh Generation

- automatic refinement 2D (1990)
- mixed-element 3D meshes (1991)
- intersection-based approach (1992)
- handling of complex device layouts, DRAW (1993)
- MESH, interactive grid generator MDRAW (1994)
- delaunization module in MESH (1997)
- adoption criteria for integration of MESH with DIOS (1998)
- normal off-setting in 2D (1998) and 3D (1999)

Numerical Algorithms

- iterative solver package PILS (1990)
- automatic switching between iterative solvers in PILS (1991)
- nonlinear elimination in SIMUL (1992)
- new block-decomposition solver in SIMUL (1993)
- hybrid solution direct-iterative (1994)
- parallel multigrid methods for device equations (1995)
- parallel sparse direct solver SUPER90 (1996)
- nested dissection algorithm, efficient parallel numerical factorization (1997)
- combined Newton-Raphson/Broyden nonlinear solver for 3D Schrödinger-Poisson, PARDISO integration in device and process simulators (1998)

Advanced Physical Models for Silicon Device Simulation



Andreas Schenk; **Advanced Physical Models for Silicon Device Simulation**; Part of the book series: Computational Microelectronics (COMPUTATIONAL); Publisher Springer Vienna (1998) DOI 10.1007/978-3-7091-6494-5

Table of contents (6 chapters)

- Front Matter: pp I-XVIII
- Simulation of Silicon Devices: An Overview: pp 1-126
- Advanced Generation-Recombination Models: pp 170-251
- Metal-Semiconductor Contact: pp 252-280
- Modeling Transport Across Thin Dielectric Barriers: pp 281-315
- Summary and Outlook: pp 316-319
- Back Matter: pp 320-354

SIMsalabim

1D drift-diffusion simulator for semiconductor devices

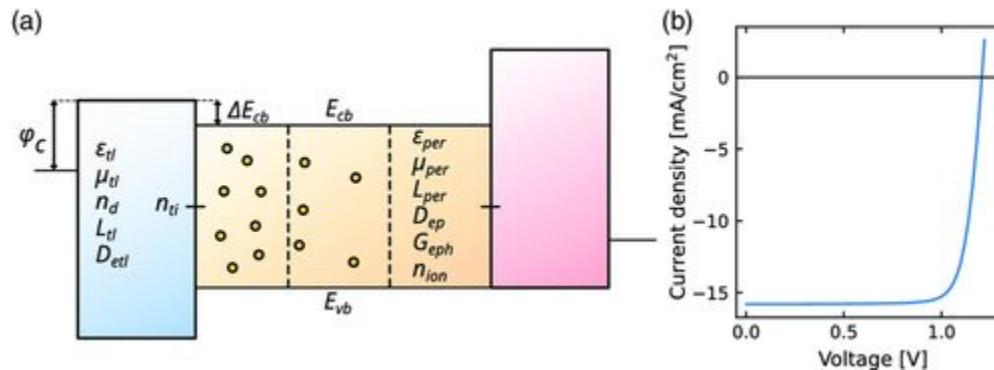


FIG: a) Schematic band diagram illustrating simulation parameters and where they take effect.

b) Current–voltage characteristic of our reference wide bandgap perovskite solar cell (PSC).

in: Koopmans, Marten, and L. Jan Anton Koster. "Voltage Deficit in Wide Bandgap Perovskite Solar Cells: The Role of Traps, Band Energies, and Effective Density of States." *Solar RRL* (2022): 2200560.

SIMsalabim: 1D drift-diffusion simulator for semiconductor devices (LEDs, solar cells, diodes, organics, perovskites). It consists of two programs that share most of their code: SimSS (simulates steady-state), and ZimT (simulates transients).

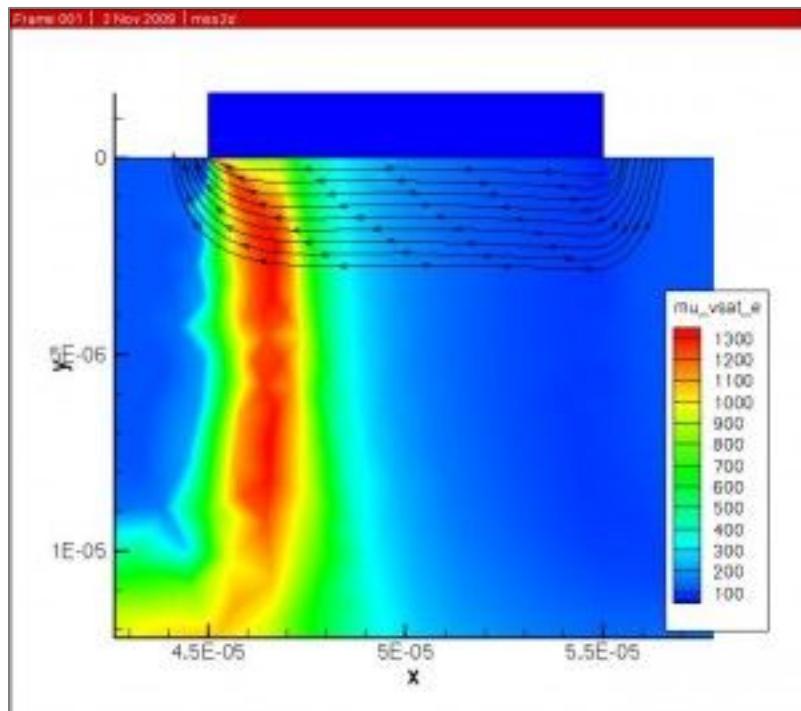
[REF] <https://github.com/kostergroup/SIMsalabim>

SCHRED simulation software calculates the envelope wave functions and the corresponding bound-state energies in a typical MOS, SOS and a typical SOI structure

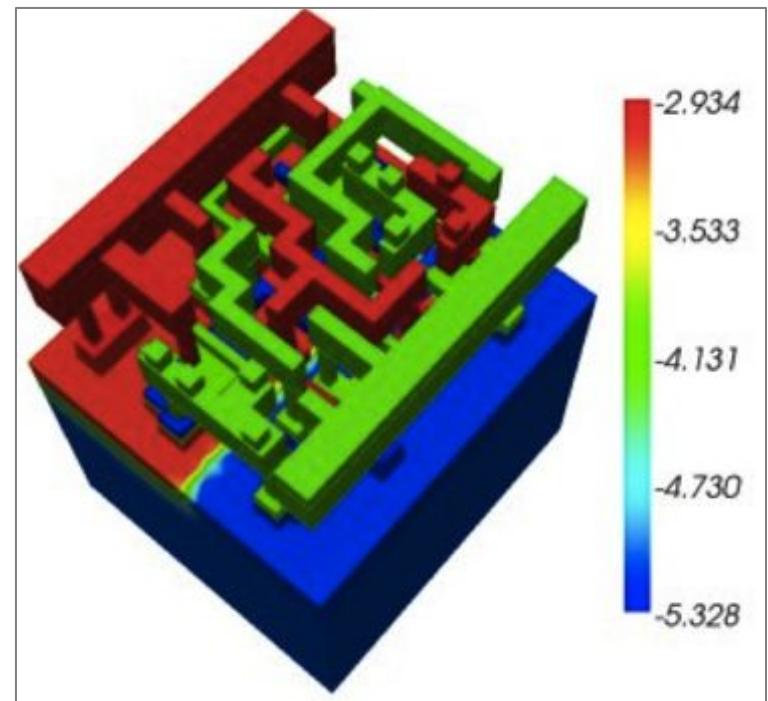
[REF] <https://nanohub.org/resources/schred/>

FOSS TCAD Simulation Tools

- DevSim TCAD
- Cogenda TCAD

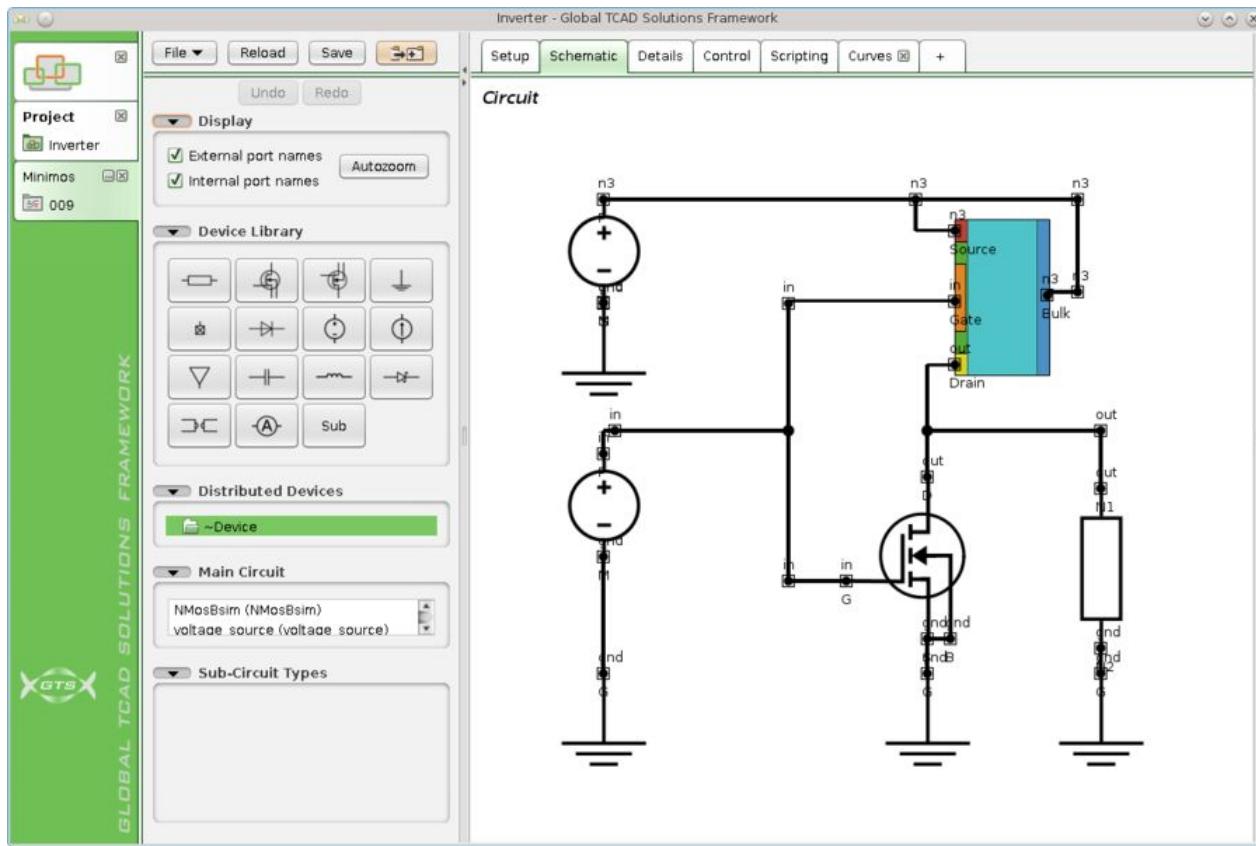


2D MOSFET simulation



3D SRAM Cell

GTS Minimos-NT: Mixed Mode



Mixed mode TCAD simulation can be done using industry-standard Spice compact models; easy-to-use schematic editor allows to quickly edit circuits and sub-circuits.

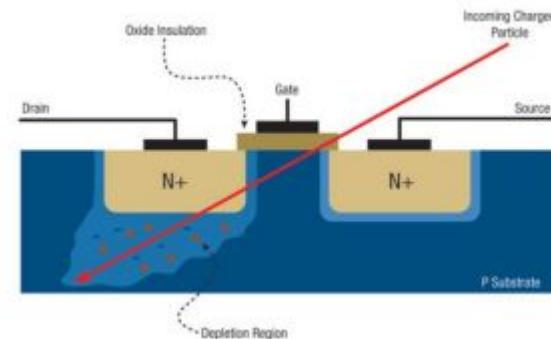
Charon: Parallel TCAD simulation

▪ Expanding Physics Capability

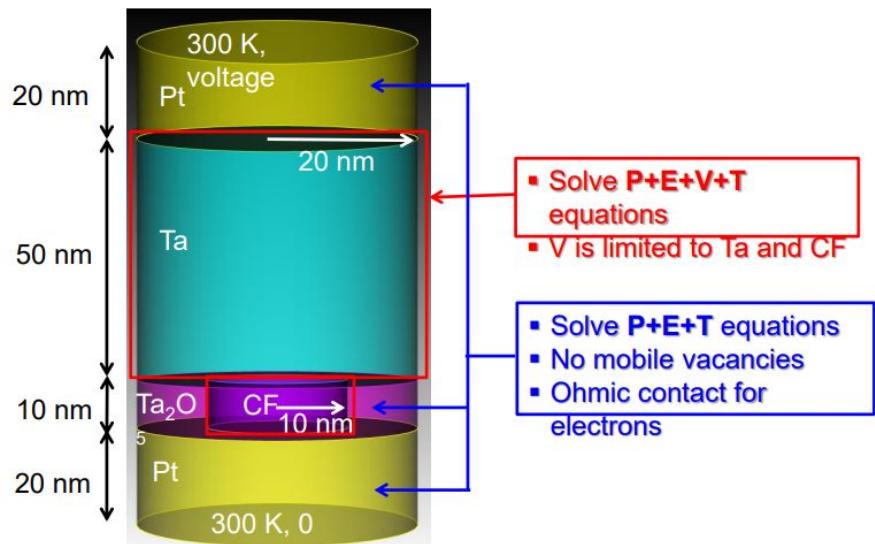
- SEE/SEU
- Simple linear charge input available
- Si HVD Analysis
- GaN development
- High Voltage Diodes (support of UWBG GC)
- HEMTs
- Frequency Domain Modeling (HB)
Both linear and non-linear
- Improved coupled electrical & thermal

▪ Next Generation Development

- In preparation of next gen computational Hardware
- Open-Source is a future path

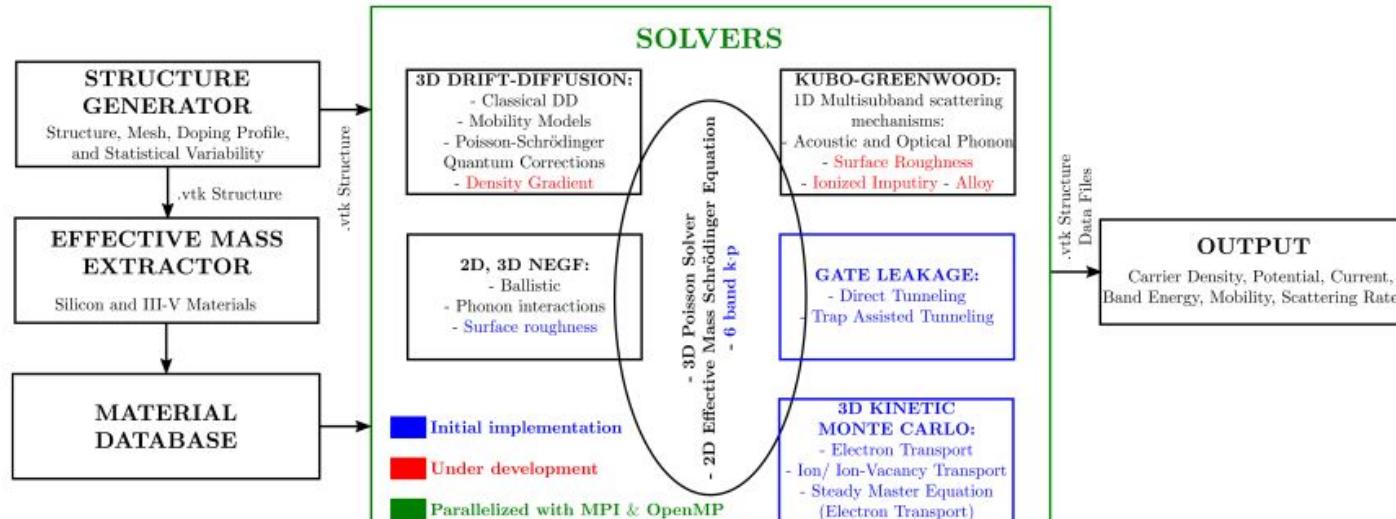


Single-Event Effects in MOSFETs

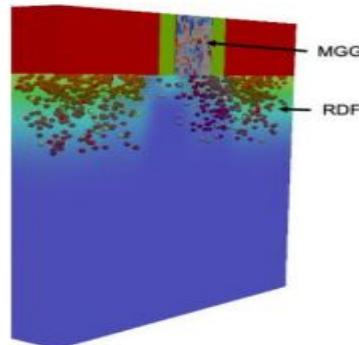


TaOx Memristor Device Structure

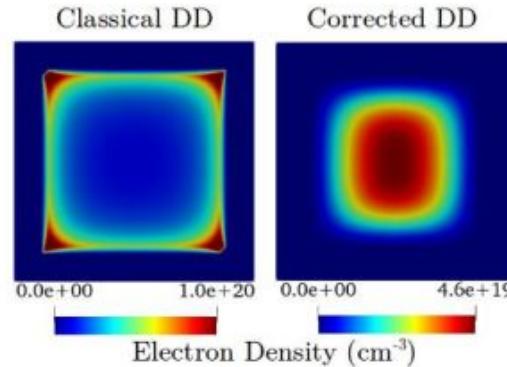
NESS: Novel Open-Source TCAD



Flowchart of NESS detailing its modular structure



Bulk MOSFET structure
and simulations statistical variability

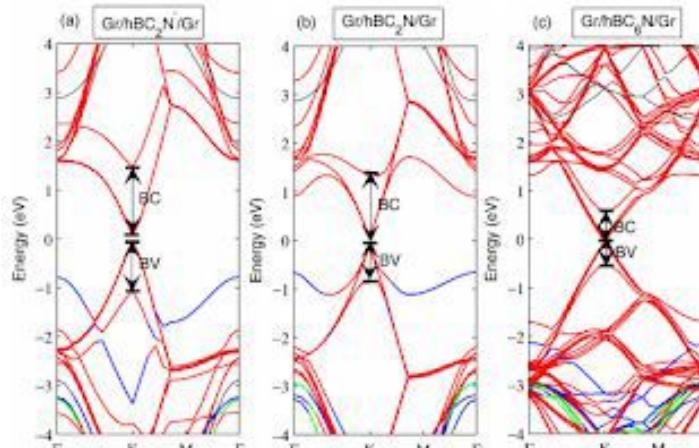


Electron density in a [110] oriented NW with
5nm x 5nm square cross section and LG=10nm for
classical (left) and quantum-corrected (right) DD

QUANTUM ESPRESSO

opEn Source Package for Research in Electronic Structure, Simulation, and Optimization

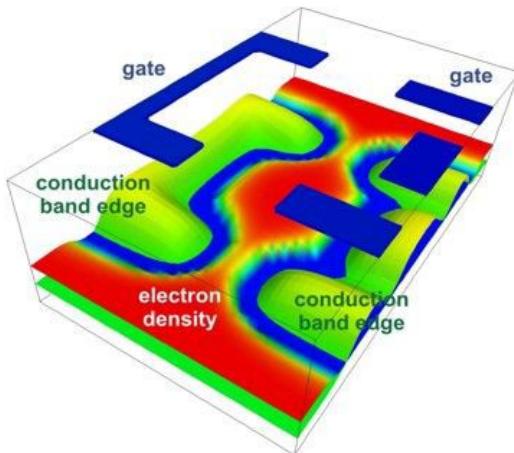
QUANTUM ESPRESSO is an integrated suite of computer codes for electronic-structure calculations and materials modeling, based on density-functional theory, plane waves, and pseudopotentials (norm-conserving, ultrasoft, and projector-augmented wave). It is freely available to researchers around the world under the terms of the GNU General Public License.



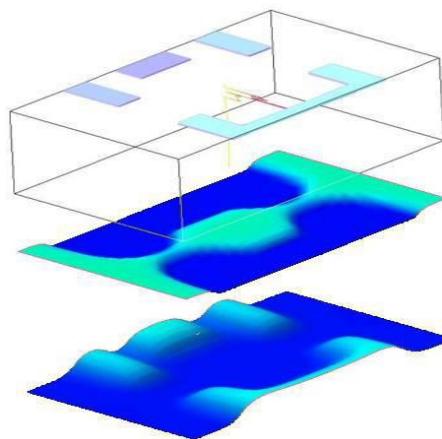
Example of the DFT Band structure for (a) graphene - hBC₂N₀ - graphene (b) graphene - hBC₂N - graphene and (c) graphene - hBC₆N - graphene supercell. BC and BV represent barrier height in the conduction band and valence band, respectively, as in paper: A comparative computational study of tunneling transistors based on vertical graphene–hBCN heterostructures Mahsa Ebrahimi, Ashkan Horri, Majid Sanaeeupur, and Mohammad Bagher Tavakoli; J. Appl. Phys. 127, 084504 (2020); DOI: 10.1063/1.5130777

Nextnano for the next Electronic and Optoelectronic Nanodevices

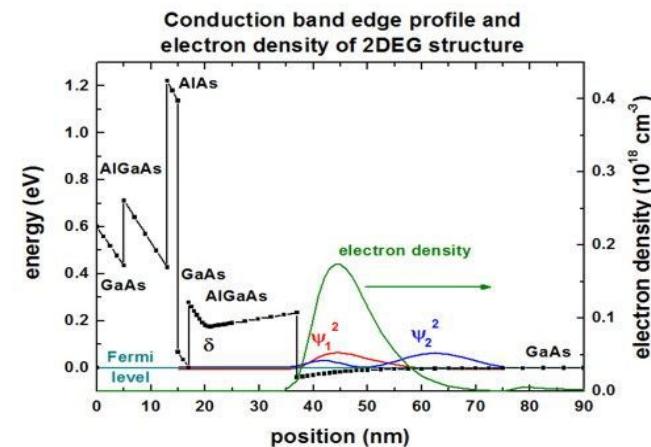
The nextnano software solves the Strain, Poisson, Schrödinger and Current equations self-consistently in one, two and three dimensions. It can be applied to a large variety of semiconductor nanostructures such as nanotransistors, LEDs, laser diodes, quantum dots, nanowires, quantum cascade lasers, HEMTs, photodetectors and solar cells. The example below is Single-electron transistor - laterally defined quantum dot based on the following paper: A. Scholze, A. Schenk, W. Fichtner; Single-Electron Device Simulation; IEEE TED 47, 1811 (2000)



The conduction band edge $E_c(x,y)$ and the electron density $n(x,y)$ for the 2DEG plane, i.e. at $z = 8$ nm below the GaAs/AlGaAs heterojunction.

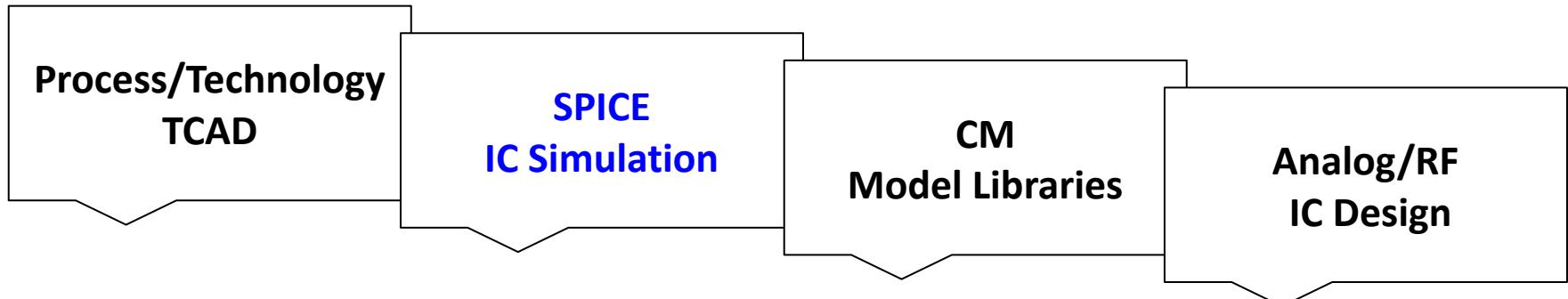


Two 2D slices through the lateral (x,y) plane at a distance of 8 nm below the AlGaAs/GaAs interface.



The calculated conduction band edge and the electron density of the heterostructure.

FOSS TCAD/EDA Tools for Compact Modeling



- Cogenda TCAD
 - DevSim TCAD
 - Stanford TCAD
 - TU Wien TCAD
 - IIS ETHZ TCAD
 - Uni Glasgow NESS
 - Nextnano
 - QUANTUM ESPRESSO
 - EM Simulators
 - MEMS Simulators
 - other
- Ngspice
 - Qucs
 - Xyce
 - GnuCap
 - FOSSEE eSim
 - other
- Verilog-A Standardization
 - ADMS
 - OpenVAF
 - MAPP
 - measurements
 - SweepMe!
 - parameterization
 - TRADICA
 - DMT
 - other
- IC Schematic
 - IC Layout Editors
 - DRC, LVS
 - other

about SPICE

CANCER: Computer Analysis of Nonlinear Circuits Excluding Radiation

* L. Nagel, Masters Report, Dept of EECS, Berkeley, CA, Dec.11, **1970**

SPICE

- * SPICE = Simulation Program with Integrated Circuit Emphasis
- * The very first analog circuit simulator introduced in **1973**, written in FORTRAN
- * Developed at University of California, Berkeley
- * Nodal analysis, few circuit elements, fixed timestep transient analysis

SPICE 2

- * Released in **1975**, still written in FORTRAN
- * Improvements: modified nodal analysis, memory allocation system, variable timestep transient using trapezoidal and Gear integration
- * Missing: parameter sweep, loop-gain and stability, RF analyses

SPICE 3

- * Released in **1989**, (re)written in C
- * Added X Window plotting

Commercial circuit simulators

- * Spectre (Cadence)
- * PSPICE (OrCAD, now Cadence)
- * APLAC (Nokia, AWR, NI, Cadence)
- * HSPICE (Synopsys)
- * Eldo (Mentor)
- * FastSpice (BDA, now Mentor)
- * SIMetrix (Simetrix Tech.)
- * ADS (Agilent)

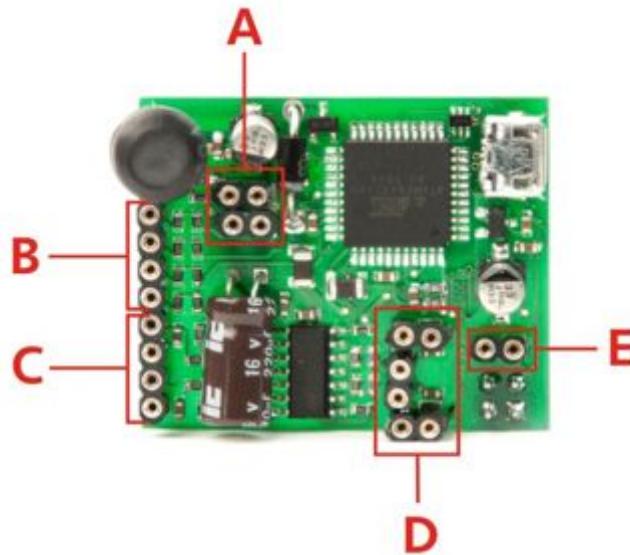
In-house circuit simulators

- * TITAN (Infineon)
- * Lynx (Intel)
- * TISPICE (Texas Instruments)
- * ADICE (Analog Devices),
- * LTspice (Linear Technologies)
- * PowerSpice (IBM)
- * Mica (Motorola/Freescale)
- * Pstar (NXP Semiconductor)

Five Powerful Lab Instruments

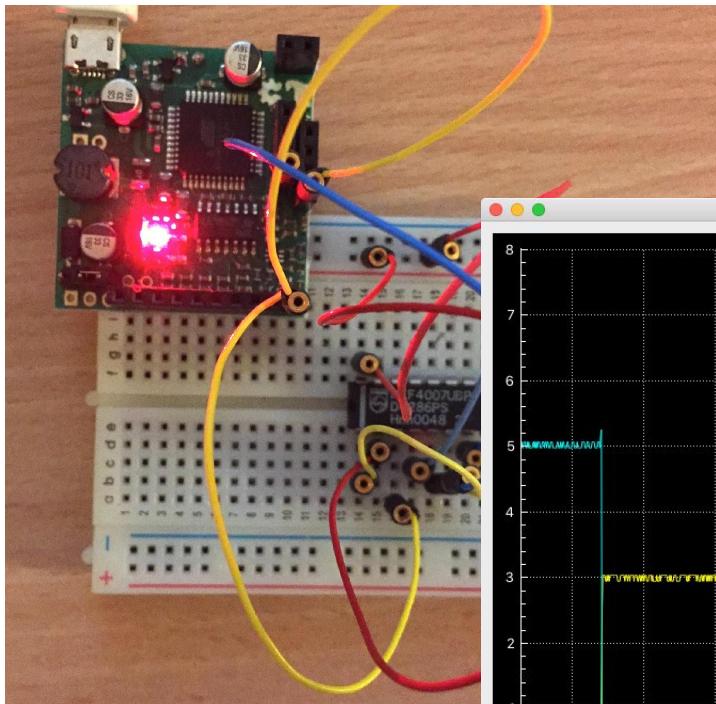
One Open Source Hardware Board

On-board is a complete arsenal of electronic engineering instruments: **only \$29**

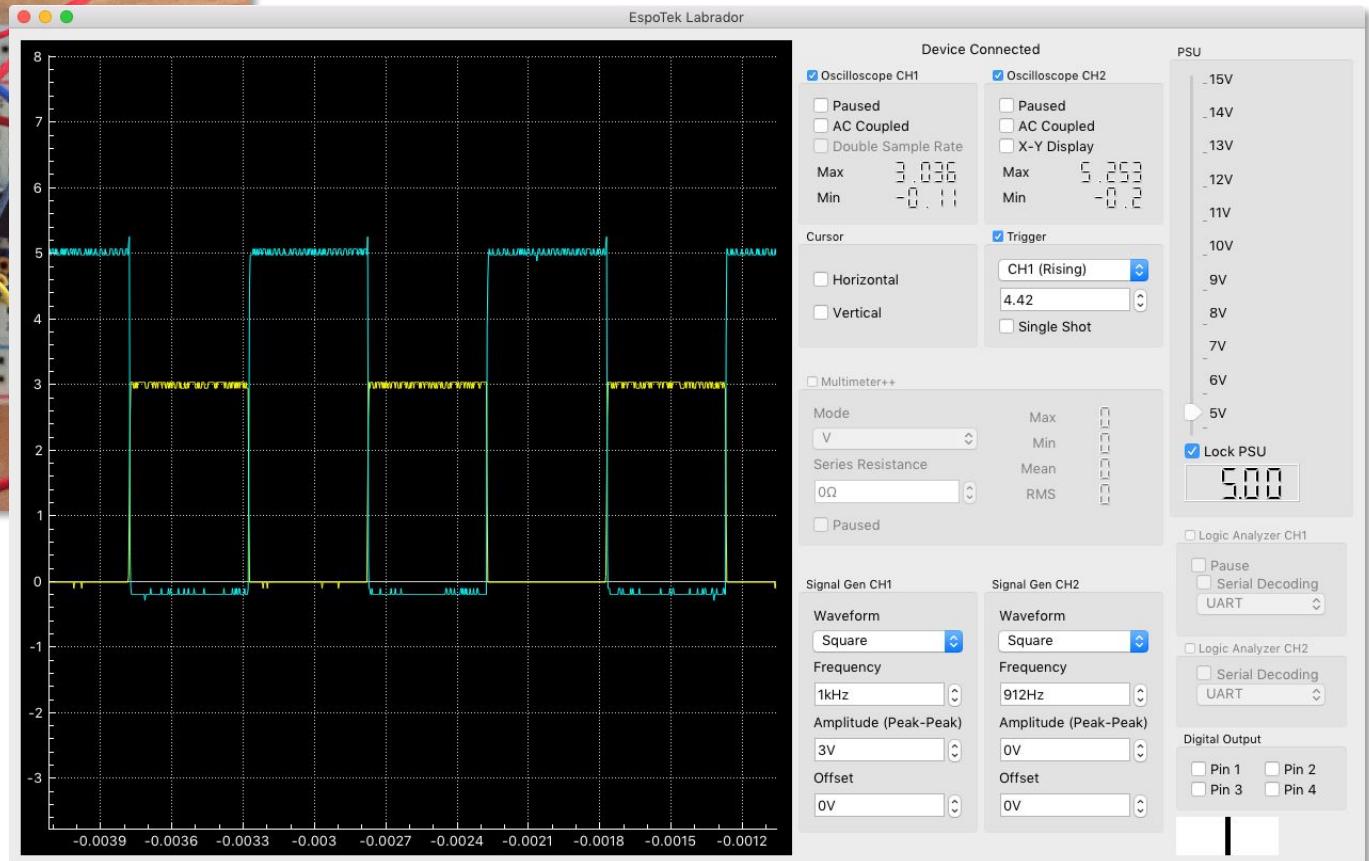


- A. Power Supply (4.5 to 15V, 1.5W max)
- B. Digital Output
- C. Function Generator (2 channel, 1MSPS)
- D. Oscilloscope/Multimeter (2 channel, 750kSPS)
- E. Logic Analyzer (2 channel, 3MSPS)

EspoTek Labrador

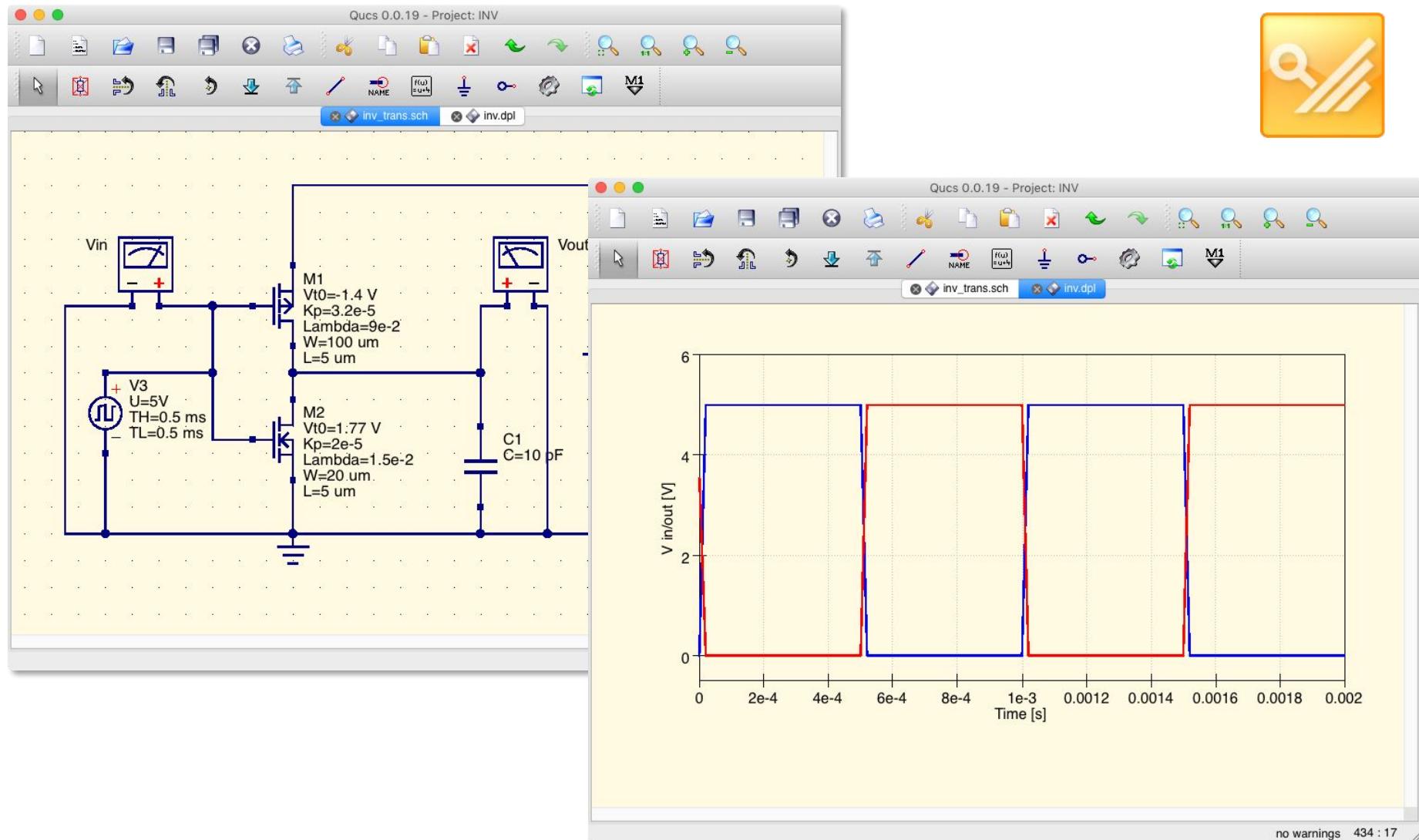


4007 CMOS inverter chip measurement



[REF] <https://espotek.com/labrador>

Qucs: Quite Universal Circuit Simulator

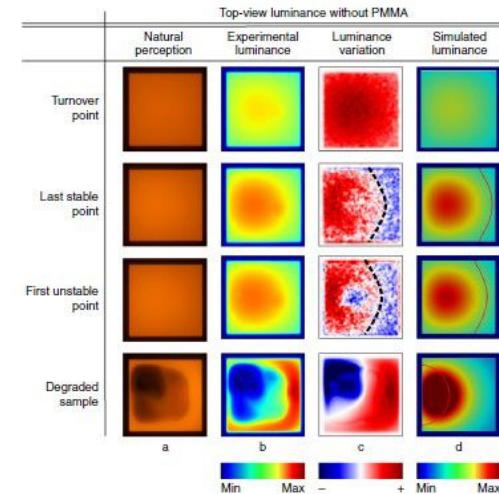
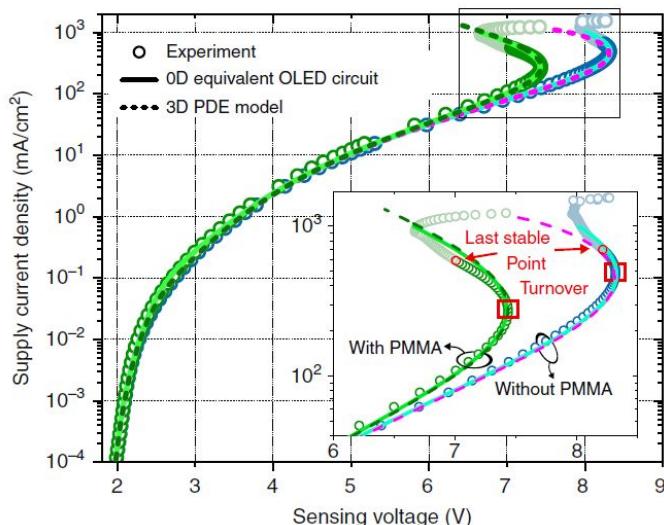
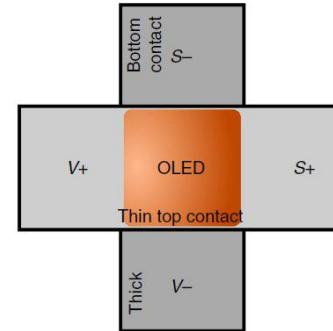


[REF] <http://qucs.sourceforge.net/>

SweepMe! <https://sweep-me.net/>

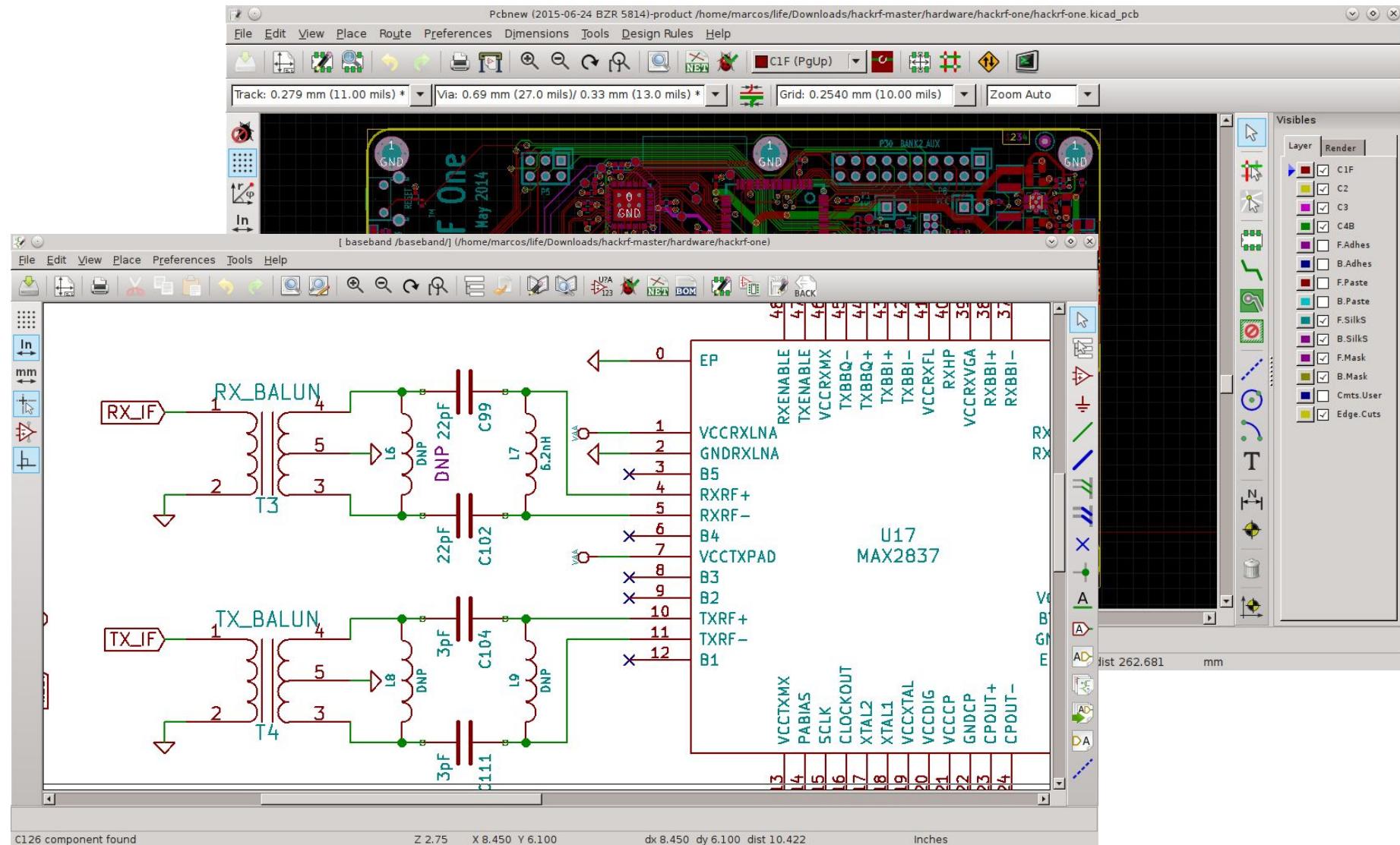
Sequencer:

Measurement tree	Value
MakeFile	ID
Temperature	HAT Control
SMU supply	Keithley26xx Ch A
SMU sense	Keithley26xx Ch B
SMU PD	Keithley2400
Camera1	Webcam

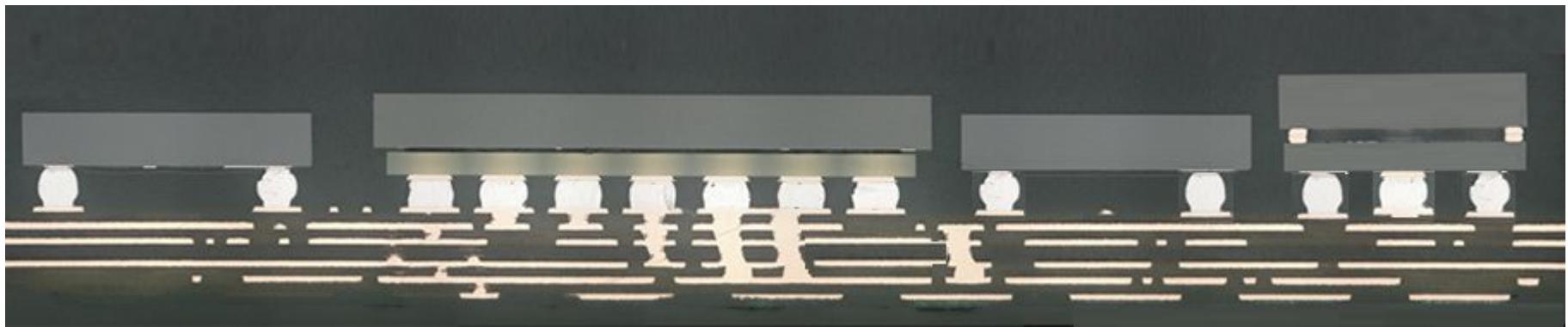


[REF] Kirch, Anton, Axel Fischer, Matthias Liero, Jürgen Fuhrmann, Annegret Glitzky, and Sebastian Reineke. "Experimental proof of Joule heating-induced switched-back regions in OLEDs." *Light: Science & Applications* 9, no. 1 (2020): 5.

ngspice & KiCAD



KiCAD: PCB Cross Section



A cross-section of a multilayer PCB with the electronic components (analog/digital ICs)

Spice/Verilog-A Simulator

The screenshot shows the Spice-SI V0.90 Verilog-A Extension Kernel interface. The main window is a Verilog-A code editor with a toolbar at the top and a hierarchical tree view on the left. The code in the editor is as follows:

```
parameter real GAMMA = 0.7 from[0.0:inf];
parameter real PHI = 0.5 from[0.2:inf];
//*** Mobility parameters (long-channel)
parameter real KP = 20E-6 from[0.0:inf];
parameter real THETA = 50.0E-3 from[0.0:inf];
analog begin // EKV v2.6 long-channel
  VG = V(g); VS = V(s); VD = V(d);
  // Effective gate voltage (33)
  VGprime = VG - VTO + PHI + GAMMA * sqrt(PHI);
  // Pinch-off voltage (34)
  VP = VGprime - PHI - GAMMA
    * (sqrt(VGprime+(GAMMA/2.0)*(GAMMA/2.0))-(GAMMA/2.0));
  // Slope factor (39)
  n = 1.0 + GAMMA / (2.0*sqrt(PHI + VP + 4.0*$vt));
  // Mobility equation (58), (64)
  beta = KP * (V/L) * (1.0/(1.0 + THETA * VP));
  // forward (44) and reverse (56) currents
  x=(VP-VS)/$vt; iff = (ln(1.0+exp( x /2.0)))*(ln(1.0+exp( x /2.0)));
  x=(VP-VD)/$vt; ir = (ln(1.0+exp( x /2.0)))*(ln(1.0+exp( x /2.0)));
  // Specific current (65)
  Ispec = 2 * n * beta * $vt * $vt;
  // Drain current (66)
  Id = Ispec * (iff - ir);
  //
  // Branch contributions to EKV v2.6 model (long-channel)
  //
  I(d,s) <+ Id;
end // analog
endmodule
```

Below the code editor is a status window displaying the following text:

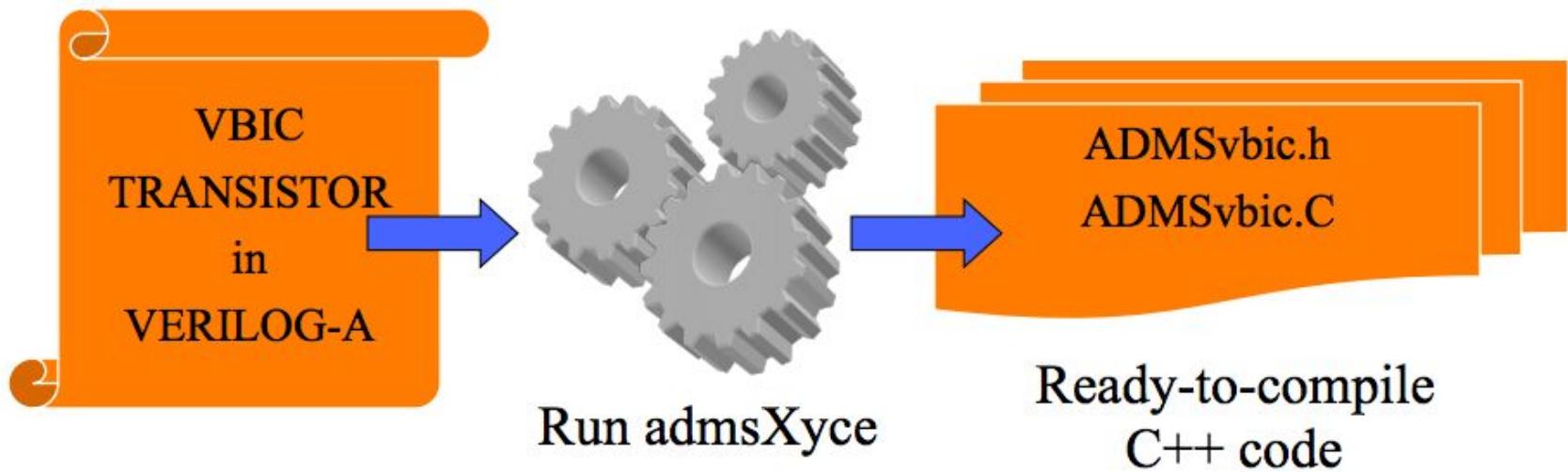
```
Spice-SI V0.90 Verilog-A Extension Kernel. Demonstration Version.
Copyright (c) 1990 by Regents of the University of California.
Copyright (c) 1995-1997 by Apteq Design Systems, Inc.
All rights reserved.
```

The bottom of the interface includes a toolbar, an output pane labeled "Output", and status indicators for help, line number, and column number.

[REF] Dan Fitzpatrick and Ira Miller. *Analog behavioral modeling with the Verilog-A language*. Springer Science & Business Media, 1998. ISBN 0-7923-8044-4

Xyce is an open source, SPICE-compatible, high-performance analog IC simulator

- Verilog-A interface, via ADMS model compiler
 - VBIC, Mextram, EKV, HiCUM, etc.
- Verilog-A: industry standard format for new models
- ADMS translates Verilog-A to compatible C/C++ code;
- API automatically handles data structures, matrices, tedious details.



[REF] <https://xyce.sandia.gov/>

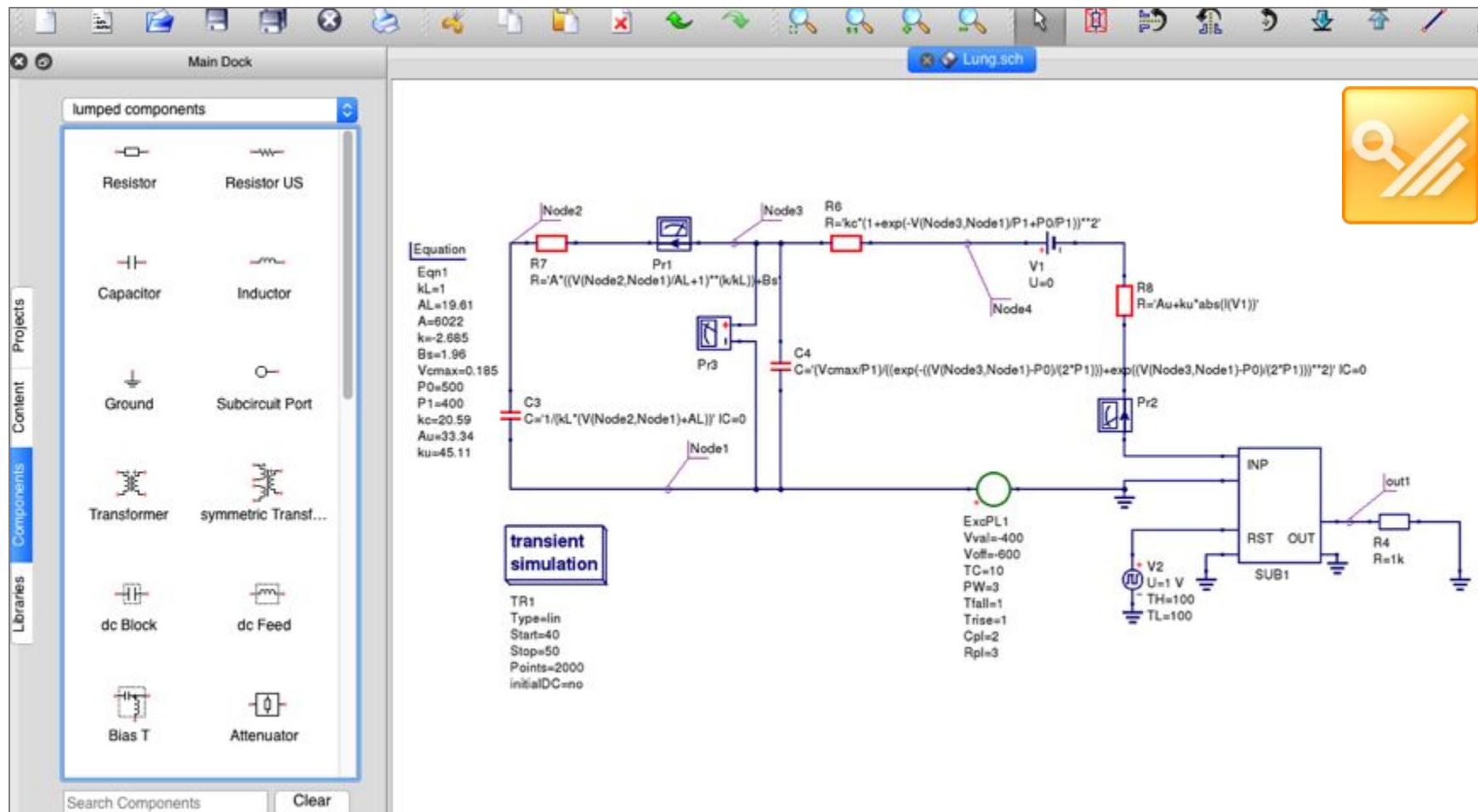


Gnucap: GNU Circuit Analysis Package

- Gnucap is a modern post-spice circuit simulator with several advantages over Spice derivatives.
- Additional Gnucap GIT repositories:
 - ADMS model compiler
 - Device models
 - Gnucap-modelgen Verilog model compiler

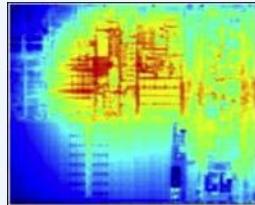
Lung/Airway SPICE Model

Qucs Implementation



[REF] F.N. Masana “Lung/Airway Dynamic Model Using ABM Elements and PSPICE”
Proceedings of the 22nd International Conference MIXDES, June 25-27, 2015, Torun, Poland

Design of Bio/Med Electronic Systems



Thermics



Optics

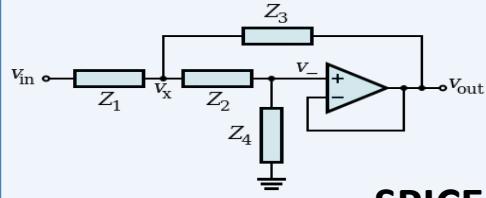


Mechanics



Fluidics

Electronic Circuit



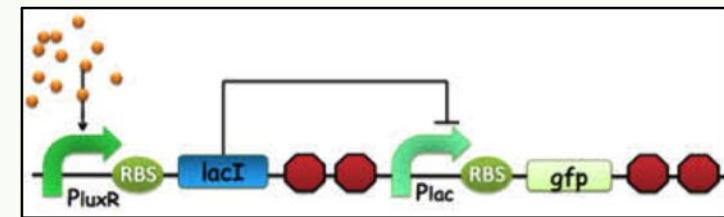
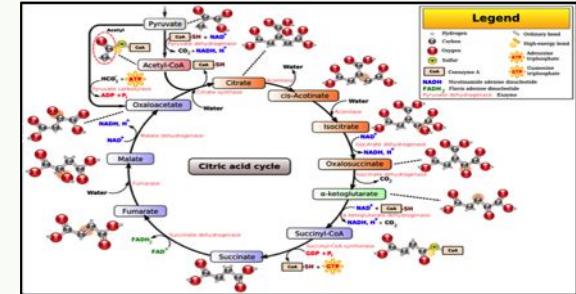
SPICE

VHDL-AMS Verilog-AMS

Modelica <http://modelica.org>

VHDL-AMS <http://www.eda.org/vhdl-ams/>

Verilog-AMS <http://www.accellera.org>



SBML

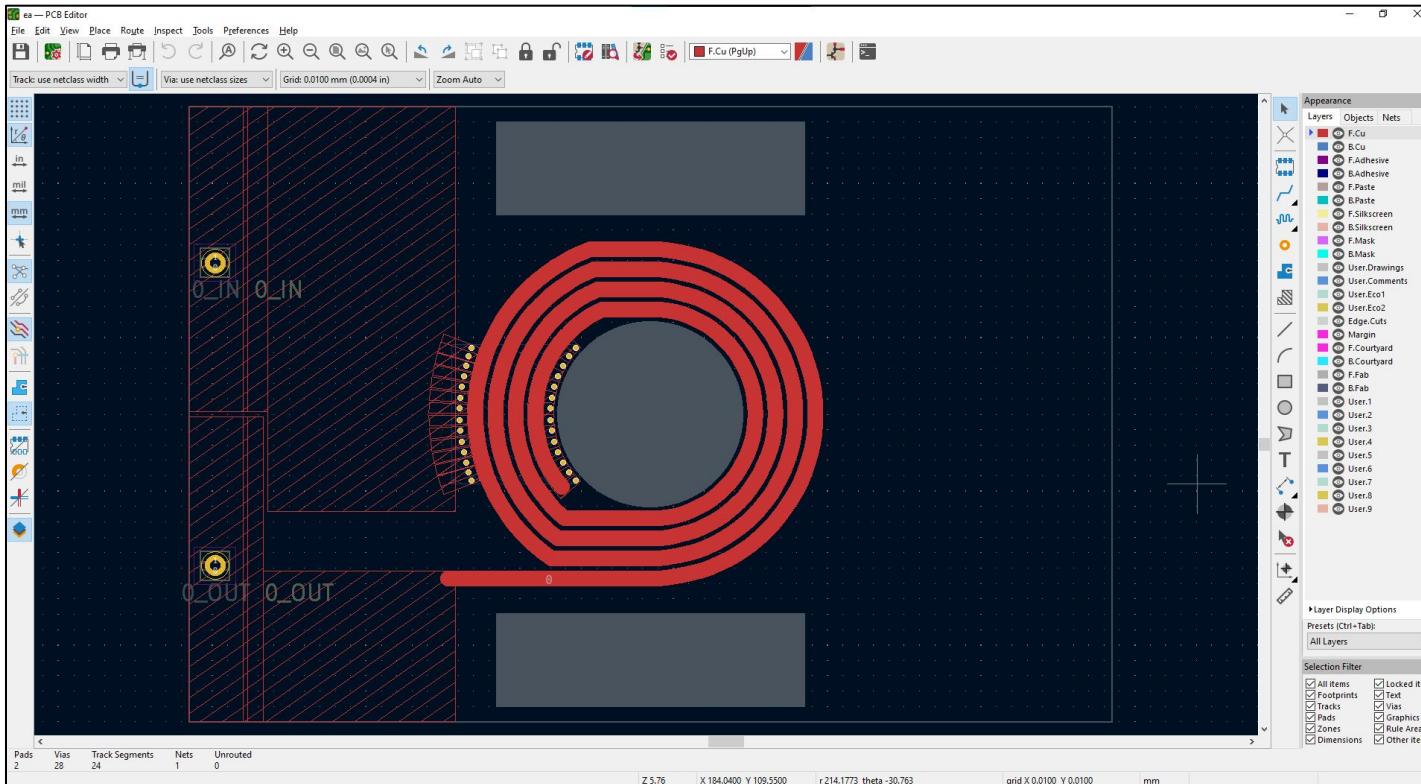
SBML XML <http://sbml.org/>

FAME <http://f-a-m-e.fame-vu.cloudlet.sara.nl/>

Cell Designer <http://celldesigner.org/>

- VHDL-AMS is a derivative of the hardware description language VHDL (IEEE standard 1076-1993). It includes analog and mixed-signal extensions (AMS) in order to define the behavior of analog and mixed-signal systems
- The **Systems Biology Markup Language (SBML)** is a representation format, based on XML, for communicating and storing computational models of biological processes.

OpenMagnetics

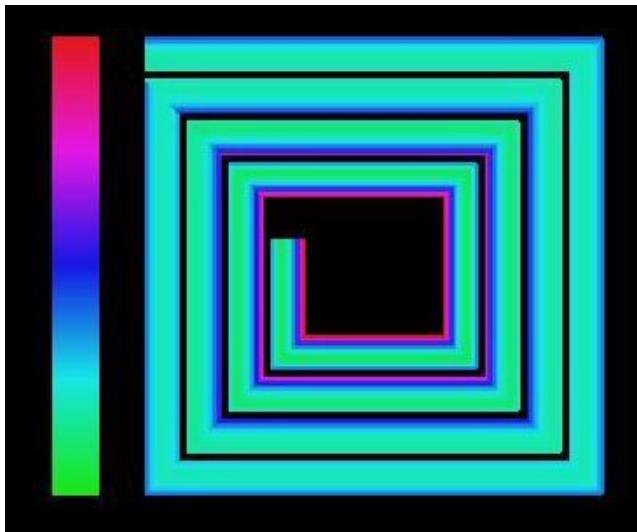


OpenMagnetics allows:

- Introduce any waveform (even by hand!) and get its harmonics, effective frequency, RMS and THD.
- Customize any magnetic core shape as you like, and get its effective parameters.
- Add gapping to your core, distributed, spacer, grinded, in any column, at any position; and get its reluctance and storable energy.
- Download the 3D model or technical drawing of your customized or commercial gapped core

[REF] <https://openmagnetics.com/>
<https://autoplanar.com/>

ASITIC: Analysis and Simulation of Spiral Inductors and Transformers for ICs



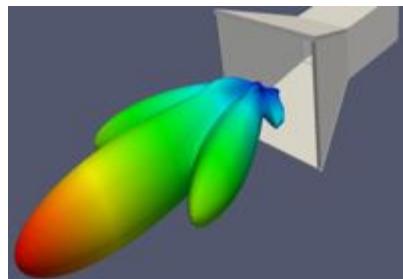
ASITIC is CAD tool that aids the RF circuit designer to optimize and model spiral inductors, transformers, capacitors, and substrate coupling. The conductive substrate plays an integral part in determining the quality factor and self-resonance frequency of monolithic passive devices. ASITIC calculations include the electrically induced losses and coupling as well as the magnetically induced eddy current losses. Skin effect and proximity effects, or eddy currents in the metallization, are also included.

FOSS Computational Electromagnetic (EM) Modeling Tools

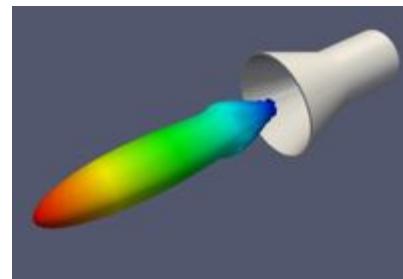
The software in this list is either free or available at a nominal charge and can be downloaded over the internet. Some of the codes require the user to register with the distributor's website. If you are familiar with other free EM modeling software that that should be added to this list, please send the name of the software, a hypertext link, and a brief description to CVEL-L@clemson.edu.

ASAP - Antenna Scatterers Analysis Program	MMANA-GAL (basic version)
AtaiTec Free 2D Field Solver	MEEP
ATLC - Arbitrary Transmission Line Calculator	MMTL
ATLC2 - Arbitrary Transmission Line Calculator 2	Multiple Multipole (MMP) Algorithms
emAnalyze	NEC2
EMAP	newFasant (student version)
EMCoS Antenna VLab SV	openEMS
EM Explorer	pdnMesh
emGine Environment	Puma-EM
ERMES	Qsci
FastCap and FastHenry	Radia
FEKO LITE	SATE Static Field Analysis Toolkit (Educational)
FEMM - Finite Element Method Magnetics	Students' QuickField
gprMax	Sonnet Lite
MagNet (Infolytica)	Trace Analyzer

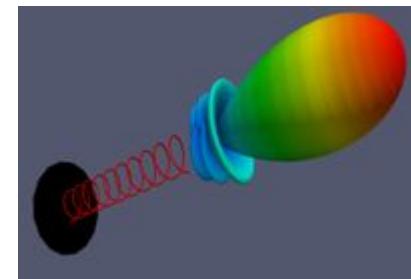
openEMS: FOSS Electromagnetic Field Solver



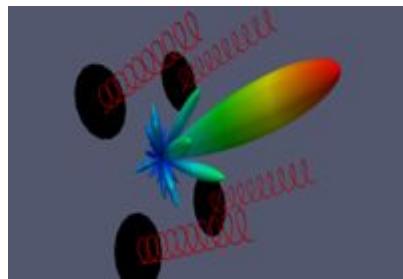
Horn antenna



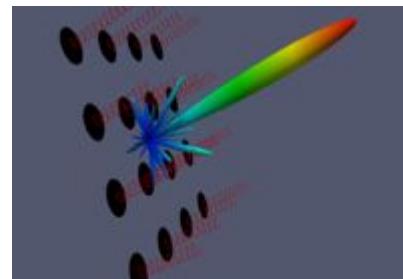
Conical horn antenna



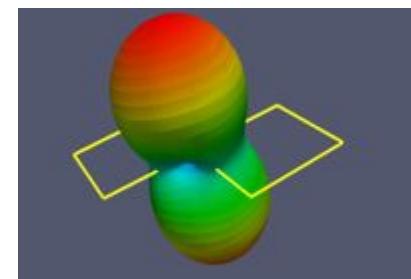
Helix antenna



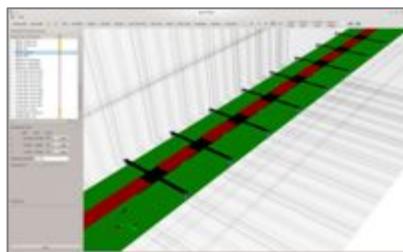
Helix antenna array



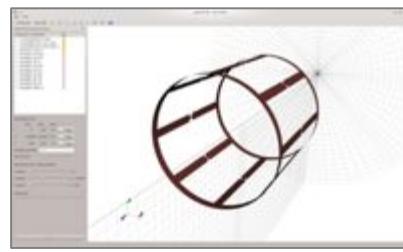
Large helix antenna array



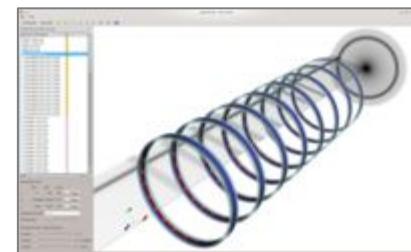
Biquad antenna



CRLH antenna

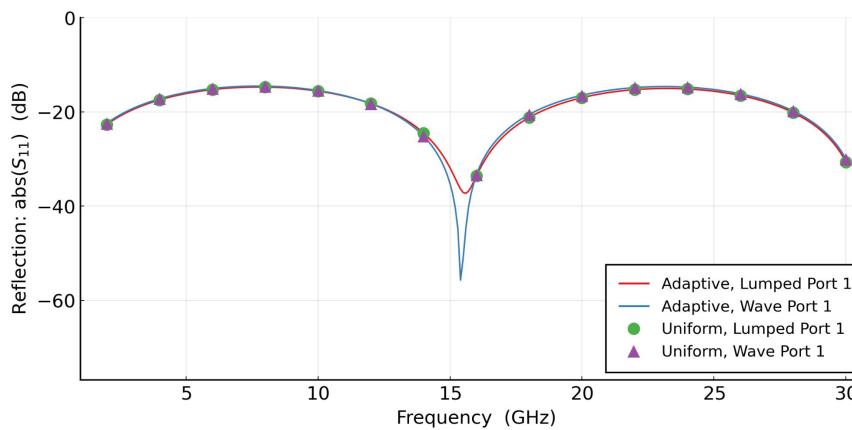
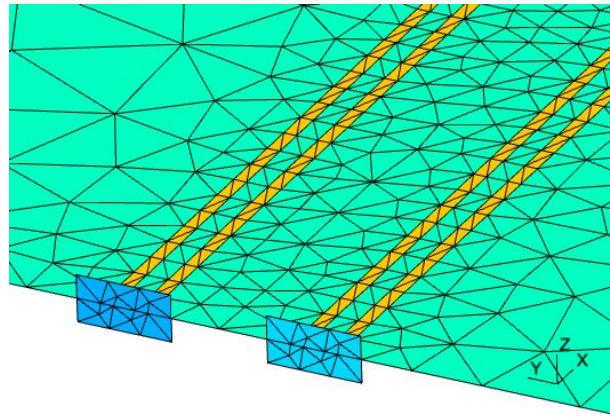
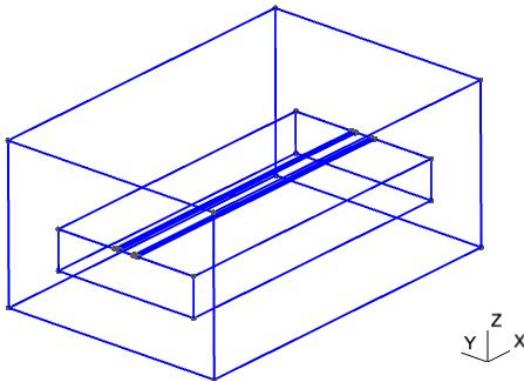


MRI birdcage model



MRI ring antennas

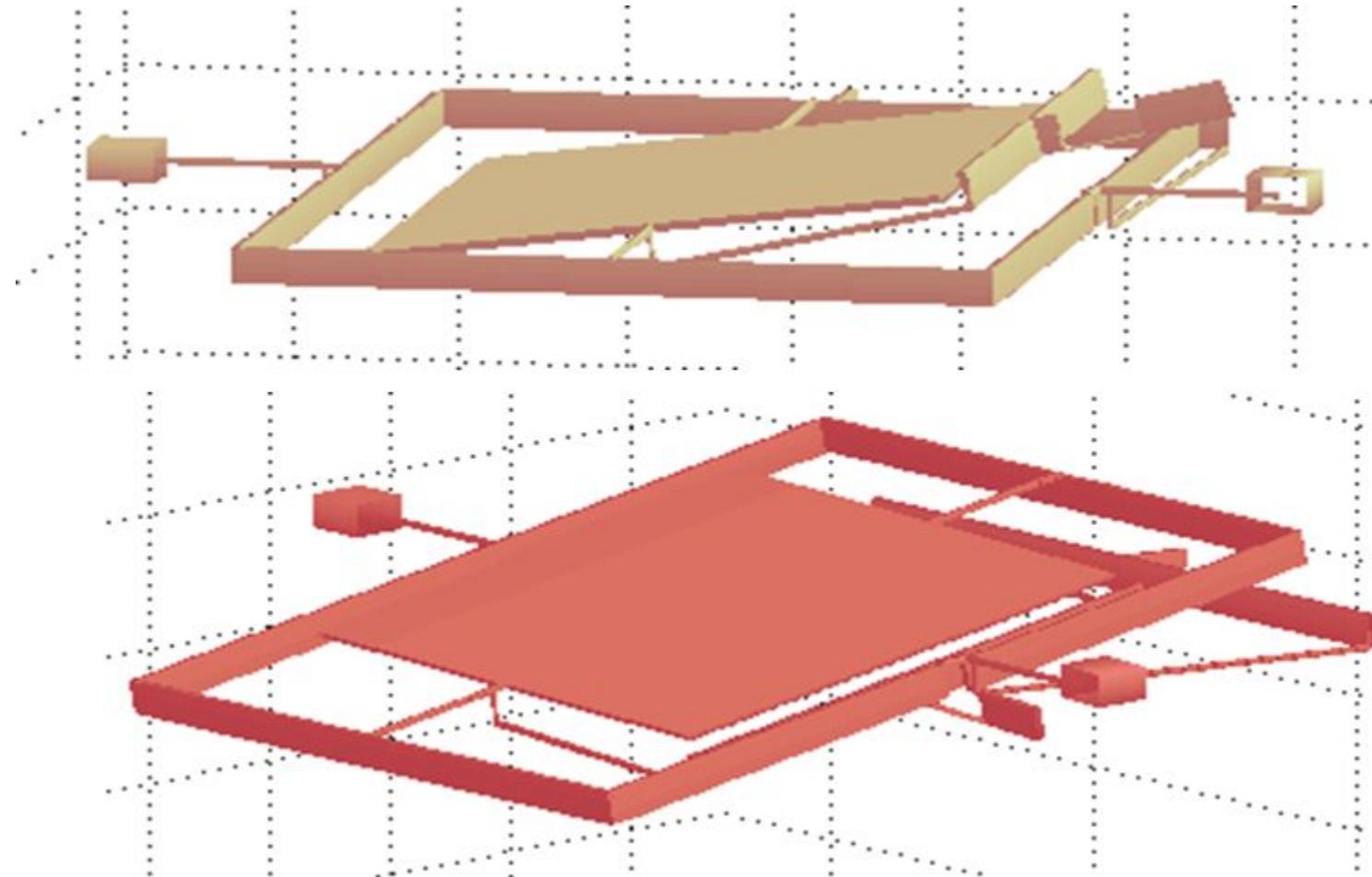
Palace: 3D Finite Element Solver for Computational Electromagnetics



Crosstalk Between Coplanar Waveguides Palace: 3D Example

[1] H. J. Visser, Antenna Theory and Applications, Wiley, Hoboken, NJ, 2012.

SUGAR: FOSS Tool for MEMS

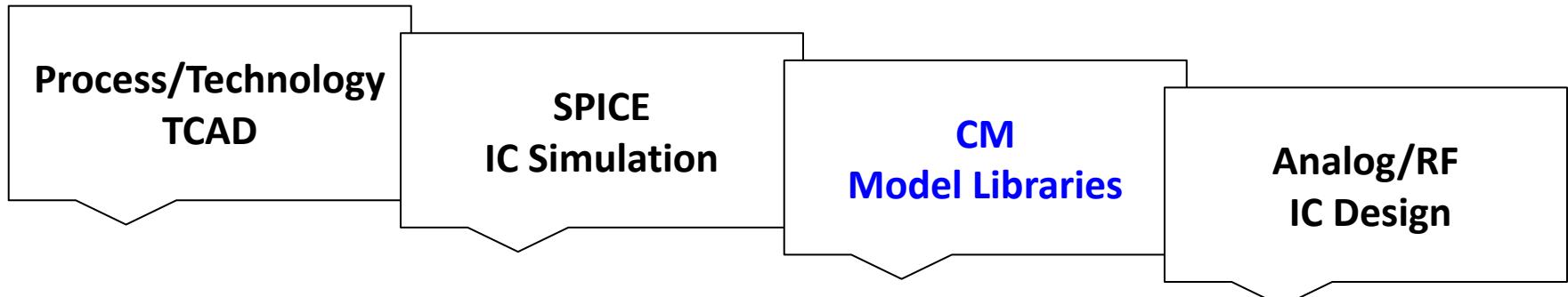


Two-degree-of-freedom optical scanner prototype
Mode 1 = 739Hz, mode 2 = 745Hz.

[REF] www-bsac.eecs.berkeley.edu/cadtools/sugar/

[REF] https://en.wikipedia.org/wiki/Vibrating_structure_gyroscope

FOSS TCAD/EDA Tools for Compact Modeling



- Cogenda TCAD
 - DevSim TCAD
 - Stanford TCAD
 - TU Wien TCAD
 - IIS ETHZ TCAD
 - Uni Glasgow NESS
 - Nextnano
 - QUANTUM ESPRESSO
 - EM Simulators
 - MEMS Simulators
 - other
- Ngspice
 - Qucs
 - Xyce
 - GnuCap
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 - other
- Verilog-A Standardization
 - ADMS
 - OpenVAF
 - MAPP
 - measurements
 - SweepMe!
 - parameterization
 - TRADICA
 - DMT
 - other
- IC Schematic
 - IC Layout Editors
 - DRC, LVS
 - other

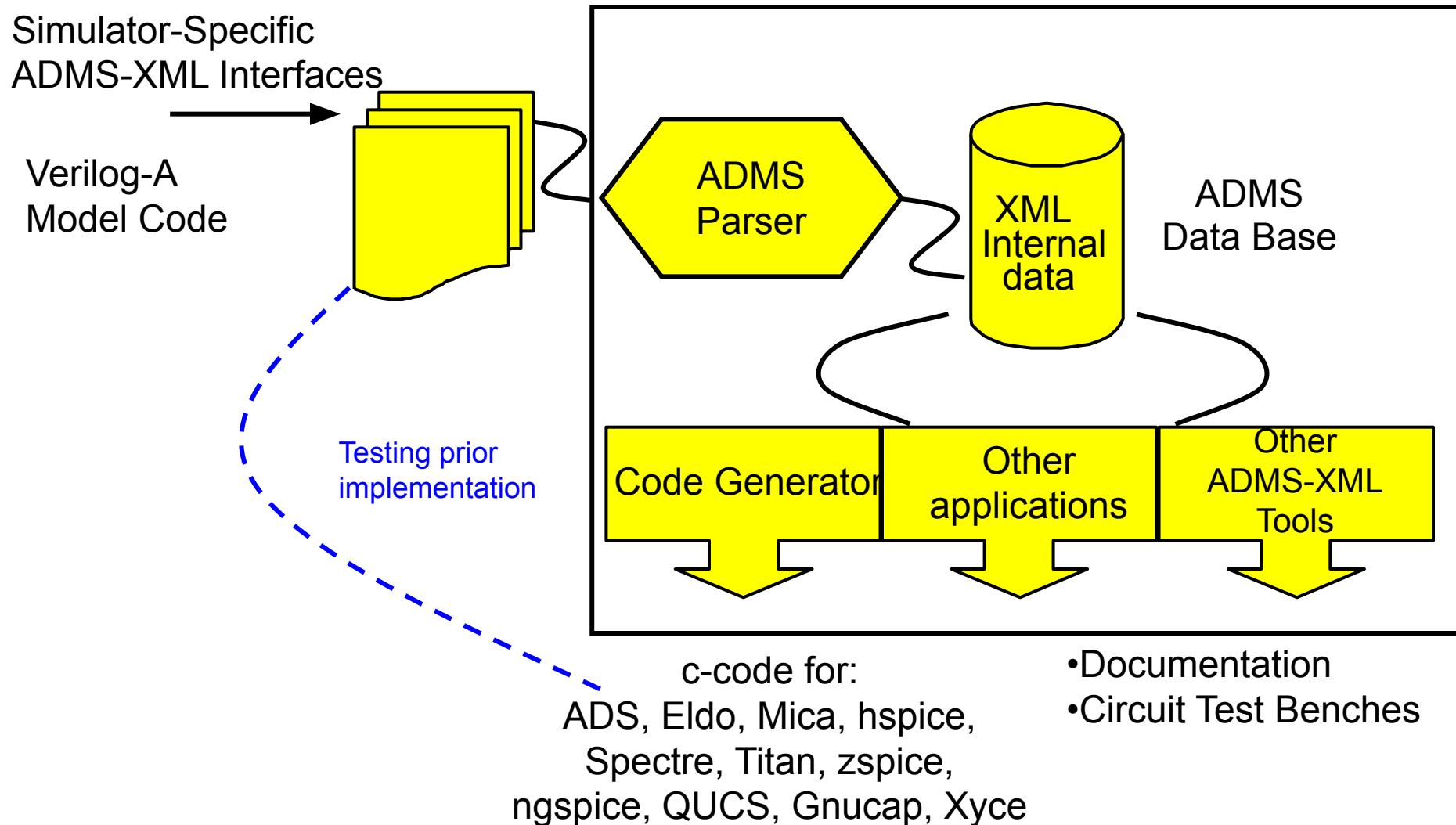
Selection of FOSS Verilog-A Tools

- ADMS
 - Still the most capable open-source model compiler available
- MAPP (Verilog-A Parser and Processor)
 - Translates Verilog-A device models into ModSpec, a device modeling specification & compiler
 - Used with the NEEDS project (<https://nanohub.org/groups/needs>)
- VALint:
 - a NEEDS Verilog-A Quality Checker
 - VALint is open-source
- VAMPyRE (Verilog-A Model Pythonic Rule Enforcer)
 - Verilog-A compact model parser and checker
 - Supported by the Compact Model Coalition (CMC)
www.si2.org/standard-models
- VerilogAE
 - Verilog-A Compiler for Compact Model Parameter Extraction
- OpenVAF: Next-Generation Verilog-A compiler
 - <https://openvaf.semimod.de/>

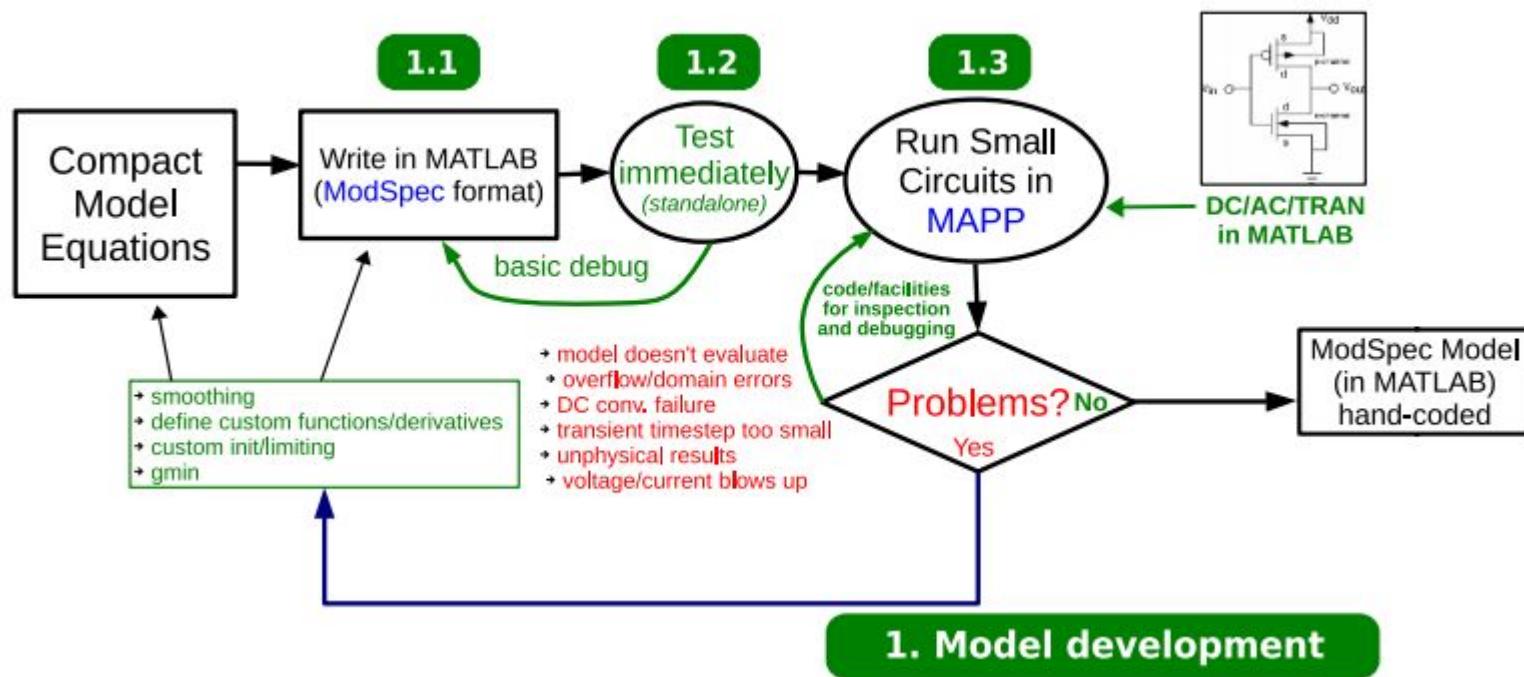
Benefits Using Verilog-AMS

- For the model developers
 - Develop once and run everywhere
 - Focus on model equation, not on implementation
- For the software vendors
 - Simplified implementation of the standard models
 - Proprietary Verilog-A models are also supported
- For the silicon fabs
 - Standardized model parameter set
- For the end-users (designers)
 - Standardized libraries and design kits

ADMS - Overview

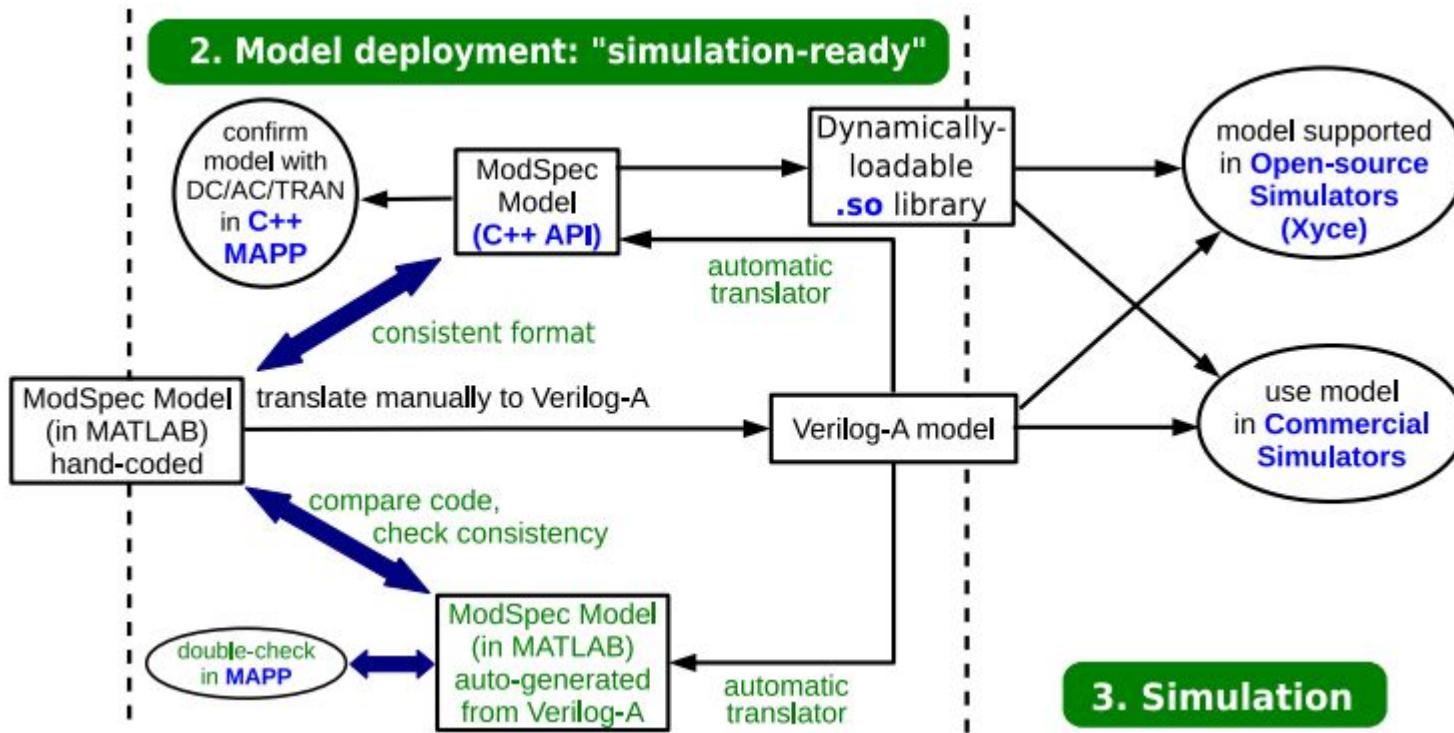


Model and Algorithm Prototyping Platform (MAPP)



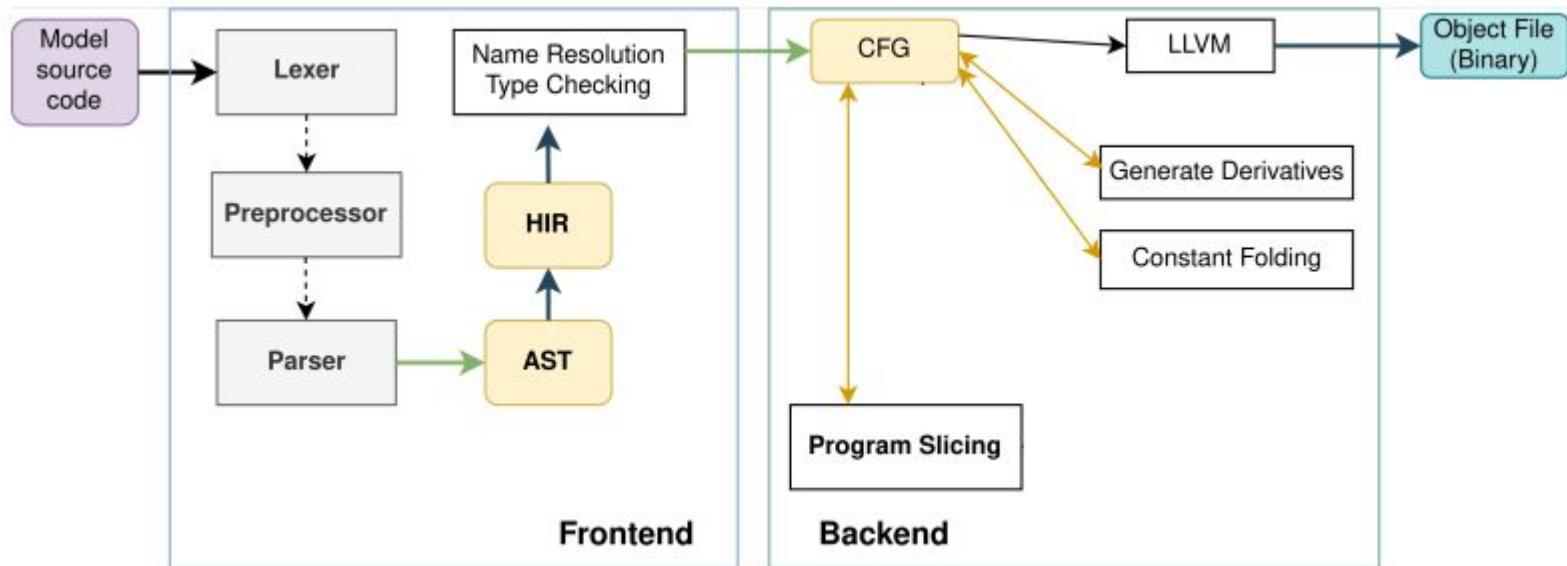
Berkeley MAPP is a MATLAB-based platform for prototyping numerical models and simulation algorithms. MAPP also runs in Octave.

Model and Algorithm Prototyping Platform (MAPP)



MAPP eases the process of developing new device models and simulation algorithms, especially for those who do not have an extensive background in compact modelling or experience coding algorithms in simulators.

OpenVAF: Next-Generation Verilog-A compiler that empowers the open source silicon revolution



OpenVAF Roadmap

- Reaching full compliance with the Verilog-A standard
 - Behavioral modelling features
 - Support for features that allow defining full circuits/full PDKs in Verilog-A
- OSDI integration in Xyce
- Noise analysis (planned for 2023)
- Improved documentation
- A detailed paper about the technical innovations in OpenVAF and attendance at international conferences

[REF] P. Kuthe, M. Muller and M. Schroter, “VerilogAE: An open source Verilog-A compiler for compact model parameter extraction”, J-EDS, vol. 8, pp. 1416–1423, 2020
<https://openvaf.semimod.de/>

FOSS EKV2.6 Verilog-A Compact MOSFET Model

Wladek Grabinski¹, Marcelo Pavanello², Michelly de Souza², Daniel Tomaszewski³, Jola Malesinska³, Grzegorz Głuszko³, Matthias Bucher⁴, Nikolaos Makris⁴, Aristeidis Nikolaou⁴, Ahmed Abo-Elhadid⁵, Marek Mierzwiński⁶, Laurent Lemaitre⁷, Mike Brinson⁸, Christophe Lallement⁹, Jean-Michel Sallese¹⁰, Sadayuki Yoshitomi¹¹, Paul Malisse¹², Henri Oguey¹³, Stefan Cserveny¹³, Christian Enz¹⁰, François Krummenacher¹⁰ and Eric Vittoz¹⁰

¹ MOS-AK Association (EU), ² Centro Universitario FEI, São Bernardo do Campo (BR),

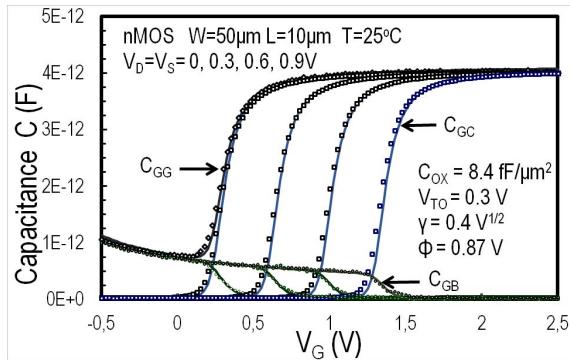
³ Institute of Electron Technology, Warsaw (PL), ⁴ Technical University of Crete, Chania (GR),

⁵ Mentor Graphics (USA), ⁶ Keysight Technologies (USA), ⁷ Lemaitre EDA Consulting,

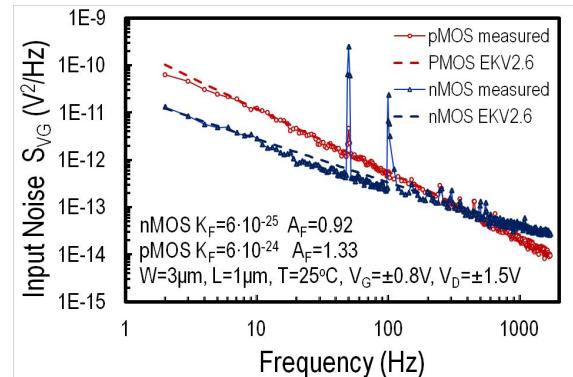
⁸ London Metropolitan University (UK), ⁹ ICube, Strasbourg University (F), ¹⁰ EPFL Lausanne (CH),

¹¹ Toshiba (J), ¹² Europractice/IMEC (B), ¹³ CSEM S.A., Neuchatel (CH)

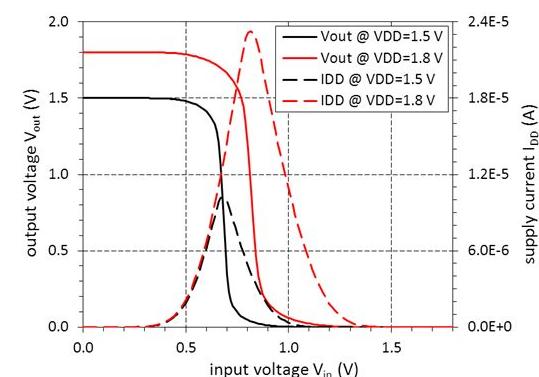
Presented at ESSDERC/ESSCIRC 2019 in Krakow



Extraction of the threshold voltage, flatband voltage and gate capacitance in n-MOSFETs based on C-V



Input power spectral density $S_{VG}(f)$ for nMOSFETs



CMOS inverter characteristics

Acknowledgments: The authors would like to acknowledge Europractice for providing free access to UMC 180nm CMOS silicon and all corresponding libraries and PDKs for the EKV2.6 test chip design and manufacturing. M. A. Pavanello and M. de Souza thank the financial support of Brazilian funding agency CNPq.
[REF] <https://github.com/ekv26/model>

EKV Long Channel Verilog-A Code

```
`include "std.va"
`include "const.va"
// ****
// * EKV MOS model (long channel)
// * https://ekv.epfl.ch/Verilog-A/
// ****
module ekv(d,g,s,b);
//
// Node definitions
inout d,g,s,b ; // external nodes
electrical d,g,s,b ; // external nodes
//
//*** Local variables
real x, VG, VS, VD, VGprime, VP;
real beta, n, iff, ir, Ispec, Id;
//
//*** model parameter definitions
parameter real L = 10E-6 from[0.0:inf];
parameter real W = 10E-6 from[0.0:inf];
//*** Threshold voltage
// substrate effect parameters (long-channel)
parameter real VTO = 0.5 from[0.0:inf];
parameter real GAMMA = 0.7 from[0.0:inf];
parameter real PHI = 0.5 from[0.2:inf];
//*** Mobility parameters (long-channel)
parameter real KP = 20E-6 from[0.0:inf];
parameter real THETA = 50.0E-3 from[0.0:inf];
```

```
analog begin // EKV v2.6 long-channel
VG = V(g); VS = V(s); VD = V(d);
// Effective gate voltage (33)
VGprime = VG - VTO + PHI + GAMMA * sqrt(PHI);
// Pinch-off voltage (34)
VP = VGprime - PHI - GAMMA
* (sqrt(VGprime+(GAMMA/2.0)*(GAMMA/2.0))-(GAMMA/2.0));
// Slope factor (39)
n = 1.0 + GAMMA / (2.0*sqrt(PHI + VP + 4.0*$vt));
// Mobility equation (58), (64)
beta = KP * (W/L) * (1.0/(1.0 + THETA * VP));
// forward (44) and reverse (56) currents
x=(VP-VS)/$vt;
iff = (ln(1.0+exp(x/2.0)))*(ln(1.0+exp(x/2.0)));
x=(VP-VD)/$vt;
ir = (ln(1.0+exp(x/2.0)))*(ln(1.0+exp(x/2.0)));
// Specific current (65)
Ispec = 2 * n * beta * $vt * $vt;
// Drain current (66)
Id = Ispec * (iff - ir);
//
// Branch contributions to EKV v2.6 model (long-channel)
//
I(d,s) <+ Id;
end // analog
endmodule
```

EKV Long Channel SPICE Netlist

```
* EKV long channel MOSFET Model
```

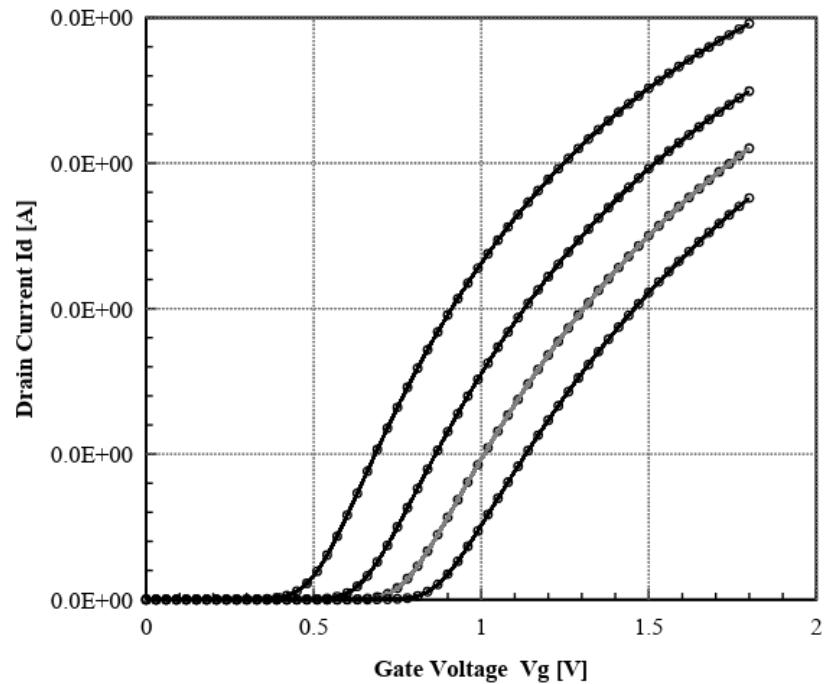
```
.verilog "ekv.va"
```

```
vd 1 0 0.05  
vg 2 0 2  
vs 3 0 0  
vb 4 0 0
```

```
xekv 1 2 3 4 ekv L=1E-6 W=1E-6
```

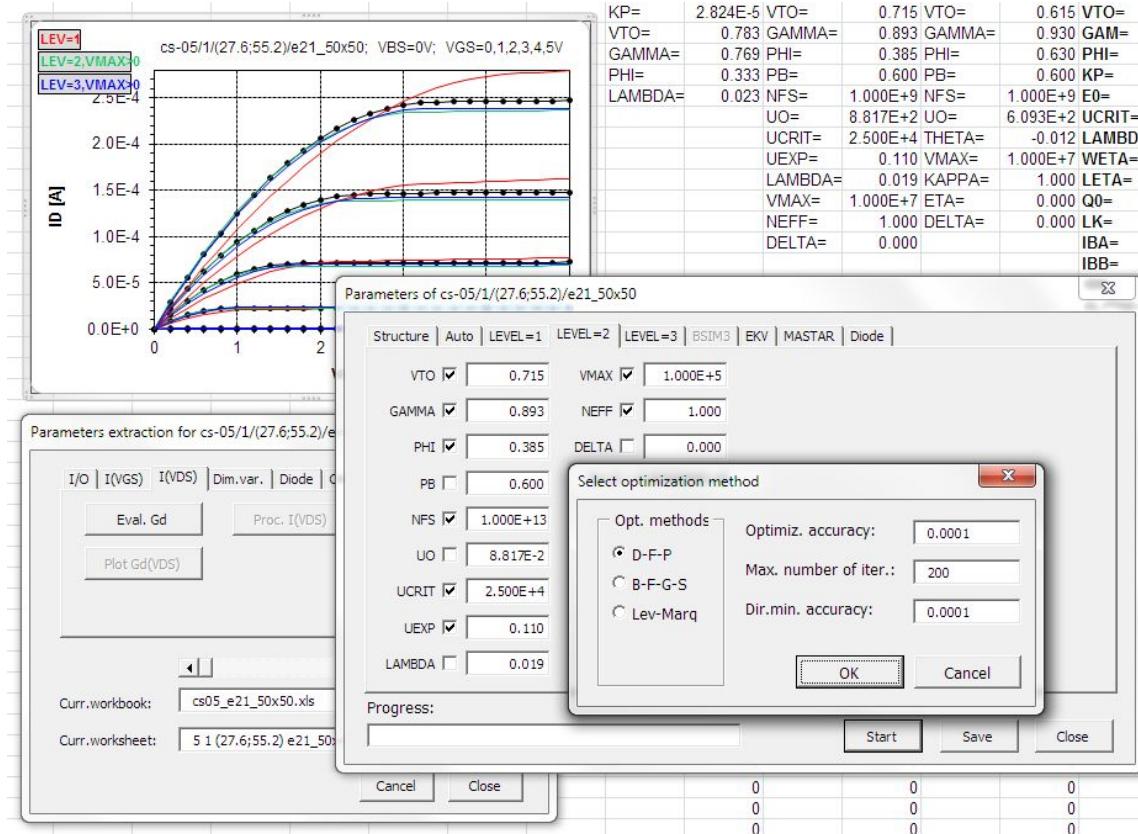
```
.dc vg 0 2 0.1
```

```
.end
```

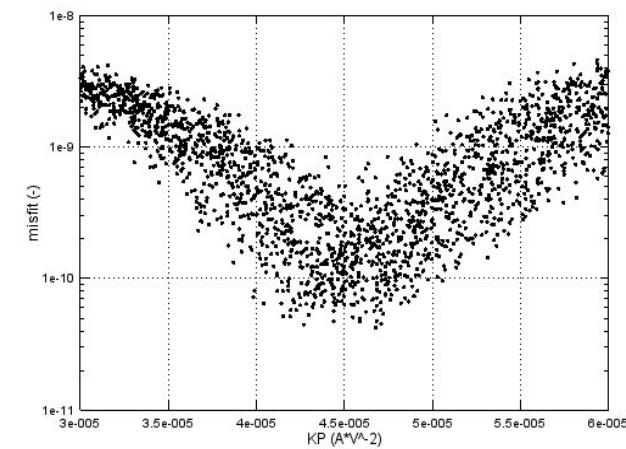
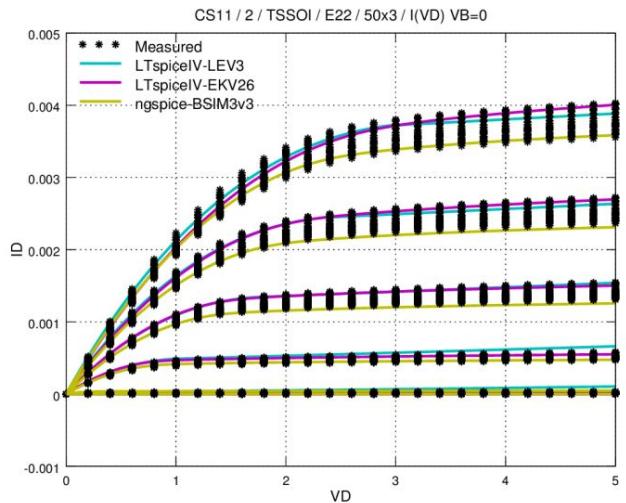
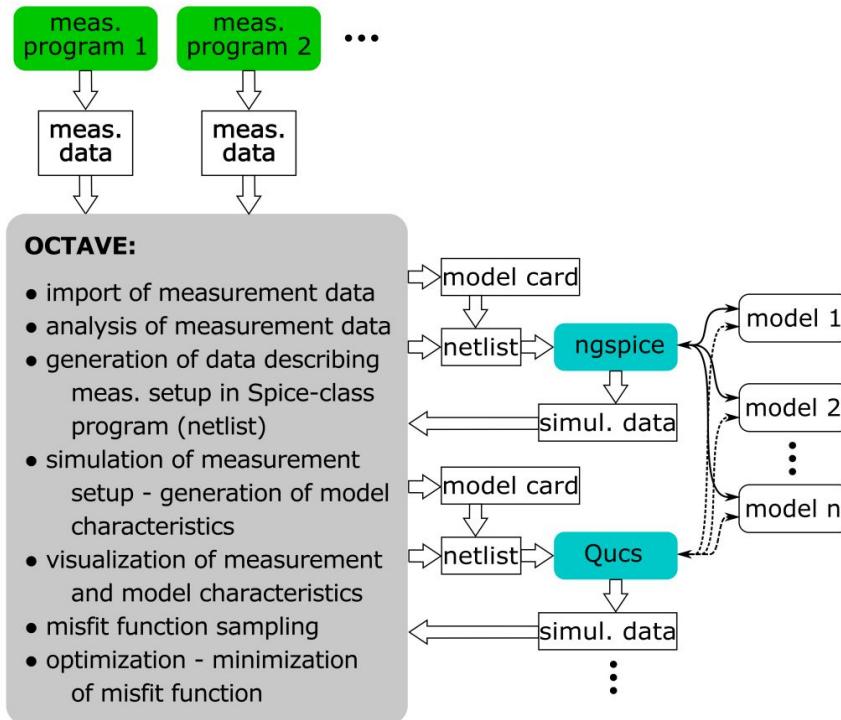


MS Excel VBA Parameter Extraction

- Local parameter extraction using MS Excel VBA optimization



Integrated Tools for Modeling and Parameter Extraction

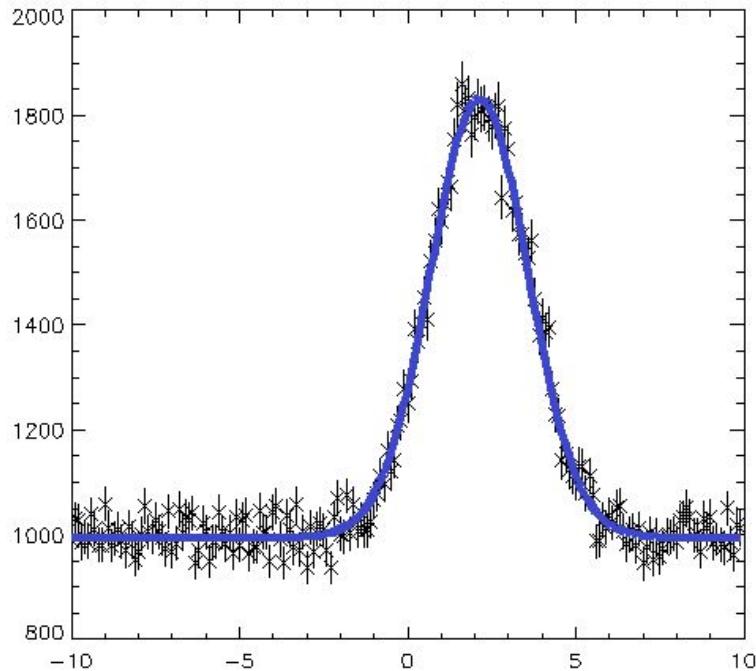


[Ref] D. Tomaszewski, G. Głuszko, M. Brinson, V. Kuznetsov, W. Grabinski, "FOSS as an Efficient Tool for Extraction of MOSFET Compact Model Parameters", MIXDES'2016

IDL Curve Fitting and Optimization

MPFIT - Robust non-linear least squares curve fitting

The IDL routines provide a robust and relatively fast way to perform least-squares curve and surface fitting. The algorithms are translated from **MINPACK-1**, which is a rugged minimization routine found on Netlib, and distributed with permission. This algorithm is more desirable than **CURVEFIT** because it is generally more stable and less likely to crash than the brute-force approach taken by CURVEFIT, which is based upon Numerical Recipes.



TRADICA

TRAnsistor DIimensioning and CAlculation program

- Provide criteria for transistor sizing
 - calculation of device dimensions
 - calculation of device configuration
- Fast means for generating consistent sets of compact model parameters based on design rules and process information
- Compact modeling/extractions for various types of devices and different compact model types
 - MOS (EKV)
 - Bipolar (SGPM, HICUM)
 - Passives (diode, res, mincap, ...)
- Hierarchy modeling with different complexities w.r.t. physical effects

[REF] K.E.Moebus, M.Schröter, H.Wittkopf, Y.Zimmermann, M.Claus; TRAnsistor DIimensioning and CAlculation program
MOS-AK Munich 2007: http://www.mos-ak.org/munich_2007/papers/07_MOS-AK_Moebus.pdf

PROFILE: Inverse Modeling Tool

The **PROFILE** [1] is a tool for inverse modeling of the semiconductor devices using 2D data and advanced optimization driver. All the files and its documentation is available at the official homepage of PROFILE:

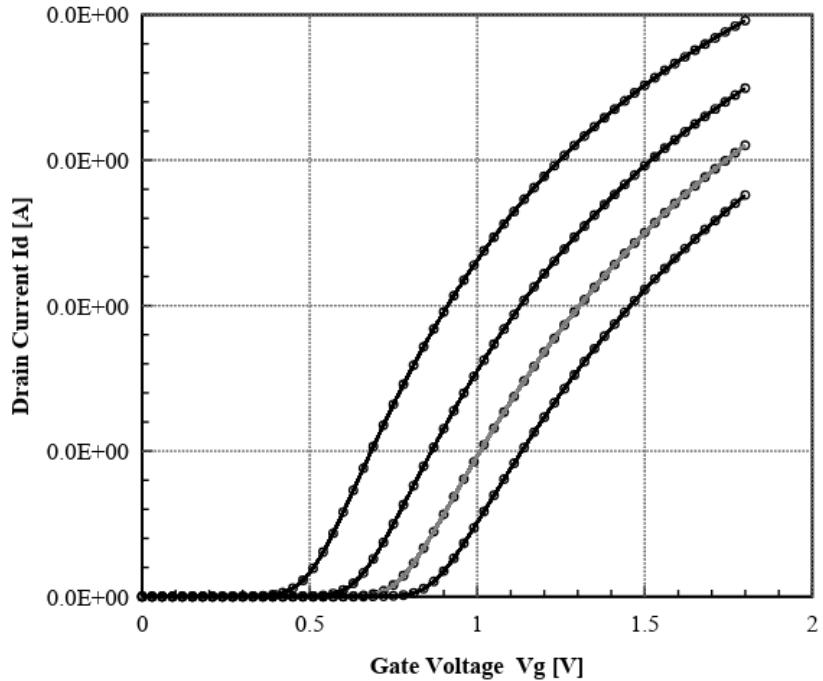
<http://profile.ewi.tudelft.nl/>

<http://sourceforge.net/projects/profile2d>

[REF] G.J.L. Ouwerling. Inverse modelling with the PROFILE optimization driver. NASECODE VI Software Forum, Dublin, July 1989.

PROFILE: Inverse Modeling Tool

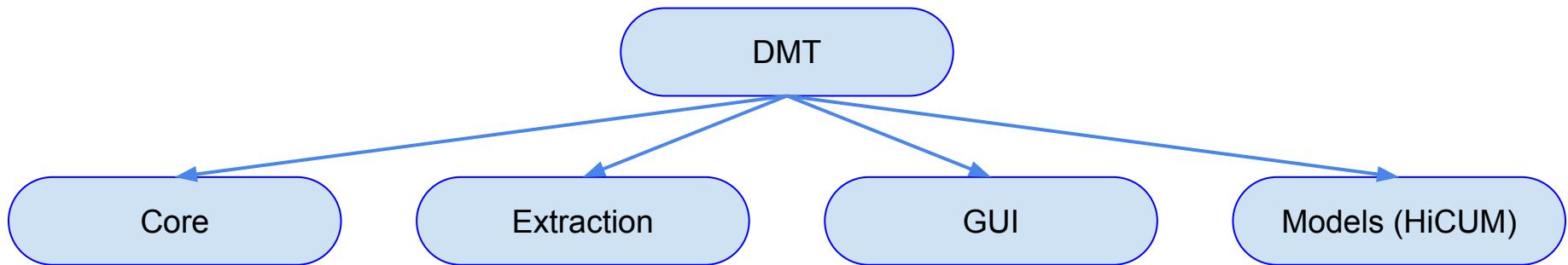
```
: main.pro : main optimization loop
type v_m i_m i_s $
var real VTO UO KP $
: read measured IV data
get IdVg.dat v_m i_m $
: set LEVEL3 parameters
VTO = 1.0
UO = 425
KP = 2E-4
: Constrain specifications
constrain VTO 0.1 2
constrain UO 100 500
constrain KP 0.1E-4 1E-3
setlm deltapr 0.01
: call external non-linear model
setext call ~/bin/profile ngspice.pro >
ngspice.log
setlm talk 2
setlm itermax 15
: levmar fits a non-linear model to
measurement data.
levmar pro i_m v_m i_s VTO KP | UO $
```



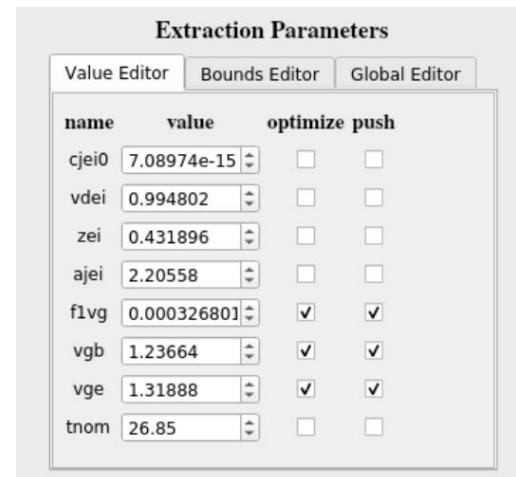
Transfer MOSFET IV characteristic
after VTO, U0, KP extraction
(o :measured, - :simulated)

DMT: Device Modeling Toolkit

Open License Parameter Extraction Toolkit For SiGe HBTs
HiCUM Group at TU Dresden



- Python + Git
 - Reasonable code quality with focus on readability
 - Automated code documentation
- "Glue" open-source software components
- Framework for extending functionality
- Interface to include circuit/SPICE and TCAD DEVICE simulators
- Modular and Reusable widgets for new GUIs
- Not restricted to a single model!



DMT GUI parameter widget

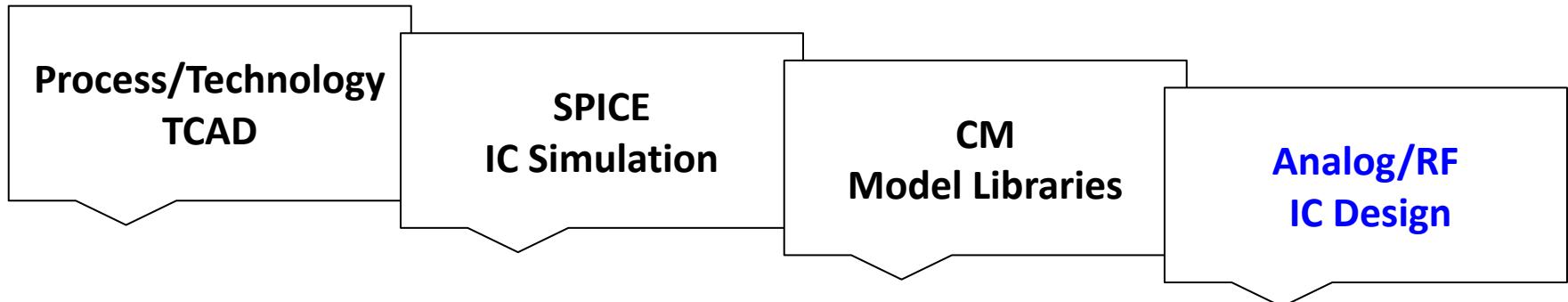
Standardized Data Exchange For Device Modeling Tools

The **MDM** file format (developed and open by **Agilent**) provides the following advantages:

- ASCII based file
- Table-based, row-column format with column header lines that make reading easy-includes a list of the innermost independent variables.
- All data tables have identical shape. A header at the top of the file provides an outline of all the data in the file. After the header has been parsed, the location of any data group can be computed quickly, permitting rapid location of arbitrary data groups scattered throughout the file. Comment lines are denoted by the exclamation character(!). The file extension for the data files is .mdm (**measured data management**).

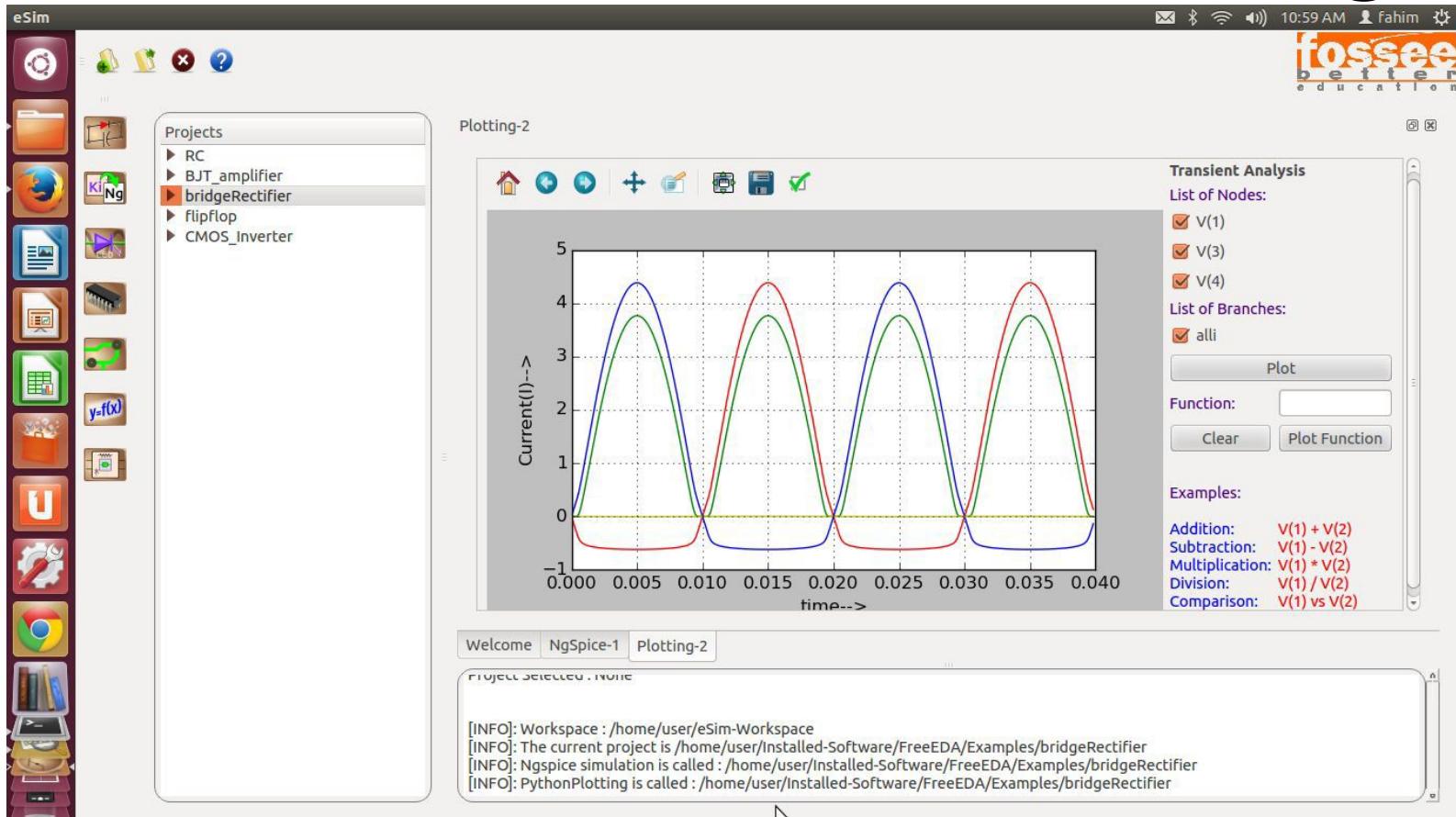
```
! VERSION = 6.00
BEGIN_HEADER
ICCAP_INPUTS
vb V B GROUND SMU1 0.1 LIN 1 0.33 0.45 12 0.01
ve V E GROUND GND 0.1 CON 0
vc V C GROUND SMU2 0.2 SYNC 1 0 vb
ICCAP_OUTPUTS
ib I B GROUND SMU1 B
ic I C GROUND SMU2 B
END_HEADER
BEGIN_DB
ICCAP_VAR ve 0
#vb vc ib ic
0.33 0.33 4.87574e-011 4.67239e-010
0.34 0.34 5.77546e-011 6.85381e-010
0.35 0.35 6.86361e-011 1.00538e-009
0.36 0.36 8.18976e-011 1.47476e-009
0.37 0.37 9.82047e-011 2.16325e-009
0.38 0.38 1.18461e-010 3.17307e-009
0.39 0.39 1.43910e-010 4.65412e-009
0.4 0.4 1.76281e-010 6.82619e-009
0.41 0.41 2.18003e-010 1.00115e-008
0.42 0.42 2.72518e-010 1.46826e-008
0.43 0.43 3.44737e-010 2.15321e-008
0.44 0.44 4.41716e-010 3.15754e-008
END_DB
```

FOSS TCAD/EDA Tools for Compact Modeling



- Cogenda TCAD
 - DevSim TCAD
 - Stanford TCAD
 - TU Wien TCAD
 - IIS TEHZ TCAD
 - Uni Glasgow NESS
 - Nextnano
 - QUANTUM ESPRESSO
 - EM Simulators
 - MEMS Simulators
 - other
- Ngspice
 - Qucs
 - Xyce
 - GnuCap
 - FOSSEE eSim
 - other
- Verilog-A Standardization
 - ADMS
 - OpenVAF
 - MAPP
 - measurements
 - SweepMe!
 - parameterization
 - TRADICA
 - DMT
 - other
- IC Schematic
 - IC Layout Editors
 - DRC, LVS
 - other

eSim FOSSEE Tool for IC Design



Features of eSim

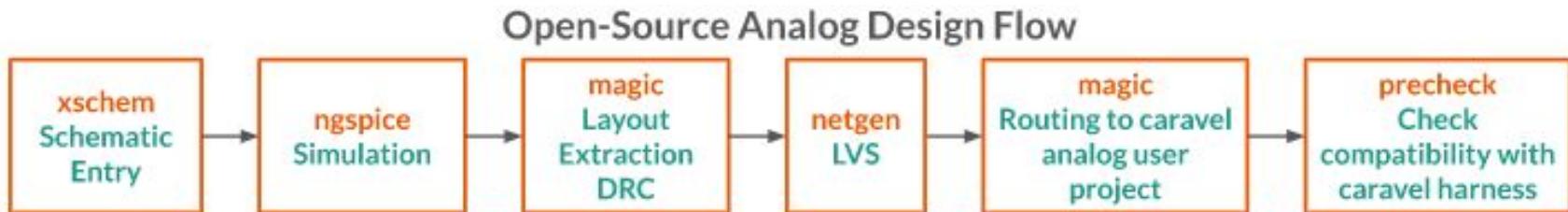
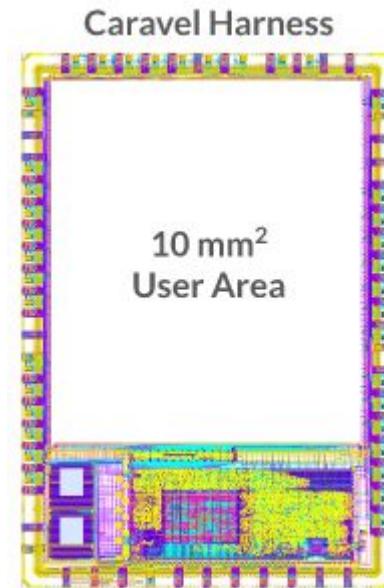
- Draw circuits using **KiCad**, create a netlist and simulate using **ngspice**
- Add/Edit SPICE Models and subcircuits using the Model / Subcircuit Builder tools
- Perform Mixed-Signal ngspice Simulation
- Design PCB layouts and generate Gerber files using KiCad
- Support for Ubuntu and Windows

[REF] <https://esim.fossee.in/home>

FOSS Analog IC Design Flow

FOSS open-source analog design flow with the following tools:

- PDK files from skywater-pdk and xschem_sky130.
- Schematic entry with **xschem**.
- Simulation with **ngspice**.
- Layout, extraction and DRC with **magic**.
- LVS with **netgen**.
- Manual routing of design using magic into the caravel analog user project. This user project is verified with precheck tool and submitted to the shuttle.



SiliWiz

Preset: inverter.json

LOAD SAVE CLEAR STL

CROSS SECTION & DRC ✓ SIMULATION

Cross Section View

DRC Errors

DRC OK

Show SPICE

* Input pulse: ramp the 'in' signal
Vin in 0 pulse (0 5 0u 50u 50u l 1)

* Extracted circuit:
M1000 out in vdd vdd pmos w=5.58u l=3.51u
+ ad=26.6166p pd=20.7u as=23.1012p ps=19.44u
M1001 out in vss vss nmos w=4.14u l=3.51u
+ ad=19.7478p pd=17.82u as=17.1396p ps=16.56u
C0 in out 0.01fF
C1 out vdd 0.06fF
C2 in vdd 0.03fF

* Models:
.model nmos nmox (vto=1 tox=15n uo=600 cbd=20f cbs=20f gamma=0.37)
.model pmos pmox (vto=-1 tox=15n uo=230 cbd=20f cbs=20f gamma=0.37)

* Simulation parameters:
.tran 500n 60u

.end

[Download MAGIC](#) [Tech File](#) [Download SPICE](#) Edit SPICE

Layers

active

- p substrate
- n well
- n diffusion
- p diffusion
- p tap
- n tap

passive

- polysilicon
- polyres
- metal1
- mim capacitor
- metal2

via

- metal1 via
- metal2 via

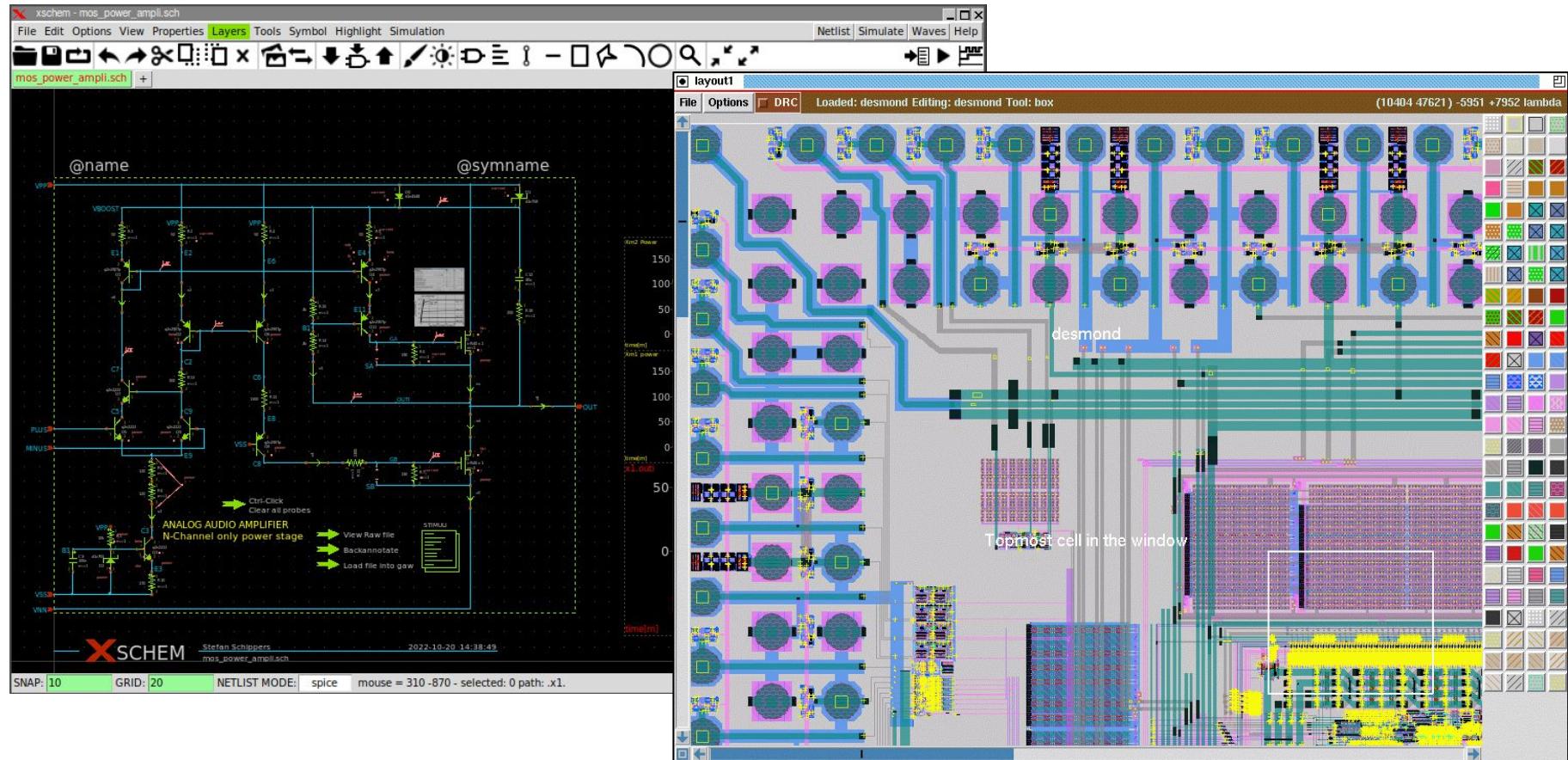
Resources

Get your digital designs manufactured for an affordable price at [Tiny Tapeout](#)

Learn advanced ASIC design with the [Zero to ASIC course](#)

SiliWiz <https://app.siliwiz.com/>
Tiny Tapeout <https://tinytapeout.com/>
Zero to ASIC course <https://zerotoasiccourse.com/>

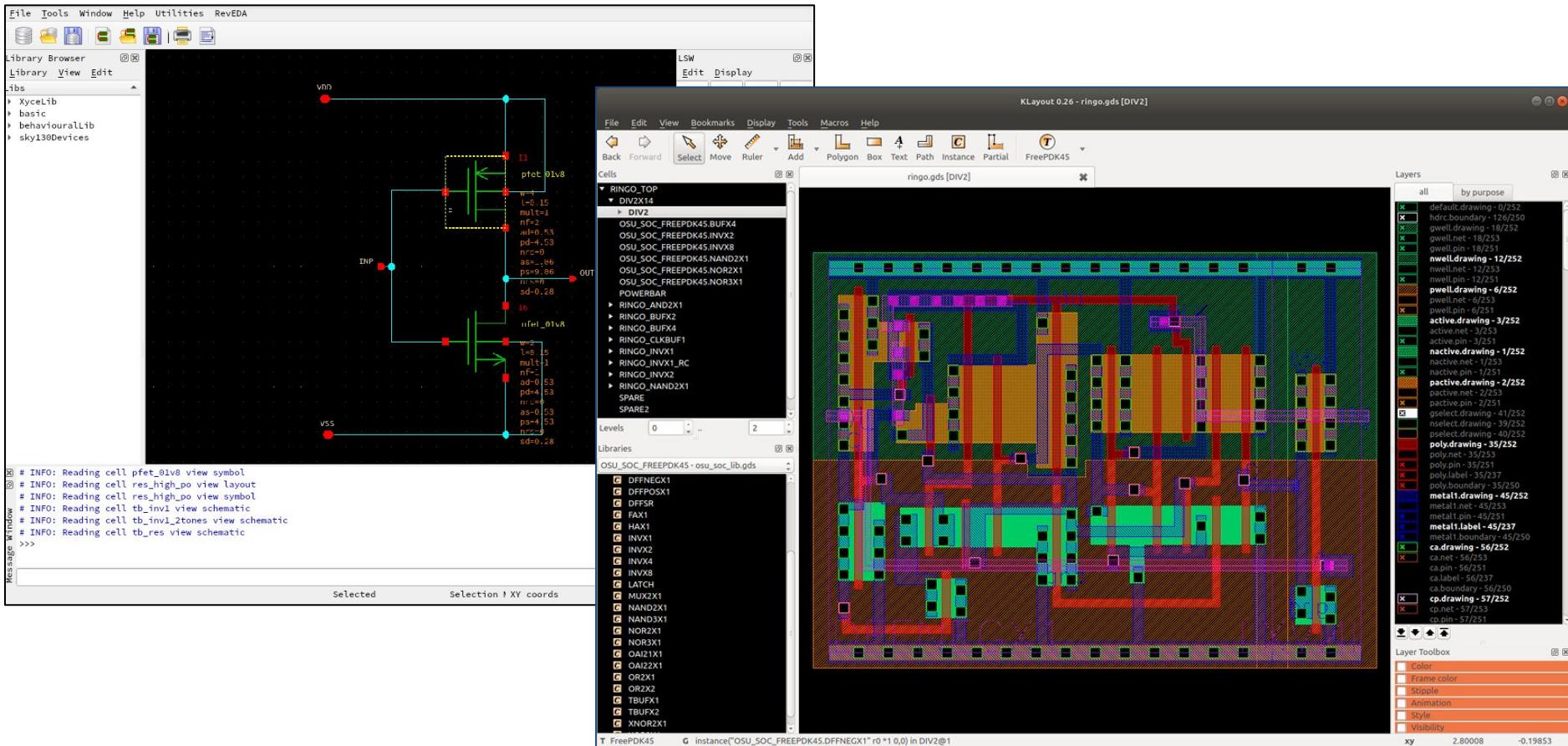
FOSS Schematic and Layout Editors



Xschem is a schematic capture program, it allows creation of hierarchical representation of circuits with a top down approach. By focusing on interfaces, hierarchy and instance properties a complex system can be described in terms of simpler building blocks. A VHDL or Verilog or Spice netlist can be generated from the drawn schematic
<https://xschem.sourceforge.io/stefan/index.html>

Magic version 8.3 is the official current released version of the program, a combined effort of the "Magic Development Team". The open-source license has allowed VLSI engineers with a bent toward programming to implement clever ideas and help magic stay abreast of fabrication technology.
<http://opencircuitdesign.com/magic/>

FOSS Schematic and Layout Editors



Revolution EDA offers a complete setup starting from schematic or Verilog-A entry, to simulation, layout, DRC and LVS. Symbols have integrated callback functions allowing accurate simulations.

[REF] <<https://reveda.eu/>>

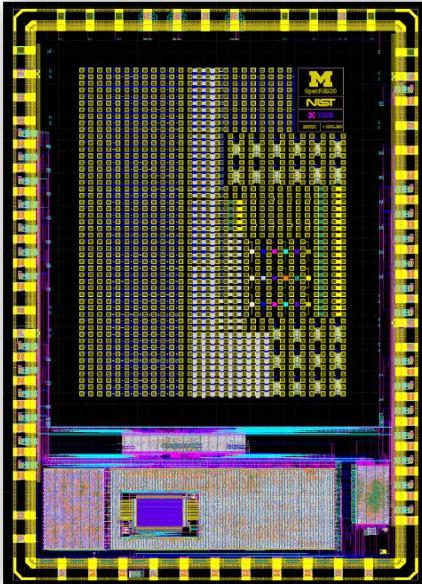
KLyaout has fast loading and accurate drawing, supports GDS and OASIS file formats with automatic uncompression of zlib compatible formats and is extensible and configurable to a large degree by custom Ruby or Python scripts

[REF] <https://klayout.de/>

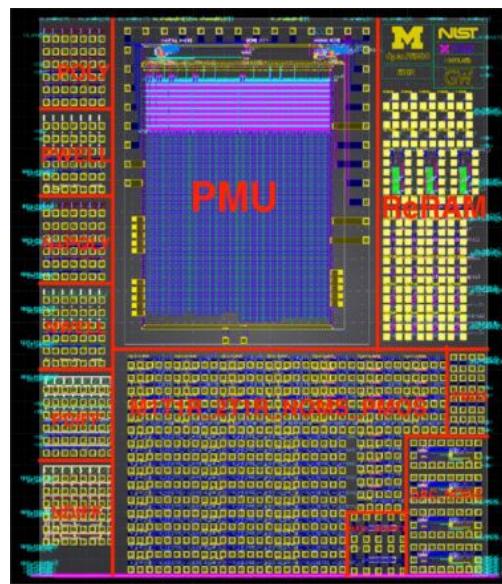
<https://peertube.f-si.org/video-channels/fsic2022/videos?sort=-publishedAt&page=2>

FOSS Hardware

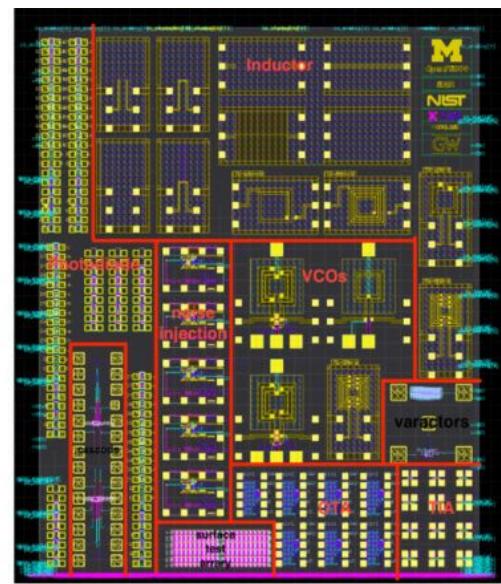
a growing movement to democratize IC design



MPW-5 chip, including over 1400 bare pads and around 500 test structures that consist of transistors, capacitors, diodes, ring oscillators (RO), lines, and via chain modules.



The IC design examples showing increasing complexity, MPW-5 was followed by MPW-6 (left) and MPW-7 (right)



Prof. Mehdi Saligane, a leader in the open-source chip design community, was among the first researchers to fabricate a successful chip as part of Google's multi-project wafer program:
<https://ece.engin.umich.edu/stories/open-source-hardware-a-growing-movement-to-democratize-ic-design>
Mehdi Saligane, UMich; Introduction to the open source EDA tool flow for IC design
https://www.mos-ak.org/silicon_valley_2022/presentations/Saligane_OpenFASoC_AWG_MOS-AK_Dec_7_2022.pdf

Open MPW Shuttle Program



Sponsored by



One of the most important aspects of semiconductor R&D is tapeout of a design. However, the prohibitive cost of tapeout and complications therein has prevented the majority of R&D folks and startups to participate. In order to promote and facilitate usage of open source FPGA technologies, Open-Source FPGA Foundation plans to offer a very simple flow for tapeout and the great news is, several of those will be free tapeouts!

The Open-Source FPGA Foundation offers a set of free and open-source tools enabling fast prototyping for FPGA chips and automated EDA support, through open standard collaboration.

<https://osfpga.org/about-us/>

Other Resources:

- SkyWater Open 130nm CMOS PDK: <https://github.com/google/skywater-pdk>
- OpenLane RTL2GDS Compiler: <https://github.com/efabless/openlane>
- Caravel Harness: <https://github.com/efabless/caravel>
- Caravel User Project: https://github.com/efabless/caravel_user_project
- Open MPW Precheck: https://github.com/efabless/open_mpw_precheck

FAQ:

- https://efabless.com/open_mpw_faq

Multi-Project Wafer MPW Service

Multi-Project Wafer (MPW) semiconductor manufacturing arrangements allow sharing mask and microelectronics wafer fabrication cost between several designs or projects

- CMP (F) started 1981 onwards <https://mycmp.fr/about-us/>
 - NORCHIP: 1981
 - AusMPC (A) 1981
 - E.I.S. (D) started 1983
 - BERCHIP in Latin America started in 1994
 - EUROEAST in East Europe 1994-1997
 - NOGAP 1986-1989
 - EUROCHIP 1989-1995
 - CMP (F): CEA-Leti Photonics Si and Photonics Si₃N₄
- EUROPRACTICE from 1995 onwards <https://europactice-ic.com/>
- IHP SG25H5_EPIC and imec Si-Photonics / SiN-Photonics
- MOSIS MPC/MPW gateway <https://www.mosis.com/>
 - Smartphotonics (NL) SMART Photonics PDK for C-band (1530–1565 nm)
- Ascent+ European Nanoelectronics Access Network
 - <https://www.ascent.network/>
- LNX SiN-Photonics TriPleX 850/1550/VIS

Where Next? FOSS to empower researchers and designers



FOSS eSim offers similar capabilities and ease of use as any equivalent proprietary software for schematic creation, simulation and PCB design, without having to pay a huge amount of money to procure licenses.
REF: <https://esim.fossee.in/>

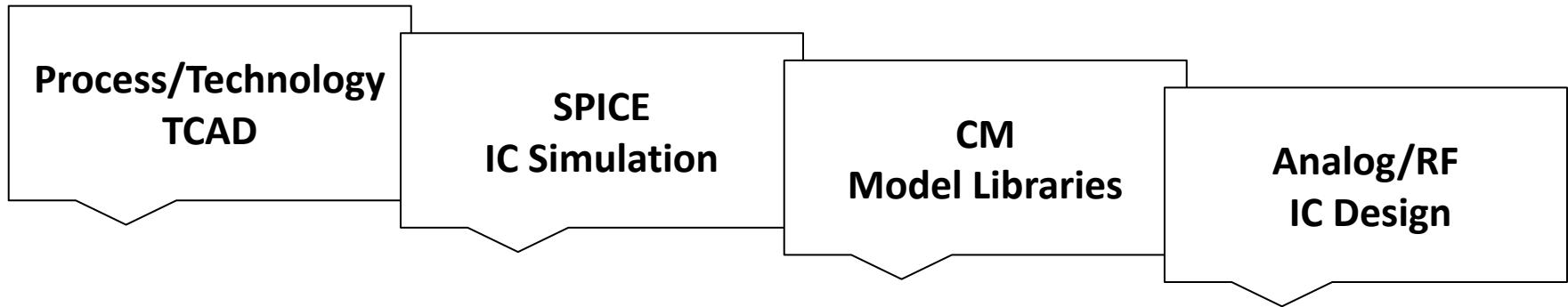
The **SSCS PICO Program**: Democratizing IC Design; it's first open-source IC design contest. The contest targets silicon fabrication using **free open** SKY130 PDK on eFabless' chipIgnite shuttle run program.
REF:<https://sscs.ieee.org/about/solid-state-circuits-directions/sscs-pico-program>



RISC-V is a **free and open** ISA enabling for a new era of processor innovation through open collaboration. Offers a new level of free, extensible software and hardware freedom on architecture, paving the way for the years ahead of computing design and innovation.
REF: <https://riscv.org/about/>

FOSS TCAD/EDA Tools

SPICE and Verilog-A Modeling Flow

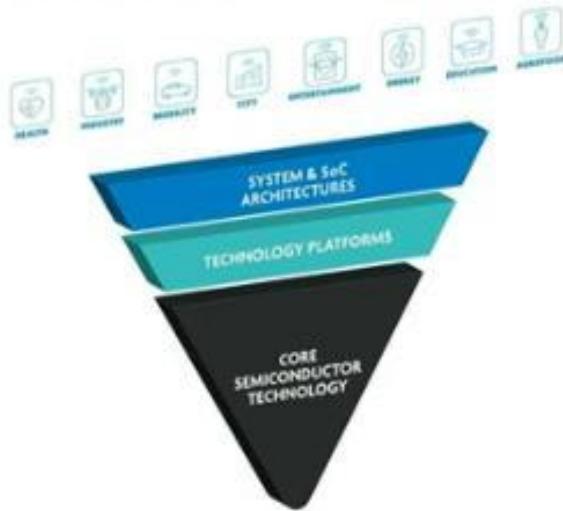


SUMMARY (Open Topics)

- Process TCAD Simulation
 - Interoperability:
Data Exchange Formats
- Compact/SPICE Modeling
 - Verilog-A Standardization
 - Simulated/Measured Data Exchange
- Analog/RF IC Design
 - Interoperability:
Netlist/Schematic Exchange Formats

Outlook: A call for Building Talent and Skills

To conclude



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International Solid-State Circuits Conference

EU Chips Act drives pan-European full-stack innovation partnerships

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A call for

System-Technology Co-Optimisation

Pilot Lines and design platforms for advanced & mature nodes innovation

Focus on Sustainable innovation

Building Talent and Skills

**full-stack innovation
partnerships**



EU Chips Act Drives Pan-European Full-Stack Innovation Partnerships
Plenary Session at ISSCC 2023 (FEB.20)
Jo De Boeck, Executive VP and CSO, imec & KU Leuven, Belgium





MOS-AK: 2023/24 Events

- IHP OpenPDK Networking Workshop
Frankfurt (Oder), June 27-28, 2023
- Special CM Session, MIXDES
Krakow (PL), June 29-20, 2023
- 5th MOS-AK/LADEC
Puebla (MX), July 3 2023
- 7th Sino MOS-AK Workshop
Nanjing (CN), Aug.11-13, 2023
- **20th MOS-AK at**
ESSDERC/ESSCIRC
Lisbon (P) Sept. 11, 2023
- 16th MOS-AK/Silicon Valley
Silicon Valley (US) Dec.13, 2023
- MOS-AK/India
EDTM Bengaluru, March 2024
- 8th Sino MOS-AK Workshop
Aug. 2024