

A new era of opensource hardware

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Assistant Professor at UIT University

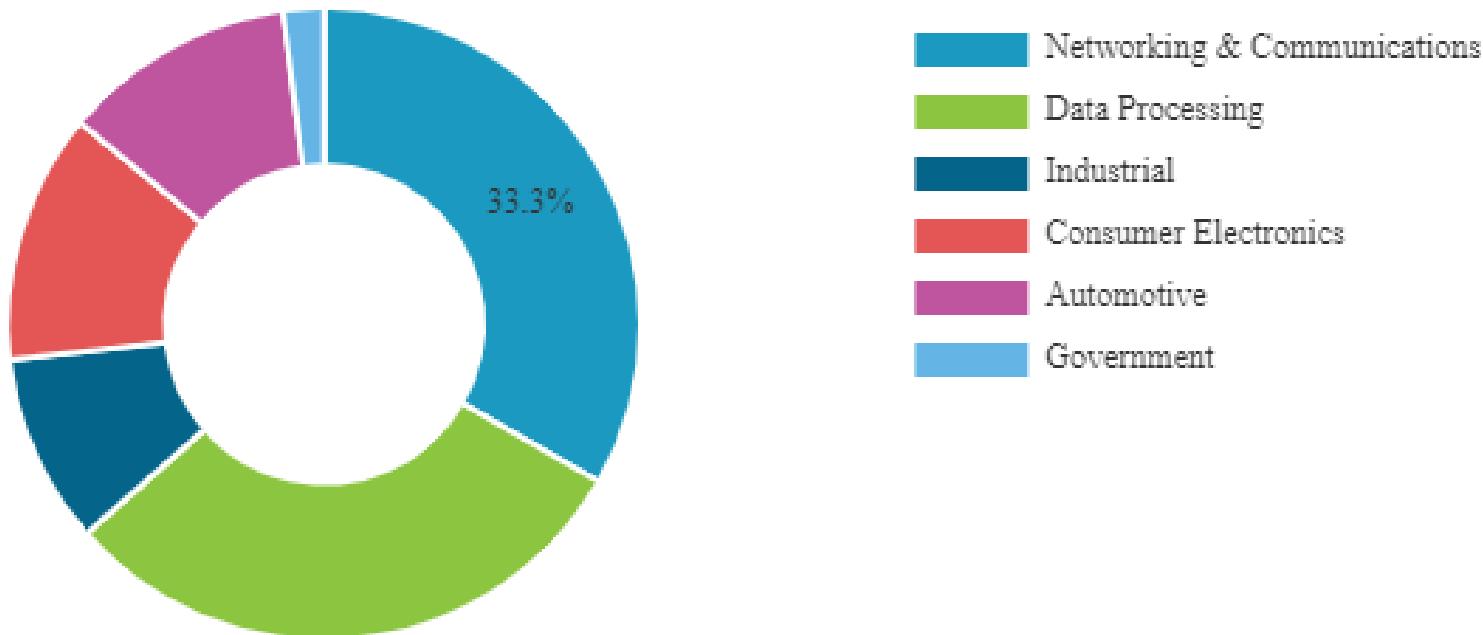
Head of Micro Electronics Research Laboratoy (MERL-UIT)

<https://github.com/merledu>

www.merledupk.org

www.uit.edu

Global Semiconductor Market Share, By Application, 2021



www.fortunebusinessinsights.com

The global **semiconductor market** is projected to grow from \$483.00 billion in 2022 to \$893.10 billion by 2029, at a CAGR of 9.2% in forecast period

Welcome To MERL

Fostering Semiconductor
Technology, IC Design,
Research and Development



B/N:

BUS RATIO	JP1	JP2	JP3
x1.5 / x3.5	OFF	OFF	OFF
X2.0	ON	OFF	OFF
X2.5	ON	OFF	ON
X3.0	OFF	OFF	ON
			OFF

Why Open Source Microprocessor?

- With the diminishing of [Moore's Law](#) *, the only way to improve performance is with customization, which leads to the development of more chip variants.
- “The open-source nature of RISC-V feeds this paradigm shift.”
- OpenRISC was introduced in 2000 and OpenSPARC has been around since 2006, way before RISC-V. Still Not gain the same momentum.
- RISC-V assumes to come at the right time to solve problems which Intel or ARM or another closed ISA might not do?

**the number of transistors in a dense integrated circuit (IC) doubles about every two years*

RISC –V an open ISA- (enabler)

- An open-source ISA means the specification is freely available for anyone to build an implementation around that specification. “There are no patents that protect the ISA,”
- RISC-V ISA allows anyone to start making his own Custom Microprocessor / SoC using available open-source hardware and Software toolchains.
- ARM and Intel are closed ISA, they charged heavy licensing fees to their customers. It is close to impossible to customize the core using closed-ISA.





CHIPS (Common Hardware for Interfaces, Processors and Systems) Alliance harnesses the energy of open source collaboration to accelerate hardware development.





TECHNOLOGIES > EMBEDDED REVOLUTION

Intel Launches \$1 Billion Fund to Build Foundry Ecosystem, Backs RISC-V

Feb. 14, 2022

Intel is joining RISC-V International, the body that oversees the open-source instruction set architecture.

Source: <https://www.hpcwire.com/2022/10/06/intel-is-opening-up-its-chip-factories-to-academia/>



Intel Is Opening up Its Chip Factories to Academia

By Agam Shah

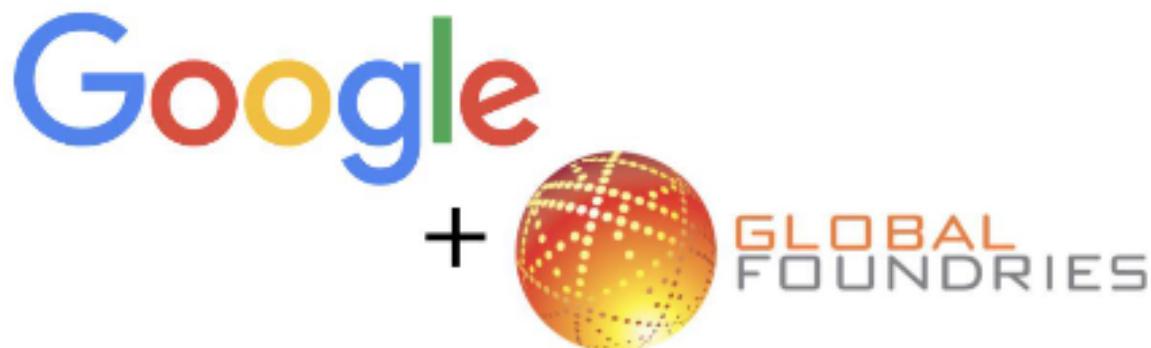
Exciting
times.....

GlobalFoundries GF180MCU Open Source PDK

license Apache-2.0 docs failing tag v0.0.0 commits since v0.0.0 22

The GF180MCU open source PDK is a collaboration between Google and GlobalFoundries to provide a fully open source process design kit (PDK) and related resources to enable the creation of designs manufacturable at GlobalFoundries's facility on their 0.18um 3.3V/6V MCU process technology.

The GF180MCU documentation can be found at <<https://gf180mcu-pdk.rtfd.io>>.



FOSS 180nm Production PDK

github.com/google/gf180mcu-pdk

Current Status -- Experimental Preview

Exciting times...



OPEN SOURCE DESIGN IN 90NM FD SOI

US Government provides \$15M to fund Open Source Design in 90nm

SkyWater Receives Funding from DOD, Partners with Google to Facilitate Open Source Design for its new 90 nm Technology Offering

ENABLED BY



Exciting times...



Alexander Glandien

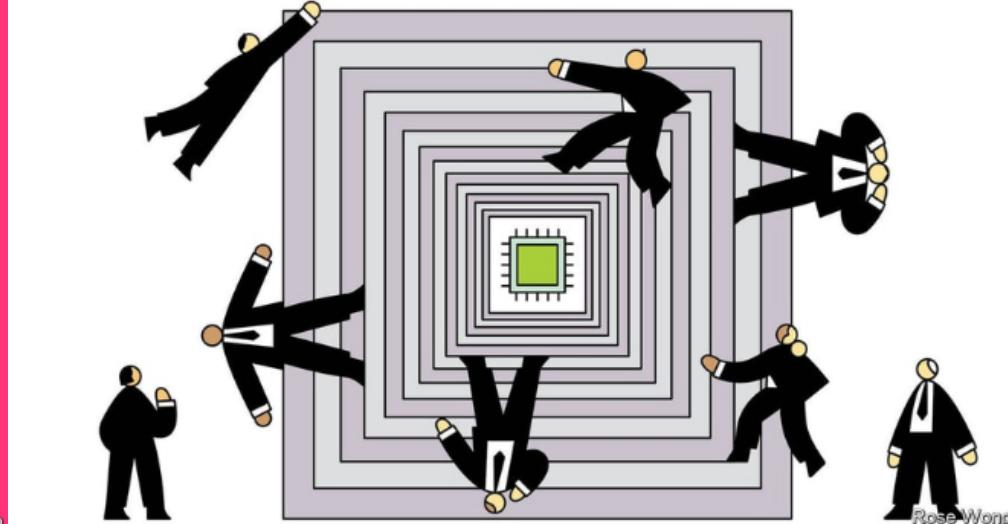
<https://www.economist.com/leaders/2019/10/03/the-rise-of-open-source-computing>

Leaders | Open season

The rise of open-source computing

It is good for competition—and may offer a way to ease the tech war

The Economist



Rose Wong

<https://www.economist.com/the-world-ahead/2021/11/01/dramatic-shifts-in-the-semiconductor-industry-will-continue>

The World Ahead | The World Ahead 2022

Dramatic shifts in the semiconductor industry will continue

MERL-UIT Initiative, an ecosystem for open source hardware development platform

- A new pedagogy is developed for enthusiast UG- students willing to learn :
 - I. RISC-V based processor designing.
 - II. System Verilog based digital designing (RTL).
 - III. Chisel-based digital designing.
 - IV. Design Verification/ Emulation on FPGA.
 - V. Backend APR- RTL to GDS-II conversion.

Using open source technologies in undergraduate engineering program.

MERL-UIT initiatives, ecosystem development

- We trained 3rd and 5th semester student of undergraduate Computer Science/Software and Electrical Engineering using our own devised methodology.
- We offer summer programs that focuses on programing skills, computer architecture, tools and opensource development platforms for developing RISC-V compute core.
- RV32I is the base ISA of RISC-V , all students must go thorough this exercise to be part of our team.

Student can Opt between

- **CHISEL** (Developed in UC-Berkeley) is a hardware construction language that allow Computer Science students to design RV32I RISC-V Processor.
- **System Verilog/ Verilog** as a HDL language that allows Computer or Electrical Engineering students to design RV32I RSC-V core.

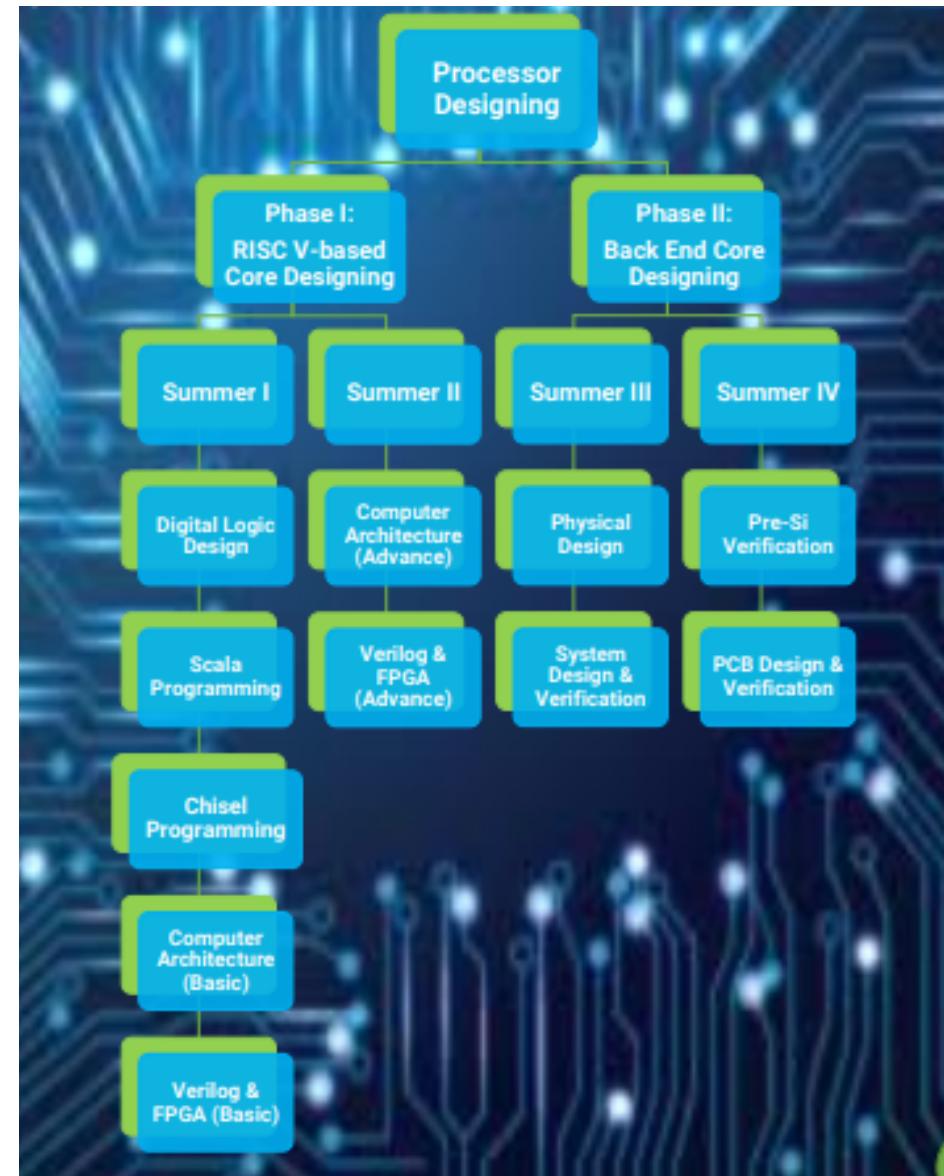
MERL-UIT Summer School Curriculum:

Requirements:

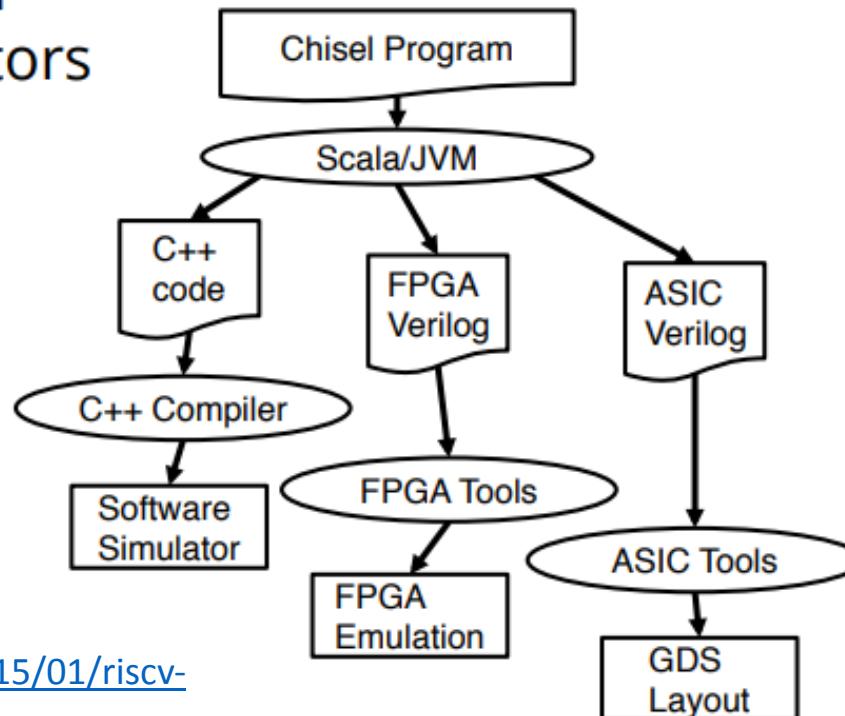
- **Genuine Interest**, as there will be extensive hard work
- **Completed 2nd Semester in BS-CS, BS-SE or BS-EL:** {Programming Fundamentals, Introduction to Computing and Digital logic Design (optional)}

Program Structure:

- 4 summer programs in Undergrad.
- Must attain Learning outcomes of each summer program to promote to another.
- Students can finish two summer program in One Summer vacations too. We are not time focused, we are outcome focused, Early you come up with outcome, earlier you are promoted.
- One to One mentorship
- **Free of Cost**

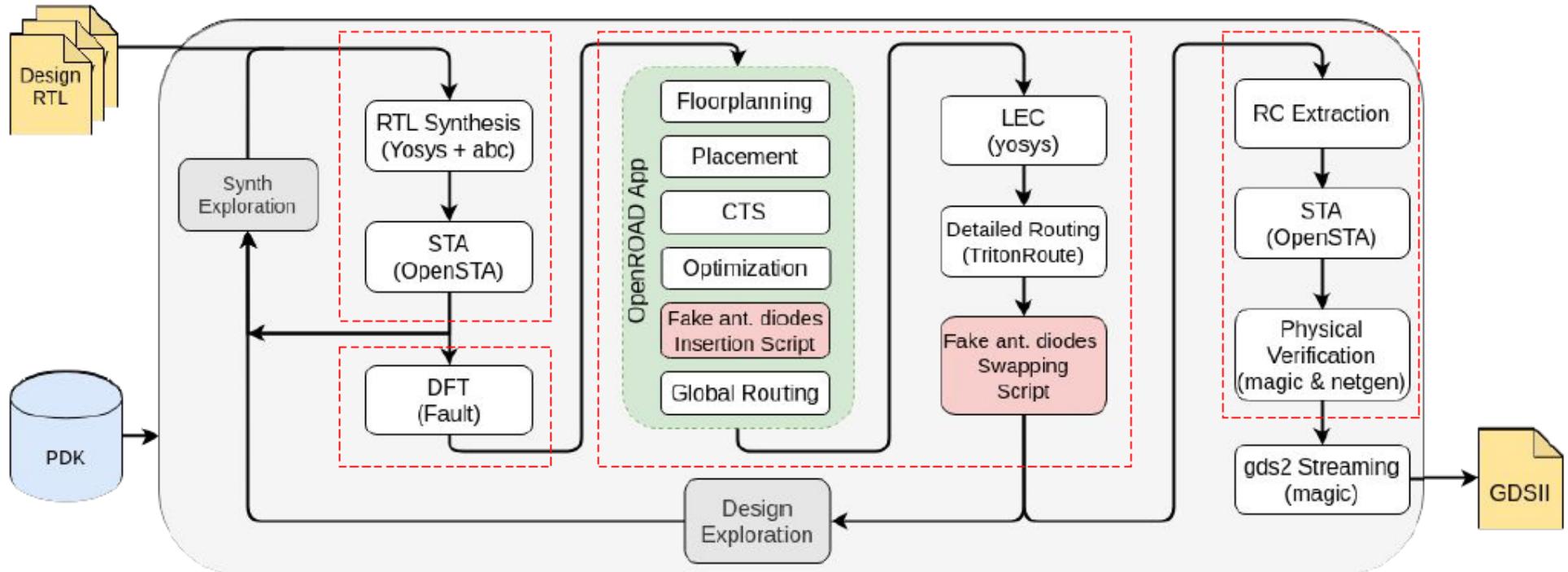


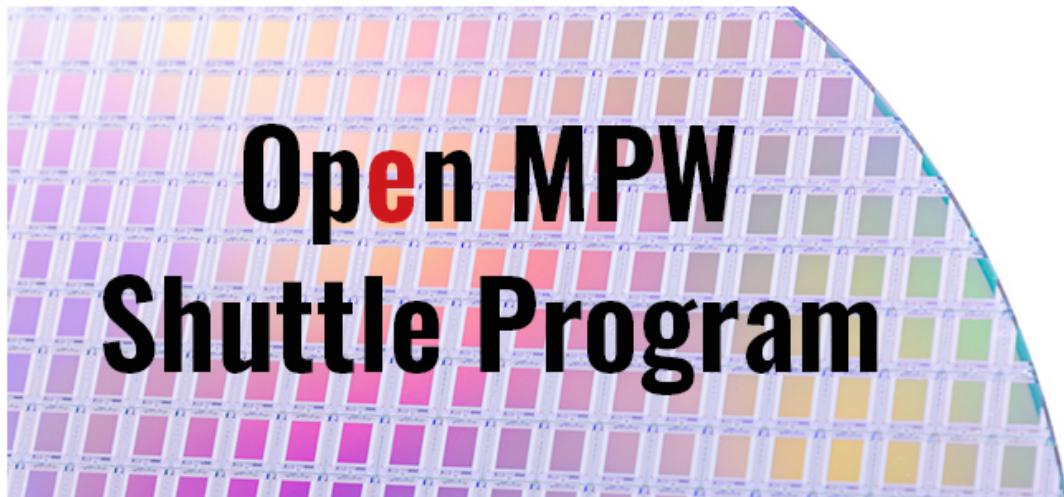
- RTL generator written in Chisel
 - HDL embedded in Scala
- Full power of Scala for writing generators
 - object-oriented programming
 - functional programming



Source: <https://riscv.org/wp-content/uploads/2015/01/riscv-rocket-chip-generator-workshop-jan2015.pdf>

Open-Lane





Open MPW Shuttle Program

efabless.com
Sponsored by
Google

WELCOME TO THE EFABLESS OPEN MPW SHUTTLE PROGRAM

The Efabless Open MPW Shuttle Program provides fabrication for fully open-source projects using the SkyWater Open Source PDK announced by Google and SkyWater.

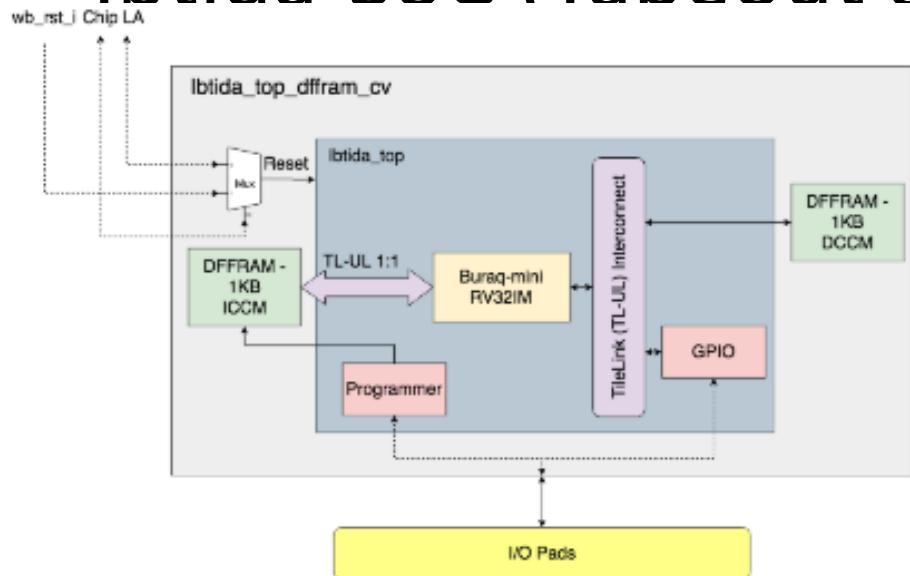
Two SoCs: short listed first ever OpenMPW-1 Shuttle

OPEN MPW SHUTTLE REQUESTS

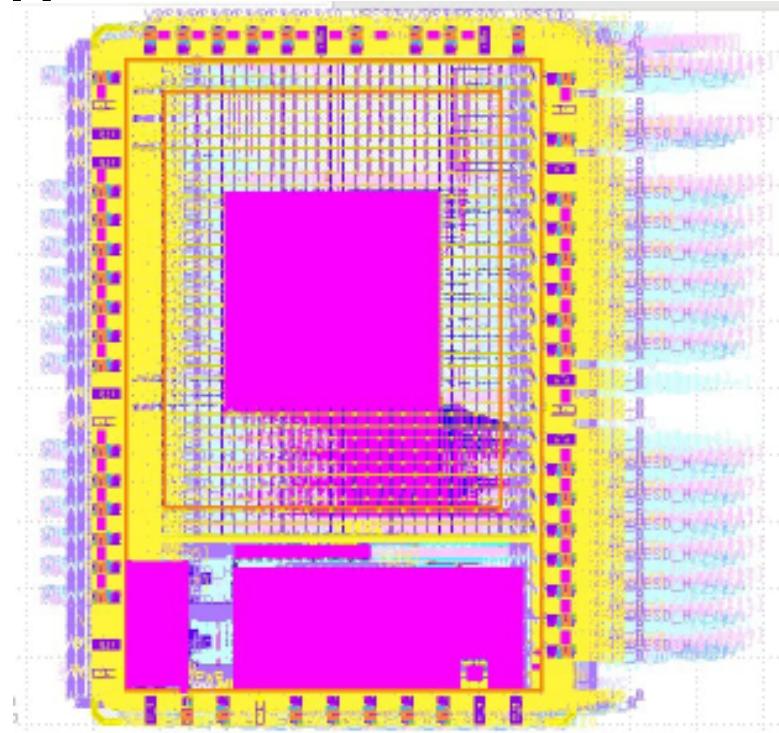
[Login](#) to interact with your Open MPW Requests

REQUEST	INFO	CATEGORY	OWNER / COMPANY	OPEN DATE	STATUS
Alvaro-Javier Alvarez, Alvaro-Javier Alvarez, Gerardo, Gerardo, Koenraadis and Iván Rodríguez-Fortáez	Info	Open MPW	Alvaro-Javier Alvarez / UPC/ESCI	Nov 26, 2020	Open
Ehsan SoC	Info	Open MPW	Zain Rizwan Khan / Micro Electronics Research Laboratory	Nov 27, 2020	Open
Harvest_OpenPDC	Info	Open MPW	Xilun Tang / UNIVERSITY OF MARYLAND	Nov 28, 2020	Open
Spectroval	Info	Open MPW	Madihah Mousavinezhad / NOVATEC	Nov 24, 2020	Open
Ensatte	Info	Open MPW	Madihah Mousavinezhad	Nov 30, 2020	Open
OpenPDC	Info	Open MPW	Ehsan Gengzhi / Ehsan Gengzhi	Nov 28, 2020	Open
Thomas Party	Info	Open MPW	Thomas Party	Nov 26, 2020	Open
Pylone	Info	Open MPW	Riyadh Suleiman / Pylone	Nov 24, 2020	Open
RAPTCore	Info	Open MPW	Shane Kelly / RAPTCore	Nov 23, 2020	Open
Philip Götting	Info	Open MPW	Philipp Götting / Westfalen Association	Nov 21, 2020	Open
Iotida SoC	Info	Open MPW	Muhammad Hadr Khan	Nov 27, 2020	Open
Bryce Roodyhough, Md Munir Hasan, Michael Stetzler	Info	Open MPW	Michael Stetzler / UNC Charlotte	Nov 24, 2020	Open

Ibtida-SoC (Tapeout at 130 nm)



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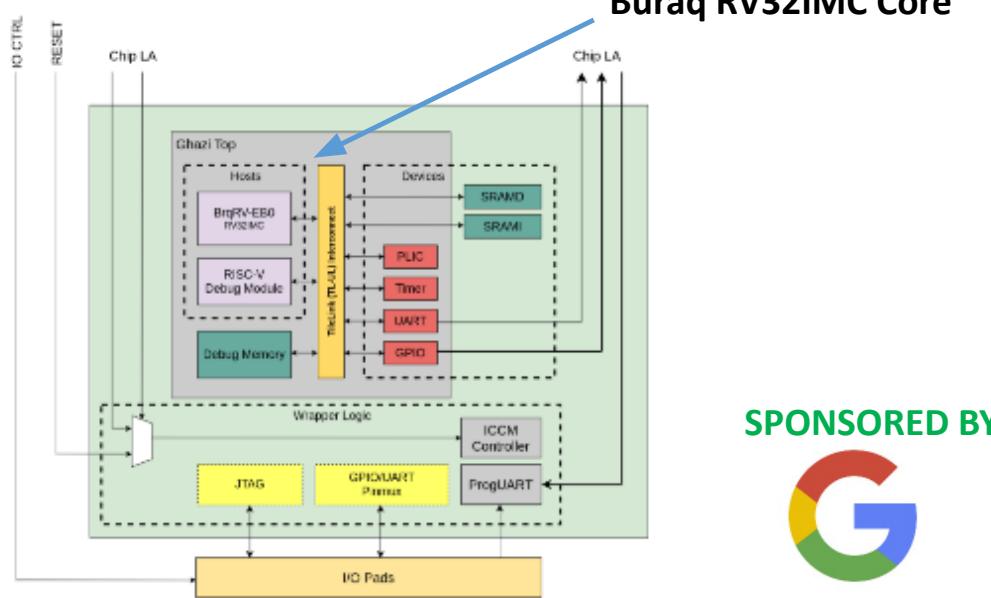


- Written in CHISEL
- Simulated on Verilator
- Emulated on Arty-7 FPGA
- GDS generated thorough OpenLane
- Used Sky-130 nm PDK

[Git Url](#)

https://github.com/hadirkhan10/caravel_ibtida_soc.git

Ghazi -SoC



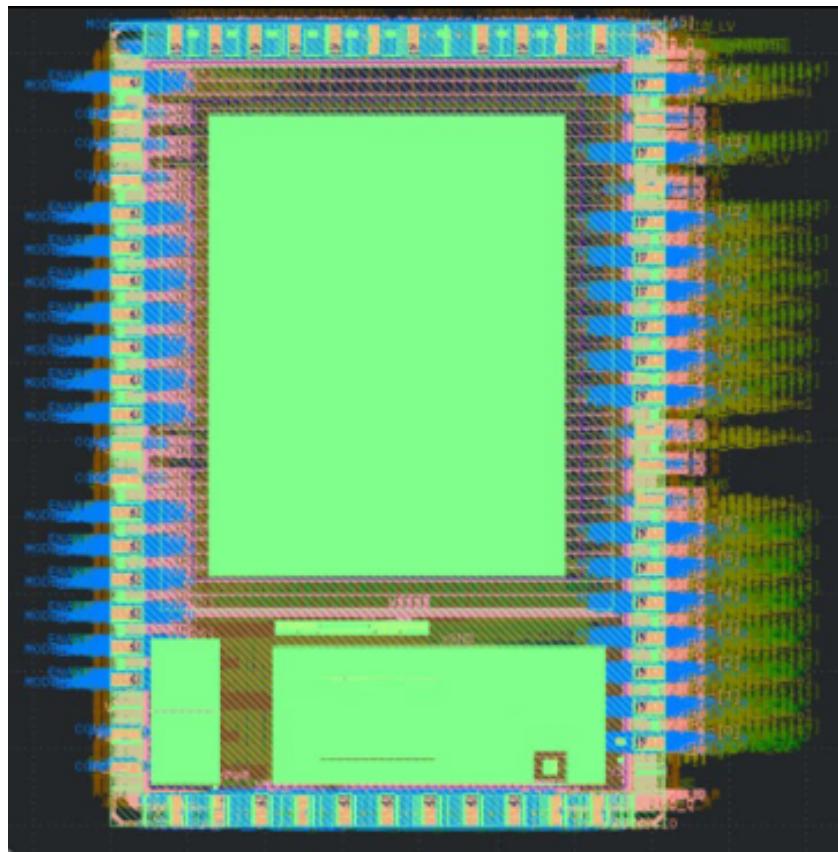
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- Written in System Verilog
- Simulated on Verilator
- Emulated on Arty-7 FPGA
- GDS generated thorough Open Lane (Open)
- Used Sky-130 nm PDK

Git Url

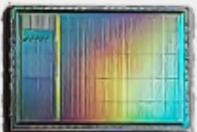
https://github.com/merledu/caravel_Ghazi_SoC.git



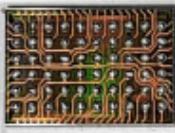
MERL-UITU SoC 2020-2021



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Accelerating Engineering Innovation



Ibtida SoC



Ghazi SoC

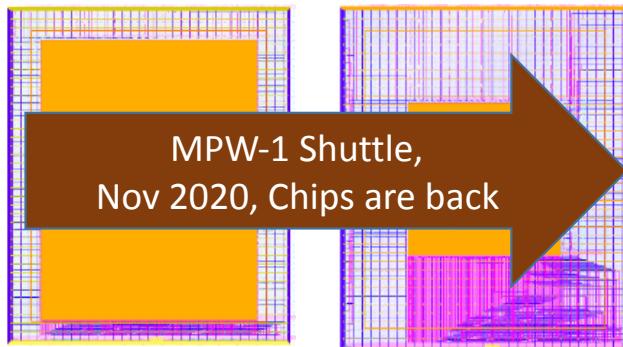
PAKISTAN's 1st OPEN SOURCE RISC-V based System on Chip

Supported by

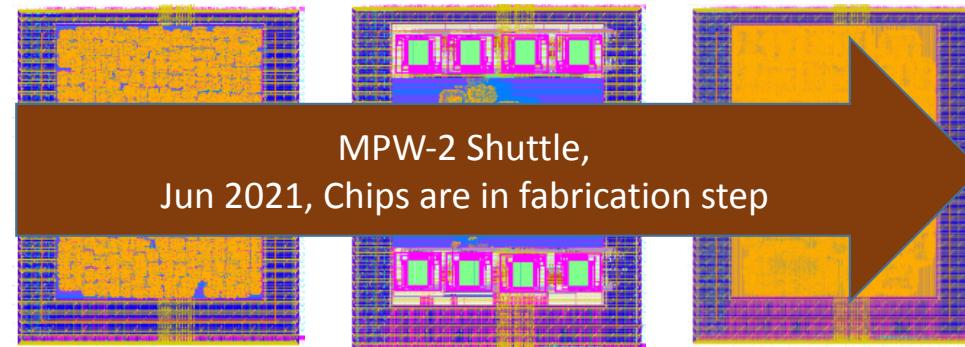


Fabricated on Skywater 130nm (OpenPDK) process node in 1st OpenMPW Shuttle

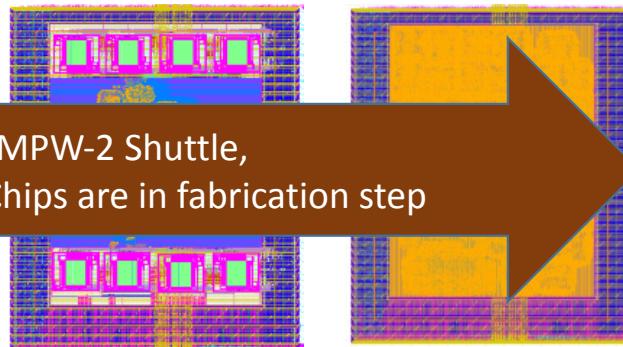
9 designs tape out by undergrad students in Google shuttle within one year



Ibtida SoC



Azadi SoC



Lexicon SoC

BrqRV SoC



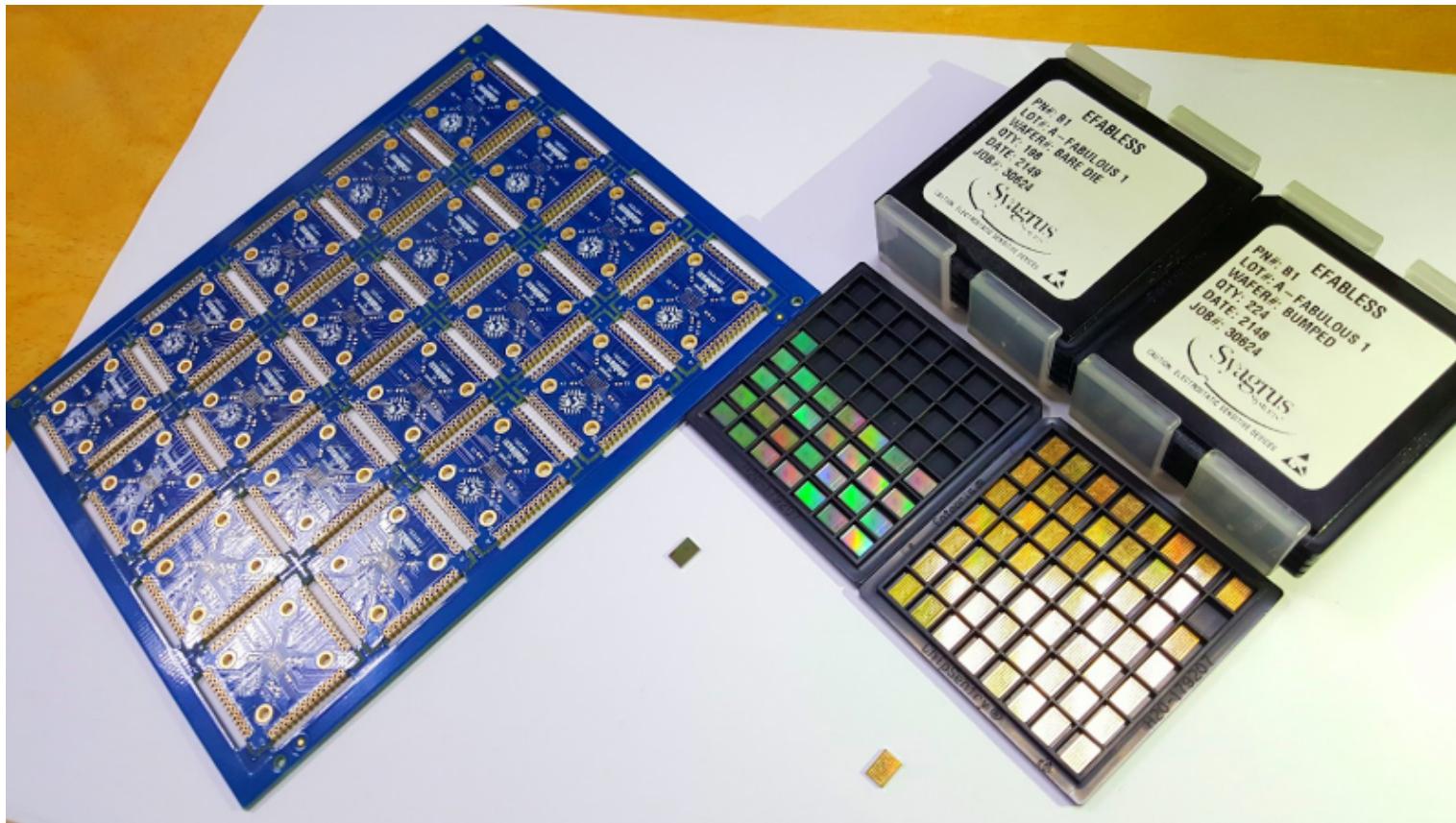
Ibtida II SoC

BRAM

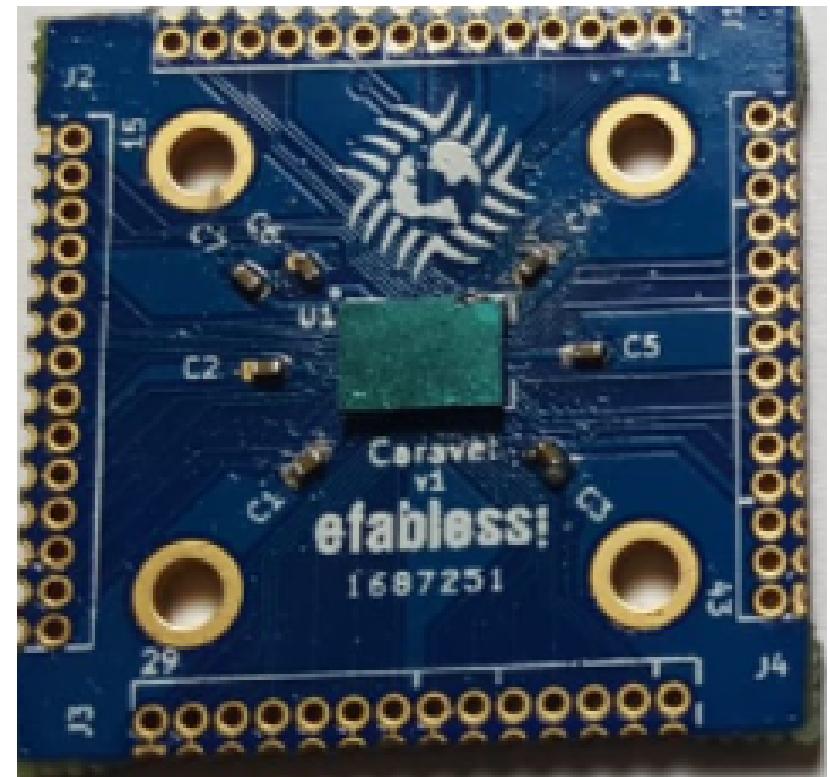
Azadi-II SoC

SRAM-based TCAM

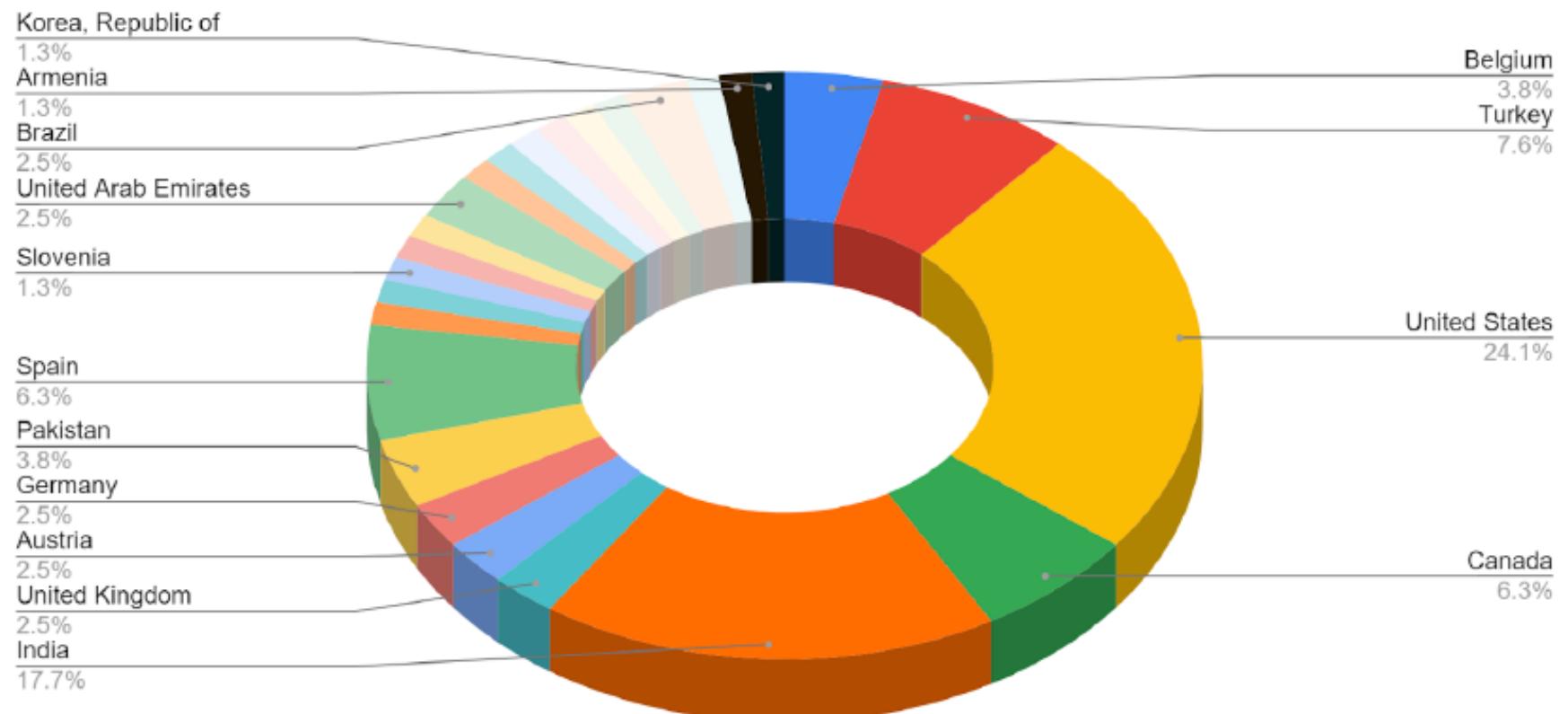
Ghazi and Ibtida (MPW-1) Chip shipped:



Chip-bring up --- going on



MPW-FIVE



79 designs from 26 different countries

MERL Software Development

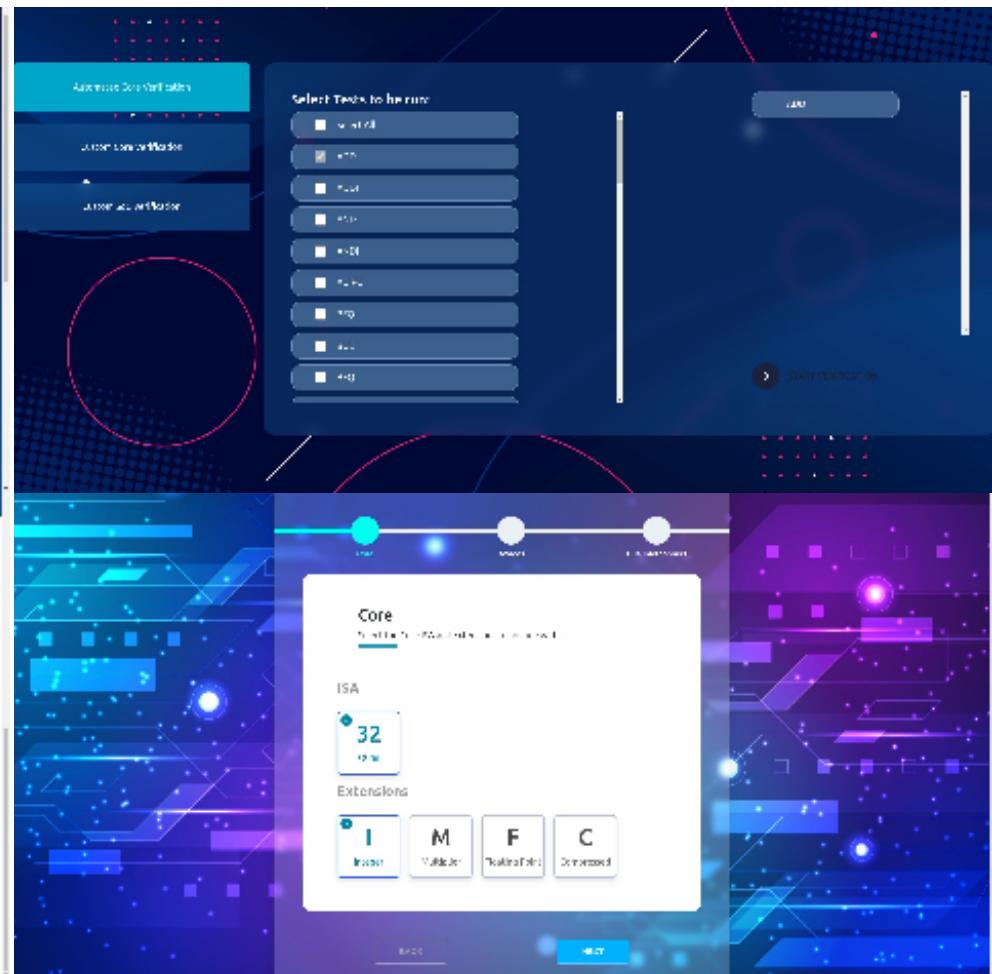
SoC-Now



Features

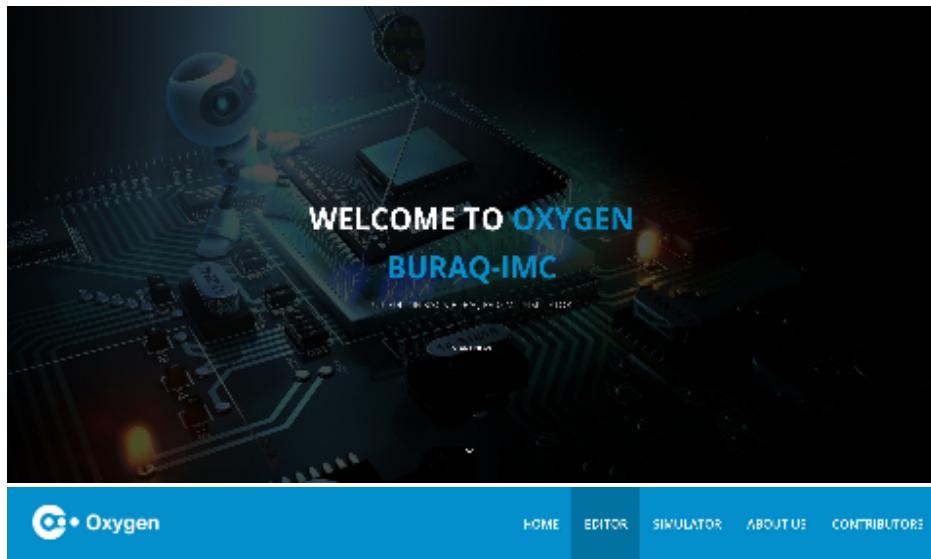


SoC-Now is a CHISEL based SoC Generator with a Web-Application for generating SoC with your required configurations.



Oxygen Simulator is a RISC-V ISA Simulator that can simulate the RISC-V based instructions graphically and also dumps hex code.

Oxygen Simulator



```

1 addi x5, x5, 1
2 addi x25, x5, 18
3 ldi $IDNACC1_LOOP:
4 addi x5, x29, 1
5 slt x25, x29, END
6 add x5, x5, x5
7 add x5, x5, x5
8 add x5, x5, x5
9 jal $IDNACC1_LOOP
10 END:

```

Oxygen
HOME EDITOR SIMULATOR ABOUT US CONTRIBUTORS

Run Step Prev Reset Dump
REGISTERS MEMORY

PC	Basic Code	Type	Imm-1	Funct-7	Funct-6	Funct-4	rs2	rs1	Funct-3	Funct-2	rd	Imm-2	Opcode
0x0	addi x5, x5, 1	I	000000000001	X	X	X	X	00000	000	X	00110	X	0010011
0x4	addi x25, x5, 18	I	0000000000101000	X	X	X	X	000000	000	X	11100	X	0010011
0x8	addi x29, x29, 1	I	0000000000000001	X	X	X	X	11101	000	X	11101	X	0010011
0xC	blt x25,x29,cond	S8	00000003	X	X	X	11101	11100	100	X	X	01000	1100011
0x10	add x7,x5,x5	R	X	00000000	X	X	00101	00110	000	X	00111	X	0010011
0x14	add x5,x5,x0	R	X	00000000	X	X	00000	00110	000	X	00101	X	0010011
0x18	add x6,x7,x0	R	X	00000000	X	X	00000	00111	000	X	00110	X	0010011

Register Name
Register Value

x0(zero)	0
x1(rz)	0
x2(sp)	0
x3(gp)	0
x4(tp)	0
x5(t0)	1
x6(t1)	1
x7(t2)	1
x8(s0)	0
x9(s1)	0
x10(a0)	0
x11(a1)	0
x12(a2)	0
x13(a3)	0
x14(a4)	0

Display Settings
Decimal Hexadecimal
 Use switch set

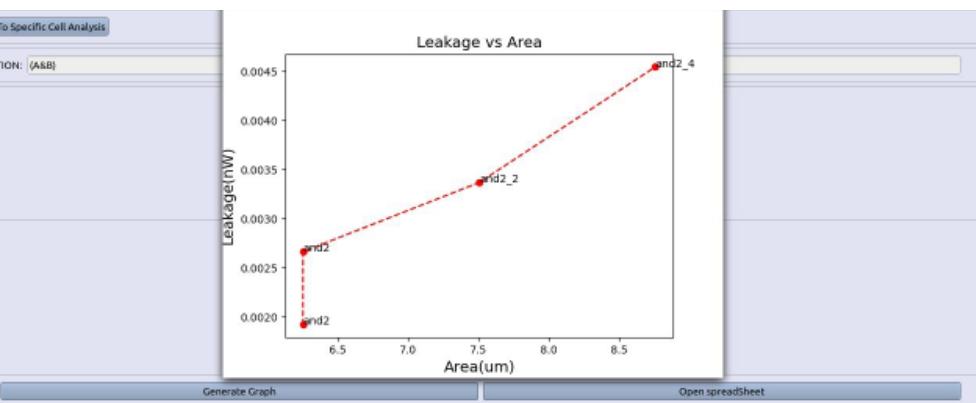
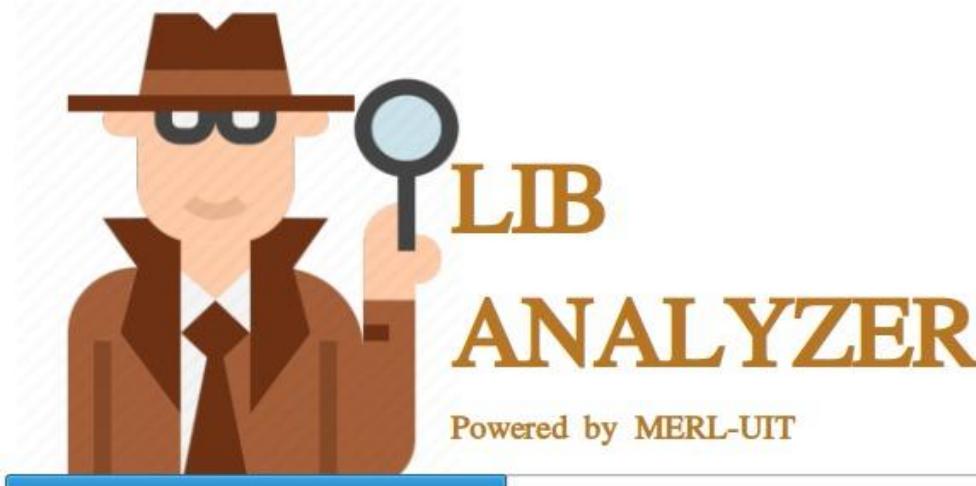
Burq Suite

Burq Suite is a automated Core Verification Suite that run test cases and generates report of verification for any core user desires.

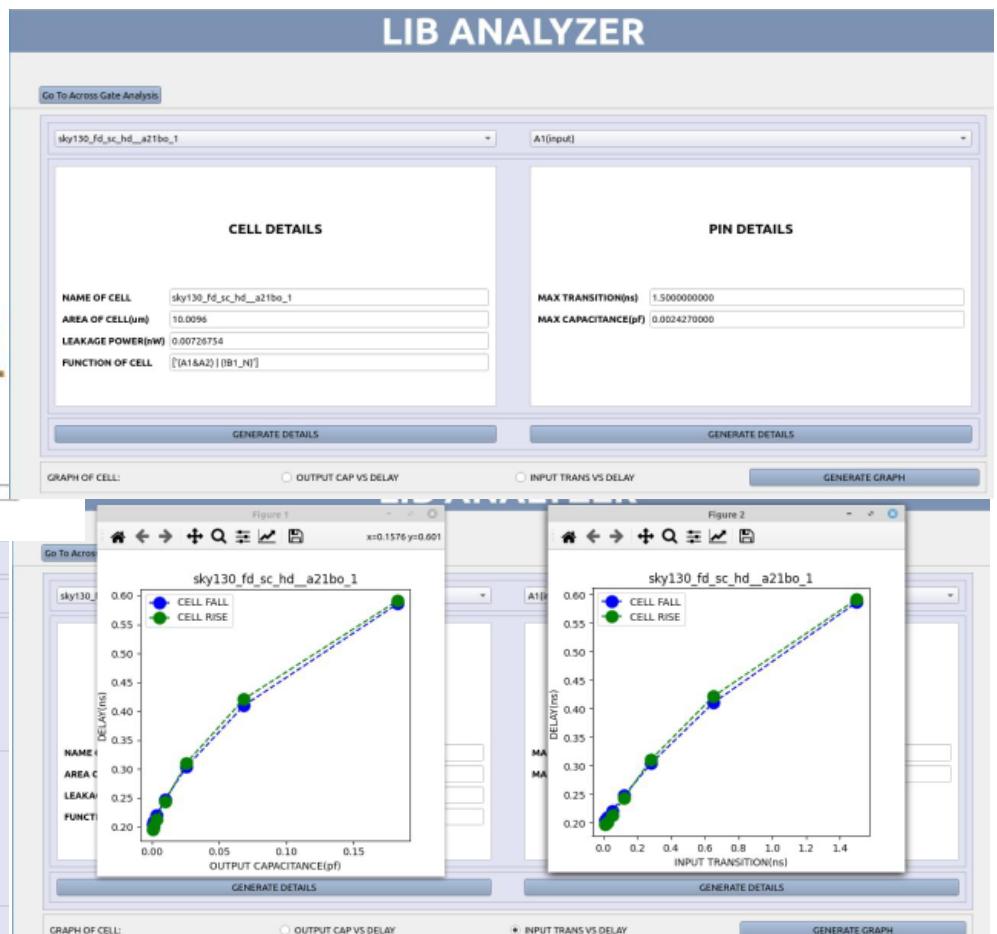
The screenshot displays the The Burq Suite interface, version v0.0.1, running on a Windows operating system. The interface is divided into several sections:

- Top Left:** A sidebar with buttons for "Create Custom Test (C)", "Custom Core Verification", "Prebuilt Core Verification", and "About Us".
- Top Center:** A "Recent Projects" section showing a single entry: "test2" (Type: prebuilt_verification).
- Center:** A main workspace for creating a new project. It includes fields for "Project Name" (Untitled) and "Project Location", and a "Core" configuration section with "ISA" (32 Bit selected) and "Extensions" (Integer (I), Multiplier (M), Floating Point (F), Compressed (C)).
- Right Side:** A "The Burq Suite" window showing a "test_results.report x" file. It lists test cases: InsertionSort, CountInversions, towers, and Stack, all marked as "Passed". Below this is a "main.elf" file viewer displaying assembly code for the main function.

Lib Analyzer



Lib Analyzer enables the user to extract information like, number of cells, area of cells, power at rising/falling edge, leakage power, delay at rising/falling edge etc. The tool further has capabilities to plot different results on a graph for a better visual judgment.



Block RAM Generator

MERL
Accelerating Engineering Innovation

BLOCK RAM GENERATOR

Powered By MICRO-ELECTRONIC RESEARCH LAB (MERL)

GET STARTED

Block RAM generator is a tool which enables the user to generate RAMs of any desired size and specification, from a user provided Block RAM. Through it a user can not only generate an RTL of the newly specified RAM, but also simulate and verify it in one click.

< OUTPUT SPECIFICATION

Number of Read Ports:

Number of Write Ports:

Memory Depth:

Data Width:

Address Width:

ASIC Synthesis Support
 FPGA Synthesis Support
 RTL Verilog Support
 Simulation Support

Example

< TECHNOLOGY USE FOR BRAM GENERATOR


TECHNOLOGY SKY130-nm

The SKY130 is a mature 180nm-130nm hybrid technology originally developed internally by Cypress Semiconductor before being spun out into SkyWater Technology and made accessible to general industry. SkyWater and Google's collaboration is now making this technology accessible to everyone!

[Learn More](#) [Generate](#)


TECHNOLOGY TSMC28-nm

TSMC became the first foundry to provide the world's first 28nm General Purpose process technology in 2011 and has been adding more options ever since. TSMC provides customers with foundry's most comprehensive 28nm process portfolio that enable products that deliver higher performance, save more energy savings, and are more eco-friendly.

[Learn More](#) [Generate](#)


TECHNOLOGY TSMC65-nm

TSMC's 65nm technology is the Company's third-generation semiconductor process employing both copper interconnects and low-k dielectrics. The technology supports a standard cell gate density twice that of TSMC's 90nm process. It offers better integration and improved chip performance.

[Learn More](#) [Generate](#)

< OUTPUT MEMORY

OUTPUT MEMORY		MEMORY BANK	
Number of Read Ports	1	Number of Read Ports	1
Number of Write Ports	1	Number of Write Ports	1
Memory Depth	512	Memory Depth	256
Address Width	9	Address Width	8
Data Width	32		
Number of Banks	2		
Number of Block RAMs	2		
Output File Path	/home/weleed1/Merl/bram_view/output/nram_512x32_1rw_2022-08-01_14-31-05		

Generate

TAPEOUT PAKISTAN – TRAINING ALL OVER PAKISTAN

MERL-UIT
PAKISTAN



MERL-UIT
PAKISTAN

Scholarship
Network

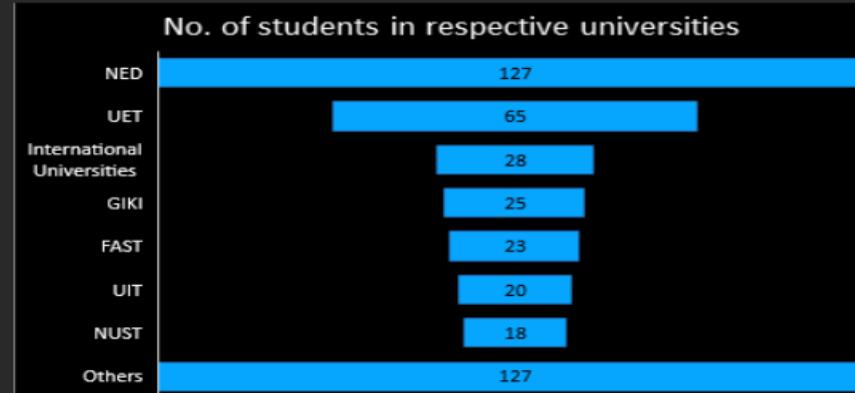
400+ Students Joined APR Training under OSFGA Foundation Project *TAPEOUT PAKISTAN* conducted by MERL-UIT

- Universities from Pakistan:

- NED
- UET
- GIKI
- FAST
- UIT
- NUST
- Others

- International Universities Including:

- IIT Bombay
- University of Arkansas
- SKKU Korea
- University of Rome
- University of Calgary, etc.



Reverse Engineering of Rocket chip

Generator

- Led by Engr. Farhan Ahmed Karim, Dr. Rumi Naqvi, Computer Science Faculty, and team lead software at MERL-UiT.
- Major Contribution: Undergraduate Students of Usman institute of Technology, Software Engineering



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December 8 - 10, 2020
Virtual Event, PST

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[Dec 8](#) [Dec 9](#) [Dec 10](#)

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Thursday, December 10 2020 - Thursday, 10 December 2020 - PST (Pacific Standard Time, GMT-8)

Sort by time ▾ Grid View

Thursday, 10 December 2020 9:00am - 10:00am 60 mins

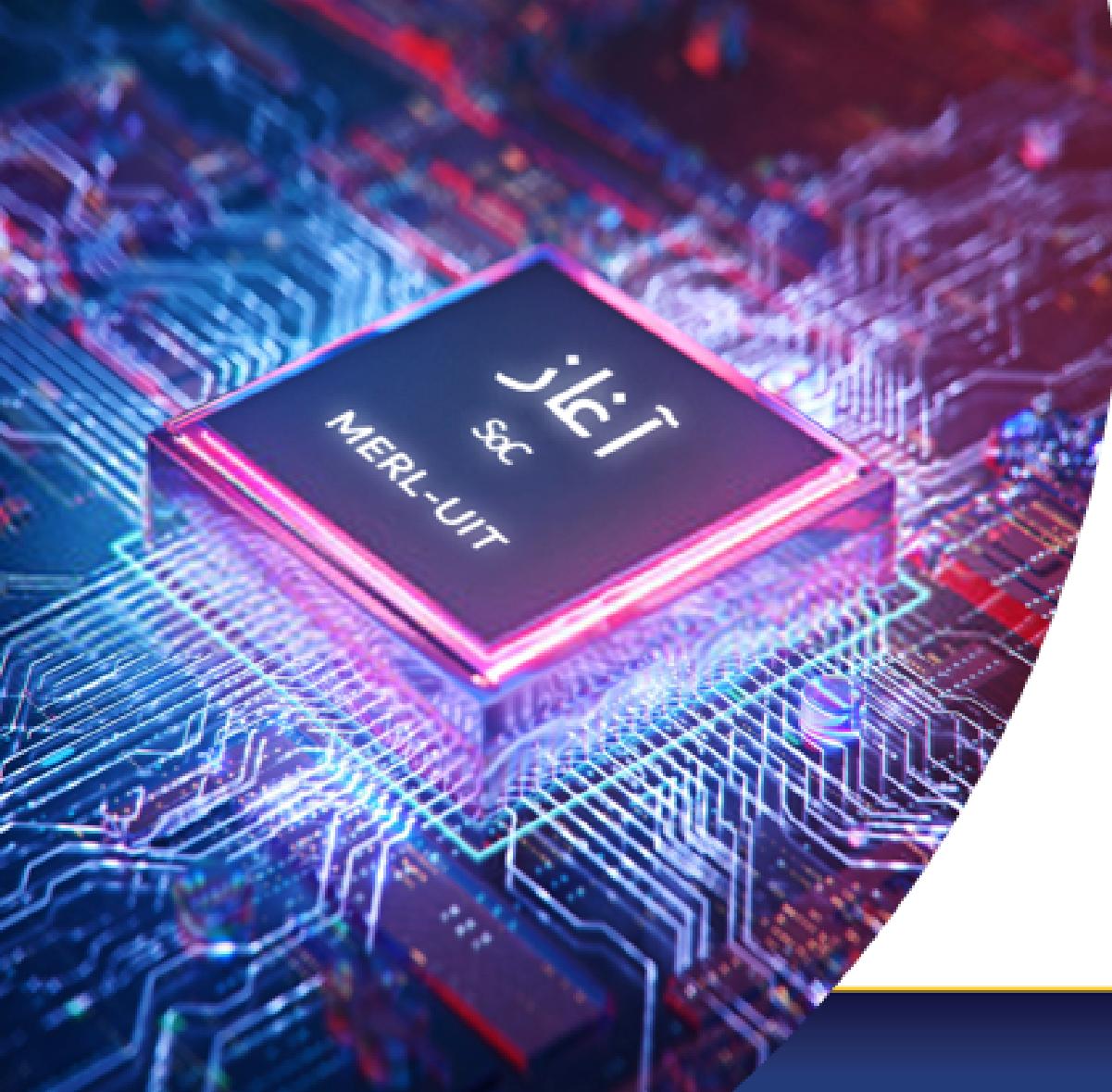
Hardware Cores/SoCs

Reverse Engineering of Rocket Chip

Roomi Naqvi - Director, Micro Electronic Research Lab -UIT



(آغاز) Aghaaz SoC The Beginning



MERL-UIT
PAKISTAN

#RISCVSUMMIT @risc_v

Collaboration during journey



[2022 Program](#)

Micro Electronics Research Lab - UITU

Accelerating Engineering Innovation



Selected as the only host organization from Pakistan- We have successfully mentored open source projects in Google Summer of Code 2022.

CONGRATULATIONS



Rameen Anwar
FACULTY MEMBER



Kinza Qamar
CLASS 2022



Talha Ahmed
CLASS 2022



Nameer Iqbal
CLASS 2023



Nimra Khan
CLASS 2023

FOR GETTING GLOBAL RECOGNITION AS CONTRIBUTOR AT

Google





We are the part of Pakistan's first National Semiconductor Plan



Zeeshan Rafique
Karachi, Pakistan

Student, Usman Institute of Technology

[Read More](#)



RISC-V Ambassador from Pakistan



Mohamed Kassem • 1st
Creating a world where a 14-year-old designs a chip
4mo •

Congratulations to the #MERL team. A fantastic example of teaming and realizing new ideas.

[Google - SkyWater Technology Foundry - Efabless Corporation](#)

<https://lnkd.in/erJqXpiS>



Pakistan's First Open Source RISC-V Microprocessor Designed at UIT- MERL



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Thank
you

