Designing of Analog/Mixed Signal IPs for Digital Processors using Open Source Tools

Syed Arsalan Jawed, PhD

Founder
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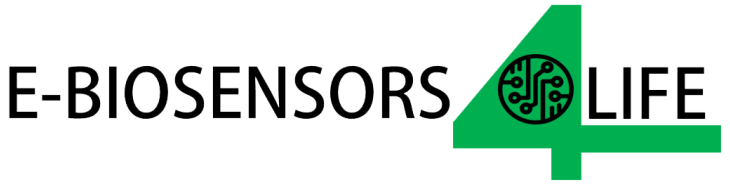


Flow of the Presentation

- The Speaker and the Team
- Challenges and Opportunities in Analog Mixed Signal (AMS) design
- Open Source Analog/ Mixed Signal (AMS) Design Platform
- IP design Ecosystem
- Conclusion

Syed Arsalan Jawed, *the reluctant PhD*

(Founder/Director/Professor/HOD/Father/Son/Husband – *the Student*)

Syed Arsalan Jawed, PhD did his Ph.D. in analog/mixed-signal Integrated Circuit (IC) design from the University of Trento, Italy in 2009. He is currently HOD Avionics at KIET. He also worked with reputed organizations: ST microelectronics Analog Devices, NESCOM, Open-Silicon, EFABLESS, and KACST

Education

- **PhD in Analog IC Design** from **University of Trento, Italy**
- Masters in System-on-Chip from **Linköping University, Sweden**

Work History

- **Professor/HOD Avionics**/Director EDCAS, **PAF KIET** [2014 - 2023]
- System Architect, **Open-Silicon Inc**. [2012 – 2014]
- Analog IC Design Consultant, **NESCOM**, Pakistan [since 2009]

Scientific Achievements

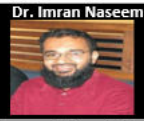
Total no of international Publications	ICs Tape-out	International Patents	Recent Research Projects 10
31	15	3	Funding PKR 170M+

Funded National and International R&D Projects

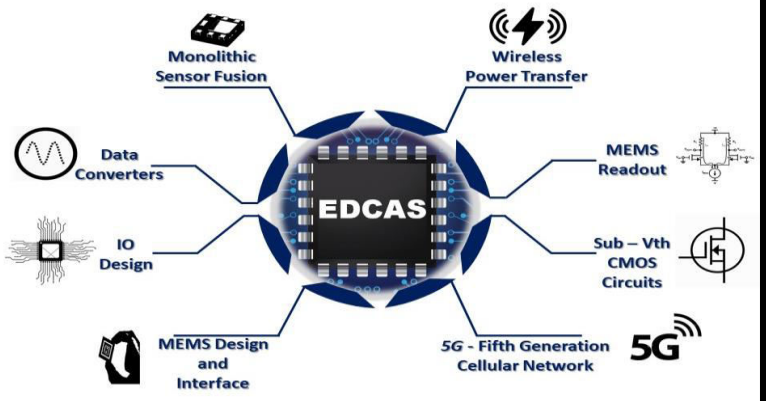
- **HEC, NCAI** **Portable Test Kit for Pathogen Detection** in 2022
- **HEC, NCRA** **Indigenous Full Flight Motion Platform** in 2021
- **PSF** **Integrated Bio sensor** in 2021
- **PAC KAMRA** **Solar Blind UV Imager Design** in 2021
- **IGNITE,KACST** **CMOS Monolithic Microsystems** in 2018.
- **HEC NRPU** **WIRELESS Power Transfer System** in 2018.
- **UAEU-Al Ain** **Vaccine Monitoring System** in 2017.
- **EFABLESS** **Bandgap Reference Circuit**, CA in 2017.
- **UAEU-Al Ain** **Ultra-low power digital standard cell library** in 2018
- **KACST, KSA** **LVDS IO Transceiver** in 2015.

Team's Profile - EBIOSENSORS4LIFE

Team consists of foreign qualified PhDs and Masters of Science who have extensively worked in academia and industry and have developed several patented systems in specialized electronic fields.

Dr. Syed Arsalan Jawed 	Principal Investigator	- Lead the designers for the design, integration, testing and documentation related to the project. - Arrange, Organize, Participate and Coordinate design activities such as literature review, functional components design, layout, testing - Arrange and Coordinate weekly research group meetings. - Lead and coordinate the reports to NCAI. - Actively participate in knowledge dissemination - Arrange and Coordinate visits to potential end-users
Dr. Imran Naseem 	Co-Principal Investigator	- Lead the Design and Integration of AI Algorithm development and backend Machine Learning - Support PI in development of reports to be sent to NCAI - Actively participate in Knowledge dissemation
Muhammad Aaquib Shahbaz 	Design Engineer-Front End Electronic Interface	- Design and simulation of the readout electronics for the test kit, as well as the system integration and testing in coordination with the PI.
Muhammad Junaid 	Design Engineer-Signal Processing and Data Management	- Controller design and data processing for the test kit, as well as the system integration and testing in coordination with the PI.
Syed Usman Amin 	Design Engineer-Application Development)	- Application Development for the test kit, as well as its integration and testing in coordination with the PI.
Sohail Ibrahim 	Design Engineer – Backend Artificial Intelligence (Jan 2021 – Mar 2022)	- Work closely with the project Co-PI in the design and integration of AI and Machine Learning algorithm development
Ali Zaman	Design Engineer – Backend Artificial Intelligence (Apr 2022– June 2022)	- Work closely with the project Co-PI in the design and integration of AI and Machine Learning algorithm development
Irfan Muqim 	Funded Masters Student	- Work with the associated sub-group leads and participate in the design, integration, testing, and documentation of the system.
Dr. Shahana Urooj Kazmi 	Consultant – Microbiologist - Expert	- Work with PI and Co-PIs offline supervised training of the server as well as biological testing of the kit.
Dr. Kausar Abbas Saldera 	Medical Expert	-Work with PI and Co-PIs offline supervised training of the server as well as biological testing of the kit
Dr. Shakil Awan 	Honorary Co-Principal Investigator (UK Partner)	- Provide an adequate number of fabricated and bio-functionalized Graphene-FETs based BioSensors
Ejaz Tayyab 	Industrial Partner	- Support in Component Procurement - Business Plan development, Mass Production and Commercialization

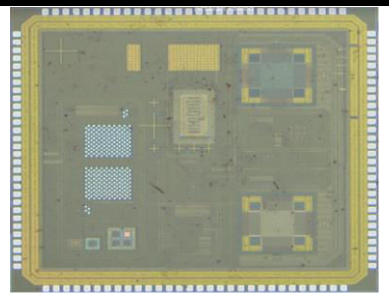
ICs/IPs Designed by the Team in last 09 Years



IC Design Focus Areas

- Monolithic Fusion of Multiple Sensors on a Single IC
- MEMS Sensor Design and Interface (Accelerometers, Bolometers, BIO-MEMS)
- Analog / Digital IP Design
- CMOS / Bi-CMOS Circuit Design
- CMOS Sub-Vth Circuits
- Ultra Low Power Circuits
- MEMS Readout Design
- IO Design
- Data Converters
- Wireless Power Transfer
- 5G Front End Circuits + Antennas

July 2020

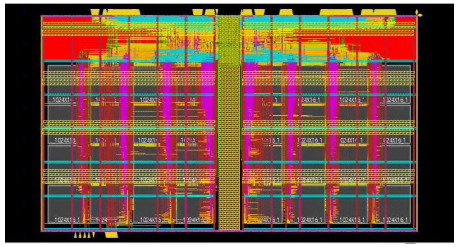


Monolithic CMOS MEMS Multi- Sensors with ROIC

April 2018

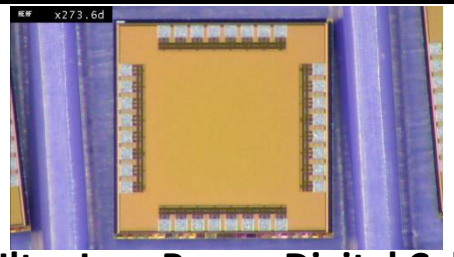
Active Quasi Circulator

March 2018



APR in 45nm for AWG

January 2018

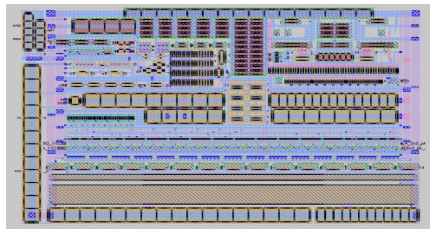


Ultra Low Power Digital Cells

January 2017

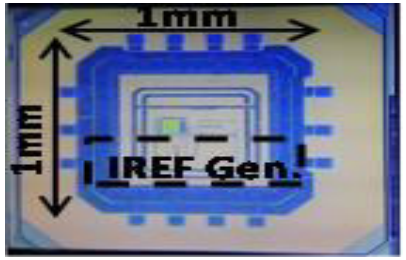
WPT Vaccine Monitoring ASIC

February 2017



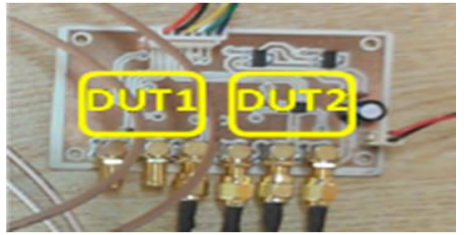
Low Power Bandgap Reference

November 2015



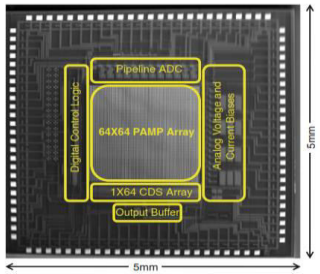
LVDS Transceiver in 110nm

September 2015



LVDS Transceiver in 150nm

September 2014

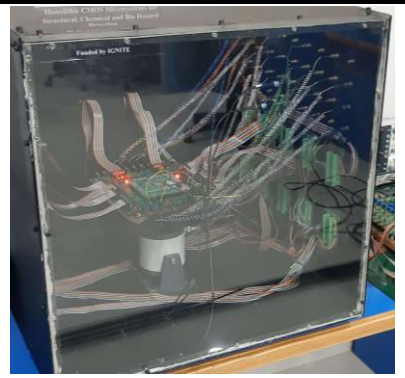
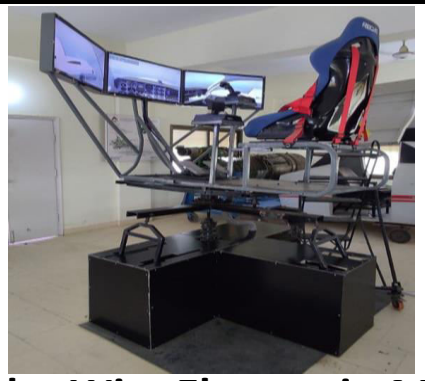
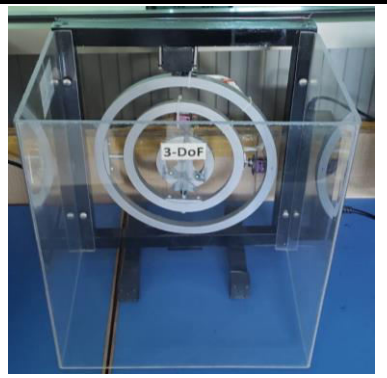


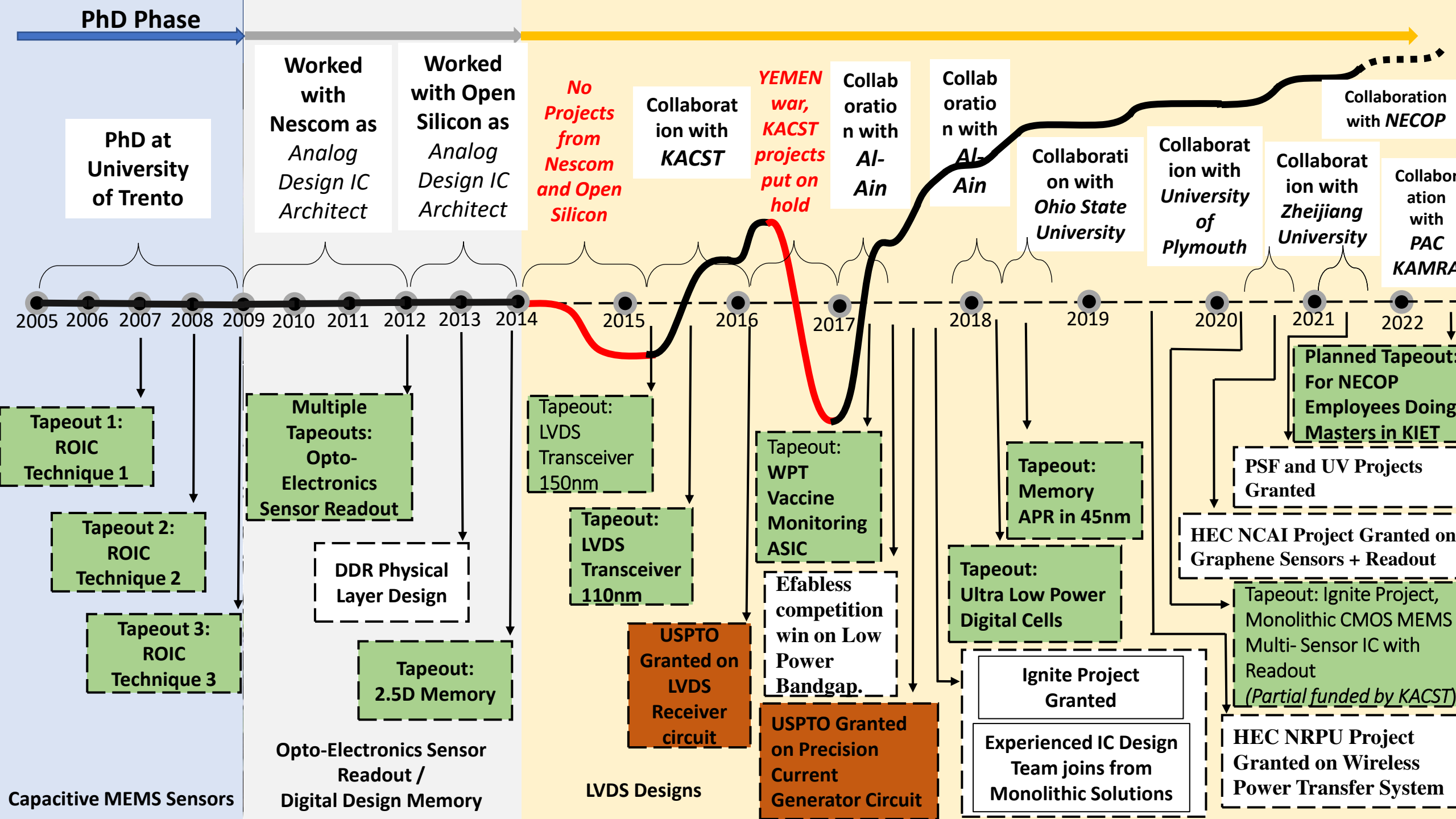
IR Imager

Systems Designed by the Team

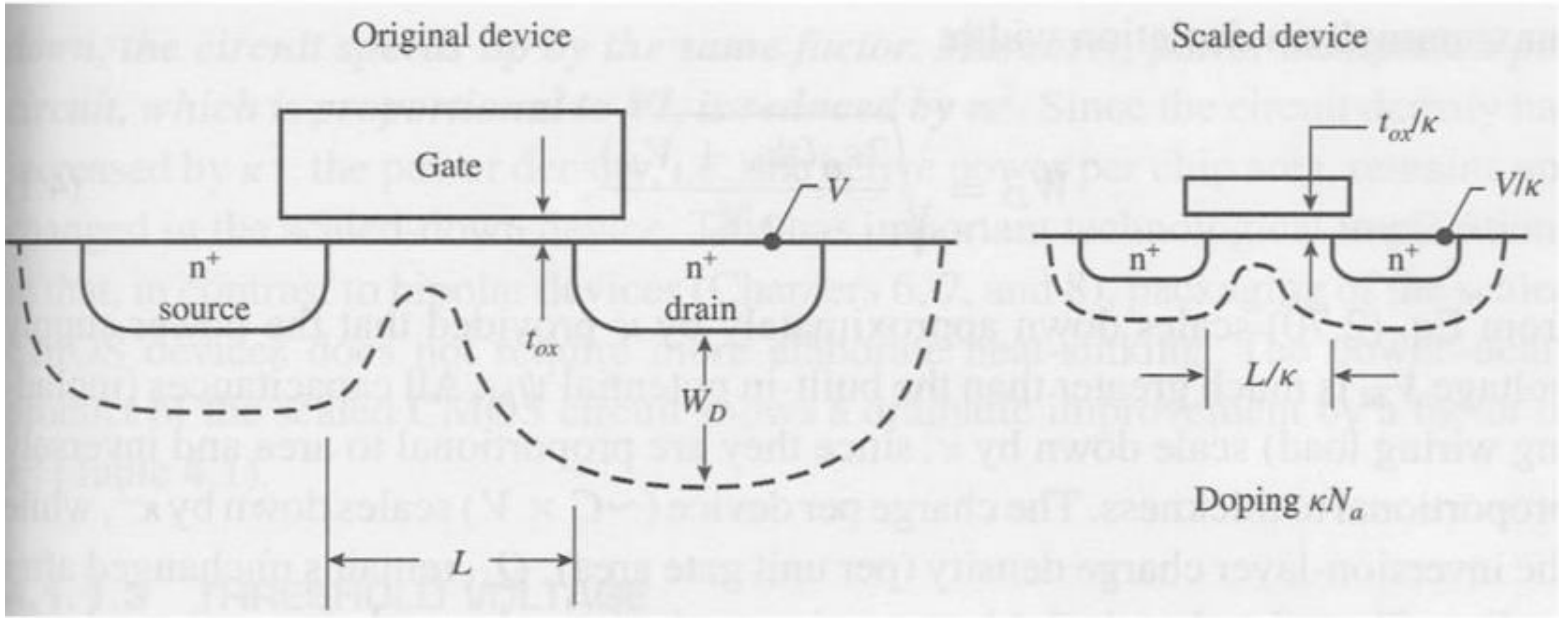
System Designed in last 5 years

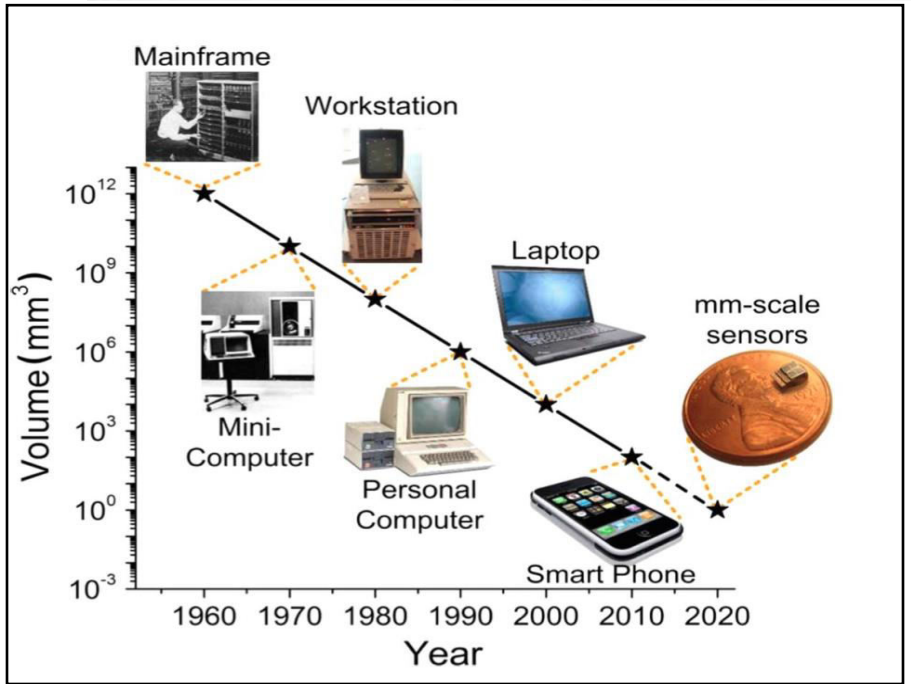
- Merge motion, visual and environmental cues with bio-sensing for more immersive experiences
- From cure to prevention through early disease detection by a pervasive network of bio-sensors
- Flight/Vehicle Simulators
- Cognitive Therapy Devices

Jan 2023	*Dec 2022*	*July 2021*
		
Gaming / ASMR Therapy Sofa for Indoors	**AI Powered POC Electronic Test Kit**	**In-house 6-DoF Full Flight Motion Simulator**
June 2020	***Nov 2019***	***Dec 2018***
		
Vibration Test Setup	**Fly-by-Wire Electronic 4 DOF Full Flight Simulator**	**First Flight Testers (FFT) / Rate Table**

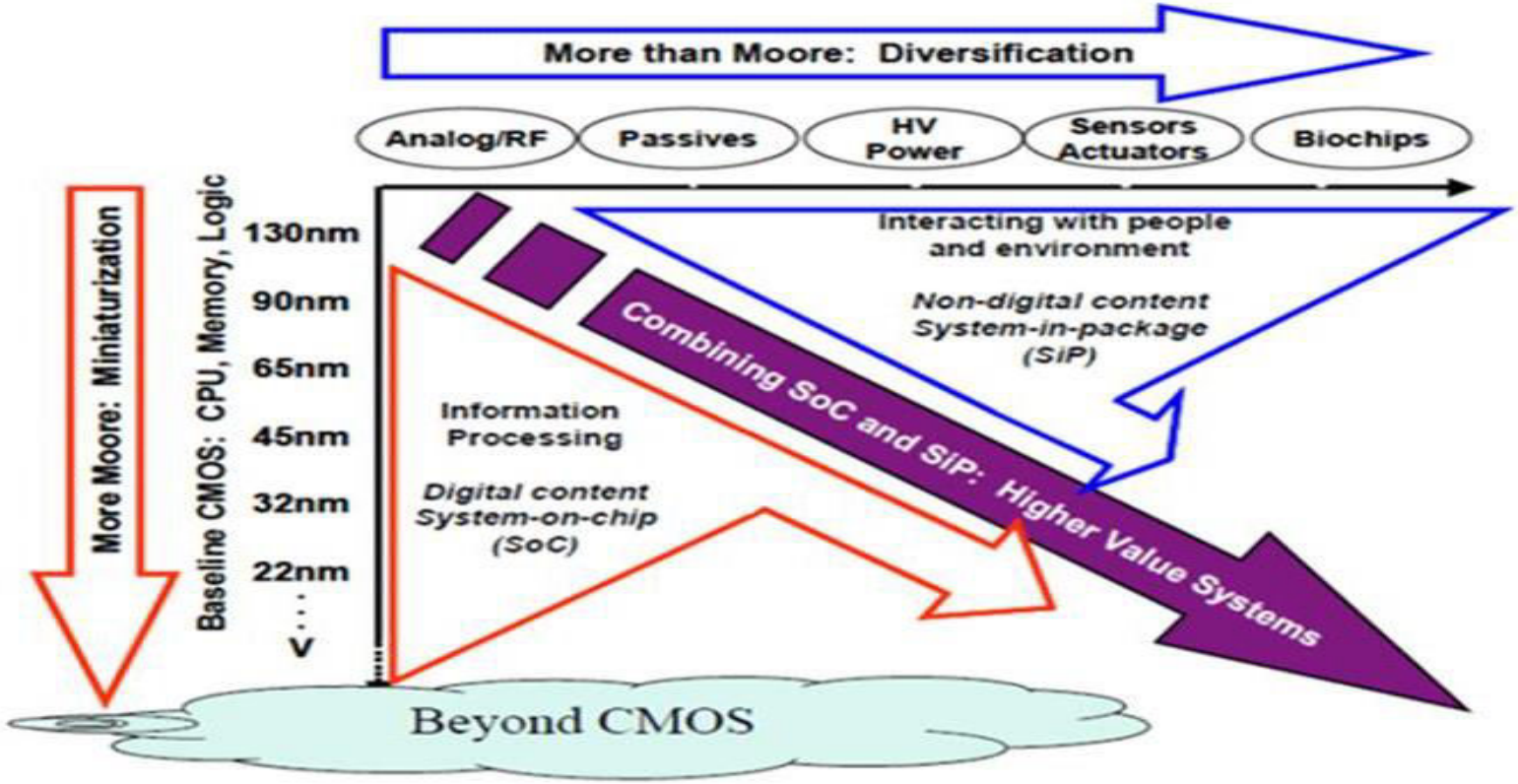

PhD Phase
PhD at University of Trento
Worked with Nescom as Analog Design IC Architect
Worked with Open Silicon as Analog Design IC Architect
No Projects from Nescom and Open Silicon
Collaboration with KACST
YEMEN war, KACST projects put on hold
Collaboration with Al-Ain
Collaboration with Al-Ain
Collaboration with Ohio State University
Collaboration with University of Plymouth
Collaboration with Zheijiang University
Collaboration with NECOP
Collaboration with PAC KAMRA
2005 2006 2007 2008 2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021 2022
Tapeout 1: ROIC Technique 1
Tapeout 2: ROIC Technique 2
Tapeout 3: ROIC Technique 3
Multiple Tapeouts: Opto-Electronics Sensor Readout
DDR Physical Layer Design
Tapeout: 2.5D Memory
Tapeout: LVDS Transceiver 150nm
Tapeout: LVDS Transceiver 110nm
USPTO Granted on LVDS Receiver circuit
Tapeout: WPT Vaccine Monitoring ASIC
Efabless competition win on Low Power Bandgap.
USPTO Granted on Precision Current Generator Circuit
Tapeout: Memory APR in 45nm
Tapeout: Ultra Low Power Digital Cells
Ignite Project Granted
Experienced IC Design Team joins from Monolithic Solutions
Planned Tapeout: For NECOP Employees Doing Masters in KIET
PSF and UV Projects Granted
HEC NCAI Project Granted on Graphene Sensors + Readout
Tapeout: Ignite Project, Monolithic CMOS MEMS Multi- Sensor IC with Readout (Partial funded by KACST)
HEC NRPU Project Granted on Wireless Power Transfer System
Capacitive MEMS Sensors
Opto-Electronics Sensor Readout / Digital Design Memory
LVDS Designs

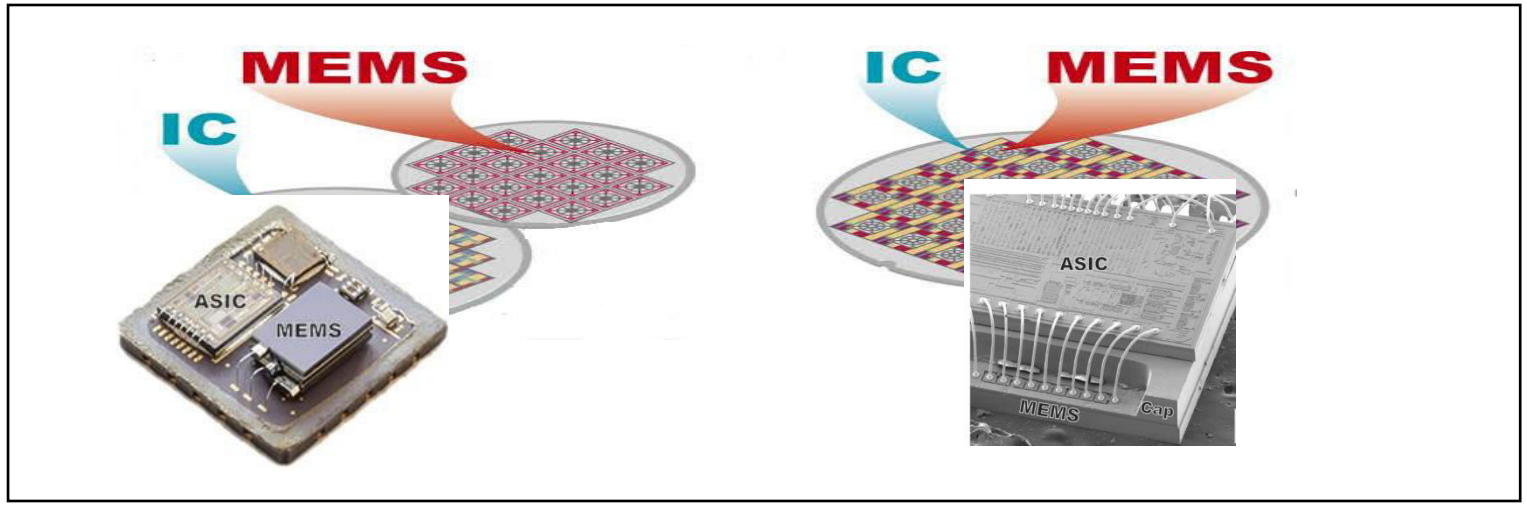
About the Technology Scaling and Miniaturization, *the Moore's Law*





The More-than-Moore Paradigm – Analog/Mixed-Signal Associates are not scaling





Why Analog resists miniaturization?

- Gain Unit is the Atomic Unit like a Digital Inverter

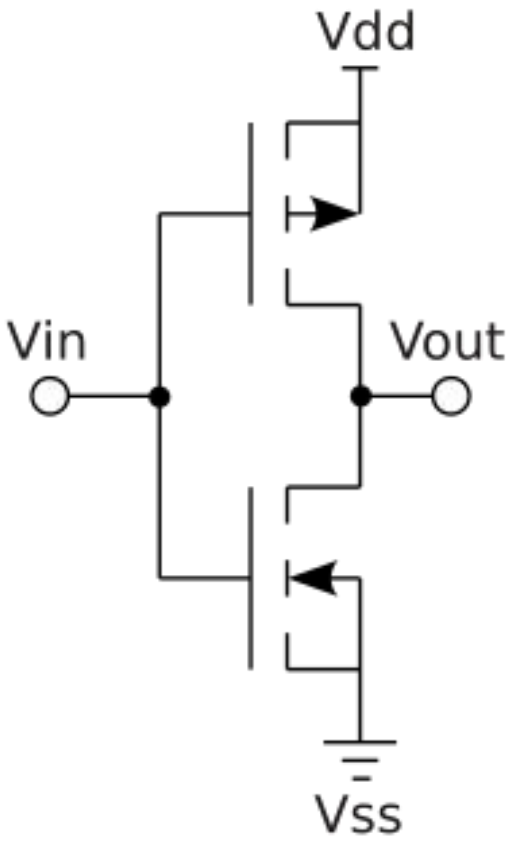
- DIBL in deep submicron reduces intrinsic gain down to 20-40dB.

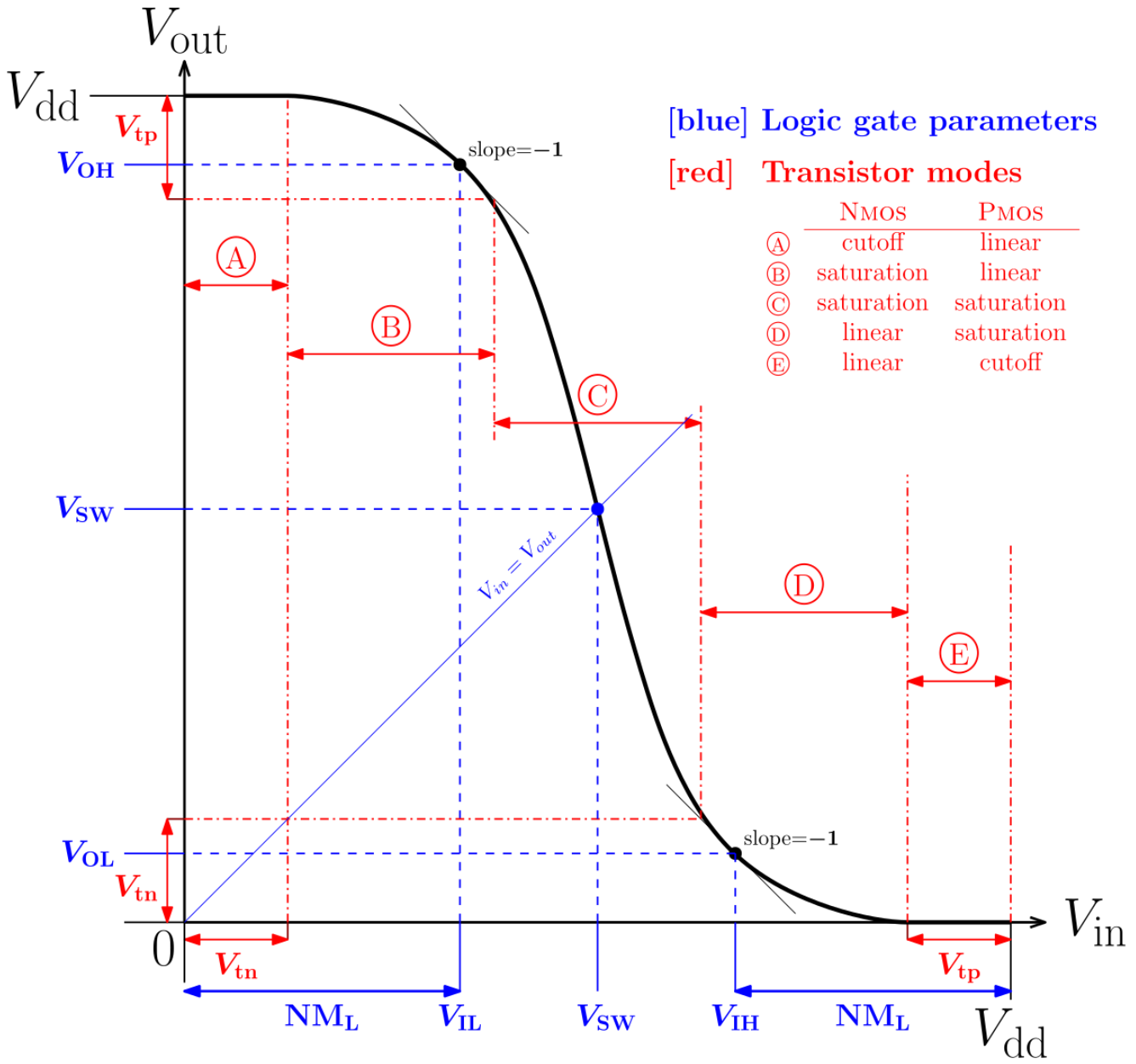
- Leakage profiles

- Integration of R and C and L are expensive

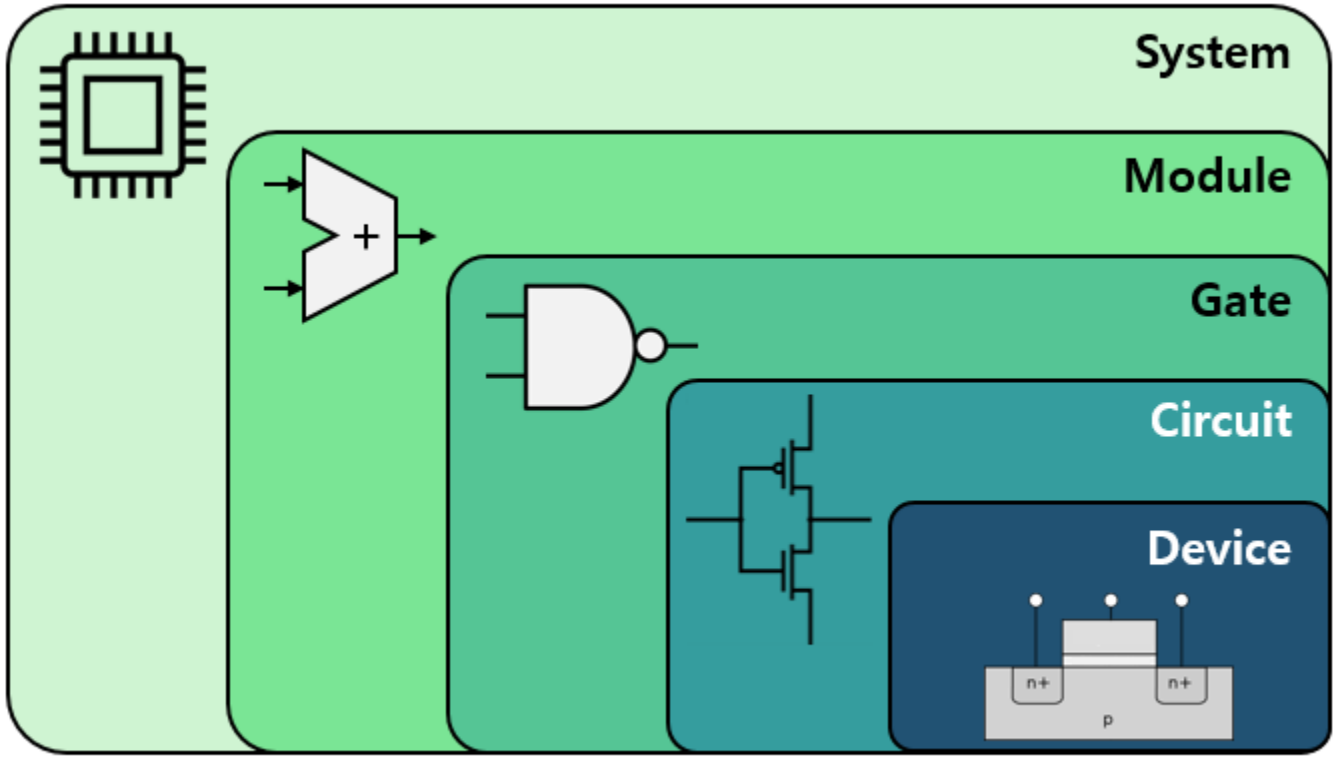
Let's Pause : What is Digital ?

If you look closely, then everything in actually analog!

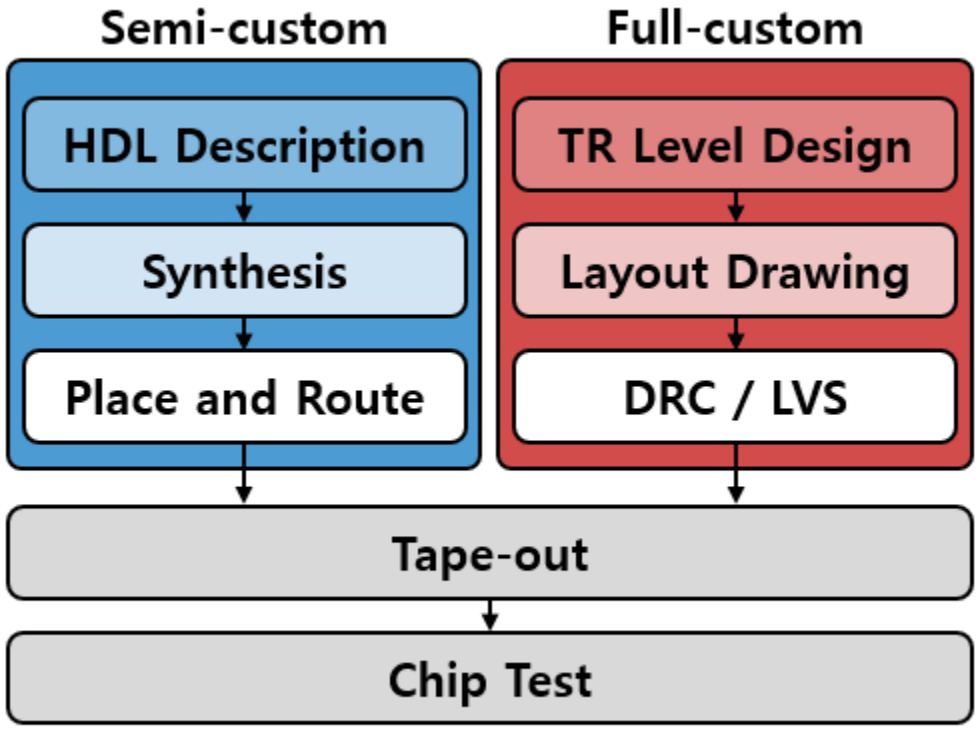




ASIC Design Flow

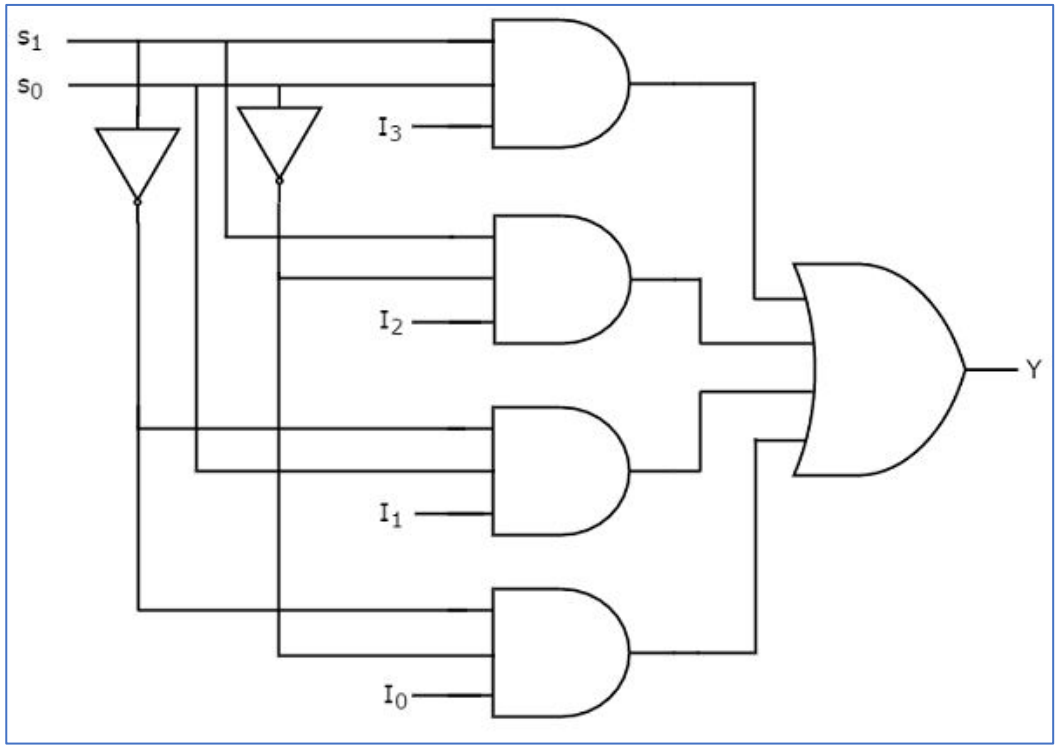


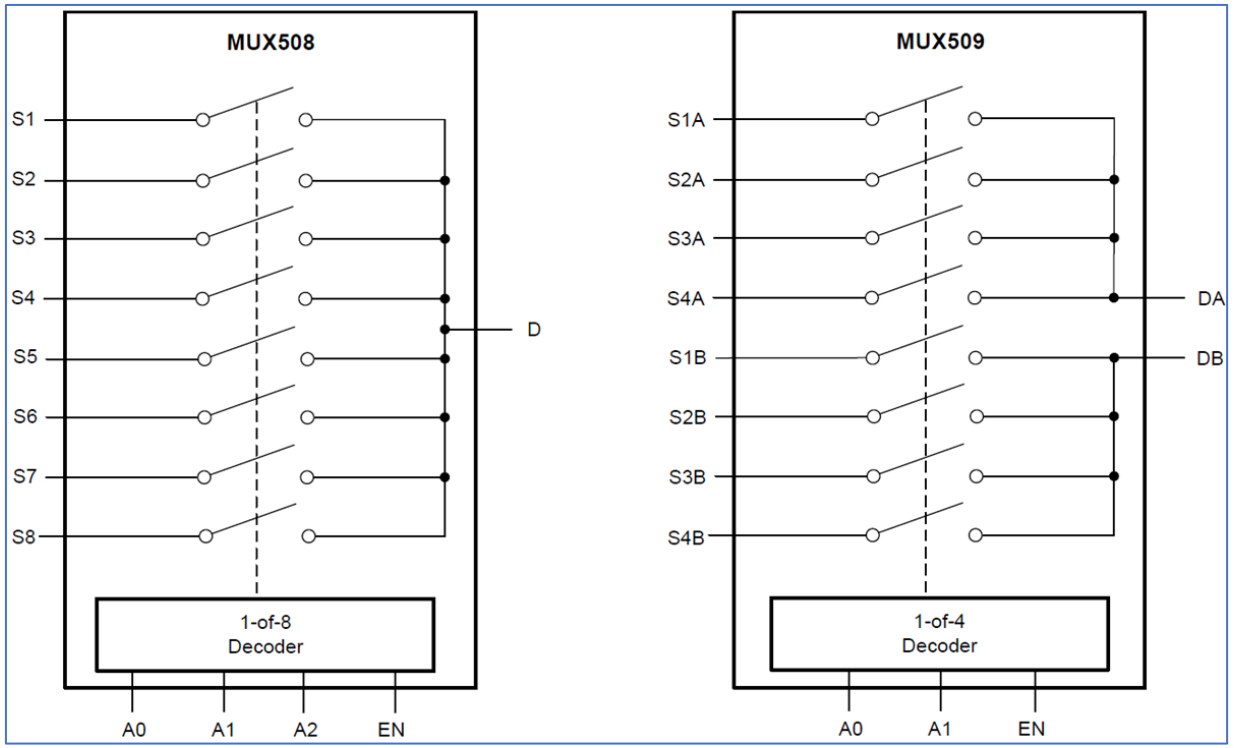
Design Abstractions



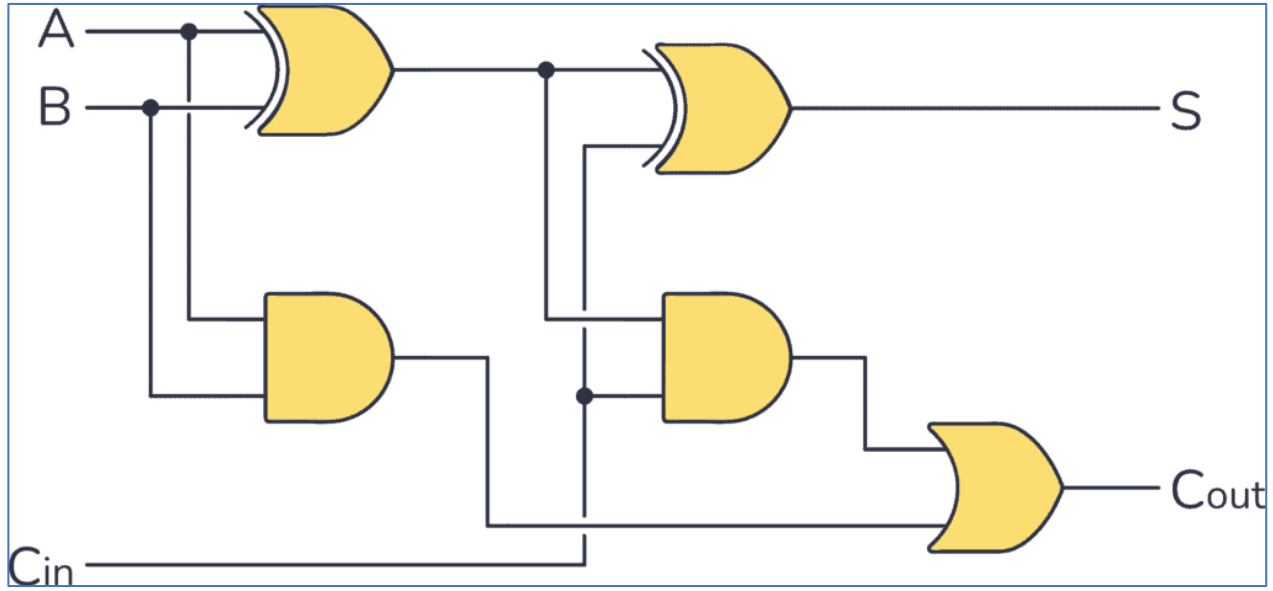
Design Flow

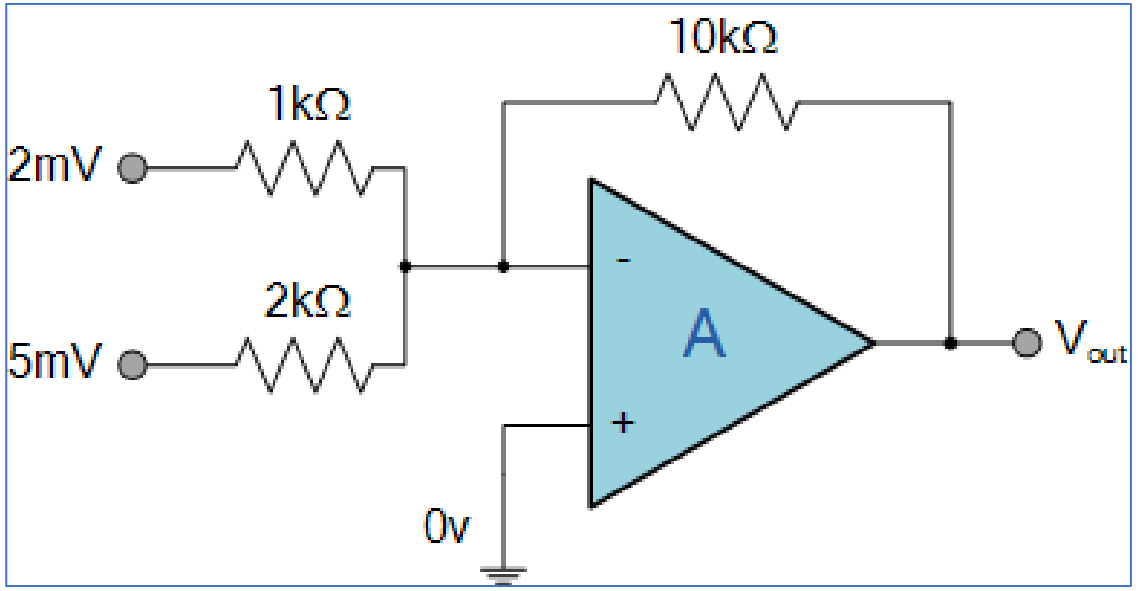
The Advantage of Lower Abstraction Level and Analog Thinking





The Associated Complexity of Analog





Why bother about analog in Digitals IC?

Starting with Simpler Blocks

Analog mixed-signal (AMS) blocks in digital ICs are of paramount importance because they enable a wide range of functionalities and features that are critical in modern electronics.

IO Cells	Require special handling of I, V , Impedance matching, signal integrity
ESD Blocks	Require very specific IV modeling and specific physical design to meet different ESD standards
Voltage References	Require deep understanding of CTAT, PTAT behaviors and directly affect NM
Current References	Critical for low power digital design and protection limits as well, require deep understanding of CTAT/PTAT
PLL	Main workhorse to generate precision oscillator blocks, require deep understanding of charge-pumps, comparators etc.
DLL	Required for delay-equalization in clock tree distribution, oscillators, require deep understanding of RC and MOSFET based delays
ADCs	Interface to the real world
DACs	Interface to the real world

Why bother about analog in Digitals IC?

Complex Cells

Analog mixed-signal (AMS) blocks in digital ICs are of paramount importance because they enable a wide range of functionalities and features that are critical in modern electronics.

Sensor Integration	Digital devices interact with the real world through sensors, AMS blocks are essential for interfacing with these sensors
Signal Processing	AMS blocks are crucial for various signal processing tasks like filtering, amplification, and modulation/demodulation
Power Management	Digital ICs often require precise and efficient power management to regulate voltage levels, minimize power consumption, and extend battery life
Control Loops	Control loops often require both analog and digital components to maintain stability and accuracy.
Data Conversion	ADCs and DACs are essential for converting real-world signals into digital format and vice versa.
Calibration & Compensation	AMS blocks are used for calibration and compensation techniques, which are essential for ensuring the accuracy and reliability of digital systems
Noise Mitigation	Analog circuitry within digital ICs can help mitigate noise and interference, improving signal integrity and overall system performance.
High Speed Interfaces	High-speed digital interfaces like USB, HDMI, and Ethernet often require analog front-end components for signal conditioning, equalization, and impedance matching
Miniaturization & Versatility	AMS blocks add versatility to digital ICs, making them Compact, multifunctional, more portable, and power-efficient, suitable for a wider range of applications

Automated vs Full Custom Design

- Full custom design is almost essential for analog and mixed-signal circuits, where the precise placement and sizing of components are critical **to achieving desired specifications/standards**

- When designing unique or unconventional architectures, full custom design provides the flexibility to **experiment with new ideas** and create custom solutions tailored to the application's specific needs

- Automated design tools might not provide adequate support for older technologies, Full custom design allows designers to **work within the limitations** of these processes effectively.

- Full custom design allows engineers to make **trade-offs between various parameters** (e.g., performance, power, area) according to specific project's needs. Automated flows focus on a limited set of design goals.

- Full custom design comes at the cost of longer development times and increased design complexity. **Automated design flows are generally more efficient for standard digital designs**, where performance requirements can be met without extensive manual optimization.

- **A mix of both FULL CUSTOM and AUTOMATED design**, leveraging the strengths of each to achieve a balance between performance, time-to-market, and resource efficiency.

AMS - OPEN SOURCE EDA

Why should we care about Open source EDA ?

- **EDA Tools availability is one of the Semiconductor Design Blocker**
  - EDA Tools have their own COST.
- **There are 3 major EDA companies :**
  - Cadence , Mentor Graphics and Synopsys
  - Spend lot of money on their RnD – Charges High Fees
  - Working with clients like Apple, NVIDIA and Qualcomm
- **The EDA industry is not all suited to support smaller guys like us.**
- **Another thing is Research and commercial industry dependence on IPs that cost a lot of money or require an NDA.**
- **Students, teachers, and other enthusiast do not necessarily have access to this type of stuff.** Hence reduces the number of people proficient with these tools.

cadence®

Mentor Graphics®

SYNOPSYS®

AMS - OPEN SOURCE EDA

Humble start but rapidly evolving

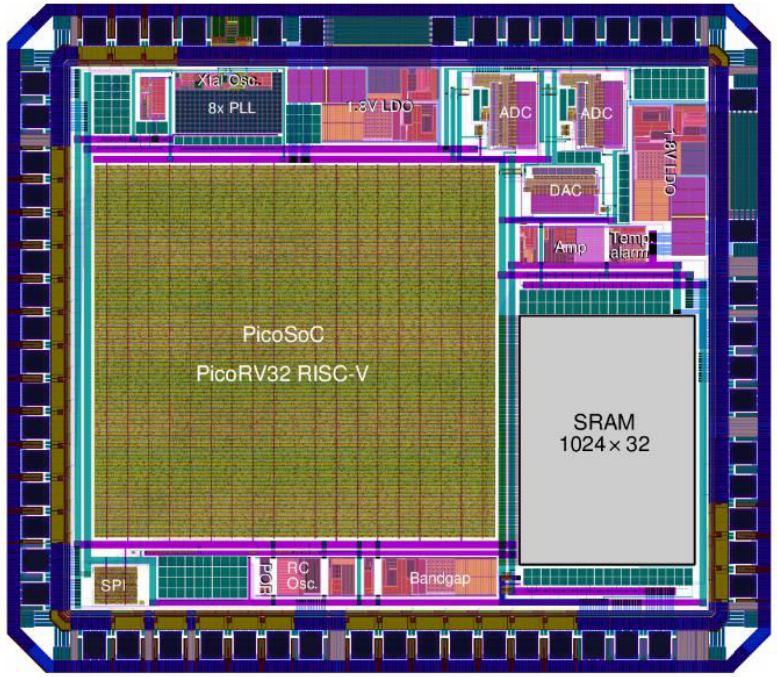
Availability and Research Benefits

- **Free Tools already existed in open source EDA ecosystem**
  - **XCHEM** is an open-source digital schematic capture program, and it can be used for analog mixed-signal design as well.
  - **NGSPICE or XYCE** are open-source general purpose circuit simulation programs
  - **MAGIC VLSI or KLayout** are used for creating and modifying circuit Layout
  - **VIS** is an open source tool used for formal verification
- **Open Source EDA offers interoperability and collaboration**

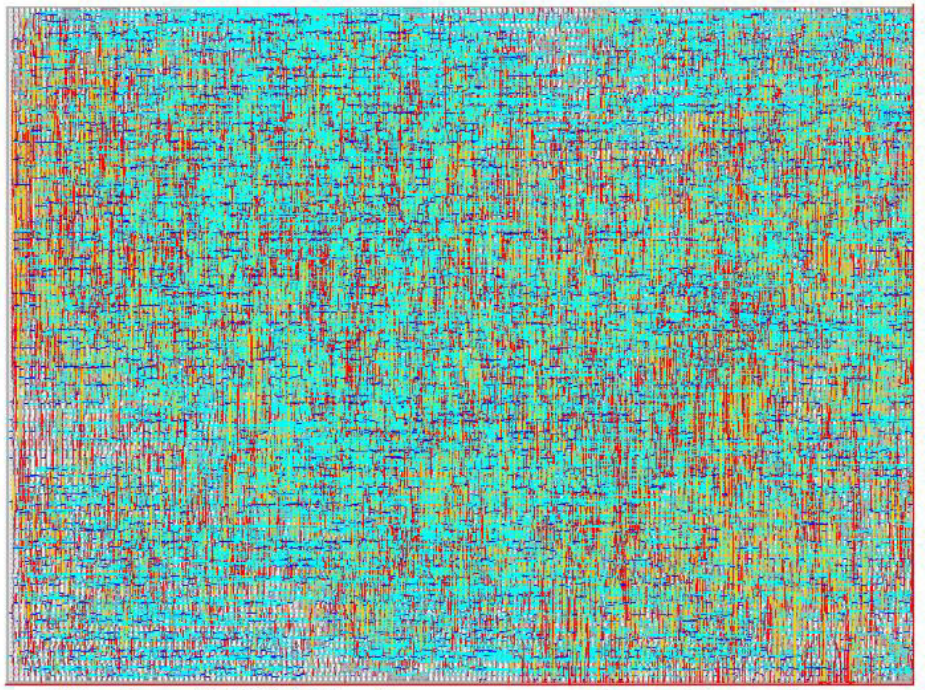
QFLOW-An Open-Source Digital Synthesis Flow

- **QFLOW –** Take Verilog source file and give physical layout (ready for fabrication)

- **QFLOW** bundled free tools together to create end-to-end software flow : YOSYS – for Verilog parser, High-level synthesis, Logic optimization and Verification, GRAYWOLF – for Cell Placement, QROUTER – for detailed Metallic Routing, VESTA - Static Timing Analysis and MAGIC – Layout Viewer.



The Raven RISC-V microprocessor from efabless

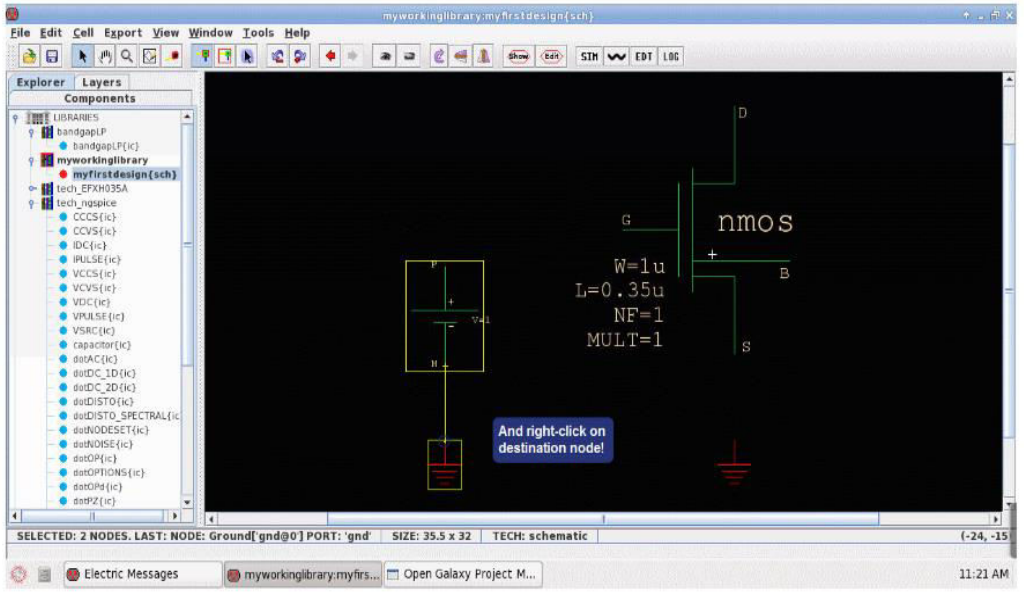


The OpenMSP430 microprocessor from OpenCores, placed and routed by qflow.

EFABLESS – The Caravel Project – SOC Harness Umbrella

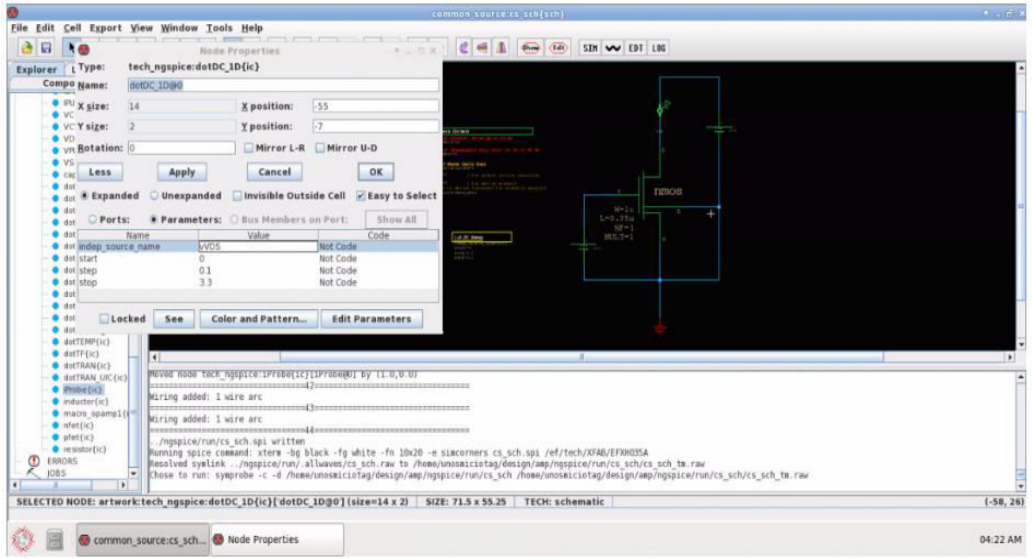
ELECTRIC – Schematic Editor

An open source tool for electric and electronic circuits. Such a circuit may comprise of JFETs, bipolar and MOS transistors, passive elements like R, L, or C, diodes, transmission lines and other devices.



NGSPICE – Simulator

Offers a wealth of device models for active, passive, analog, and digital elements. Model parameters are provided by the semiconductor manufacturer, or from foundries. The user adds her circuits as a netlist, and the output is one or more graphs of currents, voltages and other electrical quantities or is saved in a data file.

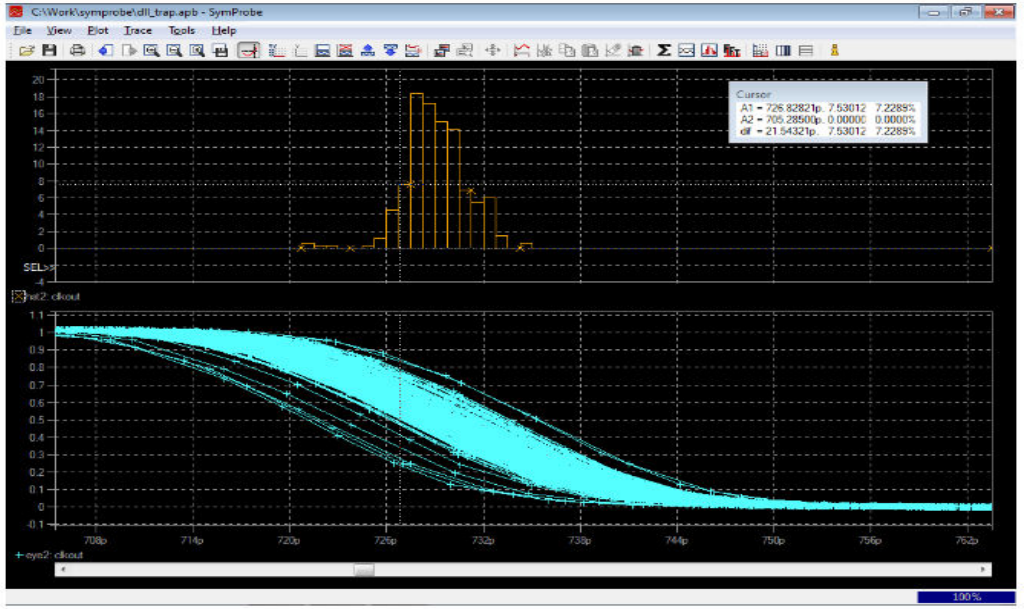


EFABLESS - OPEN SOURCE EDA TOOLS

SymProbe/GTKWave–Waveform Viewer

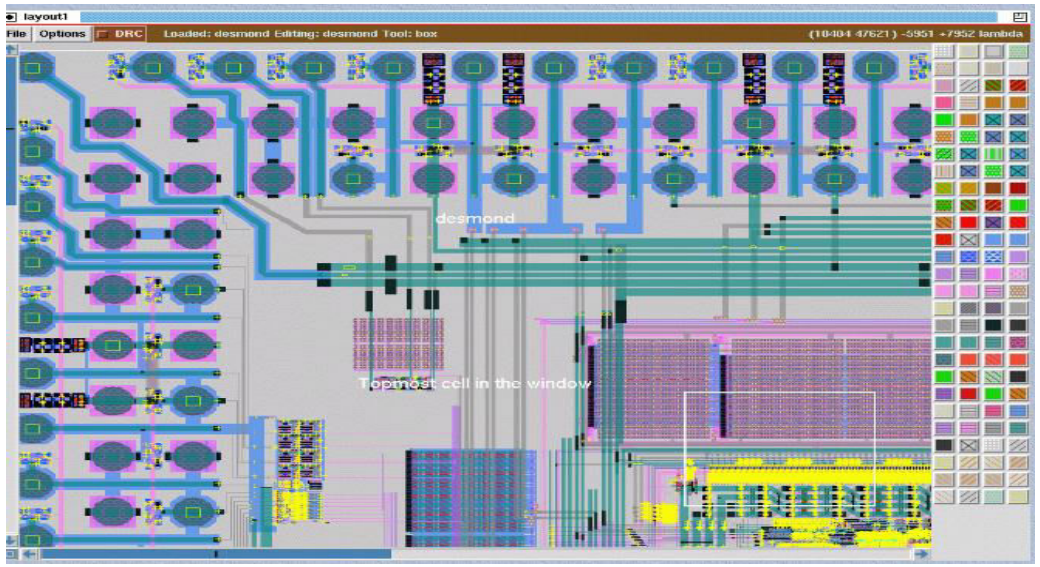
Offers all the functions designers expect in a convenient graphical interface.

- viewing results for TRAN, DC, AC, SWEEP, Monte Carlo
- customizable views of multiple plots
- multiple X/Y axes in one plot
- flexible X/Y adjustment of axes
- measurement cursor
- waveform drag-and-drop operations
- enhanced printing functionality with vector EMF waveform output



Magic – Layout

Magic is widely cited as being the easiest tool to use for circuit layout, even for people who ultimately rely on commercial tools for their product design flow.



AMS - OPEN SOURCE EDA

The Process Design Kit or PDK Roadblock

- **The PDK and EDA tools are very tightly coupled**
- **Foundry provide support to big EDA vendors**

  TSMC's only most important customer like APPLE get to see their advanced nodes.

  Even for older node you need to sign an NDA

- **For business perspective some Foundry offers away older and less sophisticated node for open sourcing.**

  Recently **Skywater** partnered with **Google** to launch a 130nm PDK – freely available on GitHub .

  Similarly programs like **FreePDK** and **OpenRoad** offers their PDKs for only academia and research purposes.

skywater TECHNOLOGY

GLOBAL FOUNDRIES

FOSS 130nm Production PDK
github.com/google/skywater-pdk

FOSS 180nm Production PDK
github.com/google/gf180mcu-pdk

Google

efabless.com

Analog IPs for Digital Chips

A Viable Business Model – Redesign, Porting.

- **Analog IPs** are specialized circuits designed to handle analog functions within a **System-on-Chip (SoC).**

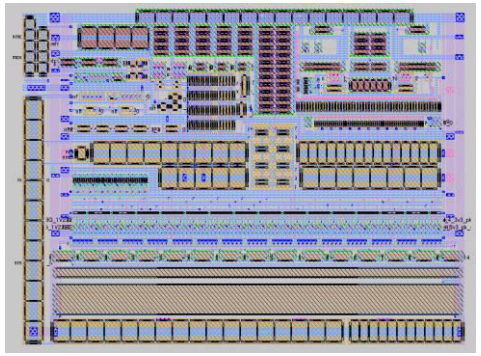
- **Analog IPs** are crucial for various applications, such as signal processing, data conversion, and power management, where analog signals need to be processed or interfaced with digital components.

- Here are some common analog IPs you might find in digital chips:

  - **Voltage Regulators:** to provide stable and regulated supply voltages to various parts of the digital chip.
  - **Analog-to-Digital Converters (ADCs):** to convert analog signals (e.g., sensor readings) into digital format so that digital processors can work with them
  - **Digital-to-Analog Converters (DACs):** converting digital values into analog signals.
  - **Phase-Locked Loops (PLLs):** PLLs are used for generating stable and precise clock signals, which are crucial for synchronous digital circuits.
  - **Analog Filters:** Analog filters, such as low-pass, high-pass, and band-pass filters, are used to shape and condition analog signals before they are processed by digital circuits.
  - **Voltage Reference Circuits:** These circuits generate stable reference voltages, which are needed

Silicon Proven Design Ips by EBioSensors4Life Team

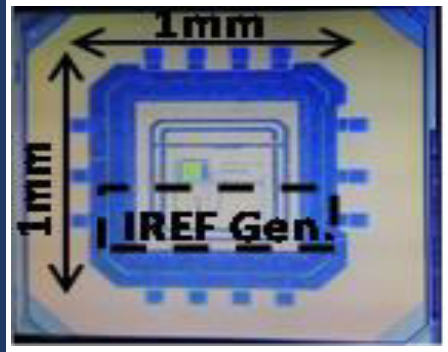
EFABLESS: Low-Power Bandgap Reference IP with EFABLESS / X-FAB



Commercially Available at the EFABLESS MARKETPLACE

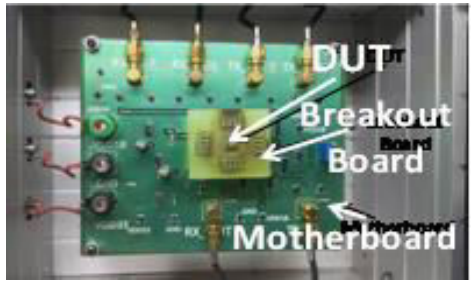
Parameter	Value	Units
Line Regulation	-392.8	Ppm/V
Load Regulation	0.02344	mV/uA
Temperature Coefficient	140.0	Ppm/°C
PSRR Positive @ 100KHz	-60.55	dB
PSRR Positive @ 1MHz	-47.49	dB
PSRR Negative @ 100KHz	-10.38	dB
Power	14.07	uW
Current	3.258	uA
Current (Standby)	0.6312	uA

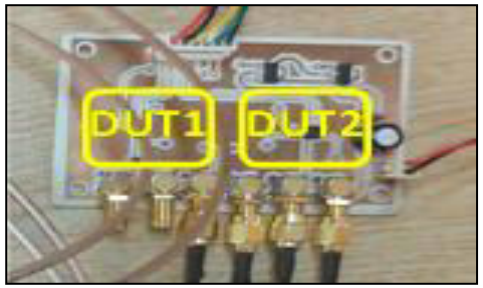
PVT-tolerant Current Reference IP (AL-AIN)



Parameter	Value	Units
Technology	150	nm
Area	0.0036	mm2
Total Power	54	uW
Reference Current	10	uA
Line Regulation	532	ppm/V
Variations	±5	%

Reconfigurable 2Gbps LVDS Transceiver IC (KACST)





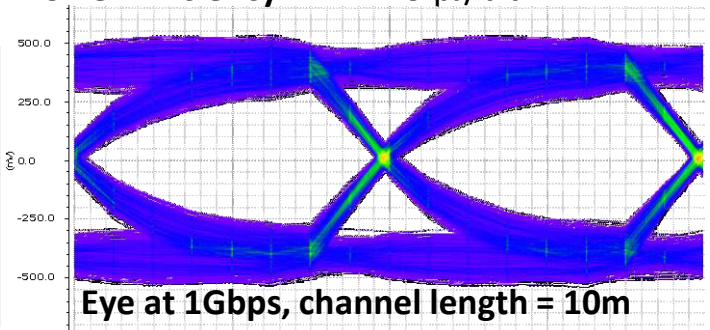
-Full-Custom Mixed-Signal Design of LVDS Transceiver

-***Silicon-Proven in both 110nm and 150nm!***

-***Cable length=*** 4 inch -- 10meters

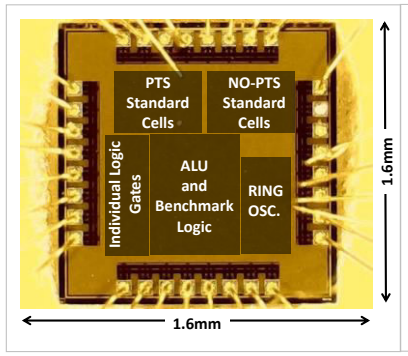
-**Power =** 17mW @ 1Gbps

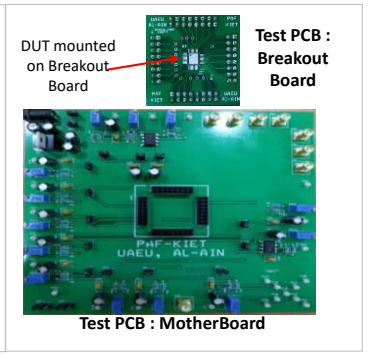
-**Power Efficiency =** 17 - 19 pJ/bit

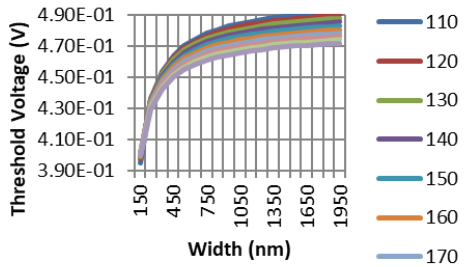


Eye at 1Gbps, channel length = 10m

Ultra Low Power Digital Standard Cell Library (AL-AIN)



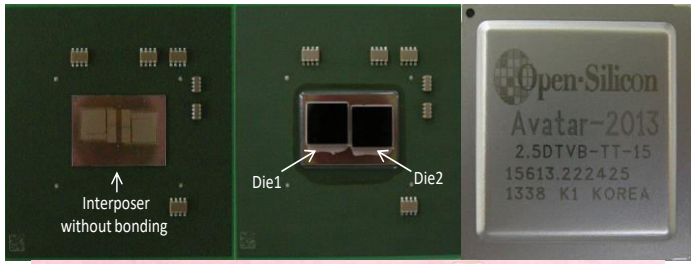


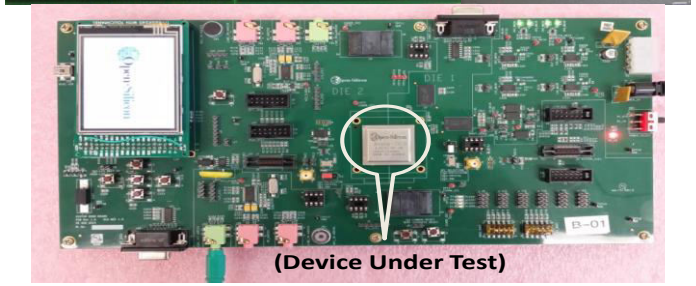


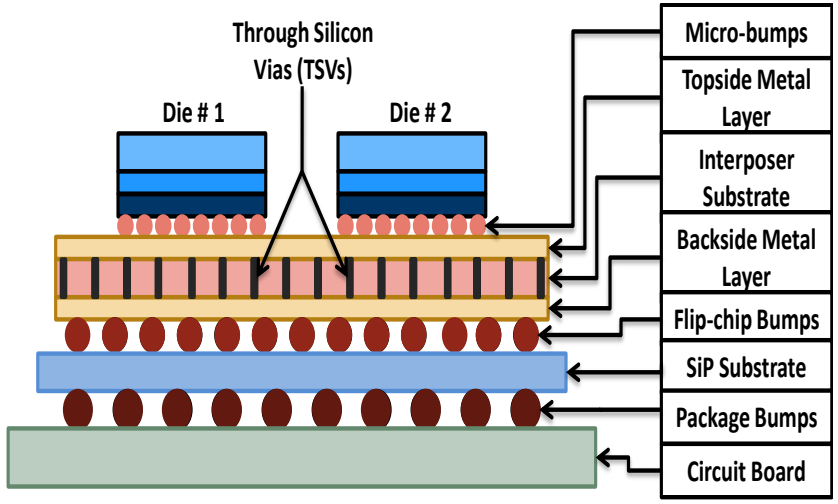
- Exploiting Inverse Narrow Width Effect in Deep Submicron Processes.
- Exploiting exponential decreases in Vth in the sub-threshold region.
- Intrinsic capacitances of the NMOS(s) and PMOS(s) scale linearly with the area.
- Exponential increase of subthreshold current competes against a linear increase in capacitances, and an improved COC is achieved.

Silicon Proven Design IPs by EBioSensors4Life Team

2.5D IO Design IP in 28nm CMOS (open silicon)







Topology	Signaling Voltage Range over the Channel	Bit-Rate (BR)	Area mm^2	Power (P)	Jitter	Leakage	FOM = P/BR (J/bit)
I	0.9V–1.8V	1Gbps	0.008	700uW	40ps	97nW	$0.7x10^{-12}$
II	0.8V–1/8V	2Gbps	0.008	1.8mW	50ps	100nW	$0.9x10^{-12}$
III	0.8V–1/8V	2Gbps	0.008	1.7mW	50ps	100nW	$0.7x10^{-12}$
IV	0.7V–1.0V	4Gbps	0.008	2mW	30ps	700nW	$0.5x10^{-12}$

Customized Digital Processor/Controller ICs Customized FPGA Architectures (OHIO State University)

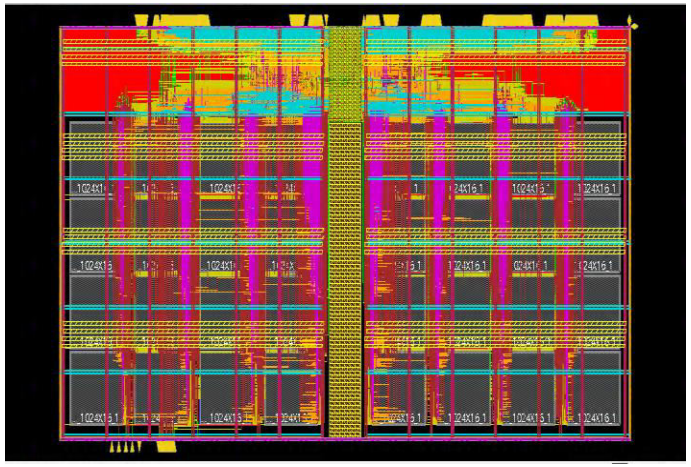
- **Secure and Customized Application-Specific Digital Processor Design at IC Level**

  Architectural Design → Design Entry → P&R → Sign Off → Fabrication → Lab Validation

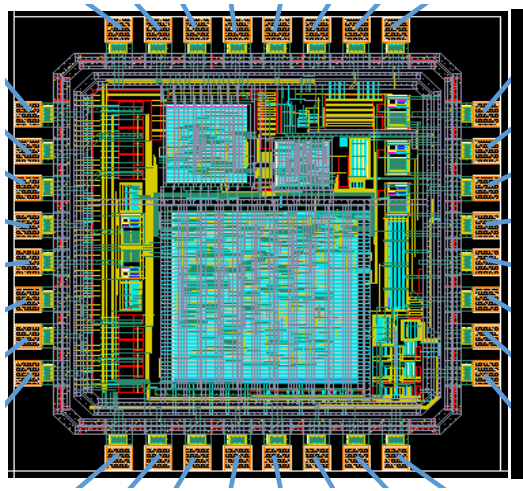
- **Custom Digital IP Design** (Medium-Density Processing Units / DSPs)

  Transistor Level → Gate Level → RTL Level → Block Level

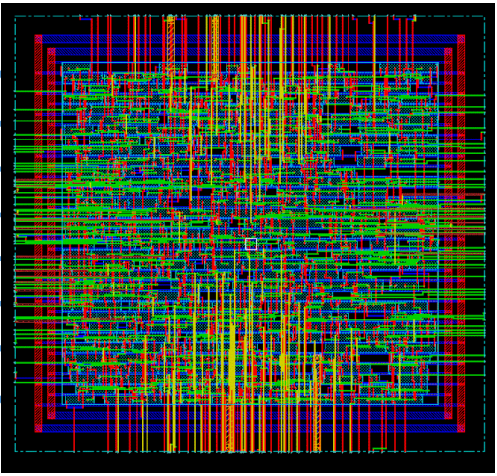
- **Customized Reconfigurable Architectures for FPGA**
  - Delivered to Ignite in 2014-15 / Delivered to Umm-ul-Qura, KSA in 2017



AWG Back End in 45nm CMOS Process, 4 GHz Design and Routing for OHIO State University



PROC. in 110nm CMOS



256 bit SPI

Conclusion

- The Analog Circuit Design is differently placed in the More Moore paradigm.
  - Gain elements require significant redesign.
  - SAR ADC is an example.
- The CAD tools still required enhanced degree of automation.
- Opensource AMS CAD tools and ecosystem are emerging for IP design
- IP design could be a viable business model depending upon expertise and area.

Thank you!