RISC-V Processor Based Chip Design

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Namal Knowledge City

An Inspiration, A Dream

Faculty
Students
Infrastructure

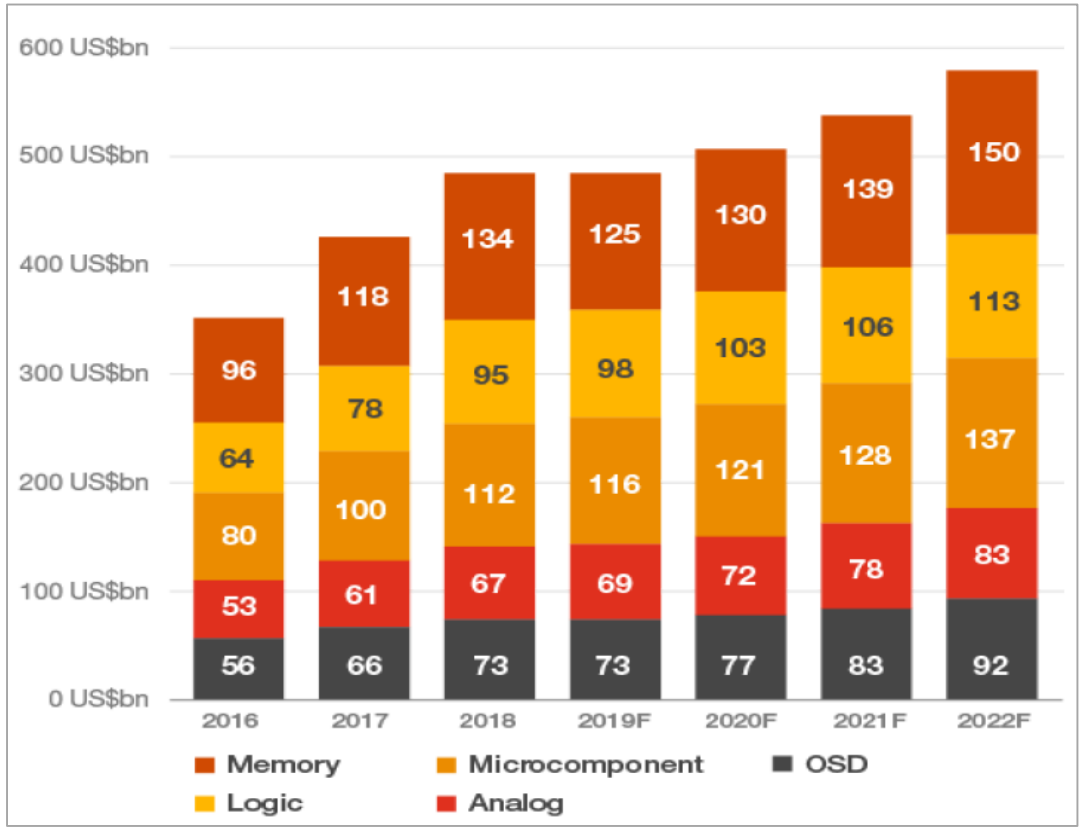
Industry Leaders
Local & Global
Partnerships

Innovation
Hard Work
Execution Excellence

Agenda

- Semiconductor & Chip Design Industry
- RISC-V and Chip Design Flow
- Open-source Tool Ecosystem Overview
- Aql Tech Solutions Processor IP Company
- RISC-V and Chip Design Opportunities

$600B Semi Industry and Top Players



Global semiconductor market, key segments (PwC Research)

Semiconductor Revenues, $Billion

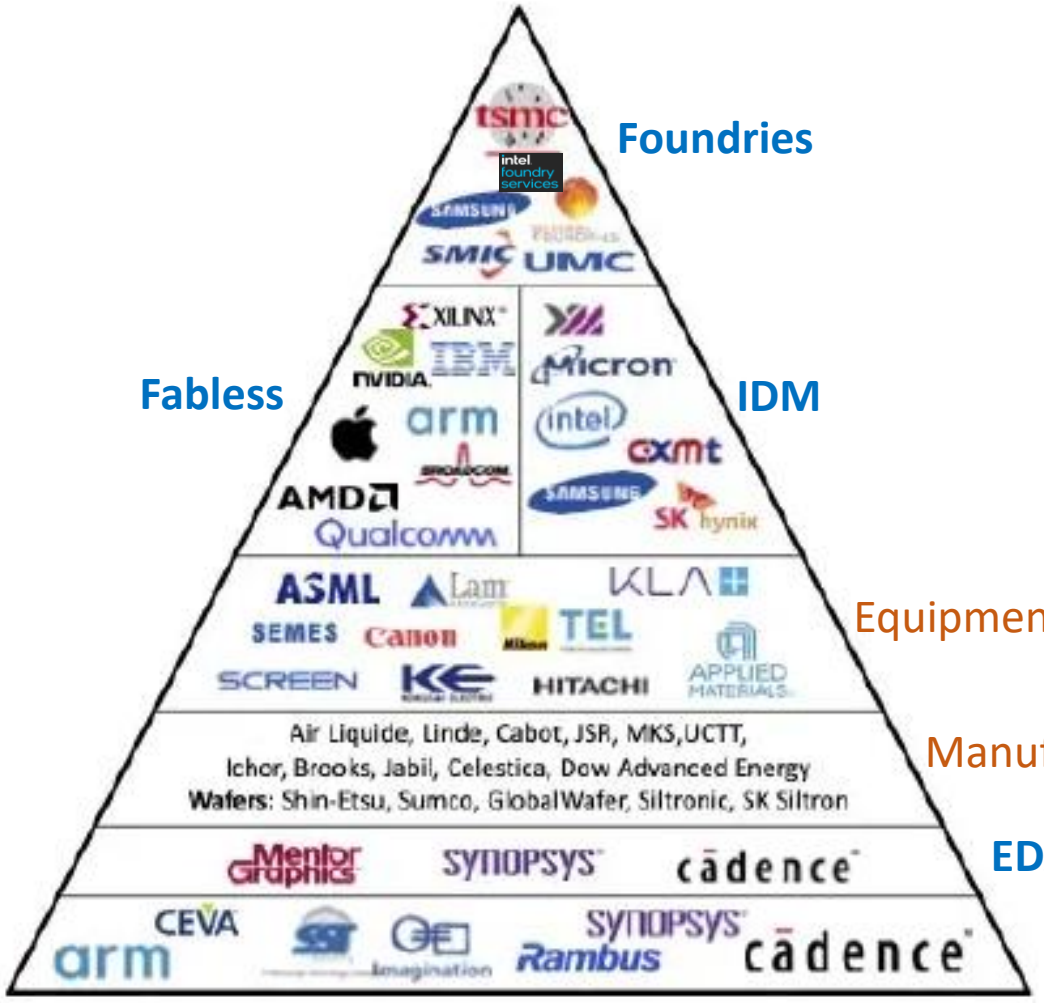
Source: Companies, Semiconductor Intelligence estimates

Rank	Company	1984	Share	Company	2023	Share
1	TI	2.4	9.3%	Nvidia	52.9	10.6%
2	Motorola	2.2	8.3%	Intel	51.6	10.3%
3	NEC	2.1	8.1%	Samsung	45.4	9.1%
4	Hitachi	1.9	7.3%	Broadcom	36.2	7.2%
5	National	1.9	7.2%	Qualcomm (IC)	29.6	5.9%
6	Toshiba	1.5	5.8%	AMD	22.2	4.4%
7	Philips	1.3	4.8%	SK Hynix	21.2	4.2%
8	Intel	1.2	4.6%	TI	18.1	3.6%
9	AMD	1.1	4.4%	Infineon	17.7	3.5%
10	Fujitsu	0.9	3.5%	STMicro	17.4	3.5%
	Top Ten Total	16	63%	Top Ten Total	312	62%
	Total Market	26	100%	Total Market	500	100%

Top semiconductor companies engaged with **RISC-V**

Industry fundamentals are the same; Innovation, Markets, Ecosystem

Semiconductor Ecosystem & Players



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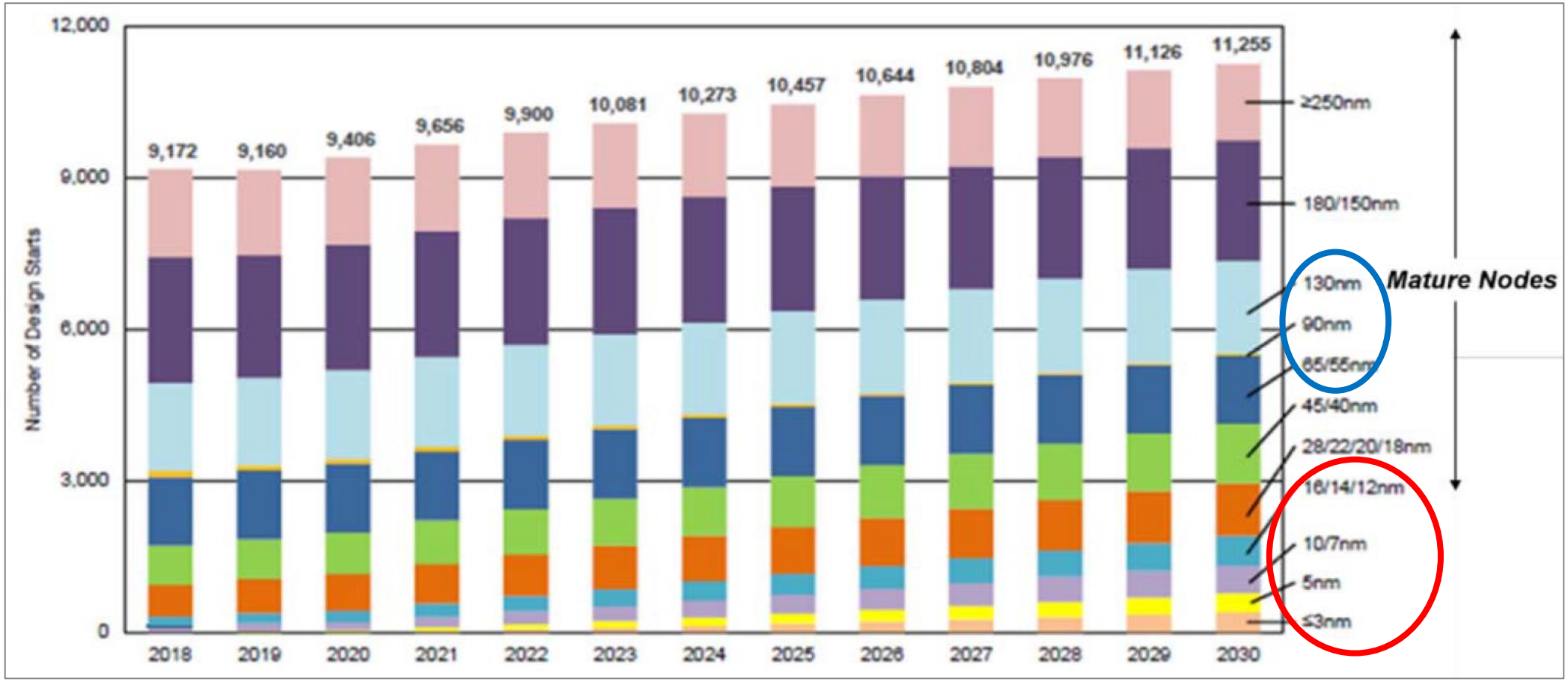
Technology Nodes and Design Trends



Driven primarily by class of target applications, PPA, TTM, Cost

SoC's and Key Design Considerations

ECONOMIC STRENGTH

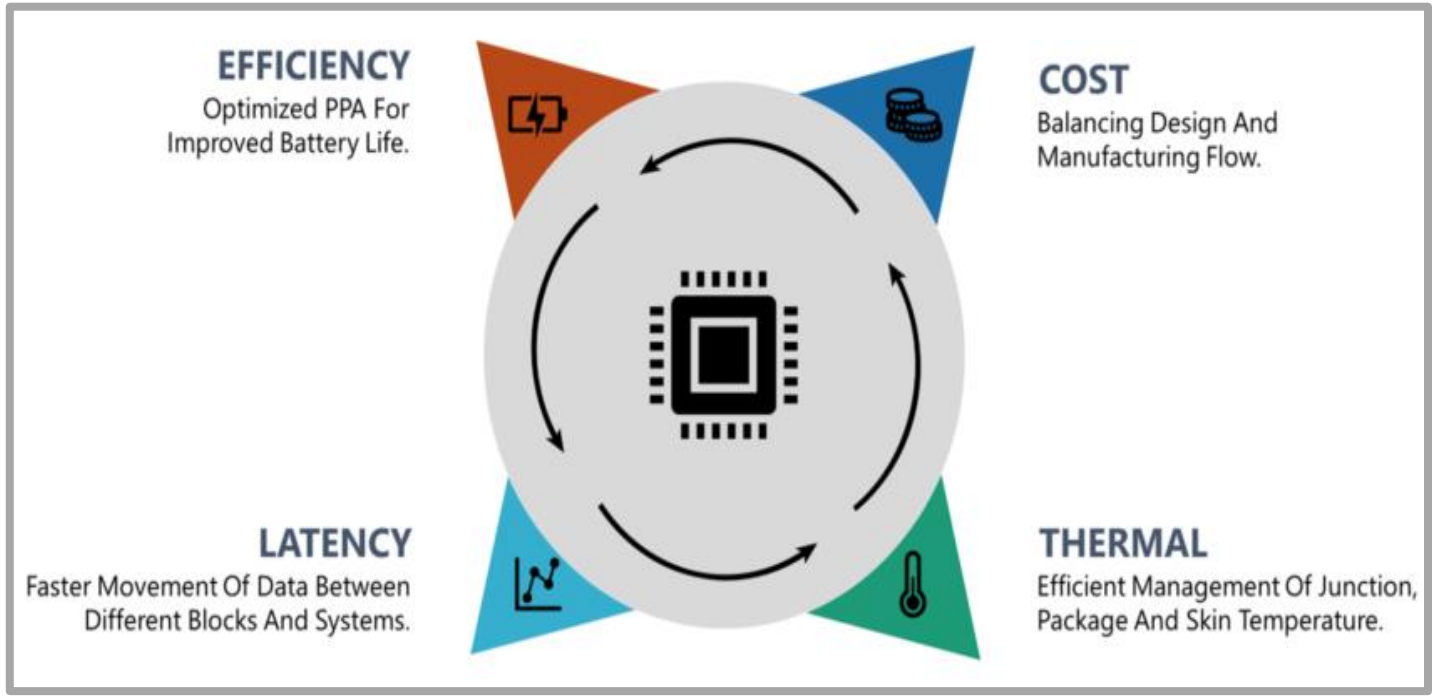
Jobs, Foreign Exchange, Investment

TECHNOLOGY LEADERSHIP

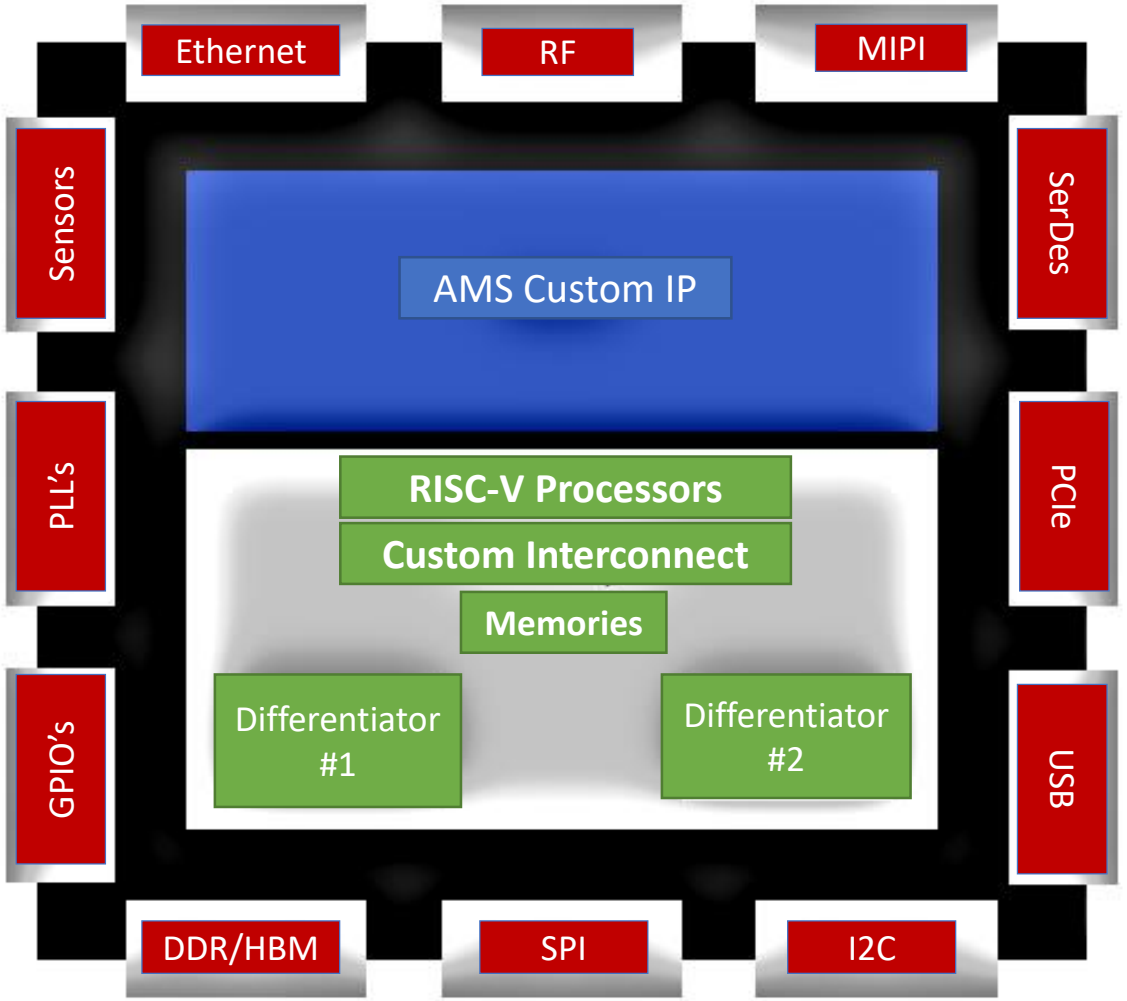
SoCs are transforming the World

NATIONAL SECURITY

Designing own SoCs is critical!



System on Chip



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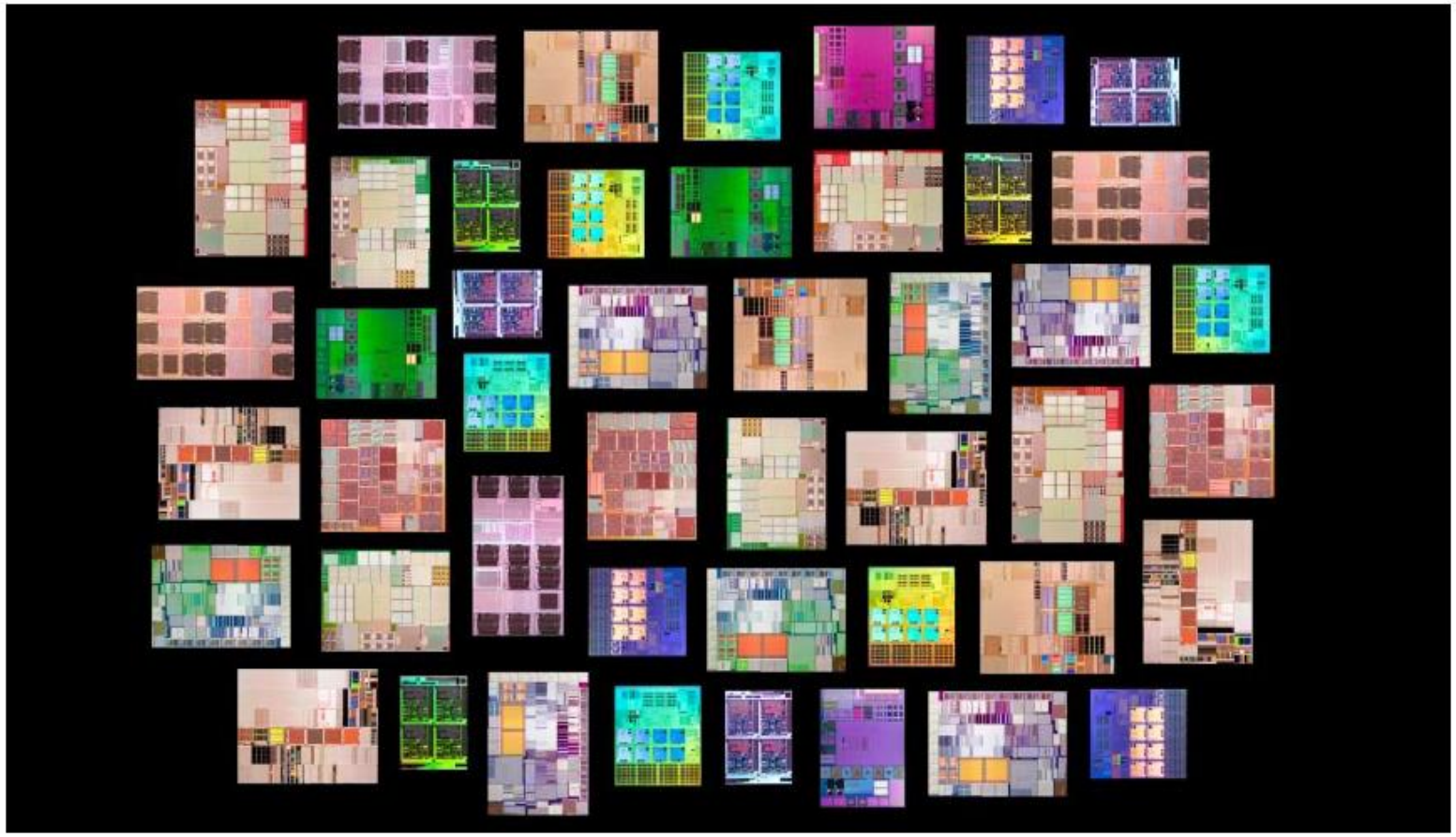
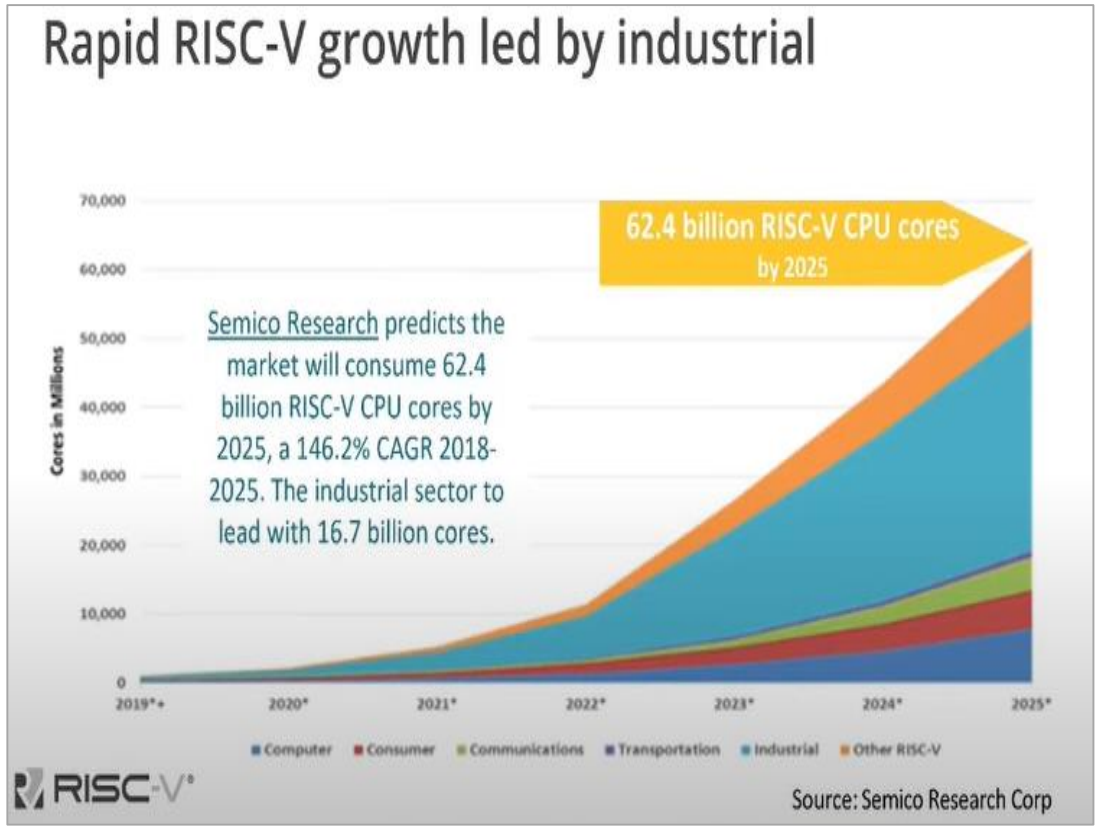
MIT Technology Review 10 Breakthrough Technologies of 2023

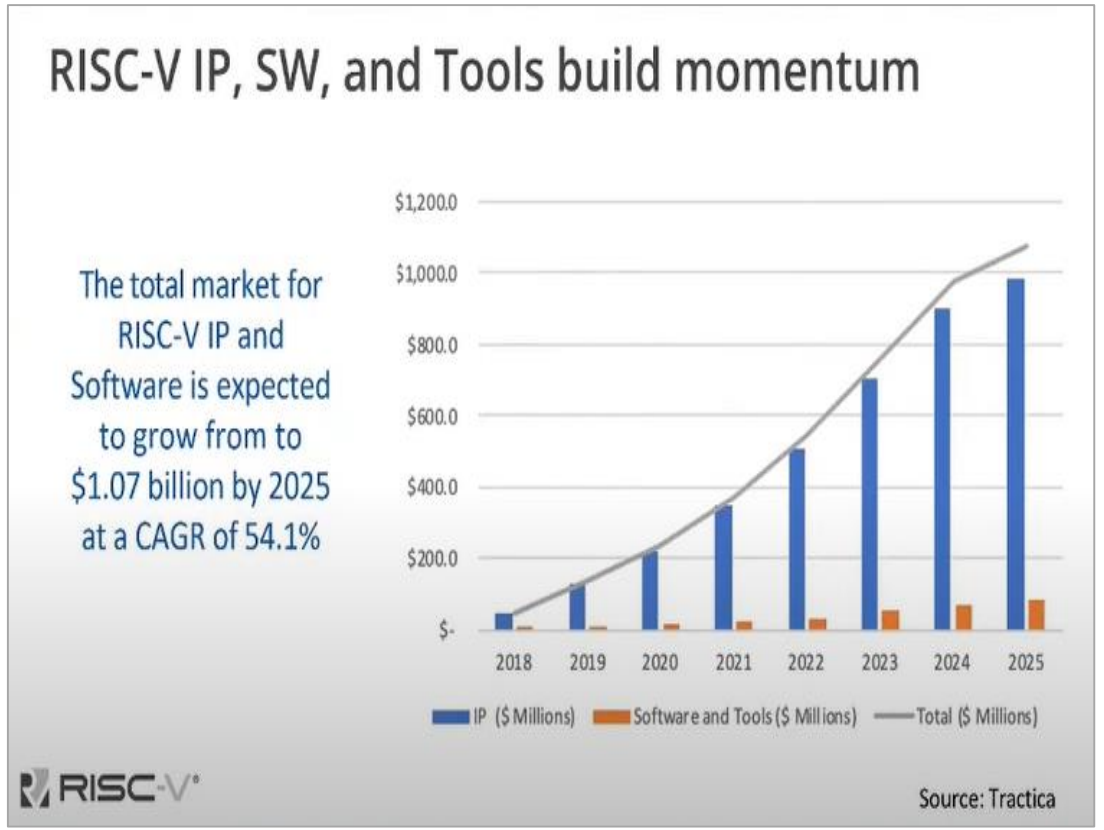
"An open standard called RISC-V is rewriting the economics of chip design and shaking up the tech sector's power dynamics."



RISC-V Market Growth



Semiconductor processor IP market roughly $4 Billion a year



Strong RISC-V IP & SW growth

$ Billions of collective RISC-V investment

RISC-V SUMMIT

- Numerous roadmaps declared across community incl SiFive, MIPS, Alibaba, Andes, etc
- $1B investment by Intel.
- Billions in government investment around the world
- >$2B in reported Venture Capital investment in start-ups
- $ Billions more in collective RISC-V community investment

intel

Intel Creates $1B Innovation Fund To Grow RISC-V Market (And Attract New Foundry Customers) ... Joins RISC-V Board

February 7, 2022

European Commission

EU announced a new European Chips Act of €15 billion This adds to €30 billion of current public investments

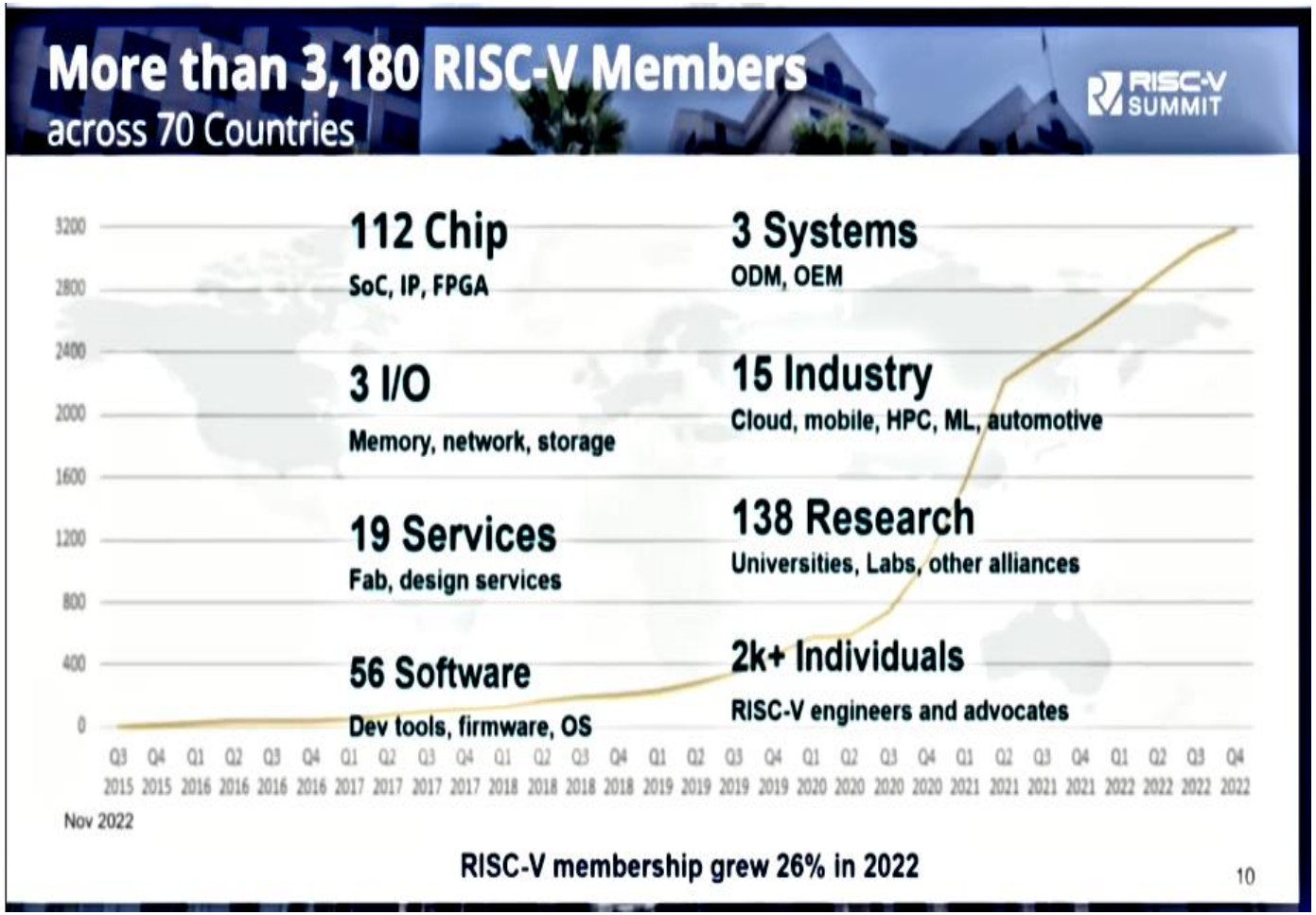
February 8 2022

MeitY

India Ministry for Electronics & Information Technology launched Digital India RISC-V (DIR-V) program for commercial SHAKTI & VEGA silicon.

April 27, 2022

Open Field for Industry & Academia



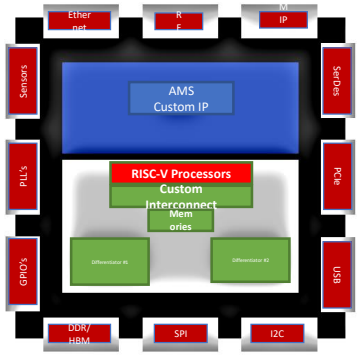
Industry

- Aql Tech Solutions, 3-4 others and more to come

Academia

- NUST, UIT (MERL), UET-Lahore, Namal, LUMS, FAST ISB, Bahria, QAU, NED and others

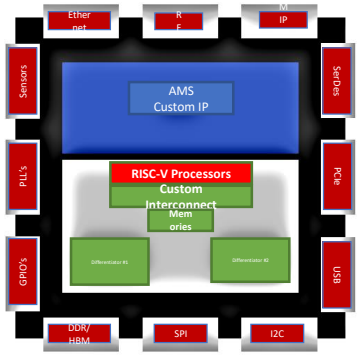
Design Challenges & Our Focus



Core, IP, Design and Verification

Frontend Implementation

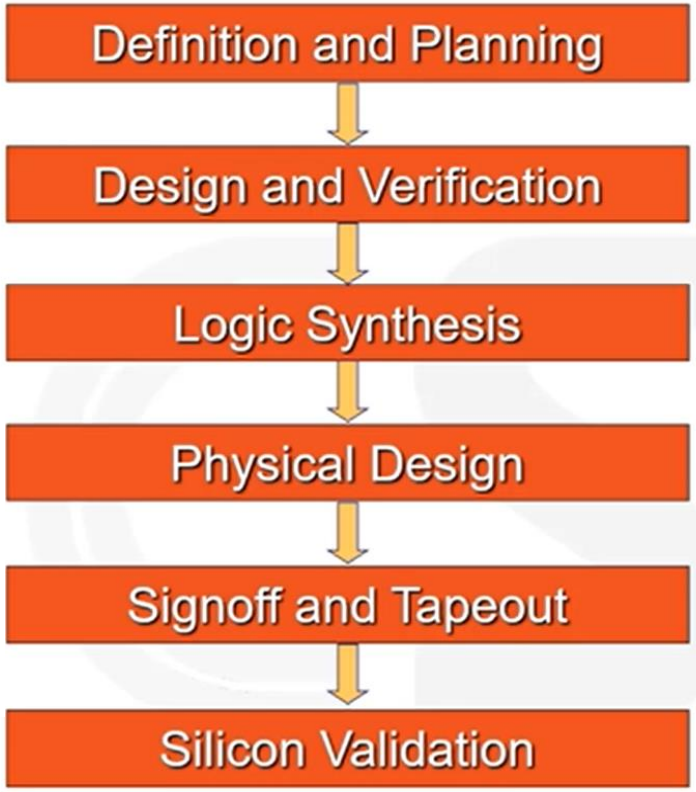
Backend Design



Building a Chip & ATS Focus

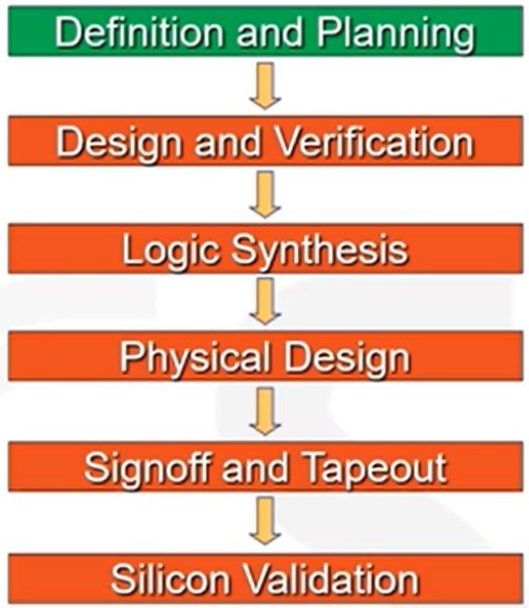
- Definition and Planning
- Design and Verification (Frontend)
- Logic Synthesis (Frontend and Backend)
- Physical Design (Backend)
- Signoff and Tapeout
- Silicon Validation

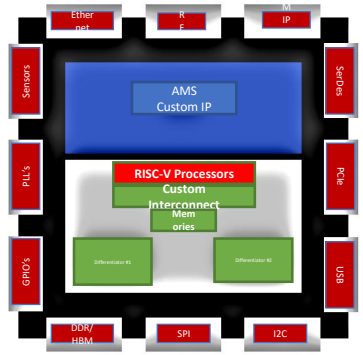
- Don't forget package & board design, software design, test plan, etc., etc., etc.

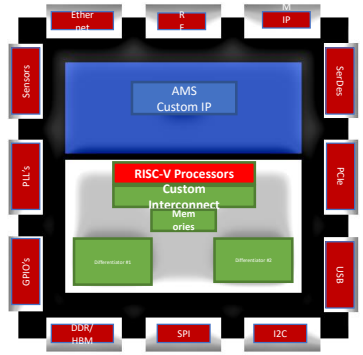


Chip Definition & Planning

- **Marketing Requirements Document (MRD)**
- **Chip Architecture**
  - Define bus structures, connectivity
  - Partition Functionality
  - High-Level System Model (Bandwidths, Power, Freq.)
  - System partitioning (HW vs SW, #Cores, Memories…)
- **Design Documents**
- **Floorplan/Board Requirements**
- **Process and fab**
- **Project kick-off – transfer to implementation**

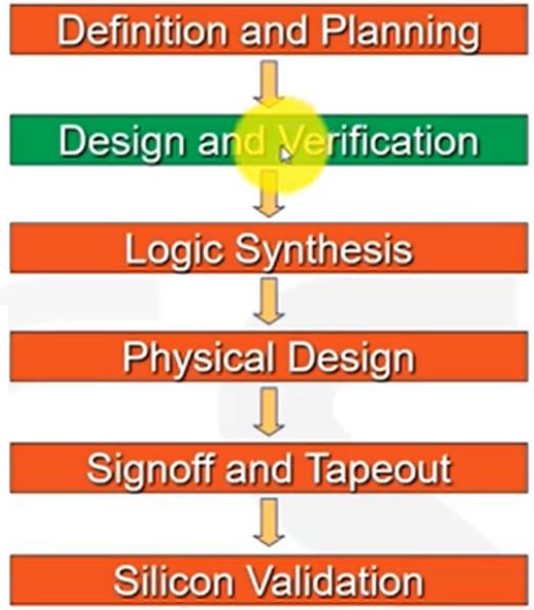


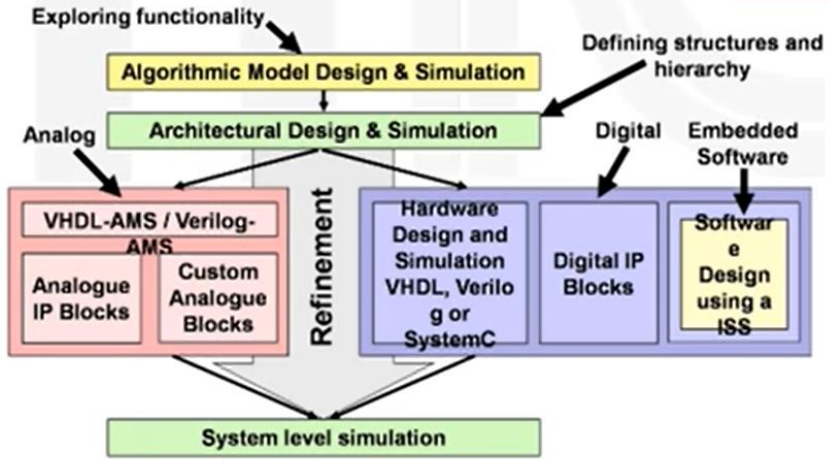




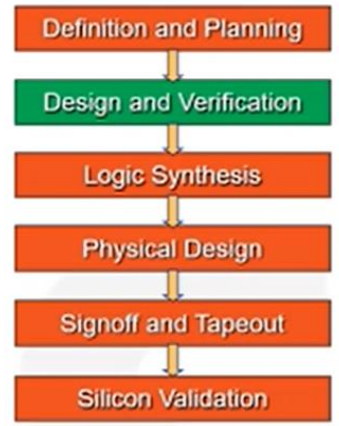
Design & Verification

- RTL (Register Transfer Level) Design
- Integration/Development of IPs
- RTL Lint/Synthesability checks
- Formal Verification
- Functional verification all the IPs:
  - Unit level
  - Sub-system level
  - Chip (SOC) level

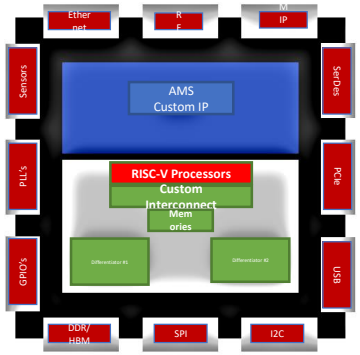


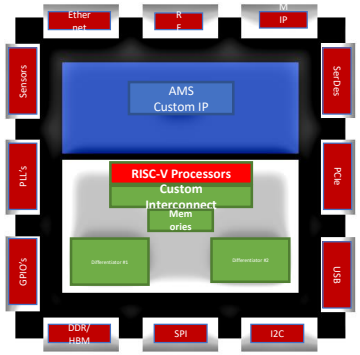


Design & Verification – IP Integration



- **Hard IP**
  - IP provided as pre-existing layouts with:
    - Timing models
    - Layout abstracts
    - Behavioral models (Verilog/VHDL)
    - Sometimes with Spice models, full-layouts
  - This is the standard delivery format for custom digital blocks
    - RAMs, ROMs, PLLs, Processors
- **Soft IP**
  - RTL Code
    - Can be encrypted
    - Instantiated just like any other RTL block
  - Sometimes with behavioral models



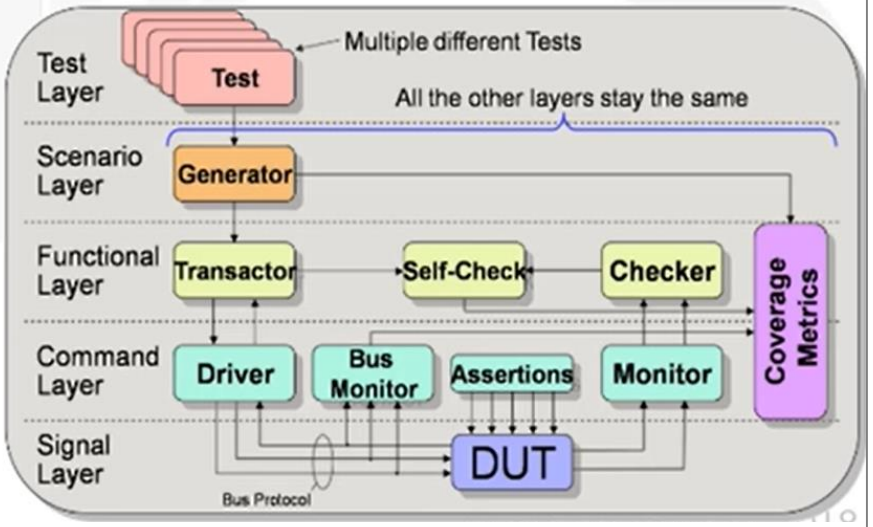


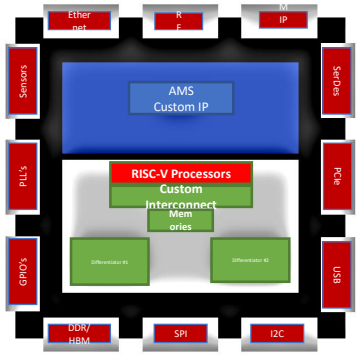
Design & Verification – Prototyping

- **Different levels of verification:**
  - Specification driven testing
  - Bug driven testing
  - Coverage driven testing
  - Regression
- **FPGA Prototyping:**
  - Synthesize to FPGA
  - Speeds up testing where possible.
- **Hardware Emulation:**
  - Big servers that can emulate the entire design.

Source: Cadence


Source: mouser.com





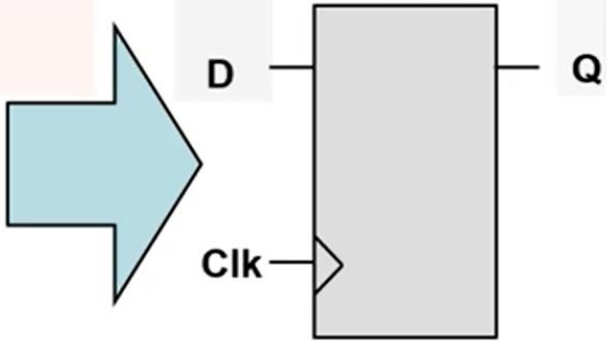
Synthesis

- **Inputs:**
  - Technology library file
  - RTL files
  - Constraint files (SDC)
  - DFT definitions
- **Output:**
  - Gate-level netlist

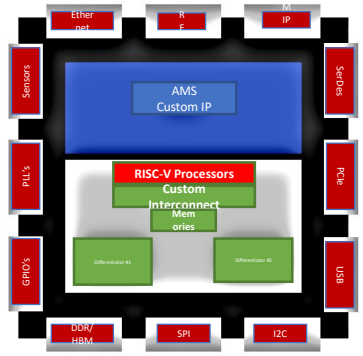
- **Synthesis**
  - Converting RTL code into a generic logic netlist
- **Mapping**
  - Mapping generic netlist into standard cells from the core library
- **Optimization**
  - To meet Timing / Area / Power constraints

Definition and Planning
↓
Design and Verification
↓
Logic Synthesis
↓
Physical Design
↓
Signoff and Tapeout
↓
Silicon Validation

```
module DFF(Clk, D, Q);
  input Clk;
  input D;
  output Q;
  always @(posedge Clk)
    Q <= D;
endmodule
```

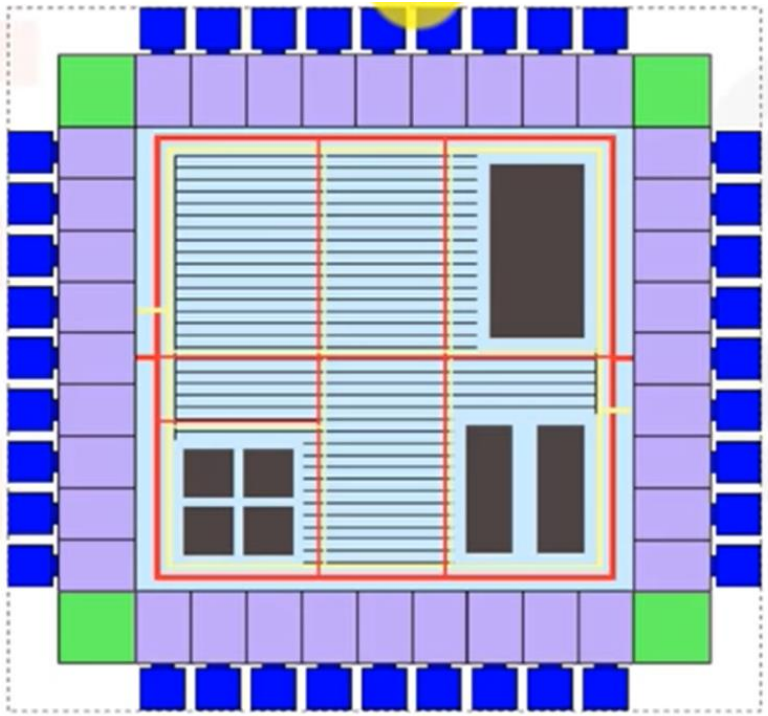


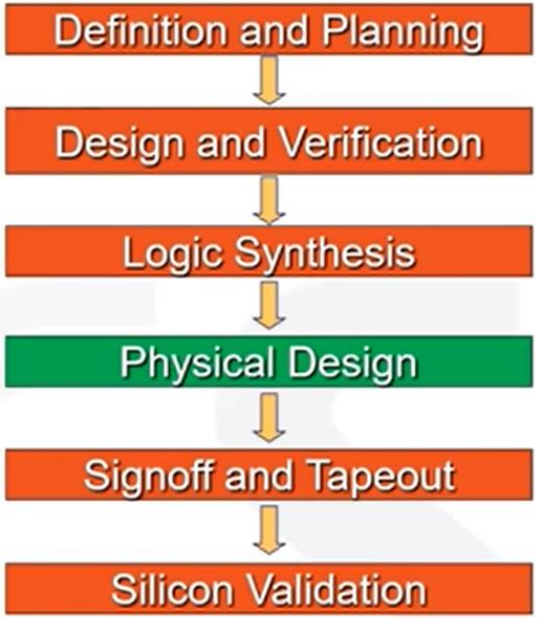
- **Post Synthesis checks**
  - Gate-level simulation
  - Formal verification (Logic Equivalence)
  - Static Timing Analysis (STA)
  - Power/Area estimation

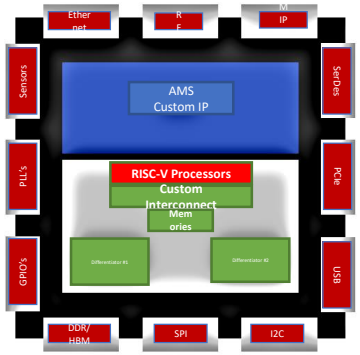


Physical Design (Backend)

- Floorplan
- I/O Ring
- Power Plan
- Placement
- Clock Tree Synthesis
- Route
- DRC, LVS, Antennas, EM
- LEC, Post-layout

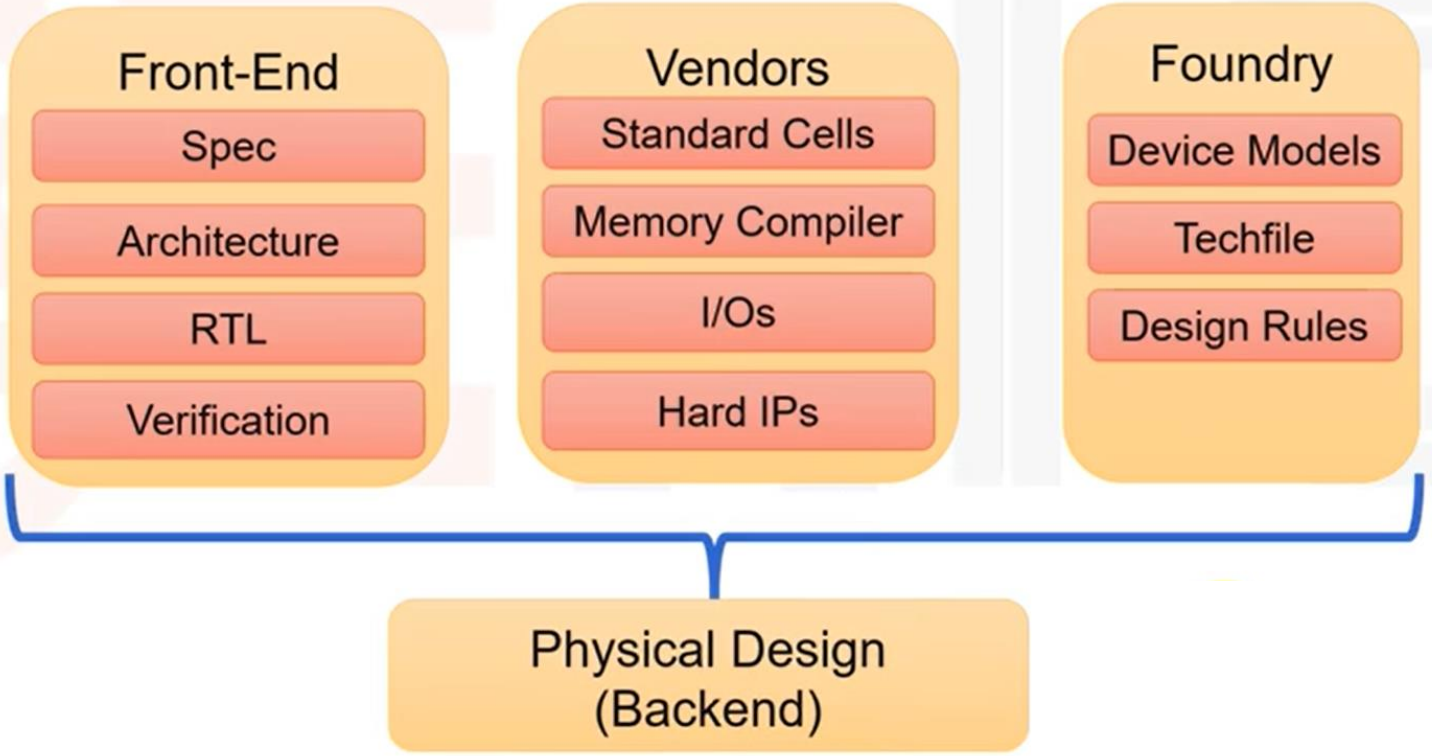


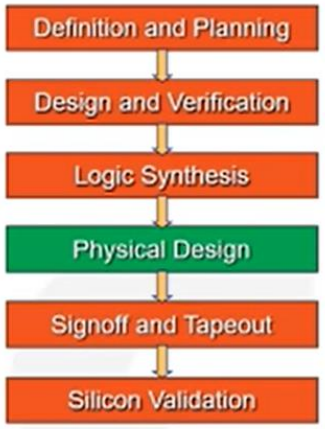


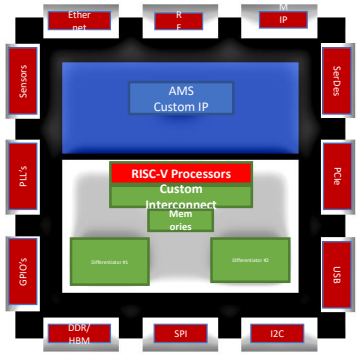


Physical Design – Backend Flow

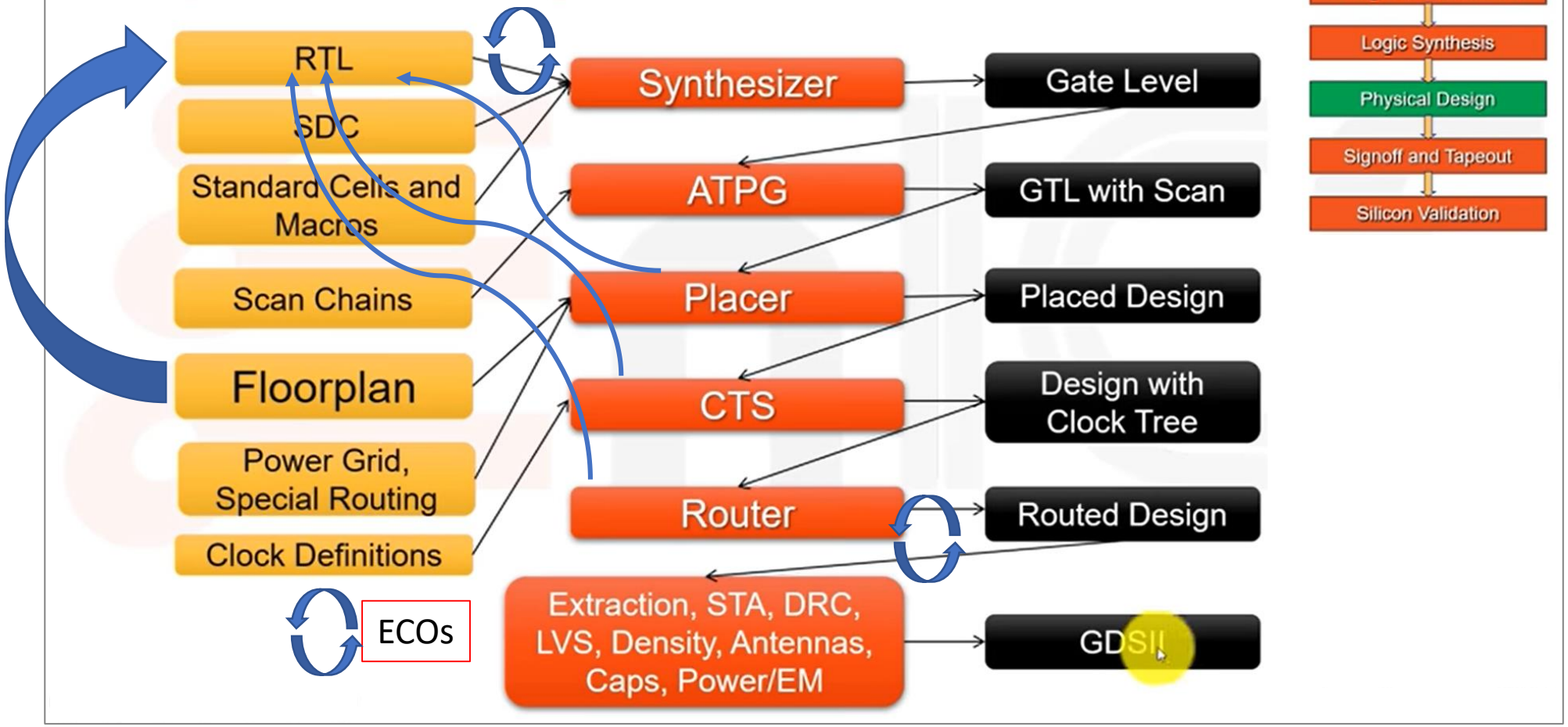
- **Physical Implementation Inputs**







Physical Design – Backend Flow



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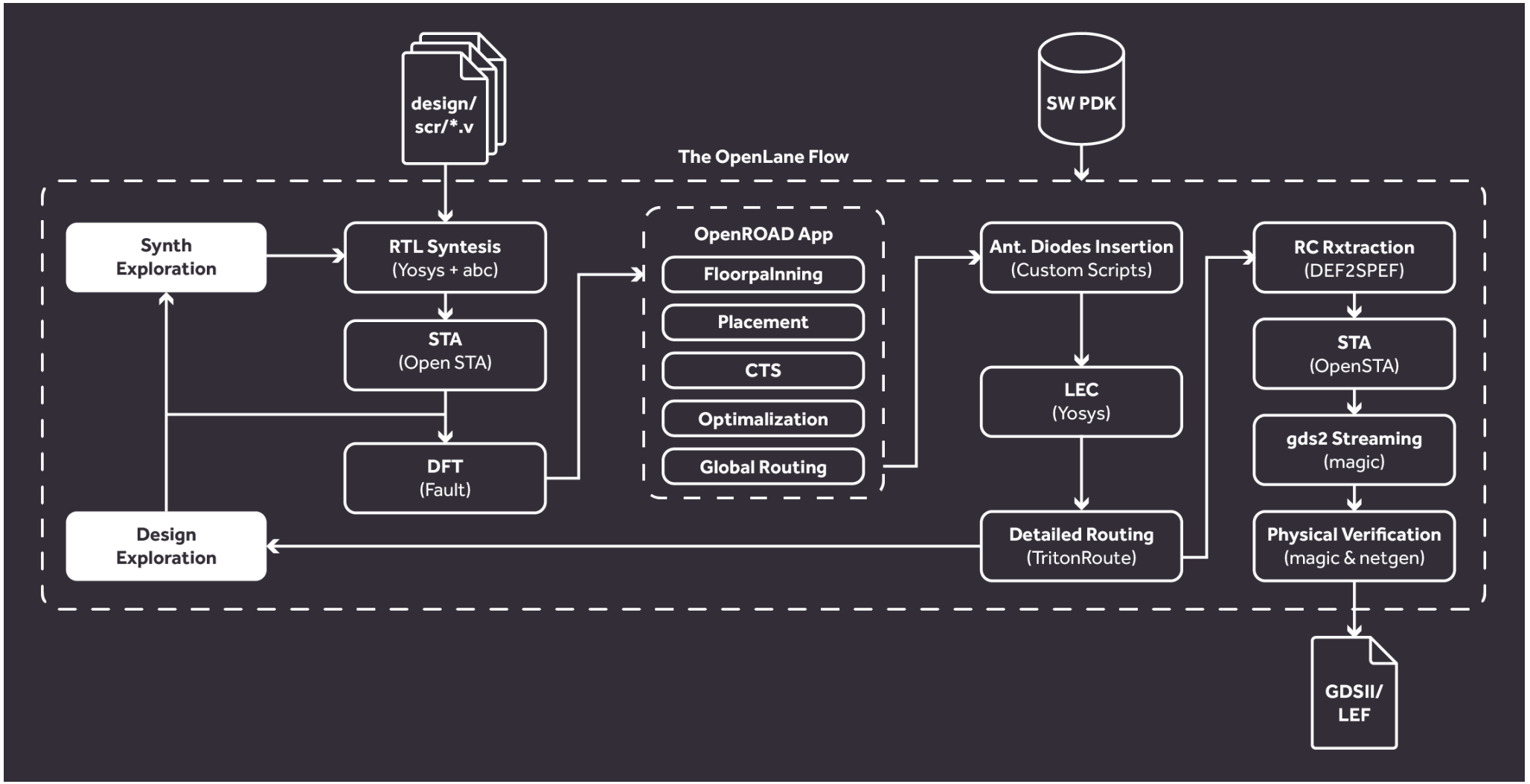
OpenLane Flow



OpenLane RTL2GDSII Flow – 1

1

Synthesis

- yosys - Performs RTL synthesis
- abc - Performs technology mapping
- OpenSTA - Performs static timing analysis on the resulting netlist to generate timing reports

(Lecture: 2 hrs, Lab: 3 hrs)
Tools: Yosys, OpenSTA

2

Floorplan and PDN

- init_fp - Defines the core area for the macro as well as the rows (used for placement) and the tracks (used for routing)
- ioplacer - Places the macro input and output ports
- pdn - Generates the power distribution network
- tapcell - Inserts welltap and decap cells in the floorplan

(Lect: 3 hrs, Lab: 5 hrs)
Tool: OpenROAD Apps

3

Placement

- RePLace - Performs global placement
- Resizer - Performs optional optimizations on the design
- OpenDP - Performs detailed placement to legalize the globally placed components

CTS

- TritonCTS - Synthesizes the clock distribution network (the clock tree)

(Lect: 2 hrs, Lab: 4 hrs)
Tools: OpenROAD Apps

OpenLane RTL2GDSII Flow – 2

4

Routing

- FastRoute - Performs global routing to generate a guide file for the detailed router
- CU-GR - Another option for performing GR.
- TritonRoute - Performs detailed routing
- SPEF-Extractor - Performs SPEF extraction

(Lecture: 3 hrs, Lab: 5 hrs)
Tools: OpenROAD Apps, Scripts, TritonRoute, DEF2SPEF

5

GDSII Generation

- Magic - Streams out the final GDSII layout file from the routed def
- Klayout - Streams out the final GDSII layout file from the routed def as a back-up

(Lect: 1 hrs, Lab: 1 hrs)
Tools: Magic, Klayout,Netgen

6

Checks

- Magic - Performs DRC Checks & Antenna Checks
- Klayout - Performs DRC Checks
- Netgen - Performs LVS Checks
- CVC - Performs Circuit Validity Checks

(Lect: 2 hrs, Lab: 3 hrs)
Tools: Magic, Klayout,Netgen, CVC

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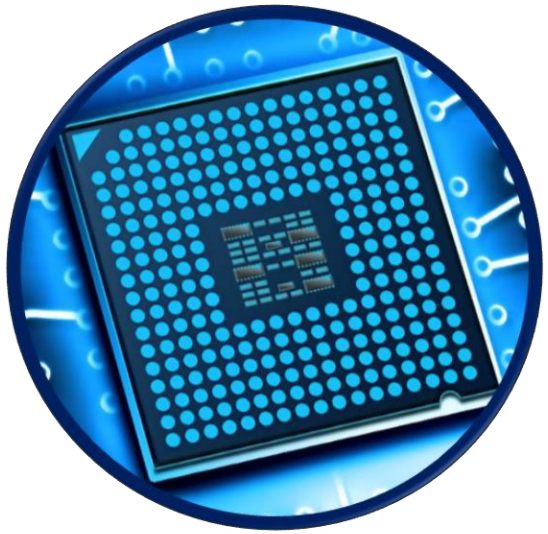
Building Bridges: IP & Chip Design

IP & SoC Markets and Applications



Cloud and data center applications top cloud providers like Amazon and Alibaba are designing their own chips.

Mobile and wireless continue rapid evolution with each generation of hardware and increased capability.

Automotive is transforming from autonomous vehicles to infotainment to safety, the whole vehicle relies on innovative electronics.

Consumer and IoT devices bring incredible innovation and volume with billions of connected devices being in the next 5-10 years.

Industrial IoT incorporating artificial intelligence in manufacturing and industrial processes.

Memory was the largest semiconductor category by sales with $158 billion in 2018, and the fastest-growing, with sales increasing

Agenda

- Semiconductor Industry Trends
- RISC-V and Opportunities in Pakistan
- Aql Tech Solutions
- Industry & Academia Collaboration
- Future Is Challenging Yet Promising

Strategic Collaboration A Must For The Ecosystem

Academia

- Technology innovation driven by passion and motivational factors
- RISC-V induction, C coding, RTL design using Verilog, industry related projects (FYP's)
- Elective course selection for 2nd 3rd year and MS programs
- BS & MS academic review
- EDA tools open-source and commercial
- Hands-on rigorous training programs, open source and commercial tools

Industry, Academia & Stakeholders

- Leaderships commitment and drive to focus on phased/time-based planning, funding, execution and delivery
- Ease of doing business, VC funding and value creation
- Building bridges, enough successful models to leverage and deploy
- Ecosystem is critical for scalability

Global Opportunities For Pakistan

USA, Canada & Europe	RISC-V, open source platforms WW	China, South Korea, Japan Asia-Pacific

Startups in Pakistan, growing the talent pool to take advantage of the strategic window of opportunity

Aql Tech Solutions Hiring Focus

Openings Now

- ASIC Design Engineer
- Design Verification Engineer
- Physical Design Engineer
- Software Engineer (LINUX, drivers)
- Power Methodology
- And more

Experienced

- 2-3 year industry experience
- 5-7 year industry experience
- 10+ year industry experience