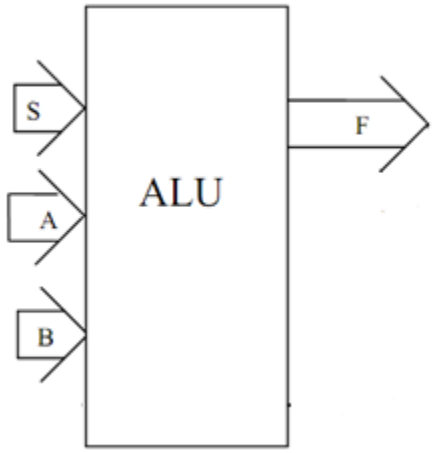
ALU Design Project

The following is the block diagram of an **8-bit ALU**. You will have to design it in order to meet the specifications given in the following functional tables. For more information regarding the table of function please refer to **M. Morris Mano, "Digital Logic and Computer Design".**



Op No.	F	Description
1	A	Transfer A
2	A+1	Increment A
3	A+B	Add A to B
4	A-B	Subtract B from A
5	A-1	Decrement A
6	A'	1's Complement of A
7	A'+1	2's Complement of A
8	A OR B	Bitwise OR
9	A XOR B	Bitwise XOR
10	A AND B	Bitwise AND
11	SHR A	Shift A to Right by 1 bit
12	SHL A	Shift A to Left by 1 bit
13	ROT A	Rotate A by 1 bit
14	Binary→BCD	Convert Binary code to BCD
15	Binary→Gray	Convert lower 4 bits of Binary code to 4 bit gray code
16	Binary→7 segment decoder code	Convert upper 4 bits of Binary code to 8 bit code for 7-segment display with decimal point

Select Input, S ($S_2S_1S_0$)	G-1 Op.	G-2 Op.	G-3 Op.	G-4 Op.	G-5 Op.	G-6 Op.	G-7 Op.	G-8 Op.
000	1	2	2	1	1	2	2	1
001	3	4	3	4	4	3	4	3
010	5	6	5	7	7	5	5	6
011	7	8	6	9	9	6	8	7
100	9	10	9	10	9	10	9	10
101	11	12	12	12	12	12	12	11
110	13	14	15	13	14	13	13	14
111	15	16	16	14	15	16	15	16

Student IDs with assigned group numbers:

Student ID	**Group No. (G)**
130205118	1
130205120	2
130205121	3
130205124	4
130205126	5
130205127	6
130205130	7
130205131	8
130205132	8
130205133	7
130205135	6
130205138	5
120205043	4

Instructions for Dsch2:

You must design all the logic blocks in your design (from inverter, AND/OR gates to 4 bit Full Adder etc.) using CMOS logic design (using MOSFETs) and the name of your designed blocks must have the names as follows:

For a 2to1 MUX, **the name should be in the form of MUX2_097 (here, replace 097 with the last three digits of your student ID.)**. Similarly, name all the blocks using the same nomenclature.

The **inputs A and B** should be provided from **Hexa Keypads**.

The **inputs S ($S_2S_1S_0$)** must be provided from **Buttons**.

The **output F** must be displayed using **Hexa displays**.

Instructions for Quartus:

You have to submit a **Verilog code for an 8 bit ALU** (the same ALU that you designed in Dsch2) and its simulation using Quartus.

The **inputs A and B** should be provided in **Hexadecimal numbers**.

The **inputs S ($S_2S_1S_0$)** must be provided using **Clock** signal.

The **output F** must be displayed as **Hexadecimal numbers**.

Warnings and Submission Deadline

Any **copied project will get a 0**. **No excuses for a delayed submission** will be accepted.

Submit your project within 10/01/17 with report after fixing your appointment with the assigned course teacher. You have to show several operations performed by your design.