# SYSC2310 A and B Introduction to Digital Systems
# Fall 2022

## Lab 1 Report

## Introduction to Logisim and Basic Logic Gates

**Student Name: Uchenna Obikwelu**

**Student ID: 101241887**

**TA Name:**

**NIVETHASIVASARAVANAN@cmail.carleton.ca**

**Lab Section: __SYSC 2310 L20__**

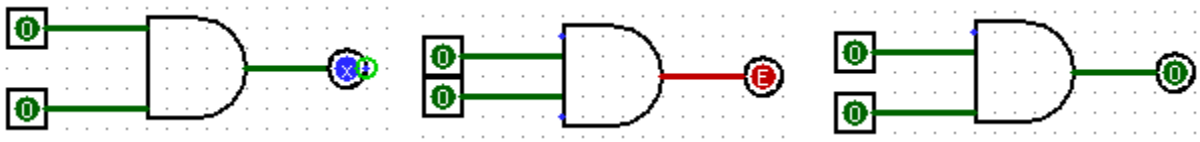
**Lab Date: 16th September 2022**

**Date Completed: 12th September 2022**

## Exercise 1: Build Basic AND Gates

## Exercise: Identify Common Mistakes

As an exercise, try to identify the mistake in each of the following circuits.



What does the ( ) symbol represent? The value at that point is unknown and the wire is not connected properly.

What does the ( ) symbol represent? Incorrect wiring of both input pins, hence, there is an **error,** and no output can be yielded.

What is the problem with the third circuit? The top input pin is not properly connected to the actual gate input hence the circuit would not yield the expected results and not simulate properly.

Why do you think these circuits are not working properly? How would you fix them?

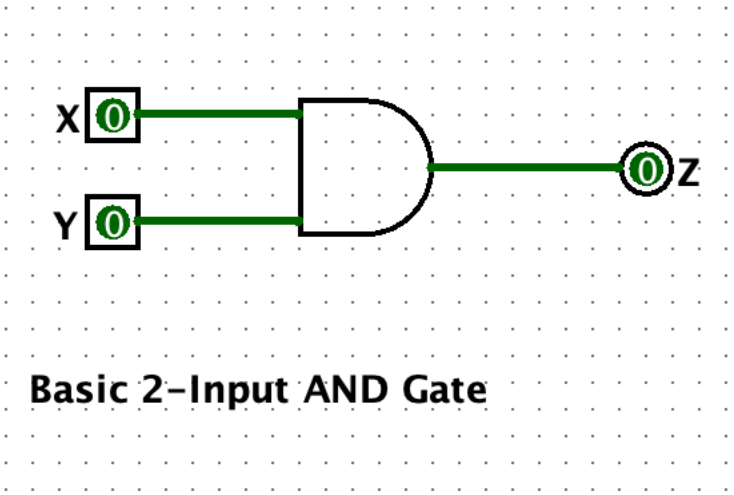
These circuits are not working properly because the common mistakes were not accounted for.

-The first circuit could be fixed by, making sure the wire from the AND gate is connected properly to the output pin and touches it. This could also be fixed by connecting wires where a green circle is. The output pin should be changed to facing west instead of east.

-The second circuit could be fixed by hovering over the input side of the gate and watch for the green circle. This tells us the actual point of input to the gate. Then, move the two input pins and connect them properly.

-The third circuit could be corrected similarly to the second. The only difference is that you move only the top input pin and put it in its correct input point.

## Screen Shot of Exercise 1 Circuit



## Copy and Paste Exercise 1 Simulation Logging File

| X | Y | Z |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |
| 1 | 0 | 0 |
| 0 | 0 | 0 |

## Exercise 2: Build Basic Logic Gates

## Complete the Truth Tables as Per Exercise 2, Point 6

| AND | | |
|---|---|---|
| X | Y | Z |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

| OR | | |
|---|---|---|
| X | Y | Z |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

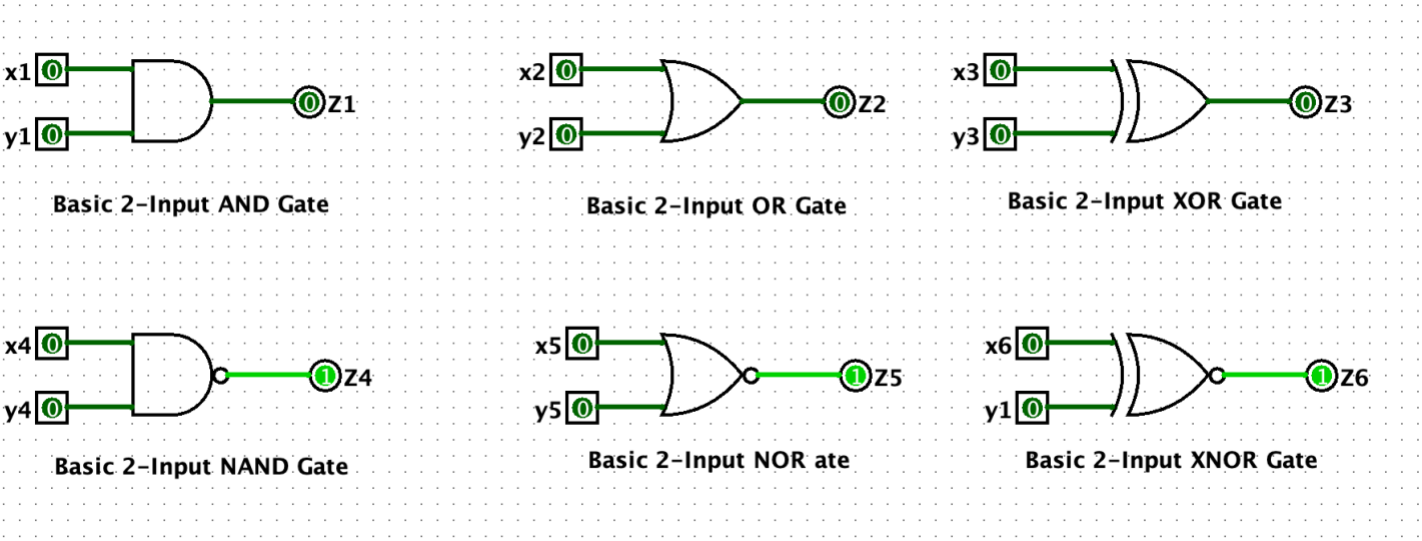
| XOR | | |
|---|---|---|
| X | Y | Z |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

| NAND | | |
|---|---|---|
| X | Y | Z |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

| NOR | | |
|---|---|---|
| X | Y | Z |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

| XNOR | | |
|---|---|---|
| X | Y | Z |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

## Screen Shot of Exercise 2 Circuit

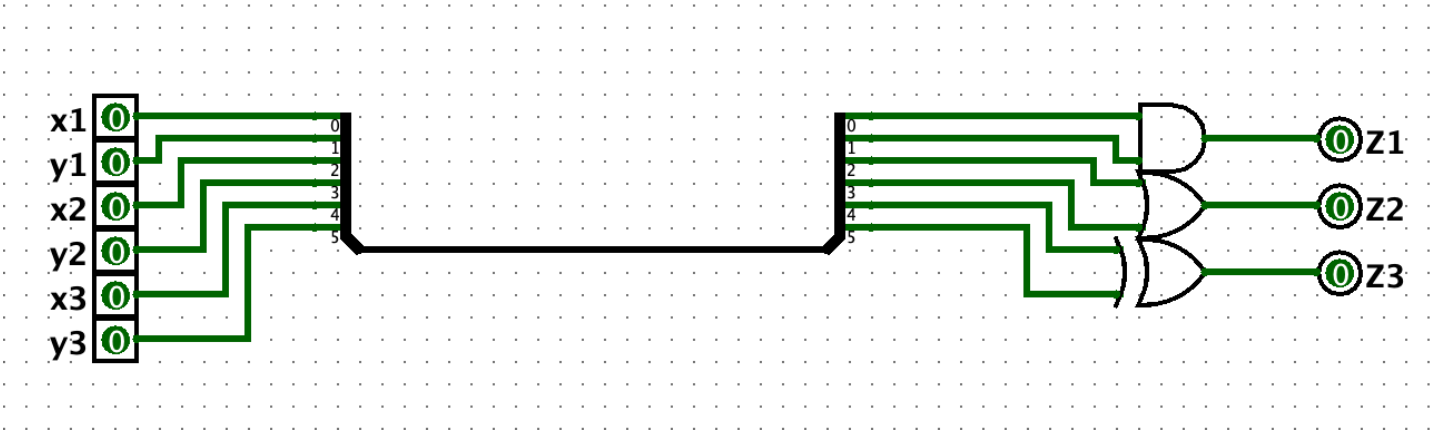


# Copy and Paste Exercise 2 Simulation Logging File

| x1 | y1 | Z1 | x2 | y2 | Z2 | x3 | y3 | Z3 | x4 | y4 | Z4 | x5 | y5 | Z5 | x6 | y6 | Z6 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |

## Exercise 3: Use of Buses and Splitters

## Screen Shot of Exercise 3 Circuit



## Copy and Paste Exercise 3 Simulation Logging File

| x1 | y1 | x2 | y2 | x3 | y3 | Z1 | Z2 | Z3 |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |

# INTRODUCTION TO DIGITAL SYSTEMS

SYSC2310 (Fall 2022)

## Lab 1: Introduction to Logisim and Basic Logic Gates

## Objectives

- Get familiar with the basic features of Logisim.
- Introduce, design, and test basic logic gates.

## Relation to course outcomes

The work in this lab is related to the two following course outcomes:

- Understand the basic building blocks of digital systems.
- Apply analysis skills to correctly describe the behavior of given combinational logic circuits.

## Preparation

- Read the Logisim Guide posted on Brightspace attentively prior to the lab.
- Take the time to read this document carefully to understand the essence of the work to be performed.

*[Using a Lab Computer]*

1. From the Windows login screen use the credentials 'students'. This will put you into the account creation script for which you provide your Carleton credentials to create the account. Once completed you log out and then log into your account directly from the Windows login screen. Keep in mind that the account on the systems network is independent of all other campus accounts.
2. Find Logisim by searching for "Logisim" in the Windows start menu.
3. If not found in Step 2, locate the 'Logisim.exe' file in the folder C:\sysc2310\logisim-win-2.7.1.exe, or download it from the lab website on Brightspace.
4. Create a new folder in your M drive with the title 'sysc2310lab'.

*[Using Your Computer]*

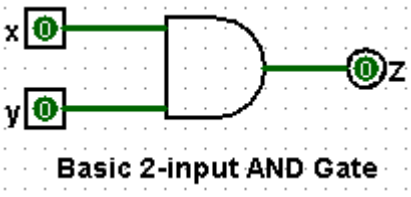
1. Download Logisim for your operating system from the "Labs" Brightspace Module.
2. Create a new folder with the title 'sysc2310lab'.

*[Everyone]*

1. Inside the 'sysc2310lab' folder, create six folders: 'lab1', 'lab2', 'lab3', 'lab4', 'lab5' and 'lab6'.
2. Inside the 'lab1' folder, create three folders 'Ex1', 'Ex2' and 'Ex3'.
3. Download 'Lab 1 Report Template.docx' from the "Labs" Module, rename the file to 'Lab 1 Report `Jane Doe`.docx' where `Jane Doe` is your name, and save to your 'lab1' folder.
4. Open your lab report document and complete the first page. Read through the rest of the document so that you are aware of what needs to be recorded.

By following these steps, you will be organized, and will start every experiment in its own folder. If any exercise depends on a previous one, copy the required file(s) from the first folder to the new one, and modify only the new copy. By the end of the term, you are required to have the files for all the exercises in every lab. TAs and lab technicians will not be able to help recover any deleted or overwritten files.

## Exercise 1: Build Basic AND Gates




1- Bring an AND gate from the library of gates in the Explorer pane to the Canvas (the drawing area). Change the 'Number of Inputs' of each gate to 2.

**Common Mistake:** Make sure you changed the 'Number of Inputs' of each gate to 2. You can also do this by selecting the gate and pressing on the number 2 on your keyboard.

2- Bring 2 input square pins ( )from the toolbar (or press Ctrl-4) and one output circle pin ( ) from the toolbar (or press Ctrl-5). You can also use the pin from the wiring library in the Explorer pane, however make sure to change the following attributes: the input pin has 'no' in 'Three-state?', and the output pin has 'Yes' for 'Output?', and Facing 'West'.

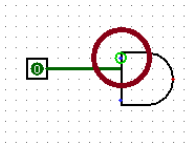
**Common Mistake:** If you are using "pin" from the "wiring library" make sure to change the attributes.

**Common Mistake:** Make sure the input pin is facing East and the output pin is facing West, otherwise you won't find the input of these elements as you expect. You can change which way the pin faces by selecting an element and pressing the arrow keys on your keyboard.

3- Label the input and output pins. Select the top input pin, type 'X' in the 'label' attribute and change the font to Bold and size 14. Repeat the same steps for the other input pin, labeled as "Y" and the output as "Z". Make sure that the 'Label Location' for the input pins is 'West' and for the output pins is 'East'.

4- Connect the 2 input pins to the inputs of the AND gates and connect the output pins to their outputs as shown in the figure above.

**Common Mistake:** Make sure you know where the inputs of the gate are. Hover over the input side of the gate and watch for the green circle. You may be connecting the input pin to somewhere near the gate inputs, not the actual inputs as shown in the figure below, and your circuit won't simulate properly. Do the same check in the output.

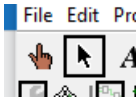


5- Add a text title to the circuit. Select the ( ) from the toolbar (or press Ctrl-3). Enter the title below the circuit as 'Basic 2-Input AND Gate'. Change the text font to Bold, size 14.

6- Now, we can simulate the circuit and log the results in a file. In order to enable logging, from the menu, click on 'Simulate', then 'Logging'. In the Selection tab, add the inputs 'X' and 'Y', and the output 'Z'. Each added signal will have a '-2' following it, to represent it as Binary data. In the File tab (the one to the right of "Selection"), click Select, navigate to the folder \sysc2310lab\lab1\Ex1, then write 'Lab1_Ex1_log.txt' in the selection and then click on "Table". (If you close the window, reopen it by following the first two steps above.)

7- Use the poke tool (  ) to change the values of the input bits. Notice the output pin.

**Common Mistake:** In Logisim, there are two modes, editing and simulation. In editing mode, you should have the cursor selected. Simulation is running in this mode, but the inputs are restricted to zeros. In the simulation mode, you should have the poke tool selected. In this mode, you can change the input values, but you can no longer edit the circuit. Before updating the circuit, you have to return to the editing mode by selecting the cursor.

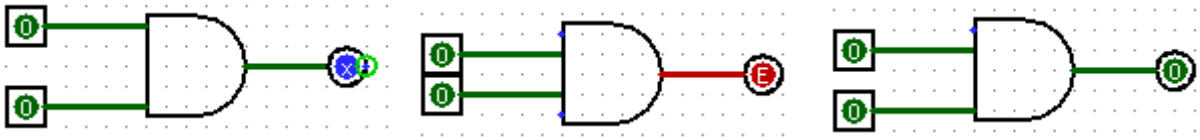



8- Open the output file 'Lab1_Ex1_log.txt' with any text editor, e.g., Notepad. Check the output of simulation.

9- Save the circuit as 'Lab1_Ex1.circ' and have the circuit file as well as the simulation file ready for your TA.

## Exercise: Identify Common Mistakes

As an exercise, try to identify the mistake in each of the following circuits.



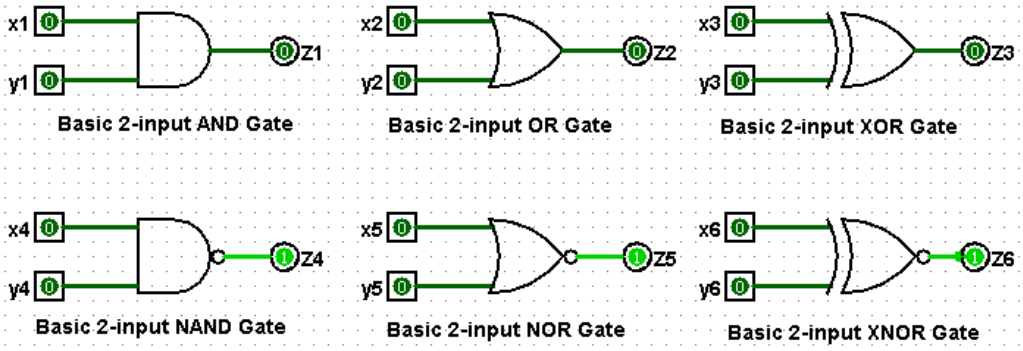
What does the (  ) symbol represent?

What does the (  ) symbol represent?

What is the problem with the third circuit?

Why do you think these circuits are not working properly? How would you fix them?

## Exercise 2: Build Basic Logic Gates




In this experiment, you will be testing all the common 2-input logic gates [AND, OR, XOR, NAND, NOR, and XNOR]

1- Copy the circuit 'Ex1.circ' from 'Ex1' folder to the 'Ex2' folder. Rename the file to 'Ex2.circ'. From Logisim, File, Open, 'Ex2.circ'

2- Add the other gates to the circuit as shown in the figure. Change the number of inputs of each gate to '2'

3- Select the input pins, the output pin, the connection wires, and the title of the AND gate circuit by clicking on the elements while holding the 'Shift' key (the Ctrl key doesn't work here). Copy and paste the elements. Move it around so that the elements are connected to the new gates in the circuit. Repeat this step until all the gates are connected properly.

4- Update the labels of the input and output pins to unique labels so that you can identify them from within the simulation file. Also, update the title of each circuit for a neat look.

5- Enable logging to a file name 'Lab1_Ex2_log.txt'

6- Simulate the circuit by using the poke tool, to test all the possible inputs and fill up the following tables.

| AND | | |
|---|---|---|
| X | Y | Z |
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

| OR | | |
|---|---|---|
| X | Y | Z |
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

| XOR | | |
|---|---|---|
| X | Y | Z |
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

| NAND | | |
|---|---|---|
| X | Y | Z |
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

| NOR | | |
|---|---|---|
| X | Y | Z |
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

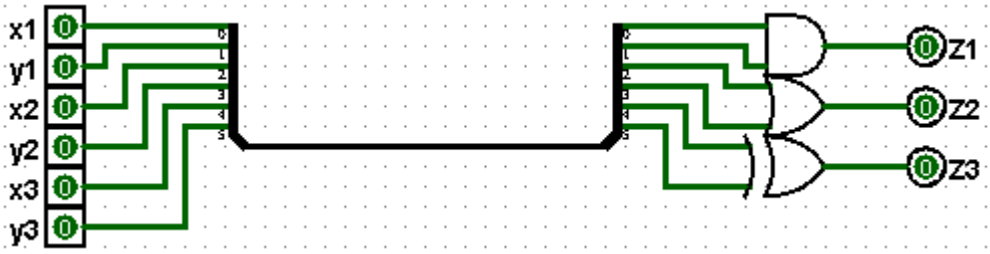
| XNOR | | |
|---|---|---|
| X | Y | Z |
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

7- Save the circuit as 'Ex2.circ'.

## Exercise 3: Use of Buses and Splitters

1- Once again, copy the ‘Ex2.circ’ from the ‘Ex2’ folder to the ‘Ex3’ folder. Rename it to ‘Ex3.circ’.

Modify the circuit to be as follows:




2- Bring two ‘Splitters’ from the wiring library. Please note that the splitter can work both as a splitter (splits a data bus into individual bit wires) or a combiner (combines multiple bit wires into a single data bus). The splitter has two important attributes: Fan Out and Bit Width In. As a “Splitter”, used in the right-side of the figure, the ‘Fan Out’ is the number of output bit wires (here, we use 6 wires connecting to the gates) while the ‘Bit Width In’ is the size of the input data bus (here, it is 6 bits).

3- Change the attributes of the Splitter on the left as follows: Facing: West and Appearance: Right-handed. Change attributes of the splitter on the right to; Facing: East and Appearance: Left-handed.

4- Also, change the attributes of all the gates to Gate Size: Narrow.

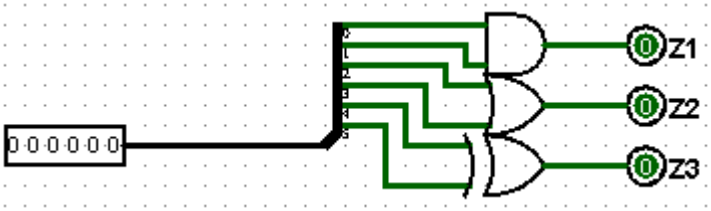
5- Enable logging to a file name ‘Lab1_Ex3_log.txt’

6- Simulate the circuit by using the poke tool, to test at least half the possible inputs.

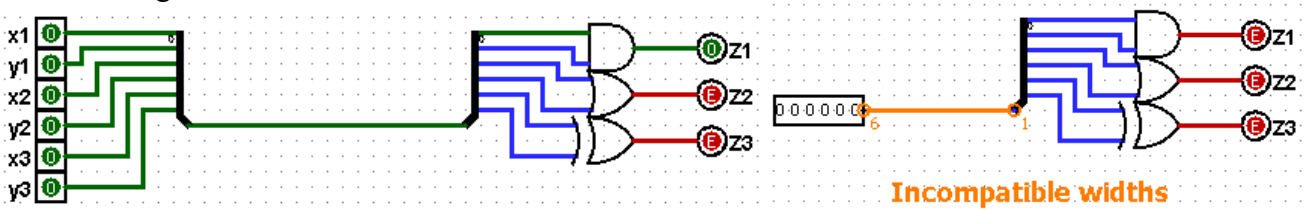
7- Save the circuit as ‘Ex3.circ’.

**Note:** The use of splitters and busses can significantly improve your schematic design.

**Note:** You can use a single input pin while changing the ‘Data Bits” attribute to ‘6’. The schematic would look like the following:



**Common Mistake**: If you forgot to change the 'Bit Width In' attribute to '6', the circuits will look like the following:




In the left circuit, the horizontal line is Green to indicate that this is just a wire, not a bus. Now, only the very first inputs to the splitter are connected, while the rest are not connected. In the right circuit, Logisim is reporting an error with 'Incompatible Widths'.

## Demonstration:

- In order to get full credit, complete all exercises, then show the TA your work and your completed lab report, and be prepared to answer questions asked by the TA.
- Save your lab report as pdf with the same file name except the file type will now be 'pdf'. **Submit your report in Brightspace right after the TA checks your work.**
- If you are not able to complete the lab during the scheduled lab time, show the TA the work that you have completed and submit your lab.
  - Your mark will be based on the work completed during the lab.
  - After the lab, finish up the lab on your own time.
    - You are encouraged to submit an updated lab report, but your mark will not increase.
- **Note:** If a student does not submit their work, 0 marks are given for the lab.
- **Note:** If a student does not show their work to a TA, 0 marks are given for the lab.