SYSC2310 A and B Introduction to Digital Systems
Fall 2022

Lab 6 Report

Sequential Logic Circuits

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TA Name: _____ETHAN_____

Lab Section: _____L20_____

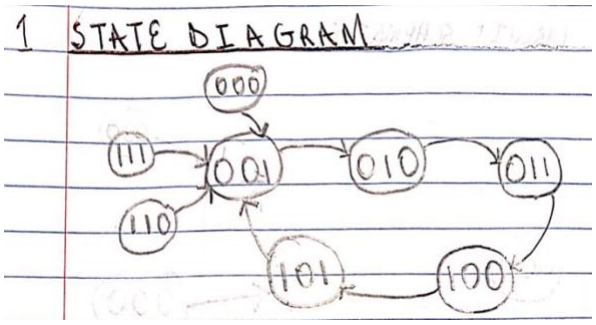
Lab Date: _6th December 2022___

Date Completed: _6th December 2022___

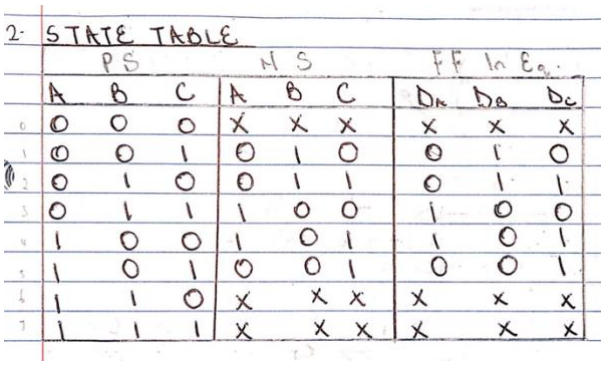
Exercise 1: Design a Design a Binary Counter

Part A: Pre-Lab Work

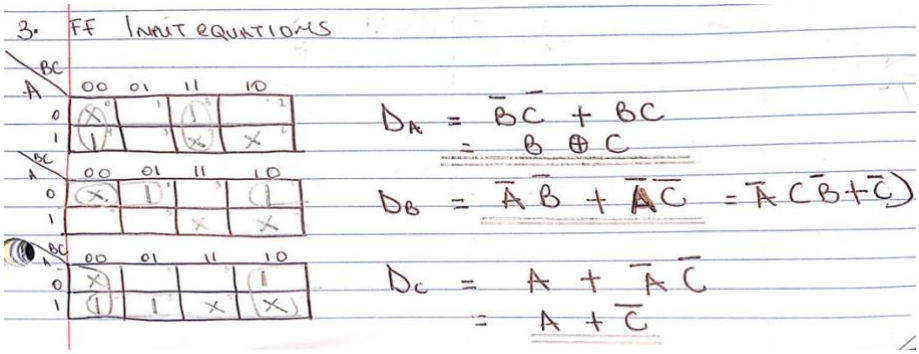
1- State Diagram



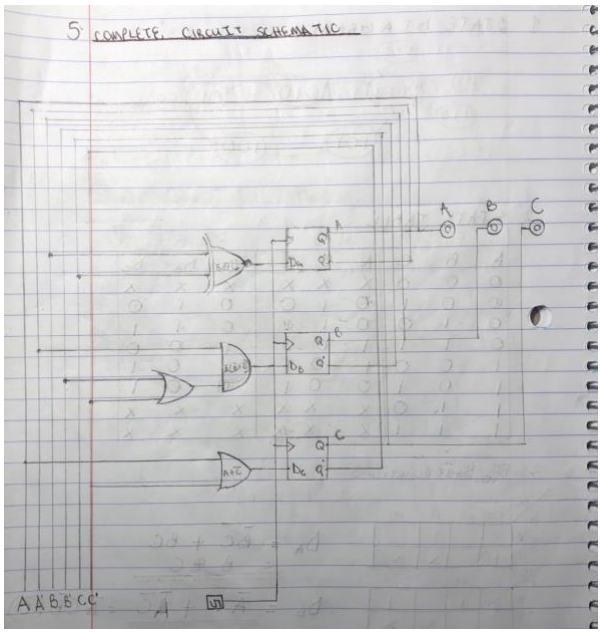
2- State Table



3- K-Maps and FF input equations

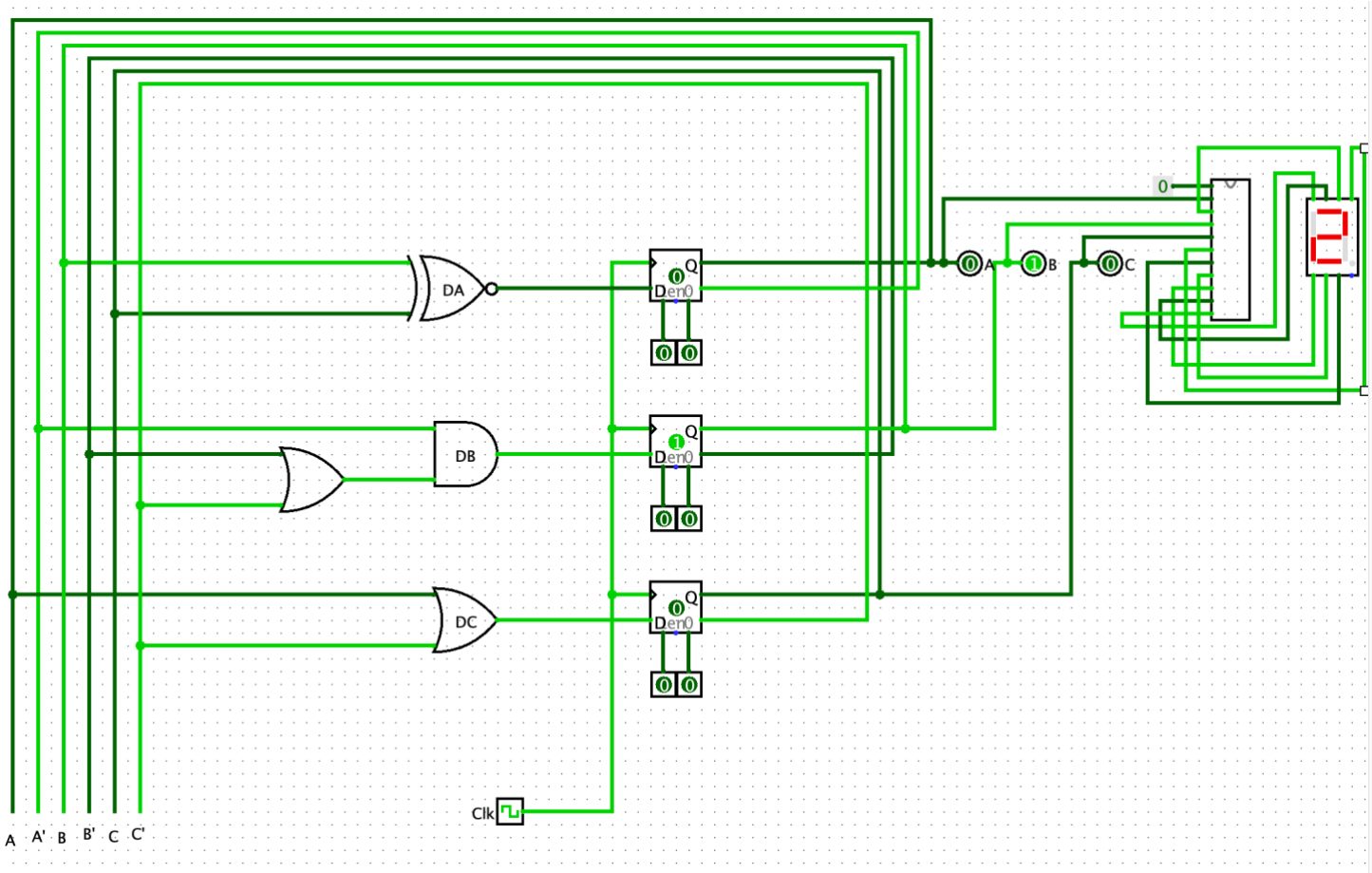


4- Circuit Schematic



Total Number of Gates (excluding the D-FFs): …4 two inputs gates: $2OR_2$, $1AND_2$, $1XNOR_2$

Screen Shot of Exercise 1 Circuit



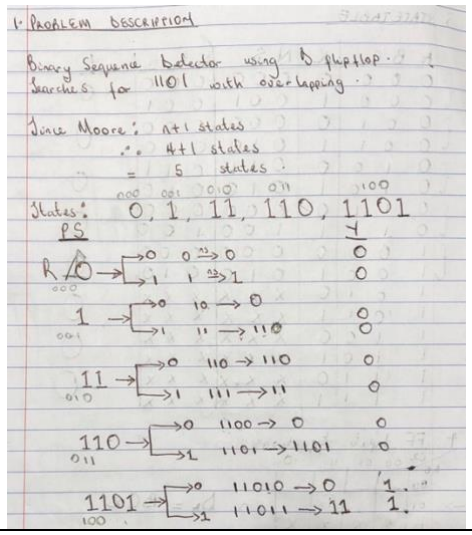
Copy and Paste Exercise 1 Simulation Logging File

Clk	A	B	C
0	0	0	0
1	1	1	1
0	1	1	1
1	1	0	1
0	1	0	1
1	0	0	1
0	0	0	1
1	0	1	0
0	0	1	0
1	0	1	1
0	0	1	1
1	1	0	0
0	1	0	0

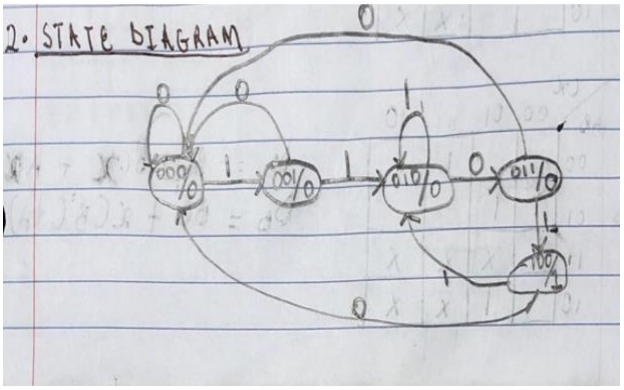
Exercise 2: Design a Binary Sequence Detector

Part A: Pre-Lab Work

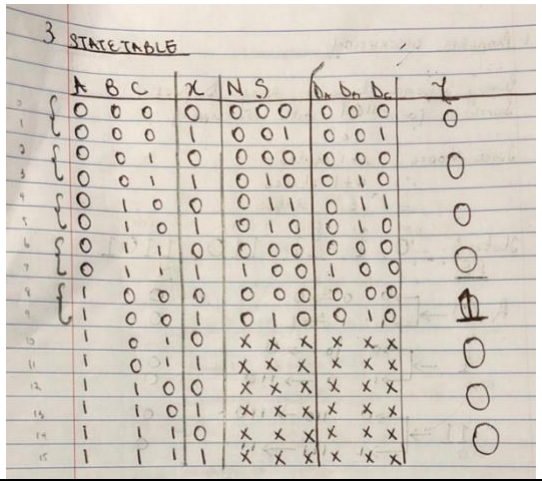
1- Problem Description:



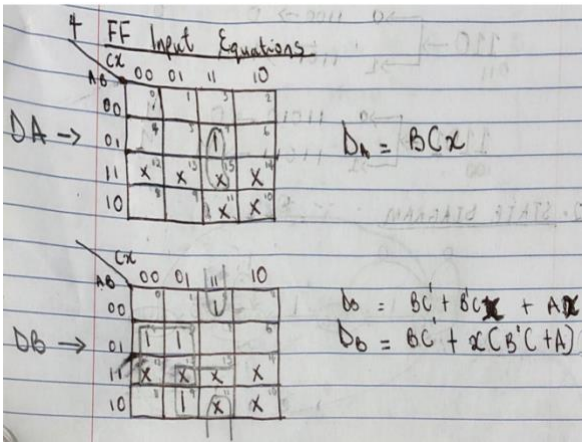
2- State Diagram

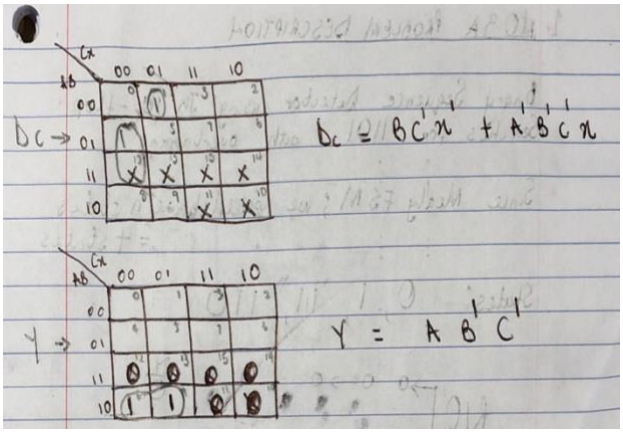


3- State Table

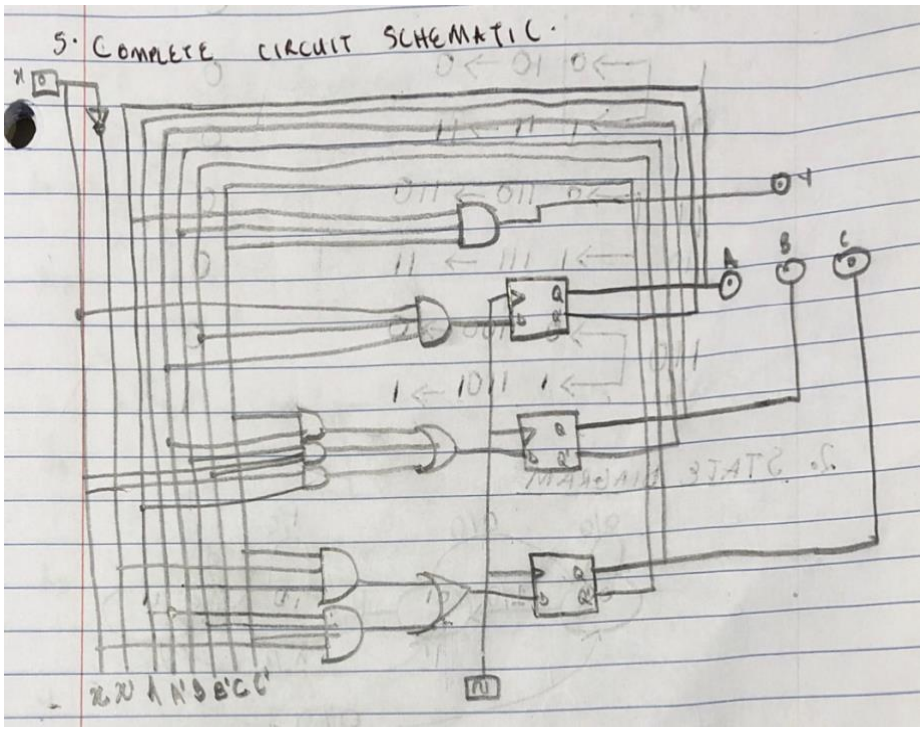


4- K-Maps and FF input equations



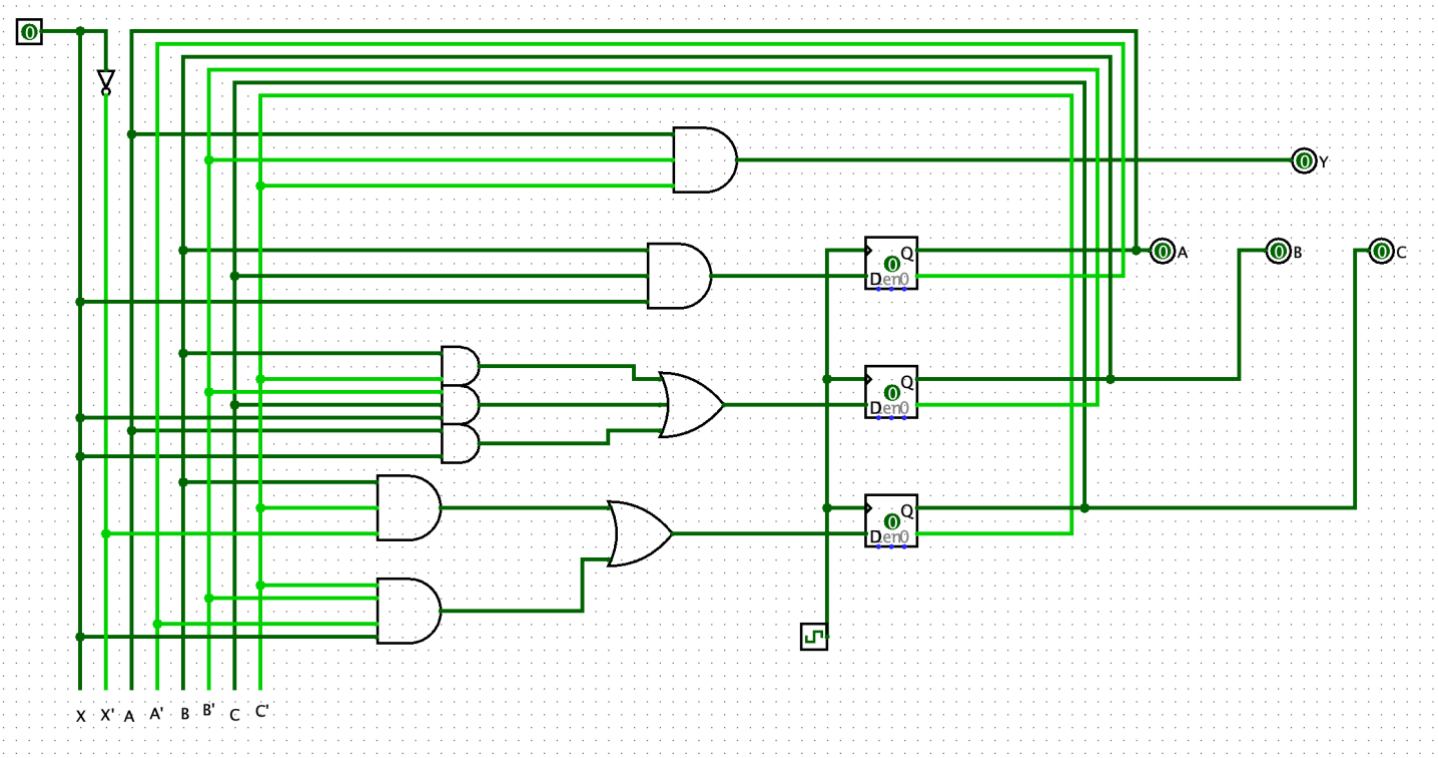


5- Circuit Schematic



Total Number of Gates (excluding the D-FFs):16 two inputs gates; $3OR_2$, $13AND_2$,

Screen Shot of Exercise 2 Circuit



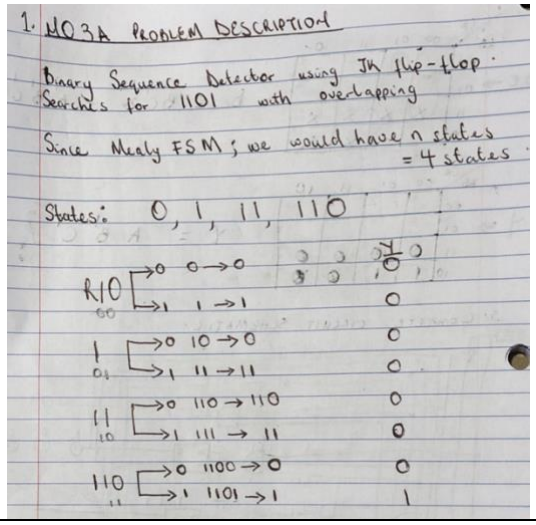
Copy and Paste Exercise 2 Simulation Logging File

A	B	C	X	Y
0	0	0		
0	0	0	0	0
0	0	0	1	0
0	0	1	1	0
0	0	1	0	0
0	0	0	0	0
0	0	0	1	0
0	0	1	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	1	0
0	1	0	0	0
0	1	1	0	0
0	1	1	1	0
1	0	0	1	1
0	1	0	1	0
0	1	0	0	0
0	1	1	0	0
0	1	1	1	0
1	0	0	1	1
0	1	0	1	0
0	1	0	0	0
0	1	1	0	0
0	1	1	1	0
1	0	0	1	1

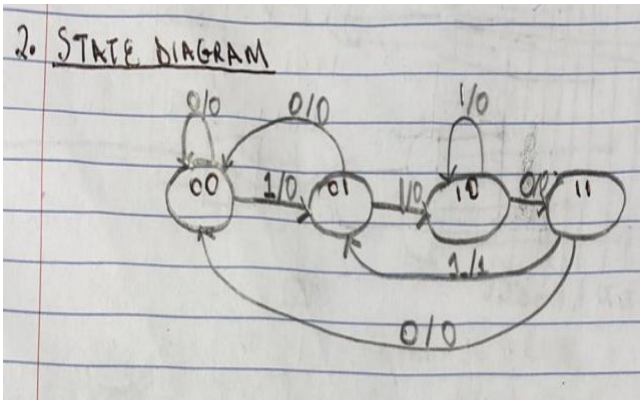
Exercise 3: Design a Binary Sequence Detector using JK flip-flops

Part A: Pre-Lab Work

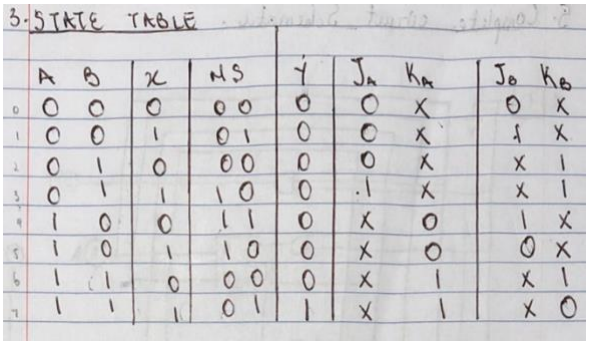
1- Problem Description:



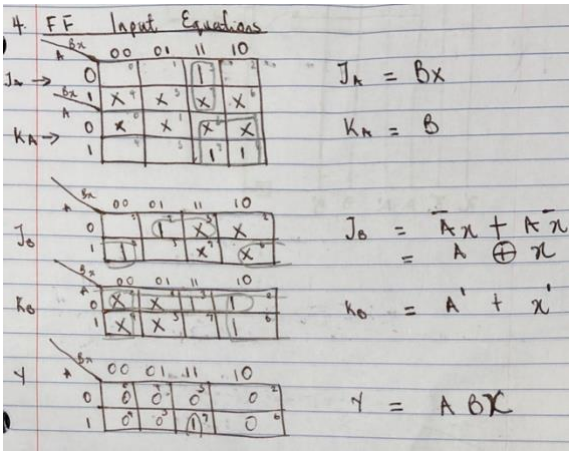
2- State Diagram



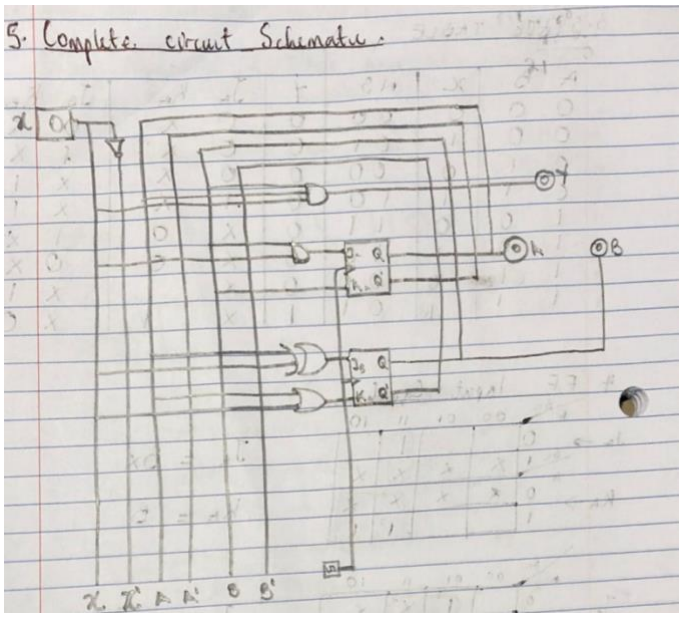
3- State Table



4- K-Maps and FF input equations

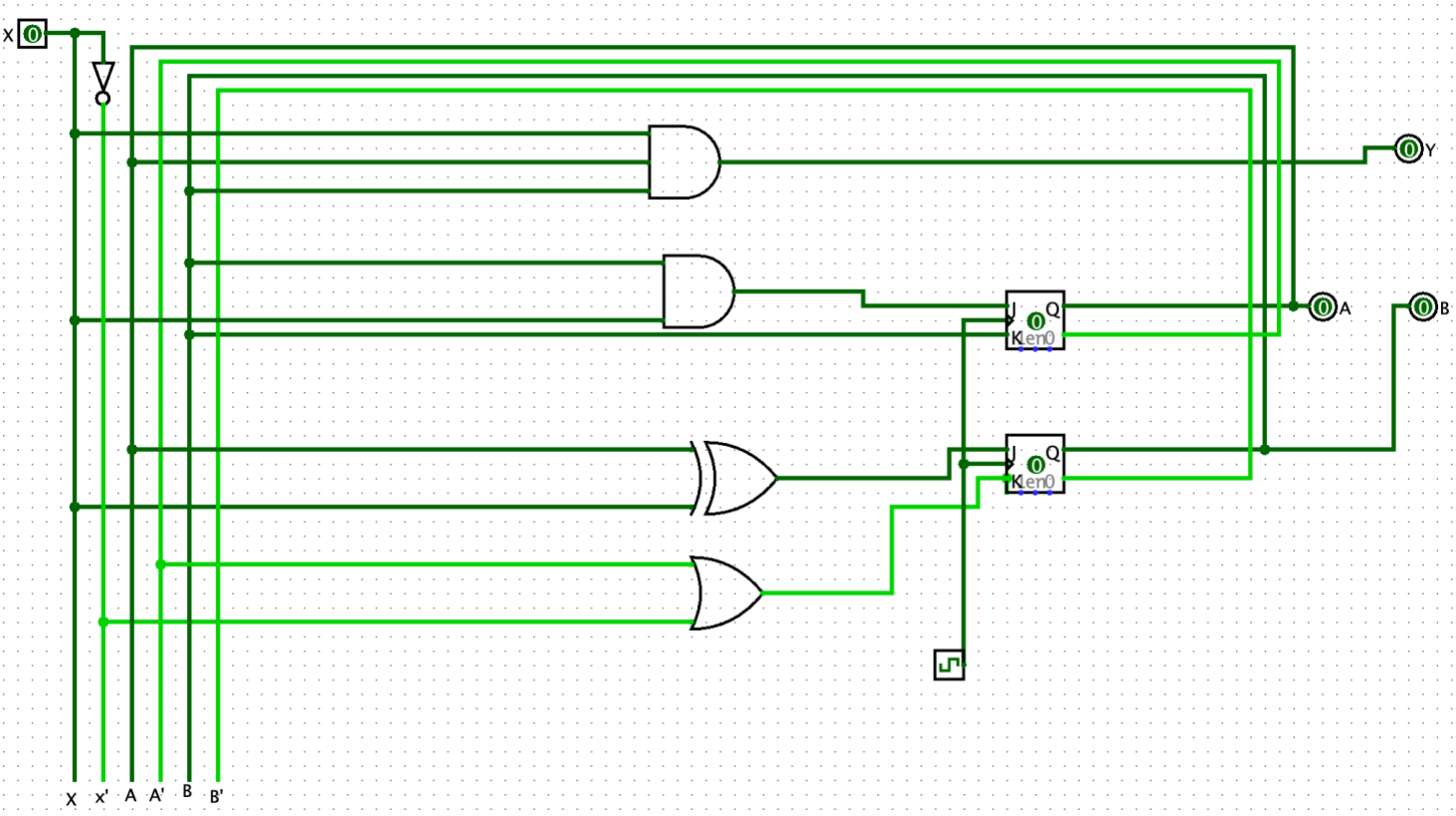


5- Circuit Schematic



Total Number of Gates (excluding the D-FFs used inside the JK-FF): 5 two input gates; 1XOR$_2$, 3AND$_2$, 1OR$_2$,

Screen Shot of Exercise 3 Circuit



Copy and Paste Exercise 3 Simulation Logging File

A	B	X	Y
0	0	0	0
0	0	1	0
0	1	1	0
0	1	0	0
0	0	0	0
0	0	1	0
0	1	1	0
1	0	1	0
1	0	0	0
1	1	0	0
1	1	1	1
0	1	1	0
0	1	0	0
0	0	0	0
0	0	1	0
0	1	1	0
1	0	1	0
1	0	0	0
1	1	0	0
1	1	1	1

INTRODUCTION TO DIGITAL SYSTEMS

SYSC2310 (Fall 2022)

Lab 6: Sequential Logic Circuits

Objectives

- Design a binary counter and a binary sequence detector

Relation to course outcomes

The work in this lab is related to the two following course outcomes:

- Able to design, implement and analyze sequential logic circuits with flip-flops.

Graded Pre-Lab Preparation

- Take the time to read this document prior to arriving to the lab in order to understand the essence of the work to be performed.
- Complete Exercise 1 Part A, Exercise 2 Part A, and Exercise 3 Part A of the lab report **before the lab**. Your answers to these pre-lab parts **will be graded**.

Preparation for the lab

1. Under your 'sysc2310lab/lab6' folder, create folders 'Ex1', 'Ex2' and 'Ex3' to save your work during this lab. Remember, by the end of the term, you are required to have the files for all the exercises in every lab. TAs and lab technicians will not be able to recover any deleted file, or any file that you have overwritten by mistake. Local Windows recycle bin doesn't work with the network M drive.
2. Download 'Lab 6 Report Template.docx' from the "Labs" Module, rename the file to 'Lab 6 Report `Jane Doe`.docx' where `Jane Doe` is your name, and save to your 'lab6' folder.
3. Open your lab report document and complete the first page. Read through the rest of the document so that you are aware of what needs to be recorded. **Complete the pre-lab parts (Exercise 1 Part A, Exercise 2 Part A, and Exercise 3 Part A) before your lab.**

Exercise 1: Design a Binary Counter

Design, construct and test a 3-bit binary counter that goes through the following sequence of binary states:

1, 2, 3, 4, 5, then back to 1.

Note that the binary states '0', '6' and '7' are not used. The counter must be self-starting; that is, if the circuit starts on any of the invalid states ('0', '6' or '7'), the counter must move on to any valid state on the next pulse and continue to work correctly. Not specifying any particular next valid state gives some flexibility in our design, allowing for the use of don't care conditions and further reduce the circuit size. The design should resemble an FSM without inputs or outputs, using **D flip-flops**. The counter is controlled only by the clock.

1.A (Pre-lab work)

Derive the following design data about the system:

1. State diagram,
2. State table,
3. FF-input equations,
4. A complete circuit schematic.

1.B (During the Lab)

- In Logisim, please use D flip-flops from the memory library. The default for these flip-flops is being +ve edge triggered. For help with the D flip-flop, please hover over the input pins to read its function, and refer to (http://www.cburch.com/logisim/docs/2.7/en/html/libs/mem/index.html).
- Please use the clock input from the wiring library. For help with the clock input, please refer to (http://www.cburch.com/logisim/docs/2.7/en/html/libs/wiring/clock.html).
- To check operation of the counter, use the 7-seg decoder display designed in previous labs.
- Enable logging to 'Lab6_Ex1_log.txt', and use the poke tool ( ) to change values of the input Clk. Notice and record the output 7-seg display.
- To check operation of the counter during the invalid states, please use the preset/clear inputs of the D flip-flop to initialize the counter to each of the invalid states ('0', '6' and '7'). Then, proceed with the clock to ensure correct transition to ant valid state.
- Save the circuit as 'Lab6_Ex1.circ'.

Exercise 2: Design a Binary Sequence Detector

Design, construct and test a binary sequence detector that can be used to search for a specific sequence of binary values within a long stream of bits. Search for the binary sequence "**1101**".

The sequence detector should be "Overlapping" signatures. For instance, the following input sequence will generate the corresponding output:

Input:	0	1	1	0	1	1	0	1	0	0	1	0
Output:	0	0	0	0	1	0	0	1	0	0	0	0

Note how one bit can be common between two detected sequences. The design should resemble a **Moore FSM**, using **D flip-flops**.

2.A (Pre-lab work)

Derive the following design data about the system:

1. Complete problem description (similar to the lecture).
2. State diagram,
3. State table,
4. FF-input equations,
5. A complete circuit schematic.

2.B (During the Lab)

- In Logisim, the circuit has only two inputs: data input (x), and the input clock (clk) and a single output (y). Use an input clock from the wiring library, and D flip-flops from the memory library.
- The flip-flops are +ve edge triggered. You should change the input (x) to a selected new value following the input sequence above before changing the clock from low to high (the +ve edge).
- Enable logging to 'Lab6_Ex2_log.txt' and use the poke tool ( ) to change values of the input (x) and the (clk). Notice and record the output (y) after each clock cycle.
- Save the circuit as 'Lab6_Ex2.circ'.

Exercise 3: Design a Binary Sequence Detector using JK flip-flops

Solve the same problem description of Exercise 2, using **JK flip-flops** in a **Mealy FSM**.

3.A (Pre-lab work)

Derive the following design data about the system:

1. Complete problem description (similar to the lecture).
2. State diagram,
3. State table,
4. FF-input equations,
5. A complete circuit schematic,
6. Compare the number of gates used in the design using D flip-flops (Ex.2), versus that using JK flip-flops (Ex.3). Include the difference in gate count between the JK-FF and the D-FF.

3.B (During the Lab)

- Implement the circuit in Logisim,
- Enable logging to 'Lab6_Ex3_log.txt' and use the poke tool ( ) to change values of the input (x) and the (clk). Notice and record the output (y) after each clock cycle,
- Save the circuit as 'Lab6_Ex3.circ'.

Demonstration:

- In order to get full credit, complete all exercises, **including the pre-lab portion**, then show the TA your work and your completed lab report, and be prepared to answer questions asked by the TA.
- Save your lab report as pdf with the same file name except the file type will now be 'pdf'. **Submit your report in Brightspace right after the TA checks your work.**
- If you are not able to complete the lab during the scheduled lab time, show the TA the work that you have completed and submit your lab.
    - Your mark will be based on the work completed during the lab.
    - After the lab, finish up the lab on your own time.
        - You are encouraged to submit an updated lab report, but your mark will not increase.
- **Note:** If a student does not submit their work, 0 marks are given for the lab.
- **Note:** If a student does not show their work to a TA, 0 marks are given for the lab.