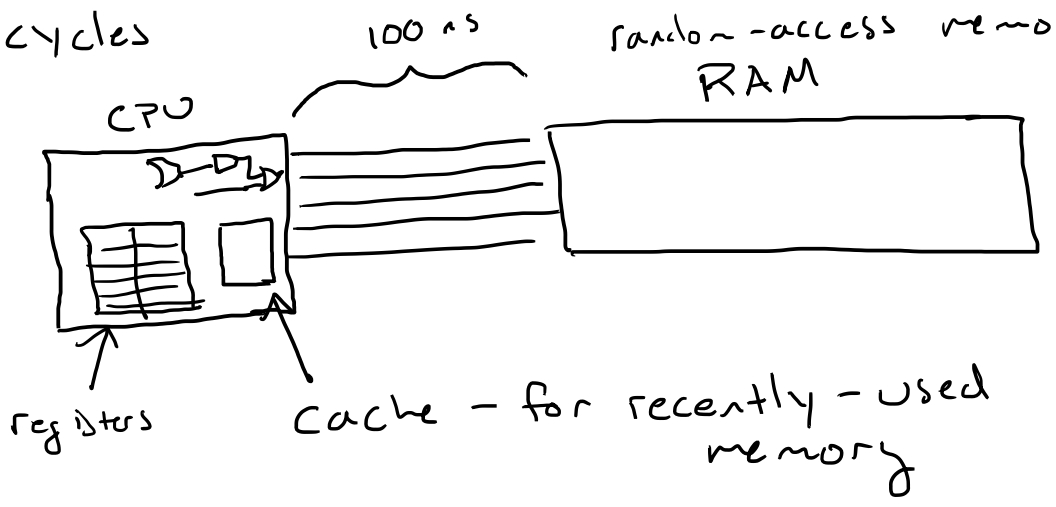
~1 GHz

giga hertz

1,000,000,000 per second

(clock) cycles




add r0, r1, r2 — instruction over registers — $10^{-9}$ s — 1 nanosecond

cache access — ~1-2 ns

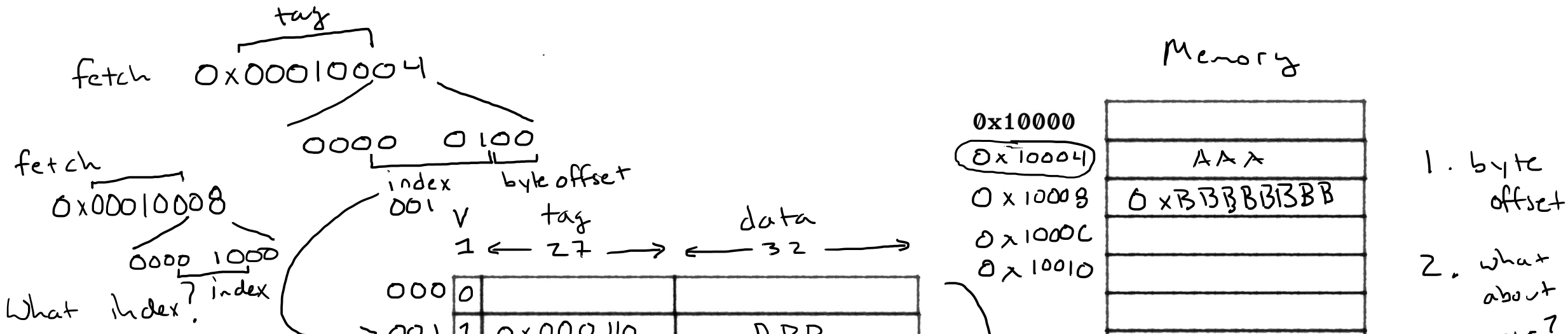
ldr r1, [r0] — $10^{-7}$ s — 100 nanos

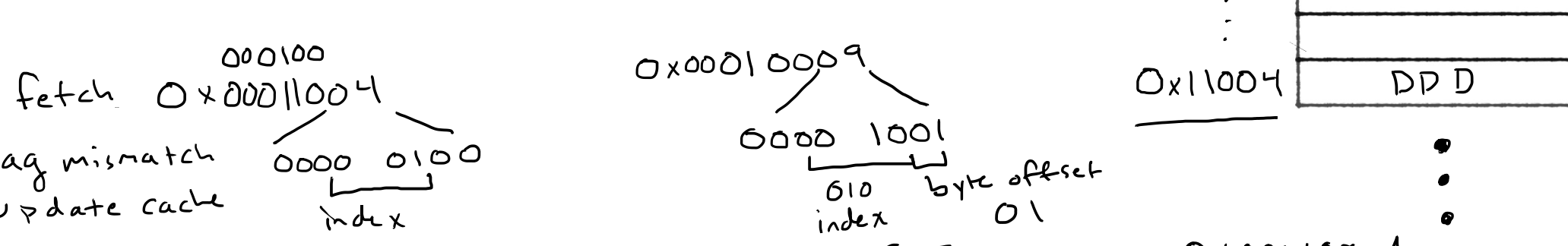
loop:

ldr r1, [r0] 100 ns

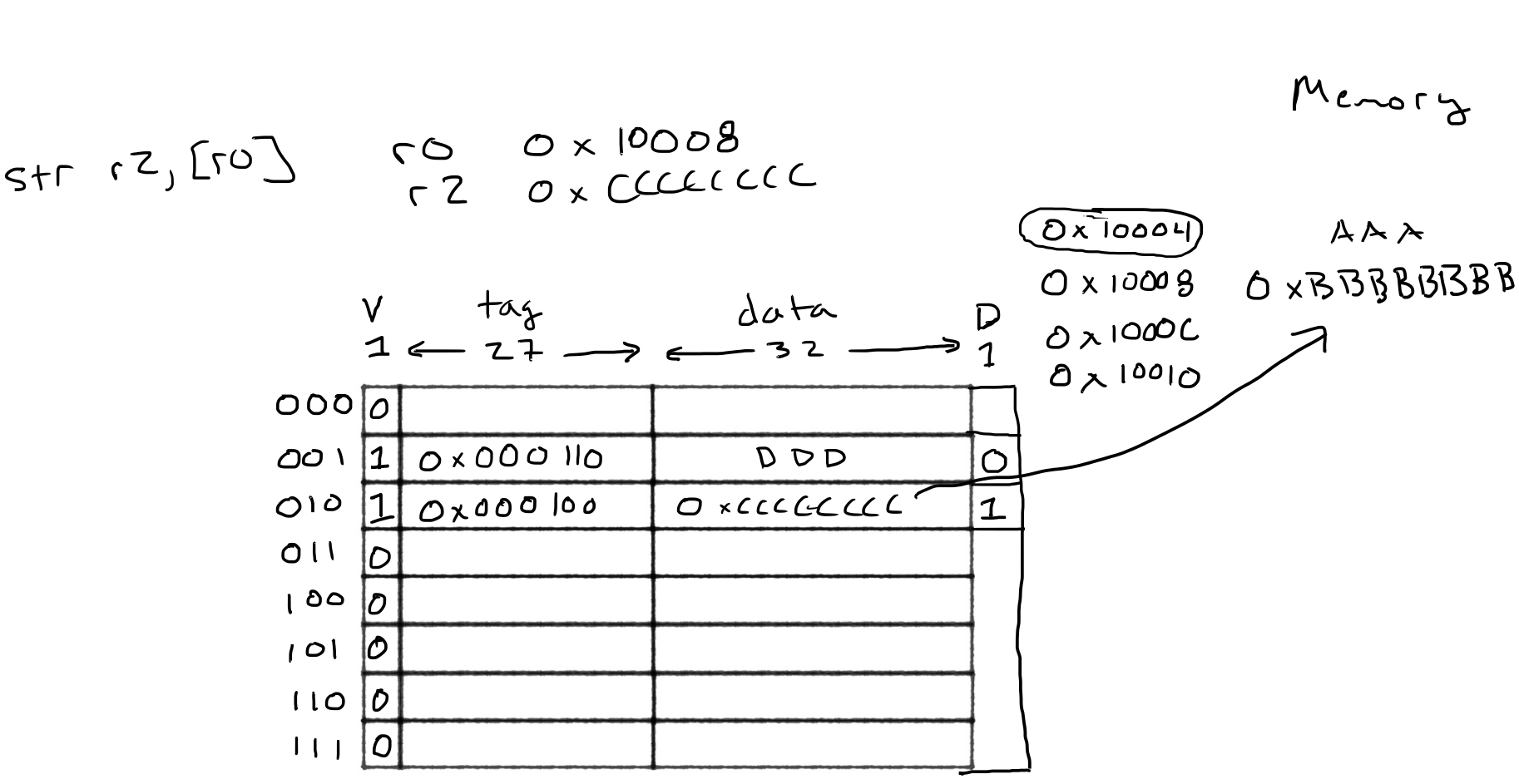
add r1, #1 1 ns

str r1, [r0] 100 ns




What about str?




Option 1:

write to cache AND to memory

write-through

Option 2:

save dirty bit when changing, save later

write-back