

VCU118 MIG Design Creation

May 2019



XTP442

Revision History

Date	Version	Description
05/29/19	9.0	Updated for 2019.1. Some screenshots not updated.
12/10/18	8.0	Updated for 2018.3. Some screenshots not updated.
06/18/18	7.0	Updated for 2018.2.
04/09/18	6.0	Updated for 2018.1.
12/20/17	5.0	Updated for 2017.4.
10/26/17	4.0	Updated for 2017.3.1. For Rev 2.0, with Production Silicon, and QSPI Flash devices.
08/31/17	3.1	Minor update to fix CR-980927.
06/20/17	3.0	Updated for 2017.2.
04/19/17	2.0	Updated for 2017.1.
12/19/16	1.0	Initial version for 2016.4.

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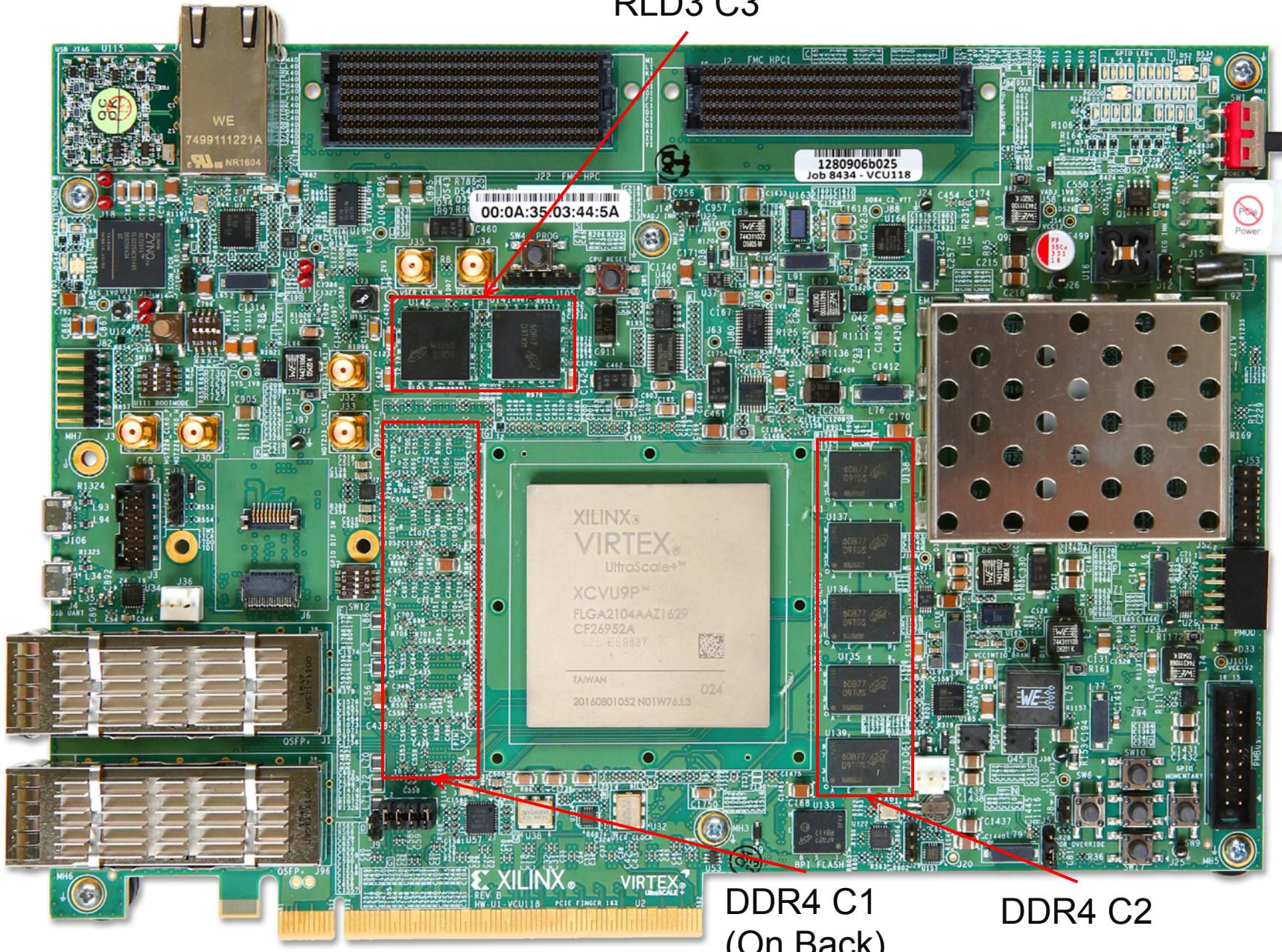
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Overview

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- > **Run MIG Example Designs**
- > **Generate MIG DDR4 C1 Example Design**
 - » Modifications to Example Design
 - » Compile Example Design
 - » VCU118 Setup
 - » Run MIG Example Design
- > **Generate MIG DDR4 C2 Example Design**
- > **Generate MIG RLD3 C3 Bit Example Design**
- > **References**

Xilinx VCU118 Board

RLD3 C3



DDR4 C1
(On Back)

DDR4 C2

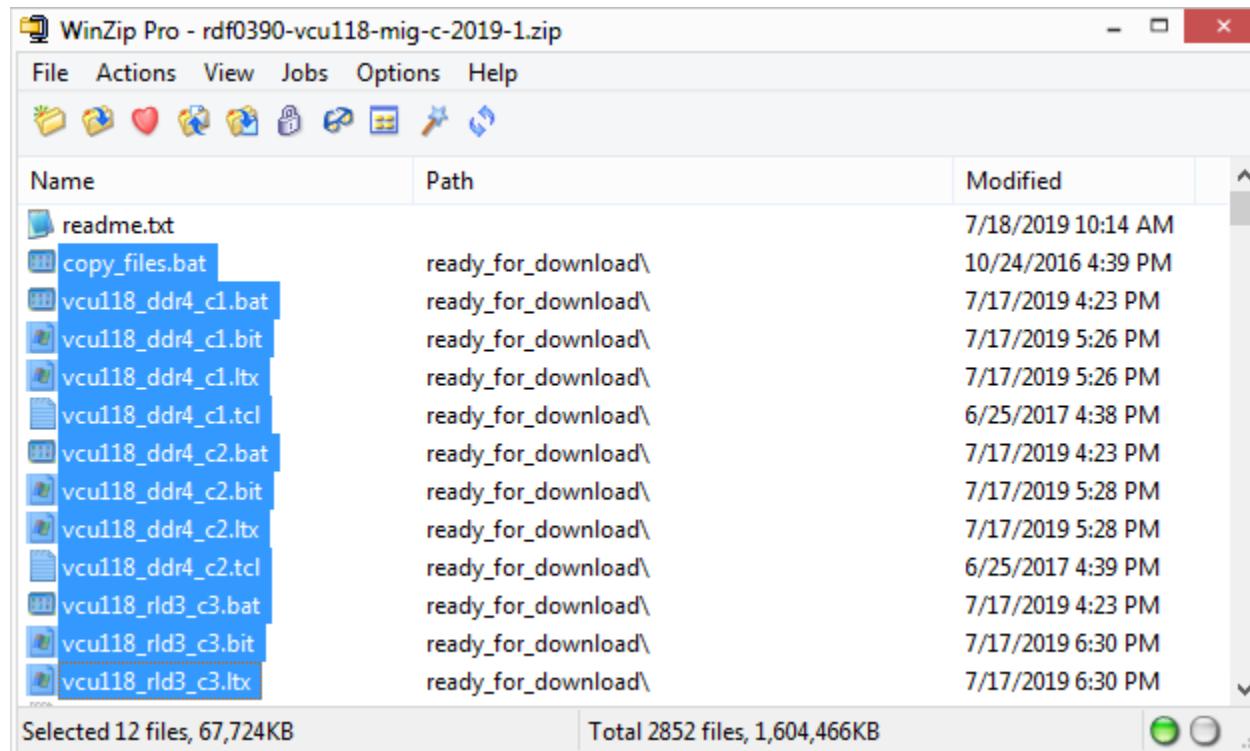
VCU118 Software Install and Board Setup

- > Complete setup steps in XTP449 – VCU118 Software Install and Board Setup:
 - » Software Requirements
 - » VCU118 Board Setup



VCU118 Setup

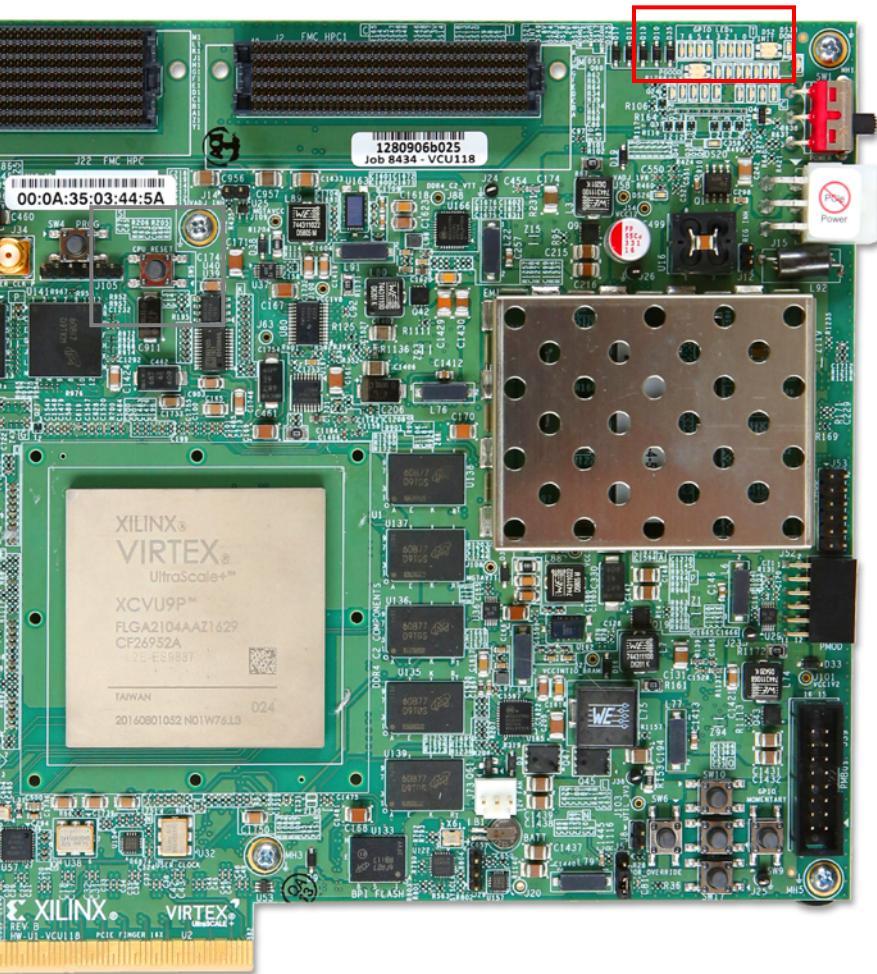
- > Open the RDF0390 - VCU118 MIG Design Files (2019.1 C) ZIP file, and extract the “ready_for_download” files to your C:\ drive:



Run MIG Example Designs



Run MIG Example Design



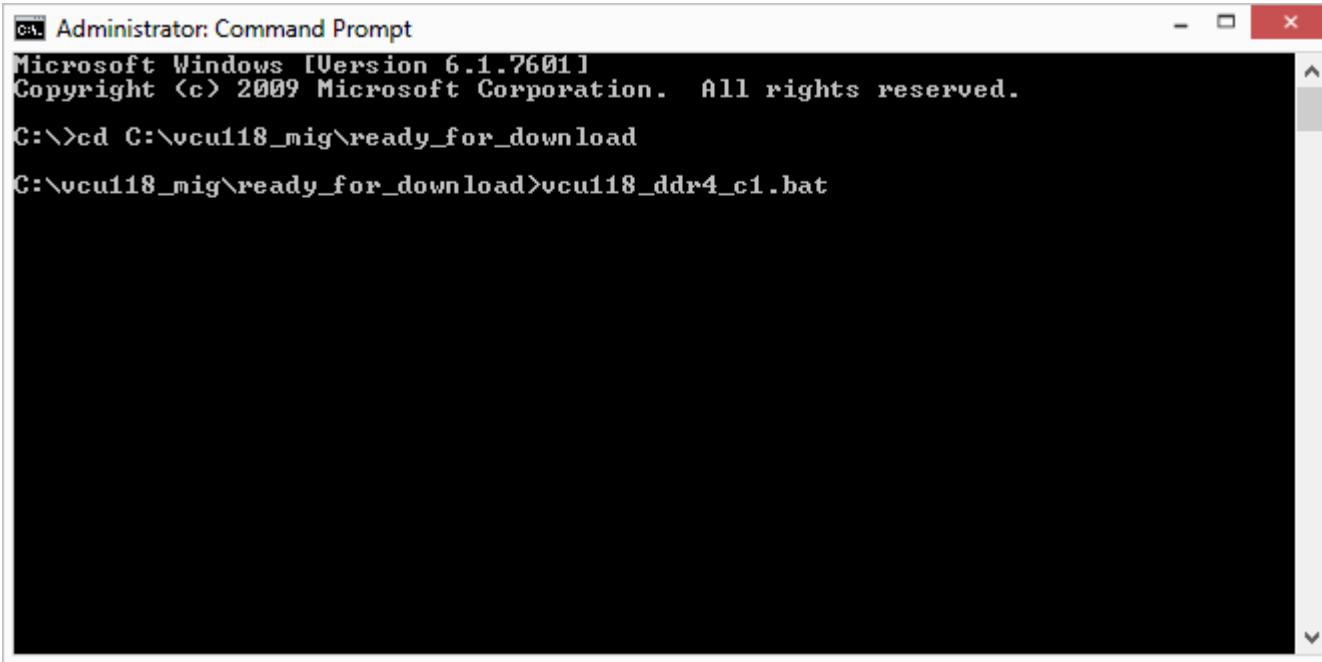
- > For the following tests:
- > After bitstream loads, LED 0 (right most LED) will be lit, and LED1 will be blinking
- > LED 3 will light and stay on
 - » This indicates Calibration has completed
- > If an error occurs, LED 0 will go out and LED 2 will light
 - » The “CPU_RESET” button, SW5, is the reset

Run MIG Example Design

- > From a Command Prompt, type:

```
cd C:\vcu118_mig\ready_for_download  
vcu118_ddr4_c1.bat
```

- > View results on LEDs



The screenshot shows a Windows Command Prompt window titled "Administrator: Command Prompt". The window displays the following text:

```
Administrator: Command Prompt  
Microsoft Windows [Version 6.1.7601]  
Copyright <c> 2009 Microsoft Corporation. All rights reserved.  
C:>cd C:\vcu118_mig\ready_for_download  
C:\vcu118_mig\ready_for_download>vcu118_ddr4_c1.bat
```

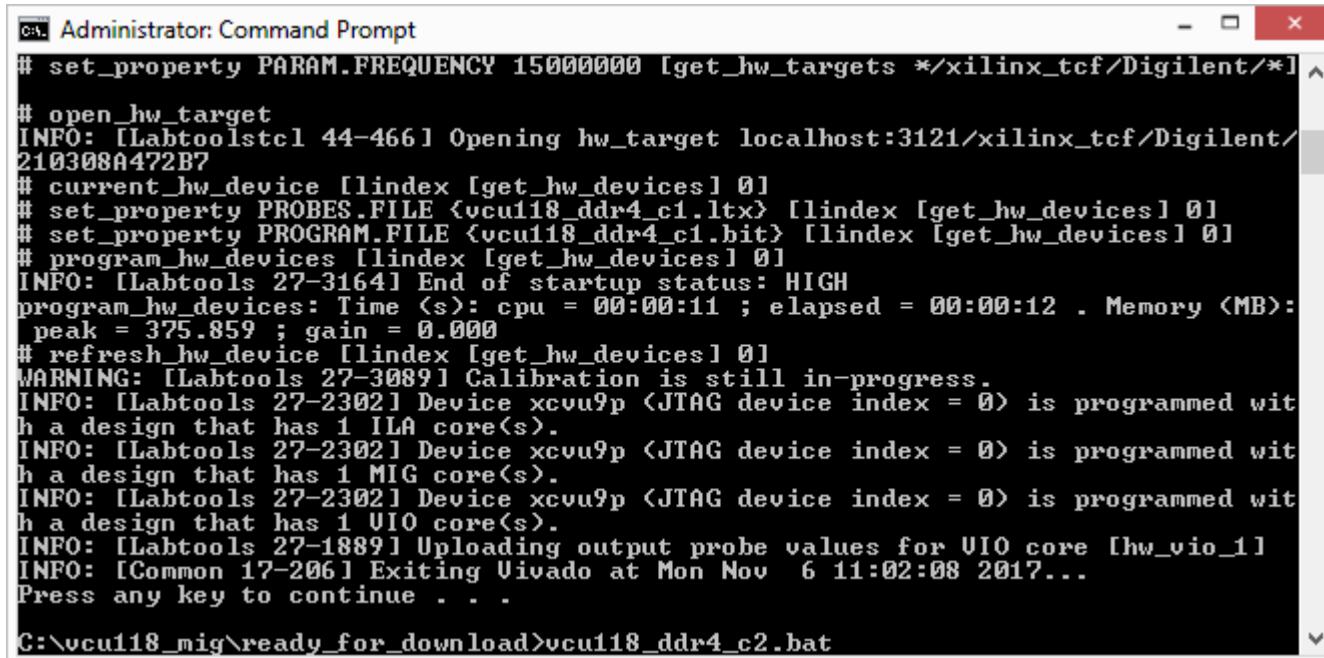
The command `vcu118_ddr4_c1.bat` has been entered and is being processed by the command prompt.

Run MIG Example Design

> Type:

`vcu118_ddr4_c2.bat`

> View results on LEDs



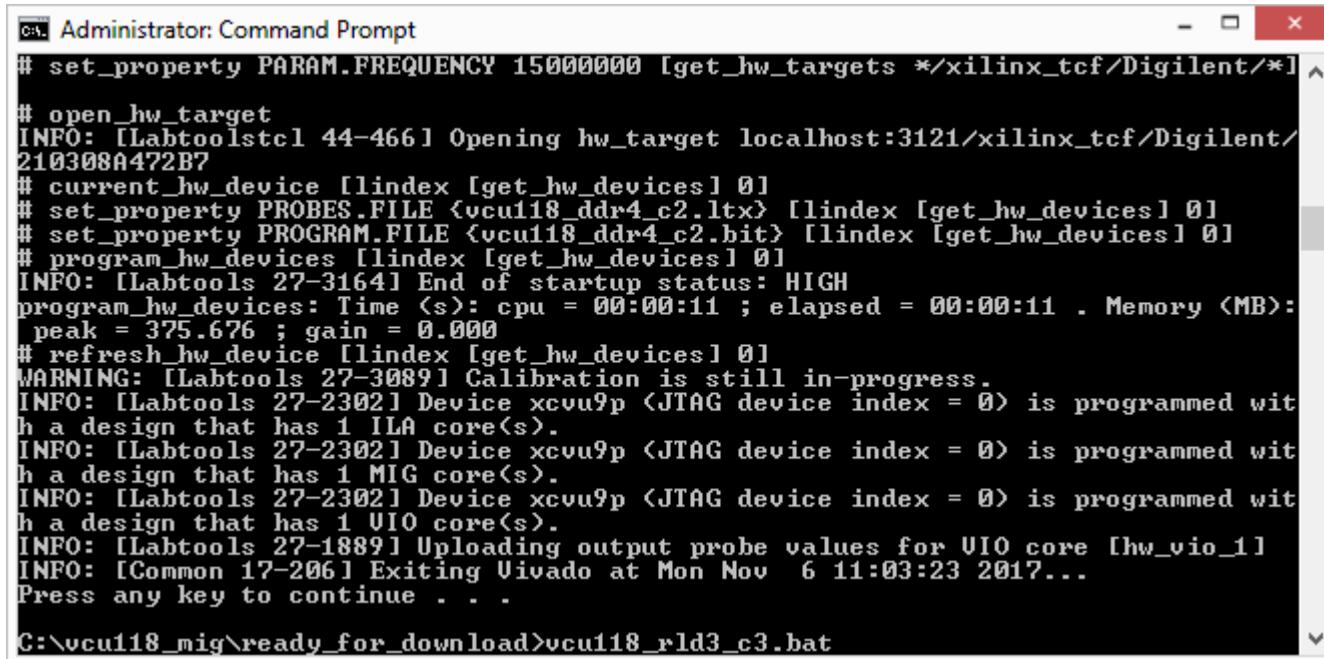
```
C:\ Administrator: Command Prompt
# set_property PARAM.FREQUENCY 15000000 [get_hw_targets */xilinx_tcf/Digilent/*]
# open_hw_target
INFO: [Labtools 44-466] Opening hw_target localhost:3121/xilinx_tcf/Digilent/210308A472B7
# current_hw_device [lindex [get_hw_devices] 0]
# set_property PROBES.FILE {vcu118_ddr4_c1.ltx} [lindex [get_hw_devices] 0]
# set_property PROGRAM.FILE {vcu118_ddr4_c1.bit} [lindex [get_hw_devices] 0]
# program_hw_devices [lindex [get_hw_devices] 0]
INFO: [Labtools 27-3164] End of startup status: HIGH
program_hw_devices: Time <s>: cpu = 00:00:11 ; elapsed = 00:00:12 . Memory <MB>: peak = 375.859 ; gain = 0.000
# refresh_hw_device [lindex [get_hw_devices] 0]
WARNING: [Labtools 27-3089] Calibration is still in-progress.
INFO: [Labtools 27-2302] Device xcvu9p (JTAG device index = 0) is programmed with a design that has 1 ILA core(s).
INFO: [Labtools 27-2302] Device xcvu9p (JTAG device index = 0) is programmed with a design that has 1 MIG core(s).
INFO: [Labtools 27-2302] Device xcvu9p (JTAG device index = 0) is programmed with a design that has 1 UIO core(s).
INFO: [Labtools 27-1889] Uploading output probe values for UIO core [hw_vio_1]
INFO: [Common 17-206] Exiting Vivado at Mon Nov 6 11:02:08 2017...
Press any key to continue . . .
C:\vcu118_mig\ready_for_download>vcu118_ddr4_c2.bat
```

Run MIG Example Design

> Type:

`vcu118_rld3_c3.bat`

> View results on LEDs



```
# set_property PARAM.FREQUENCY 15000000 [get_hw_targets */xilinx_tcf/Digilent/*]
# open_hw_target
INFO: [Labtools 44-466] Opening hw_target localhost:3121/xilinx_tcf/Digilent/210308A472B7
# current_hw_device [lindex [get_hw_devices] 0]
# set_property PROBES.FILE {vcu118_ddr4_c2.ltx} [lindex [get_hw_devices] 0]
# set_property PROGRAM.FILE {vcu118_ddr4_c2.bit} [lindex [get_hw_devices] 0]
# program_hw_devices [lindex [get_hw_devices] 0]
INFO: [Labtools 27-3164] End of startup status: HIGH
program_hw_devices: Time <s>: cpu = 00:00:11 ; elapsed = 00:00:11 . Memory <MB>:
peak = 375.676 ; gain = 0.000
# refresh_hw_device [lindex [get_hw_devices] 0]
WARNING: [Labtools 27-3089] Calibration is still in-progress.
INFO: [Labtools 27-2302] Device xcvu9p (JTAG device index = 0) is programmed with a design that has 1 ILA core(s).
INFO: [Labtools 27-2302] Device xcvu9p (JTAG device index = 0) is programmed with a design that has 1 MIG core(s).
INFO: [Labtools 27-2302] Device xcvu9p (JTAG device index = 0) is programmed with a design that has 1 UIO core(s).
INFO: [Labtools 27-1889] Uploading output probe values for UIO core [hw_vio_1]
INFO: [Common 17-206] Exiting Vivado at Mon Nov 6 11:03:23 2017...
Press any key to continue . . .
C:\vcu118_mig\ready_for_download>vcu118_rld3_c3.bat
```

Generate MIG DDR4 C1 Example Design

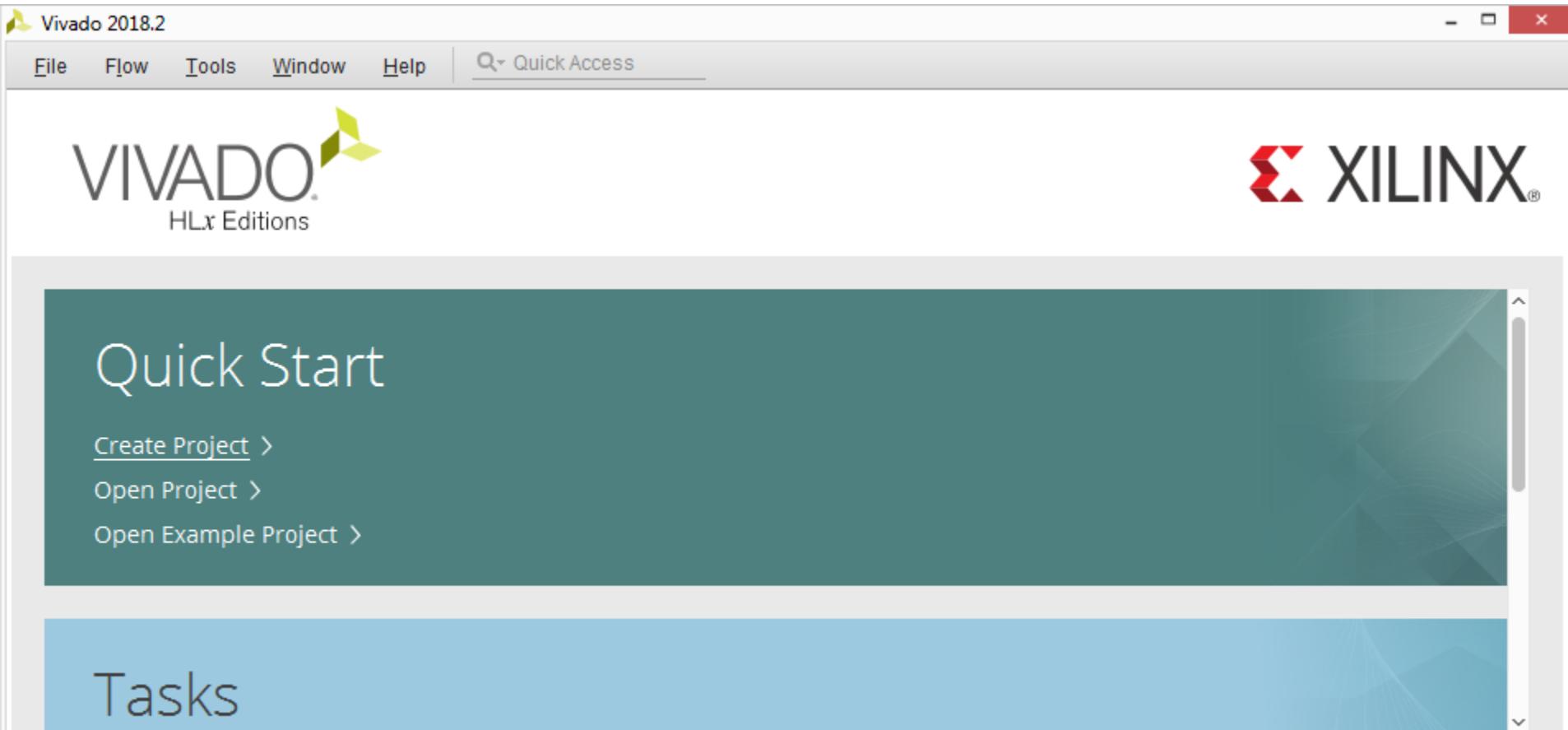


Generate MIG DDR4 C1 Example Design

> Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2019.1 → Vivado

> Select Create Project



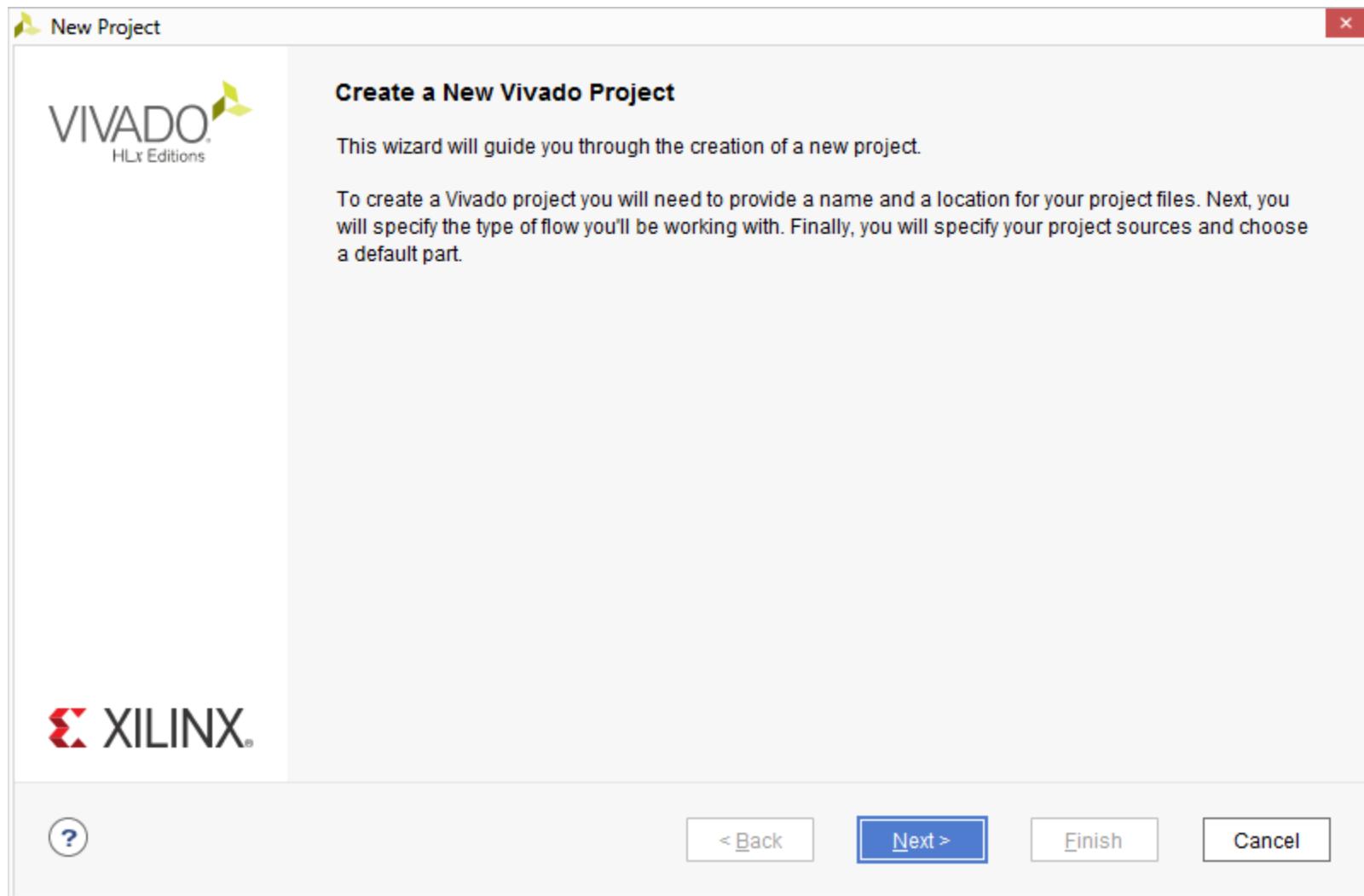
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Note: Presentation applies to the VCU118

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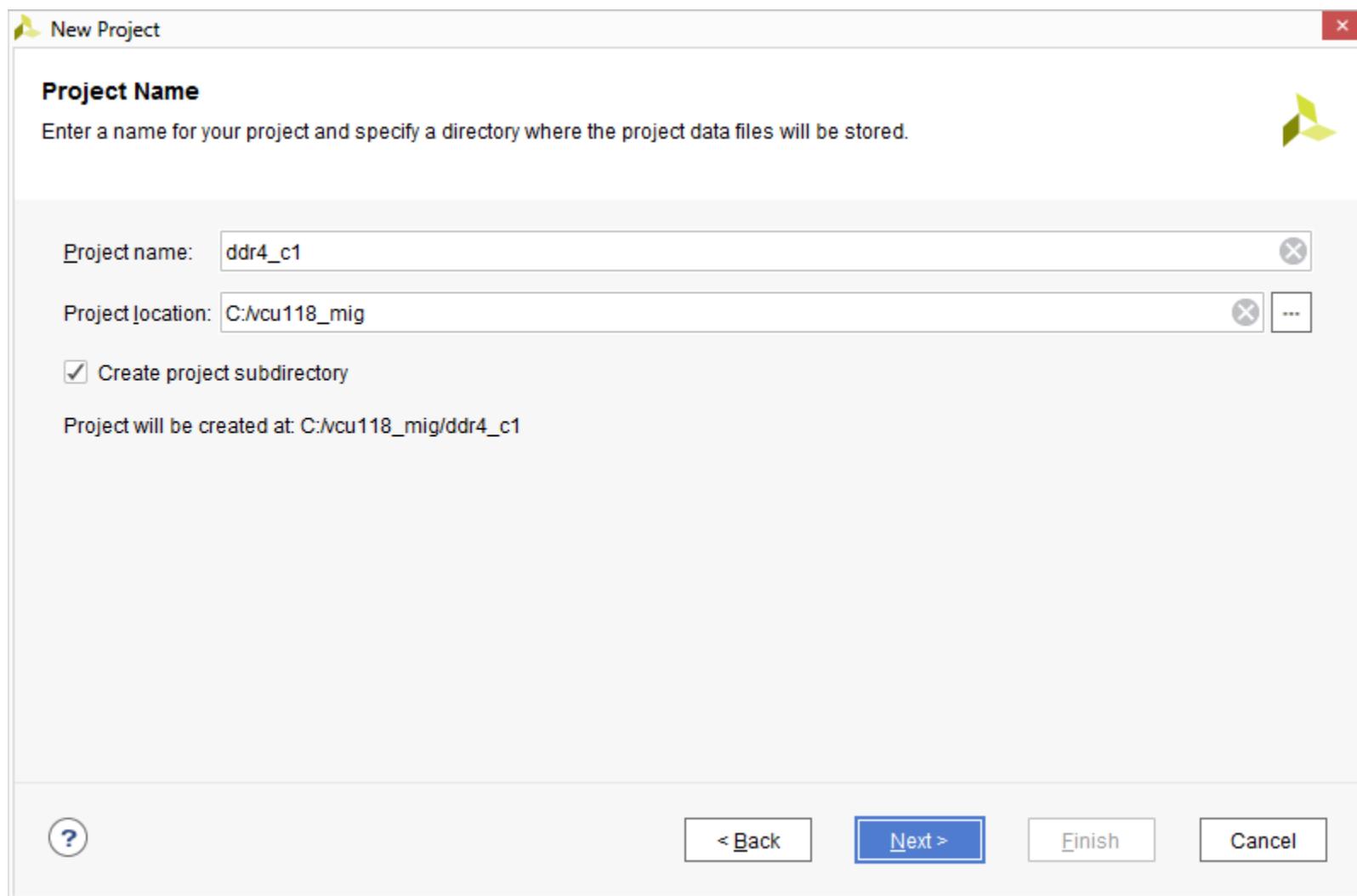
Generate MIG DDR4 C1 Example Design

> Click Next



Generate MIG DDR4 C1 Example Design

- > Set the Project name to ddr4_c1 and location to C:/vcu118_mig
 - » Check Create project subdirectory

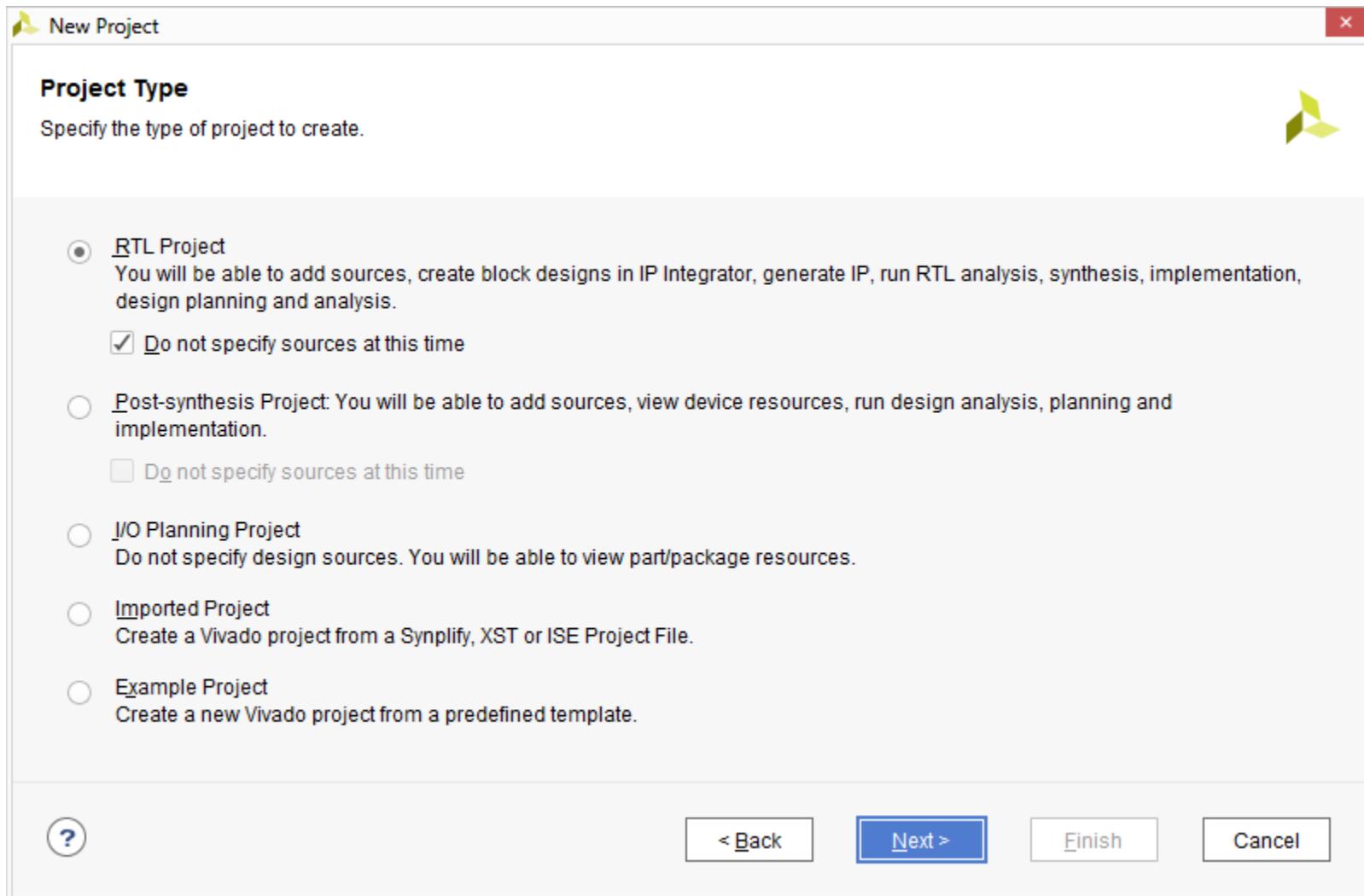


Note: Vivado generally requires forward slashes in paths

Generate MIG DDR4 C1 Example Design

> Select RTL Project

» Select Do not specify sources at this time



Generate MIG DDR4 C1 Example Design

- > Under Boards, select the VCU118 Rev 2.0

New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Parts | Boards

Reset All Filters

Vendor: All Name: All

Search:

Display Name	Preview	Vendor	File V
Virtex UltraScale+ VCU118 Evaluation Platform		xilinx.com	2.0
Virtex UltraScale+ VCU1525 Acceleration Development Board		xilinx.com	1.1

< >

?

< Back

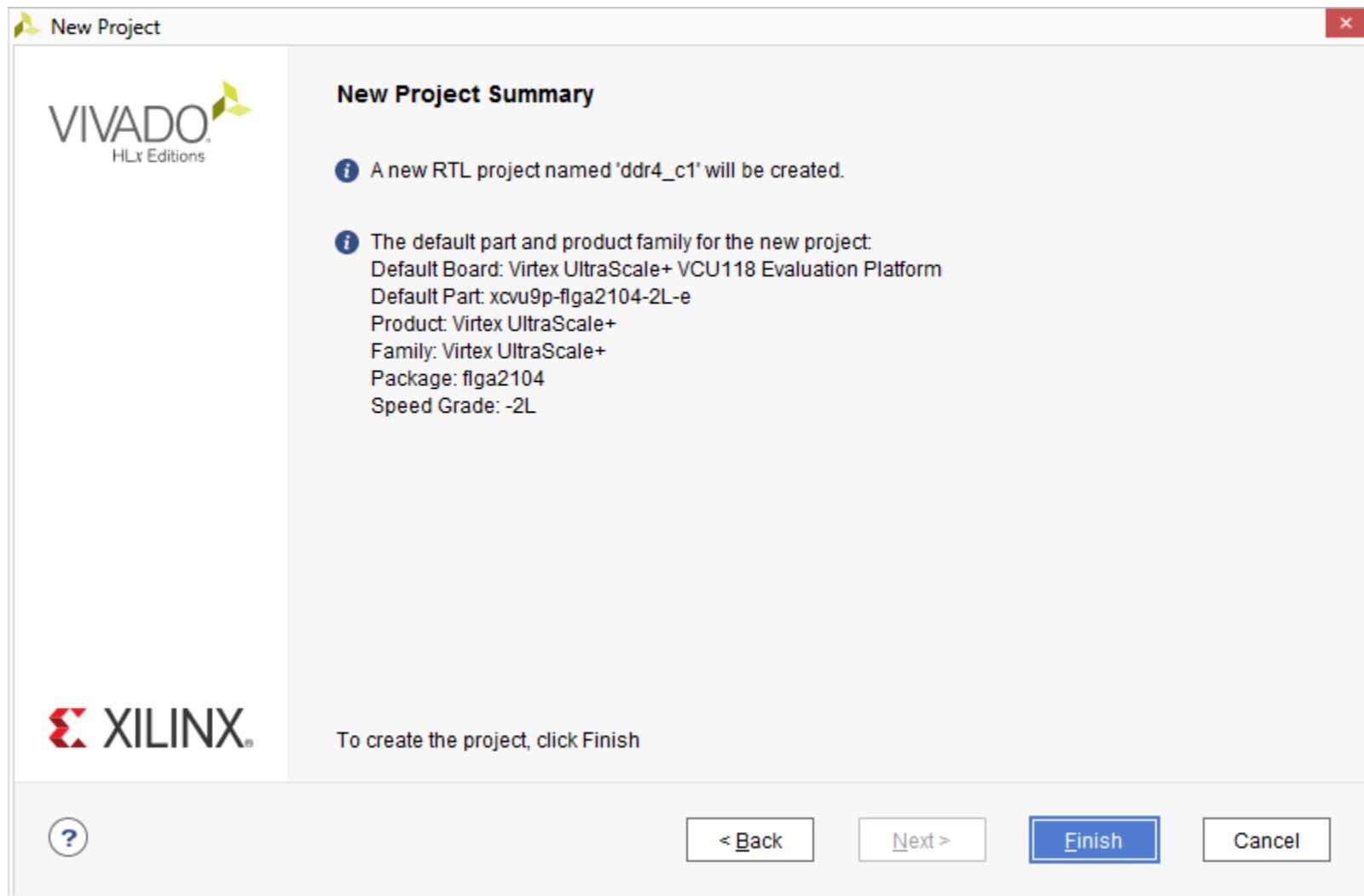
Next >

Finish

Cancel

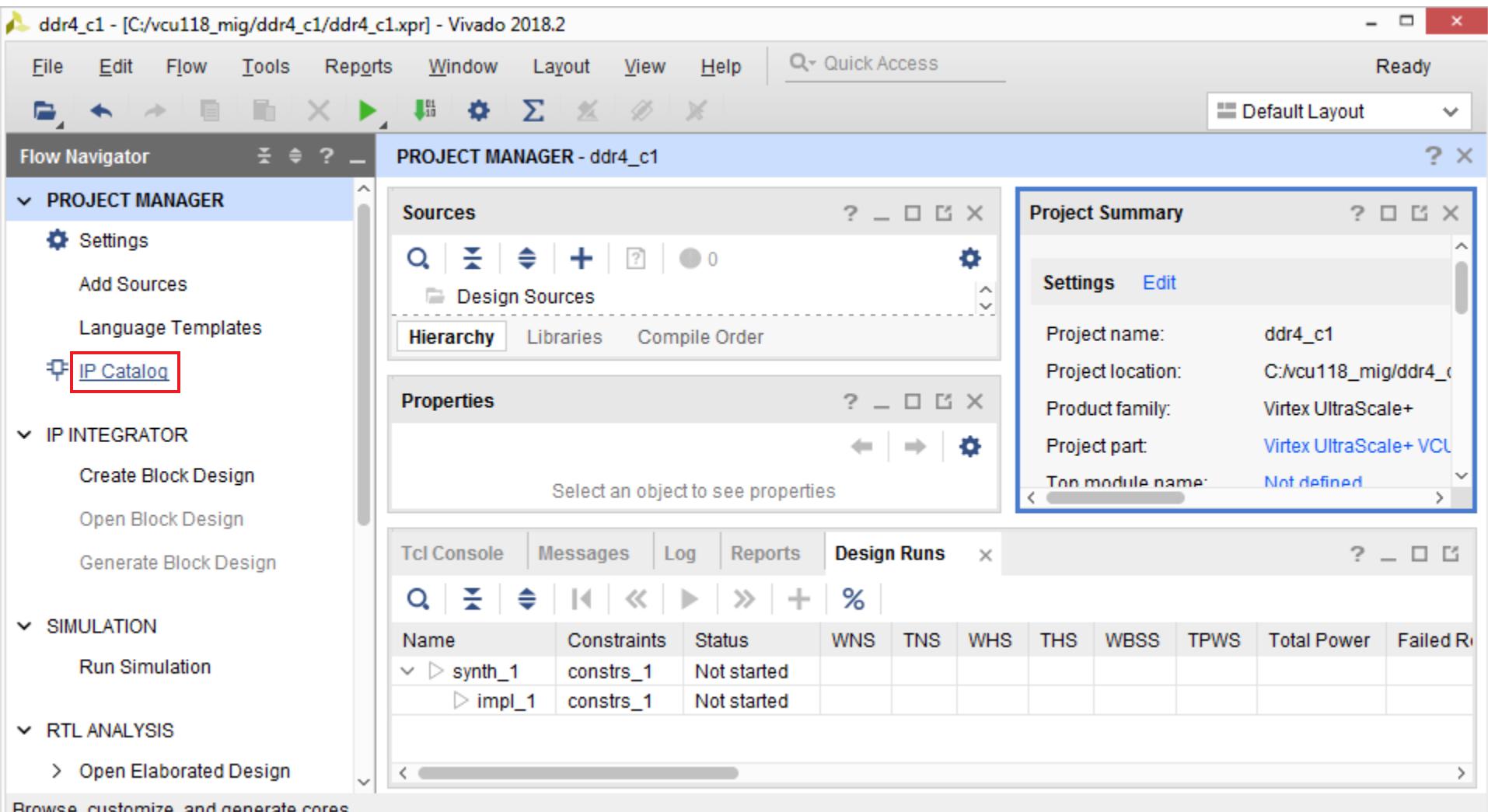
Generate MIG DDR4 C1 Example Design

> Click Finish



Generate MIG DDR4 C1 Example Design

> Click on IP Catalog



Generate MIG DDR4 C1 Example Design

> Select DDR4 SDRAM (MIG), v2.2

The screenshot shows the Vivado 2018.2 interface with the project "ddr4_c1" open. The "PROJECT MANAGER" section is selected in the left sidebar. In the center, the "IP Catalog" tab is active, displaying a list of cores and interfaces. The "Memories & Storage Elements" category is expanded, showing "ECC", "External Memory Interface", and four sub-options: "DDR3 SDRAM (MIG)", "DDR4 SDRAM (MIG)", "LPDDR3 SDRAM (MIG)", and "QDRII SDRAM (MIG)". The "DDR4 SDRAM (MIG)" option is highlighted with a blue selection bar. Below the table, the "Details" section shows the selected item's name and version: "Name: DDR4 SDRAM (MIG)" and "Version: 2.2 (Rev. 5)".

Name	Type	Status	License	VLM
AXI4	AXI4	Production	Included	xilinx
Memories & Storage Elements				
ECC				
External Memory Interface				
DDR3 SDRAM (MIG)	AXI4	Production	Included	xilinx
DDR4 SDRAM (MIG)	AXI4	Production	Included	xilinx
LPDDR3 SDRAM (MIG)		Production	Included	xilinx
QDRII SDRAM (MIG)		Production	Included	xilinx

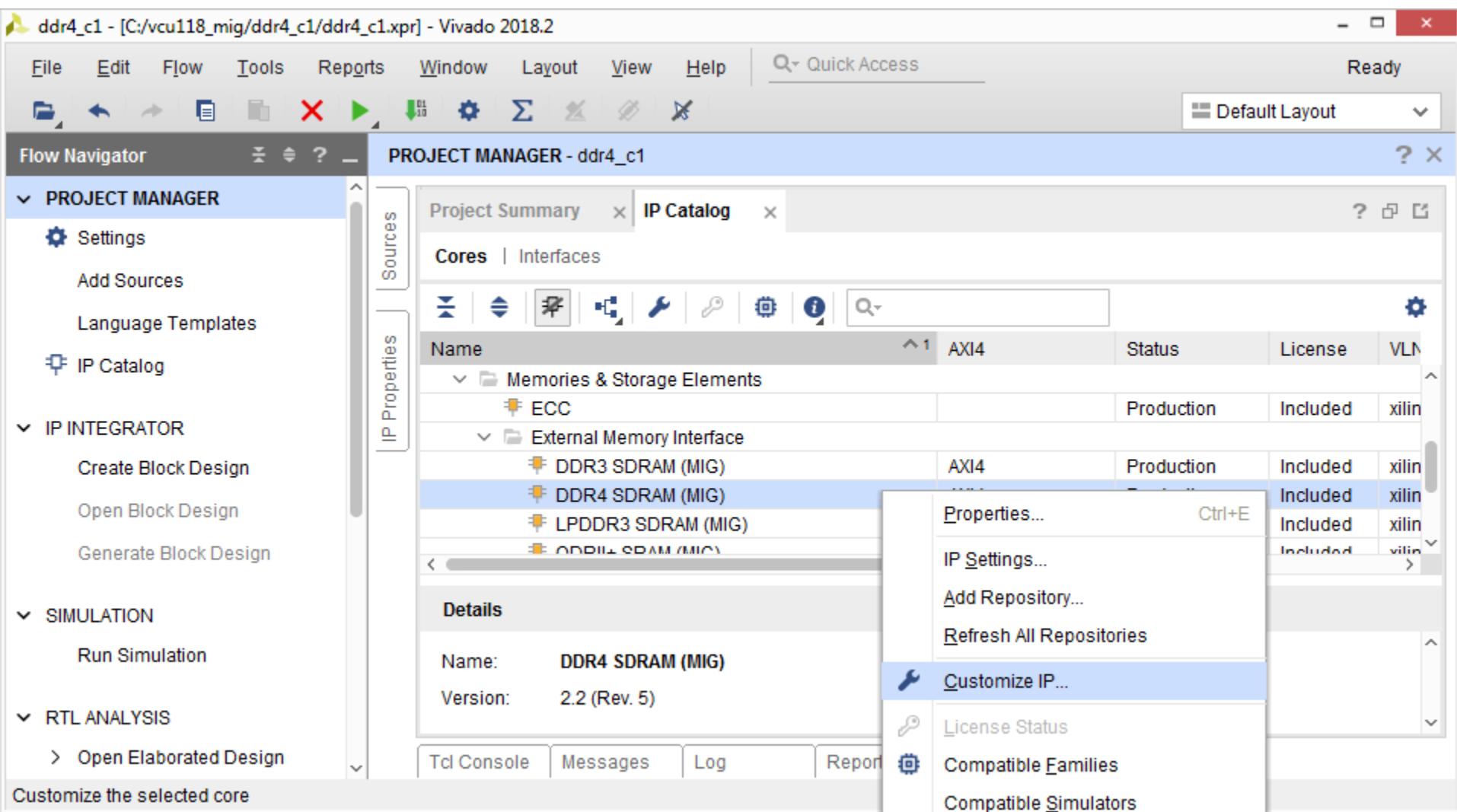
Note: Presentation applies to the VCU118

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Generate MIG DDR4 C1 Example Design

- > Right click on DDR4 SDRAM (MIG)

- » Select Customize IP



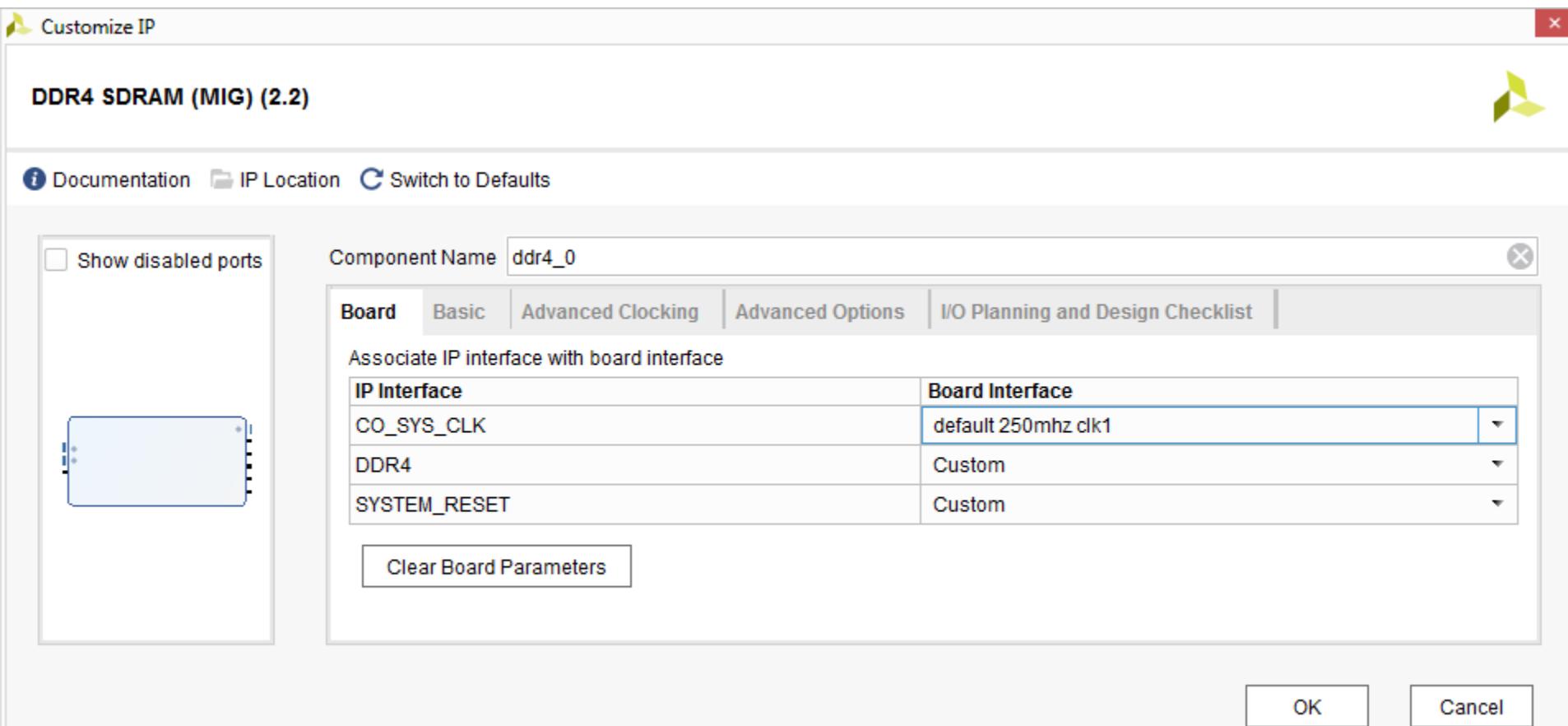
Note: Presentation applies to the VCU118

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Generate MIG DDR4 C1 Example Design

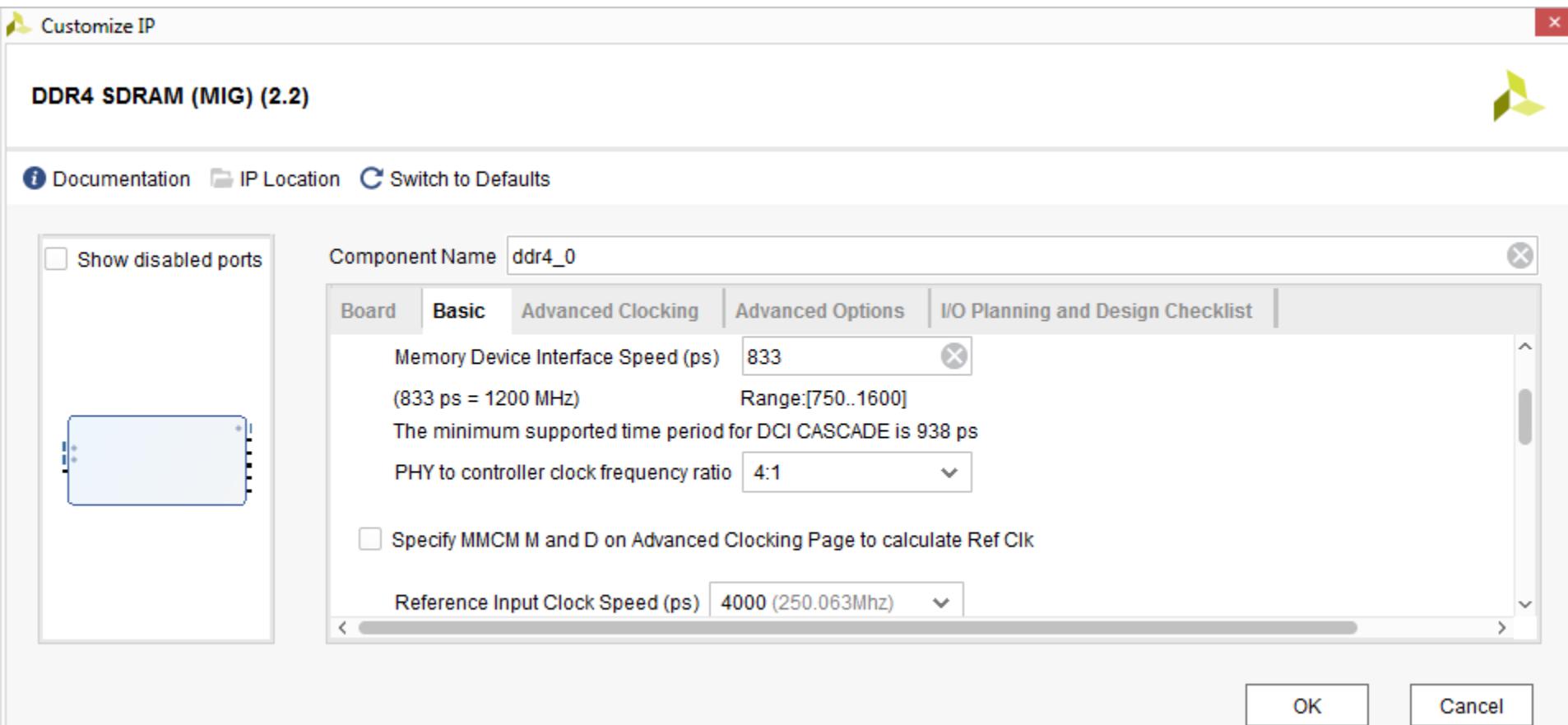
> Under the Board tab, set the DDR4 interfaces

- » Set CO_SYS_CLK to default 250mhz clk1
- » Set DDR4 to Custom
- » Set SYSTEM_RESET to Custom



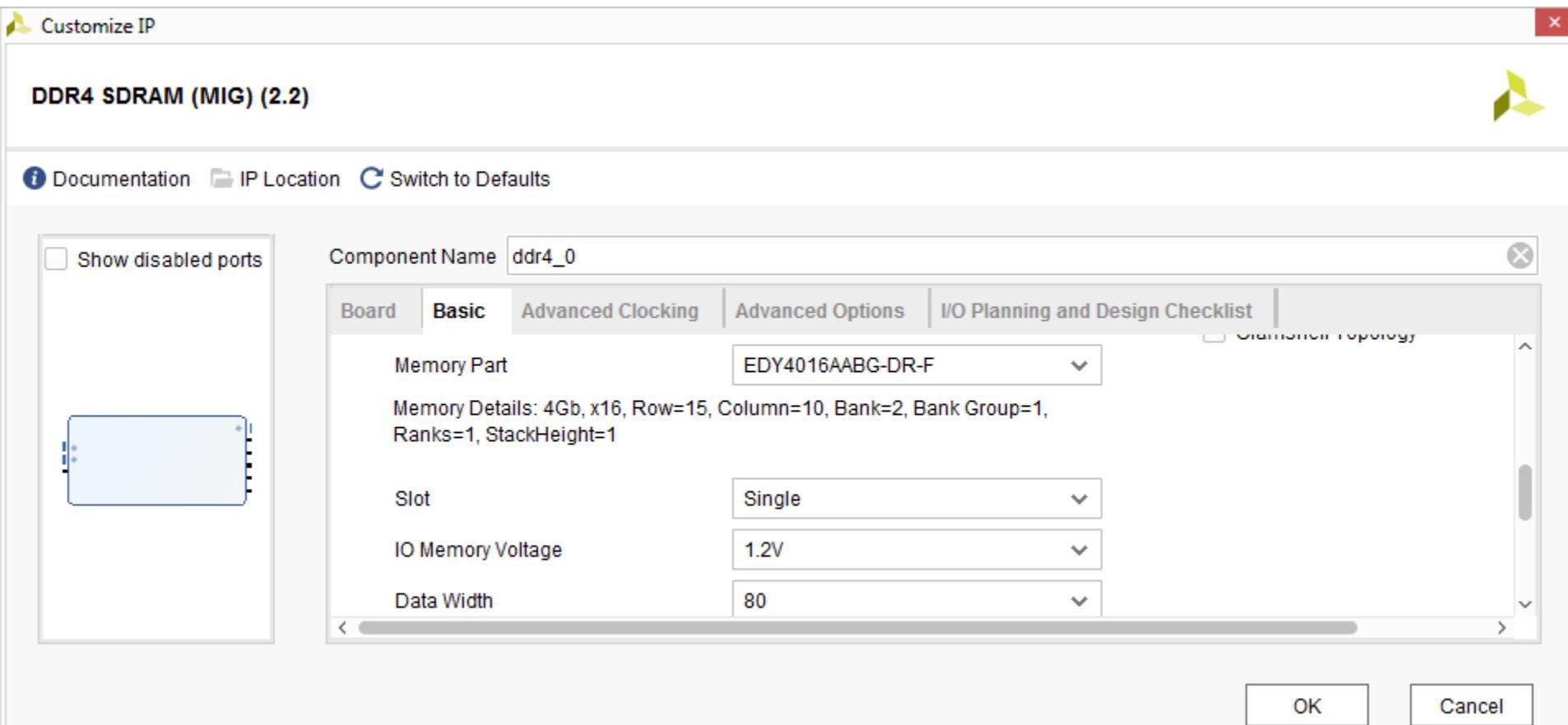
Generate MIG DDR4 C1 Example Design

- > Set the Clock period to 833 for 2400 Mb/s operation.
- > Set the Input Clock to 4000 ps for 250 MHz
- > Scroll down



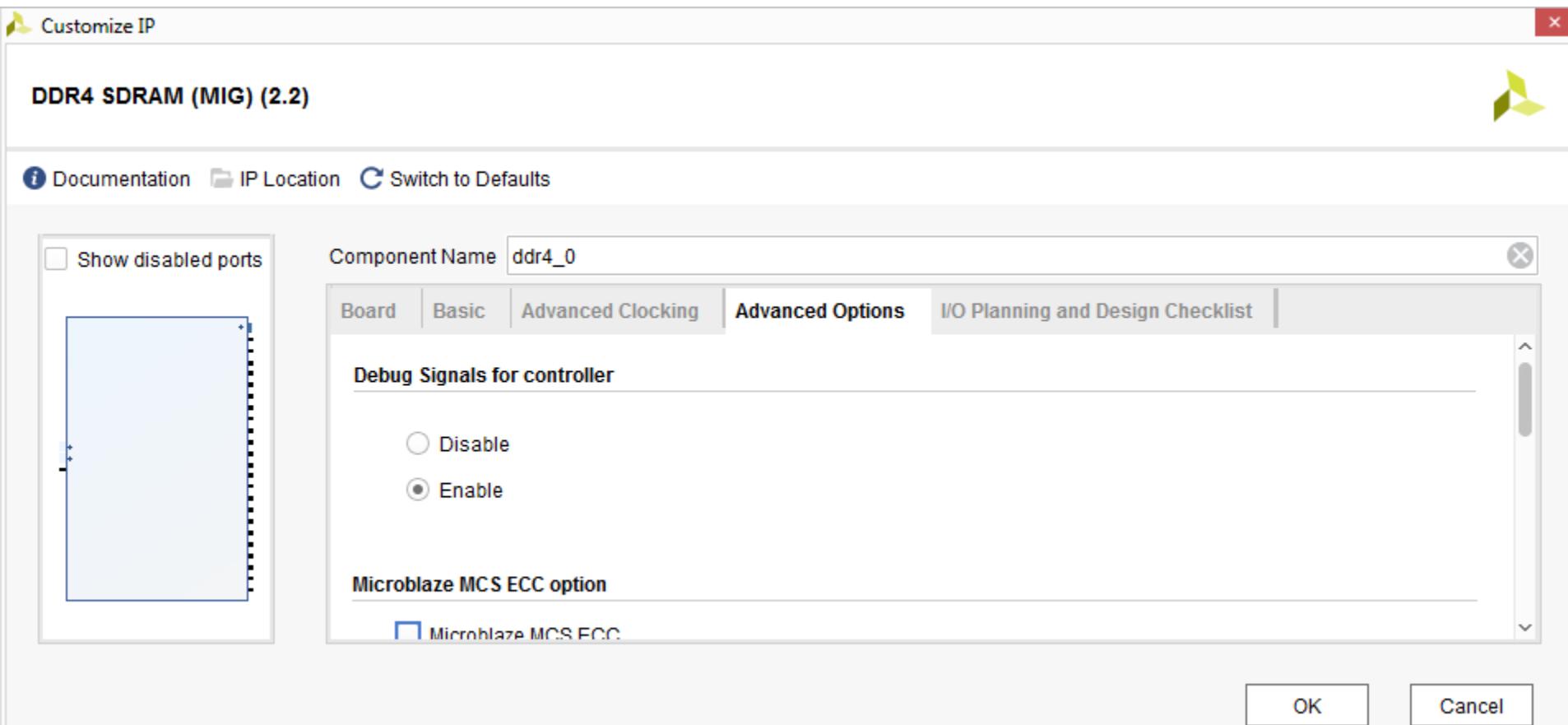
Generate MIG DDR4 C1 Example Design

- > Set the part to EDY4016AABG-DR-F
 - » Note: this part is equivalent to the MT40A256M16GE-083E used on the VCU118
- > Set the Data Width to 80 and click the Advanced Options tab



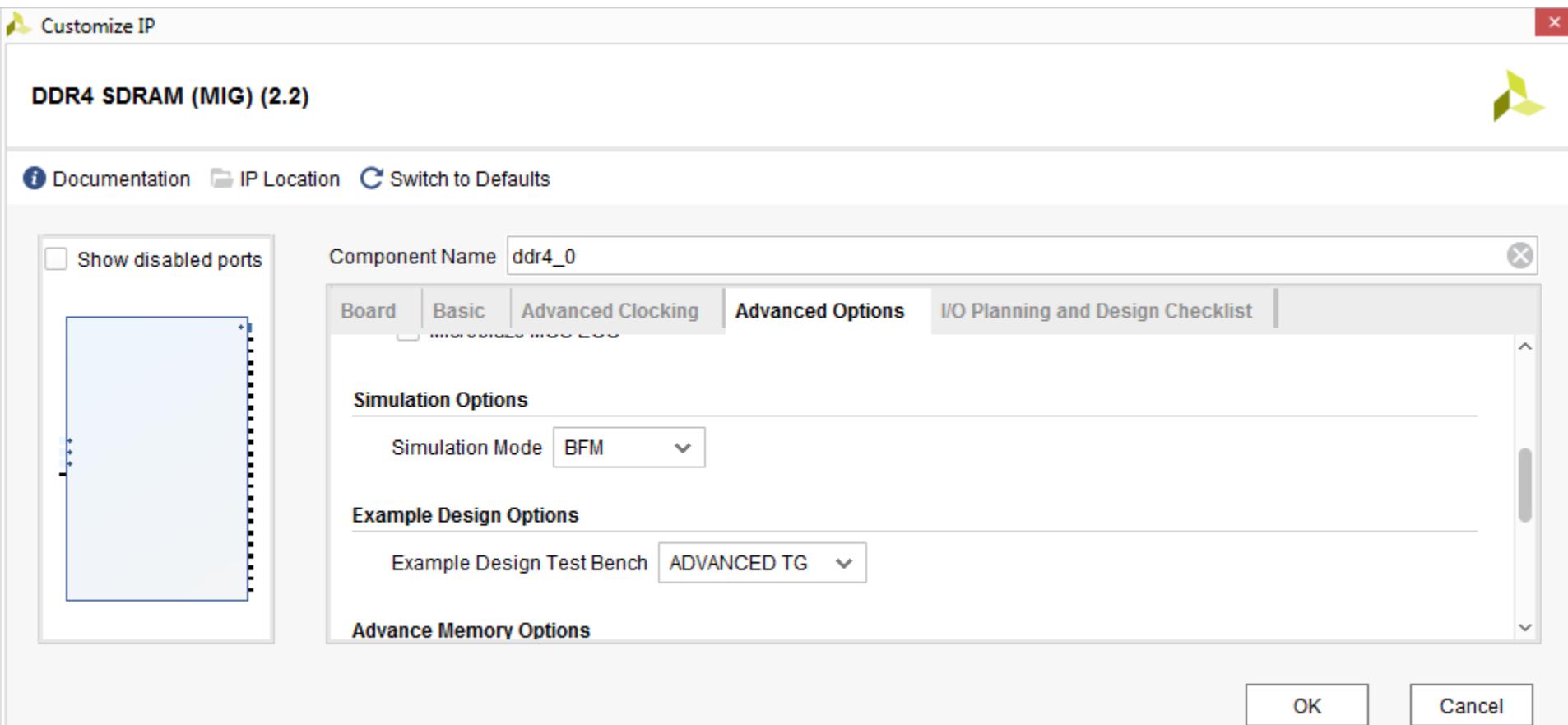
Generate MIG DDR4 C1 Example Design

- > Set the Debug Signals to Enable
- > Scroll down



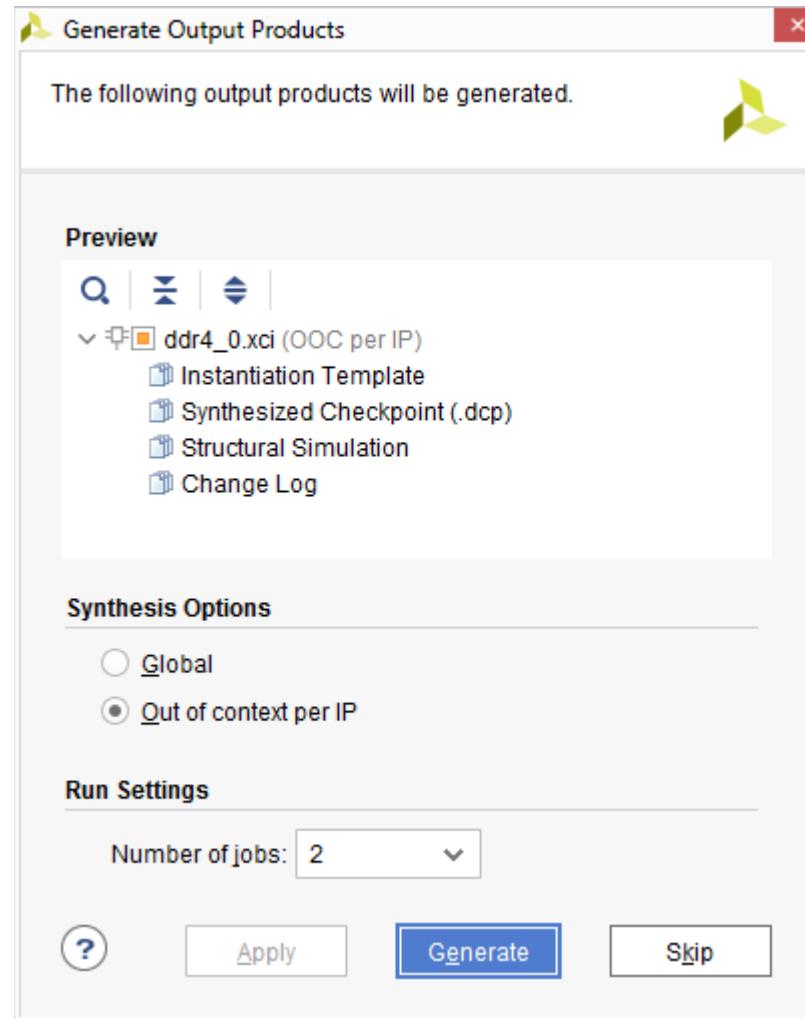
Generate MIG DDR4 C1 Example Design

- > Set the Example Design Test Bench to ADVANCED TG
- > Click OK



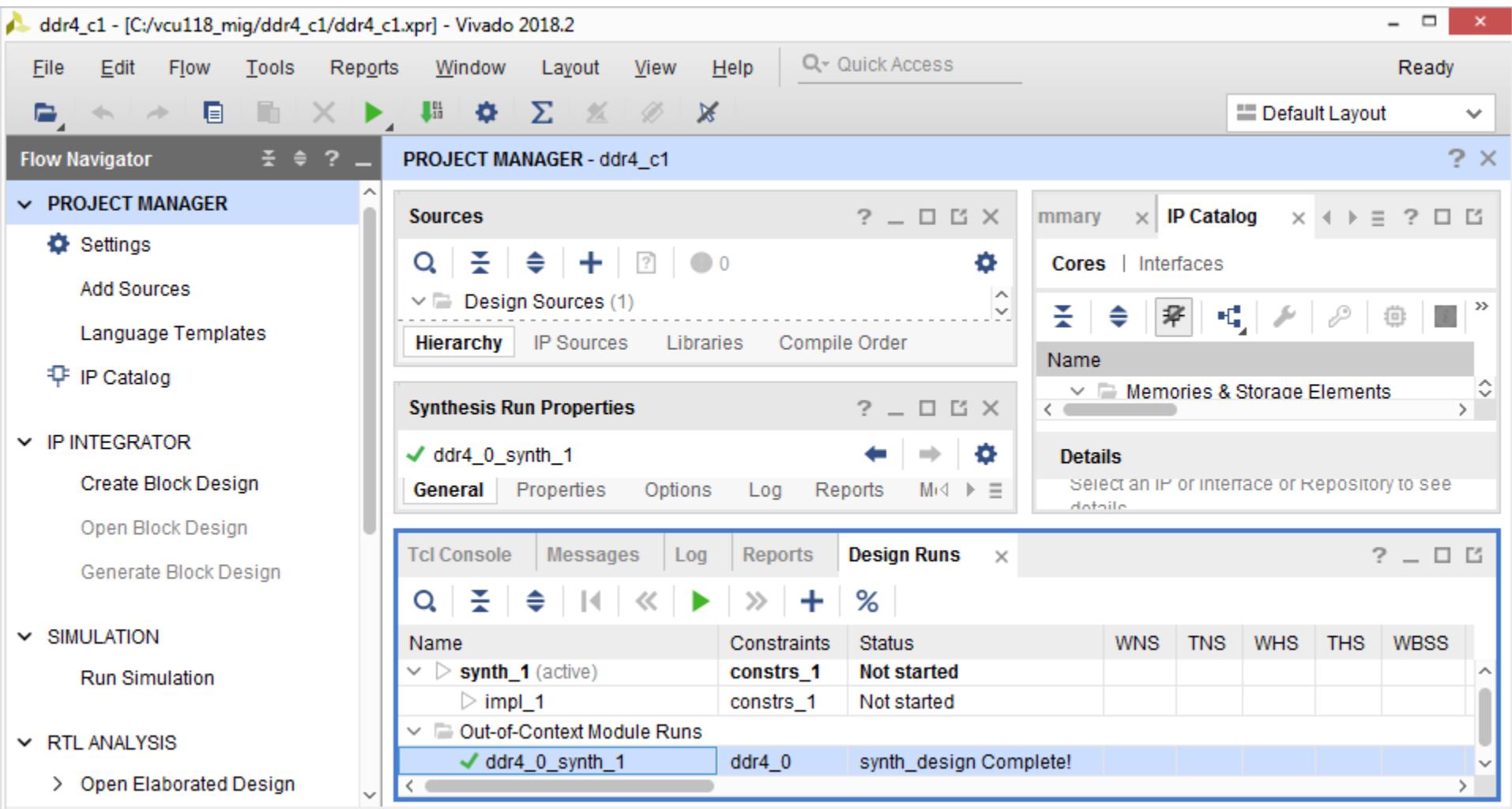
Generate MIG DDR4 C1 Example Design

> Click Generate



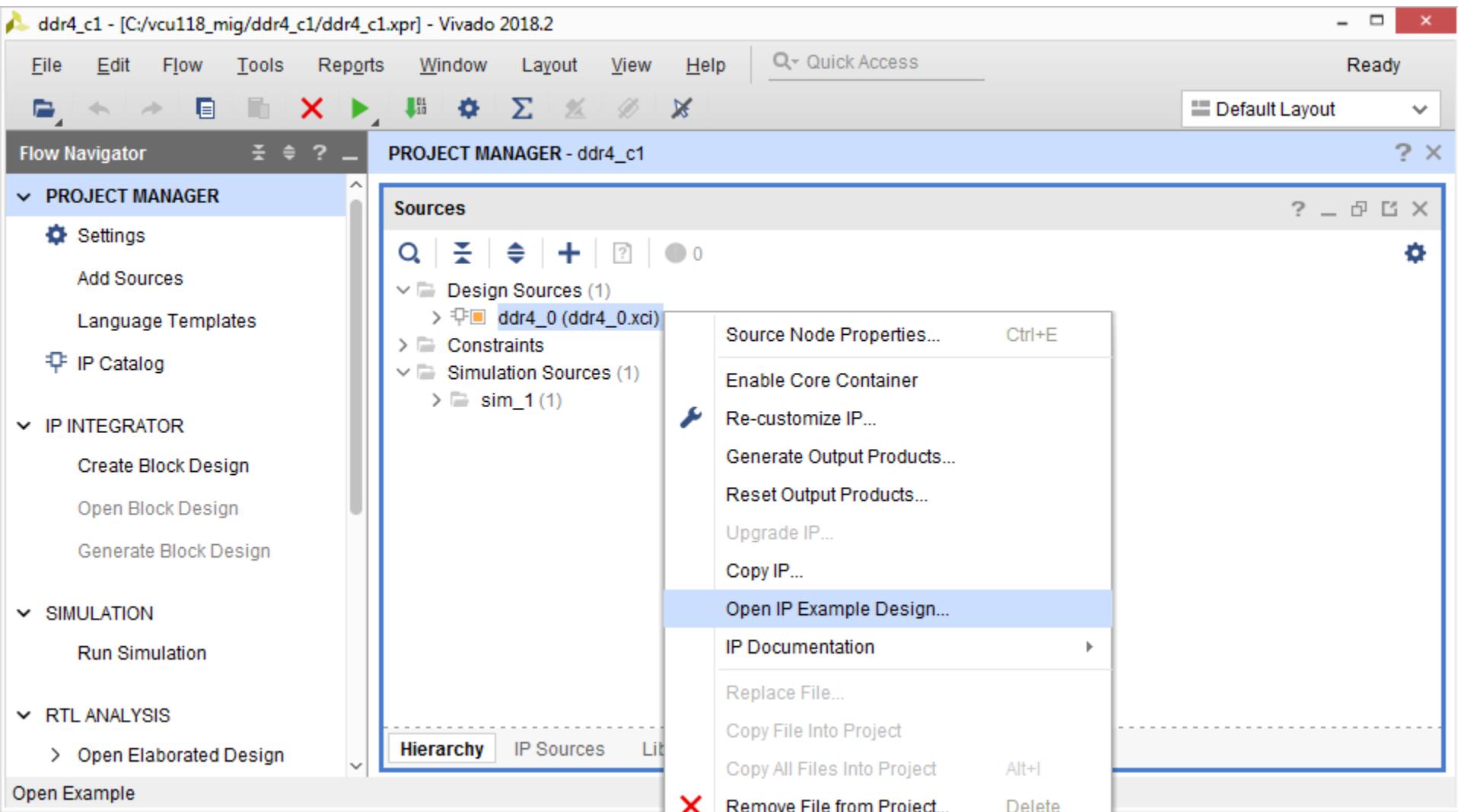
Generate MIG DDR4 C1 Example Design

- > Wait until checkmark appears on ddr4_0_synth_1



Compile Example Design

- > Right click on ddr4_0 and select Open IP Example Design...

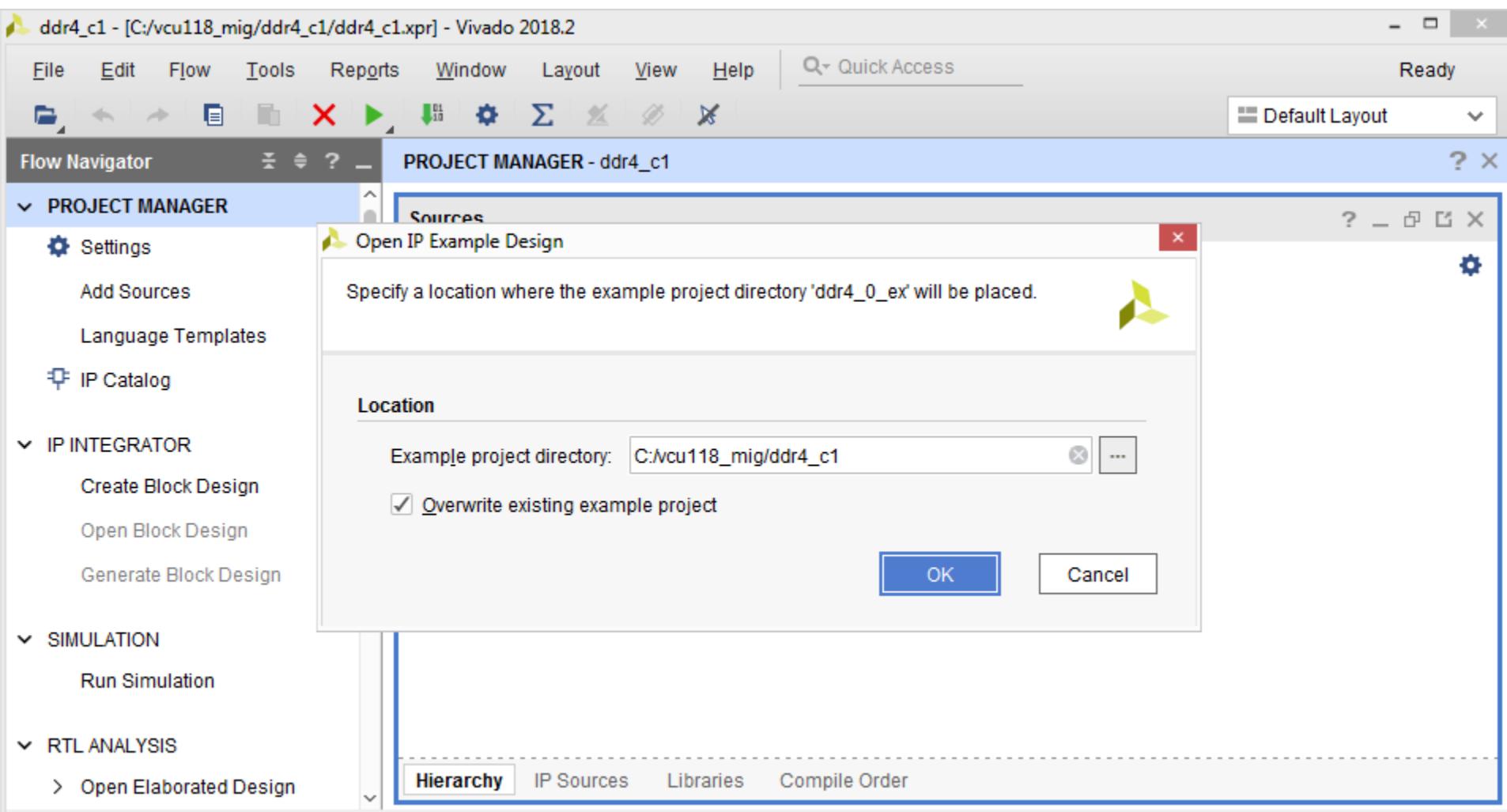


Note: Presentation applies to the VCU118

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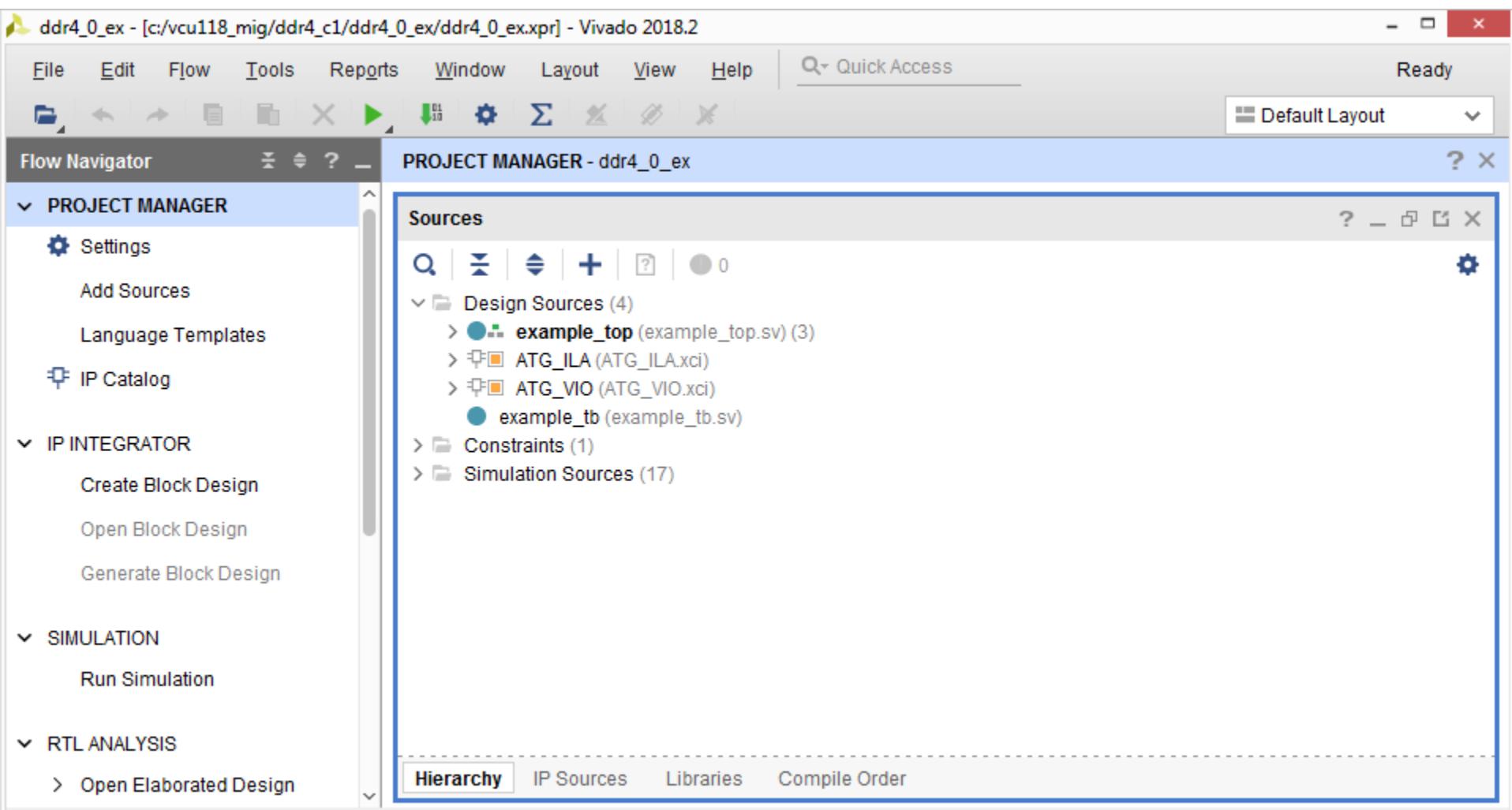
Compile Example Design

- > Set the location to C:/vcu118_mig/ddr4_c1 and click OK



Compile Example Design

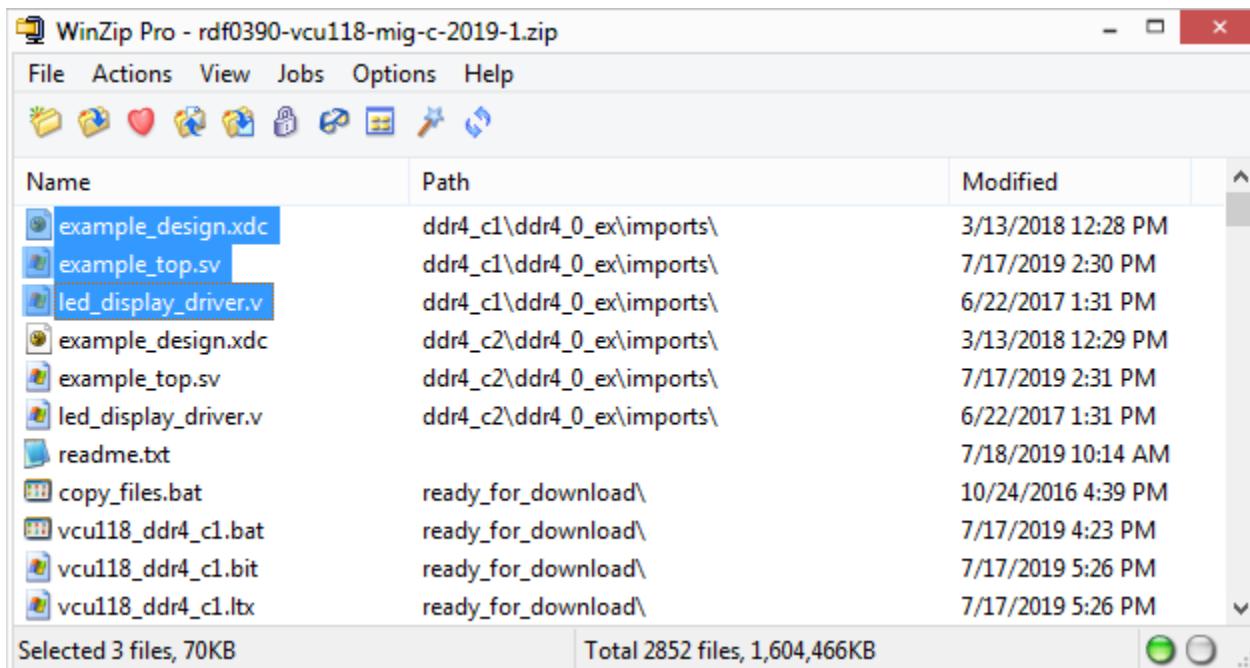
- > A new project is created under <design path>/



Note: The original project window can be closed

Modifications to Example Design

- > From the **RDF0390 - VCU118 MIG Design Files (2019.1 C) ZIP file**
 - » Extract the ddr4_c1 files, example_design.xdc, example_top.sv, and led_display_driver.v
 - » Overwrite these three existing files in your ddr4_c1 MIG design
 - » Do this after creating the Example Design; changes only affect the Example Design



Modifications to Example Design

> Modifications to the example design

- » Added RTL and XDC modifications to drive LEDs
- » The following commands will add the led_display_driver.v and create the required VIO IP
- » From the Tcl Console, run these commands:

```
add_files -norecurse
```

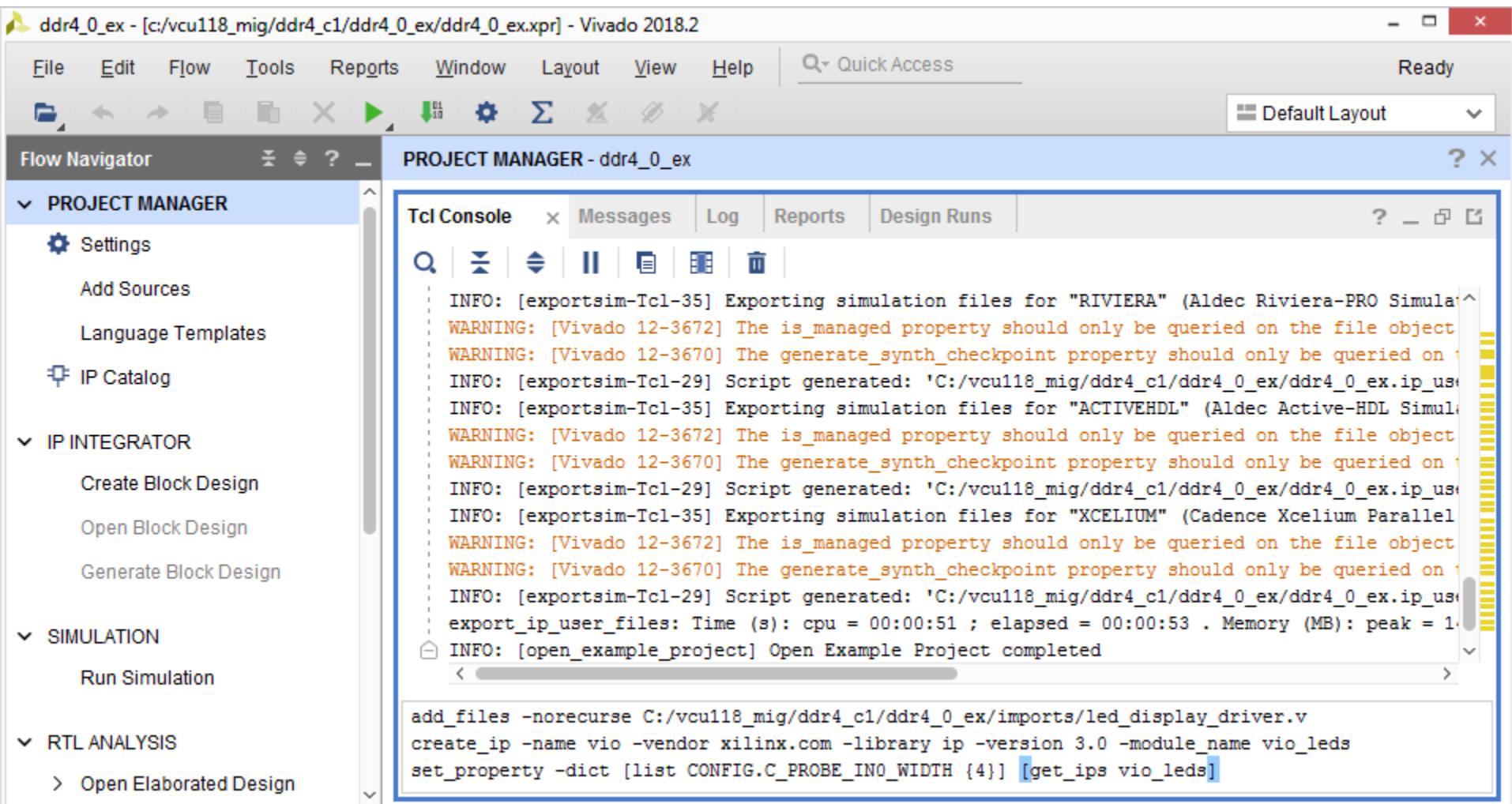
```
C:/vcu118_mig/ddr4_c1/ddr4_0_ex/imports/led_display_driver.v
```

```
create_ip -name vio -vendor xilinx.com -library ip -version 3.0 -module_name  
vio_leds
```

```
set_property -dict [list CONFIG.C_PROBE_IN0_WIDTH {4}] [get_ips vio_leds]
```

Modifications to Example Design

- > Press enter after entering Tcl commands



Modifications to Example Design

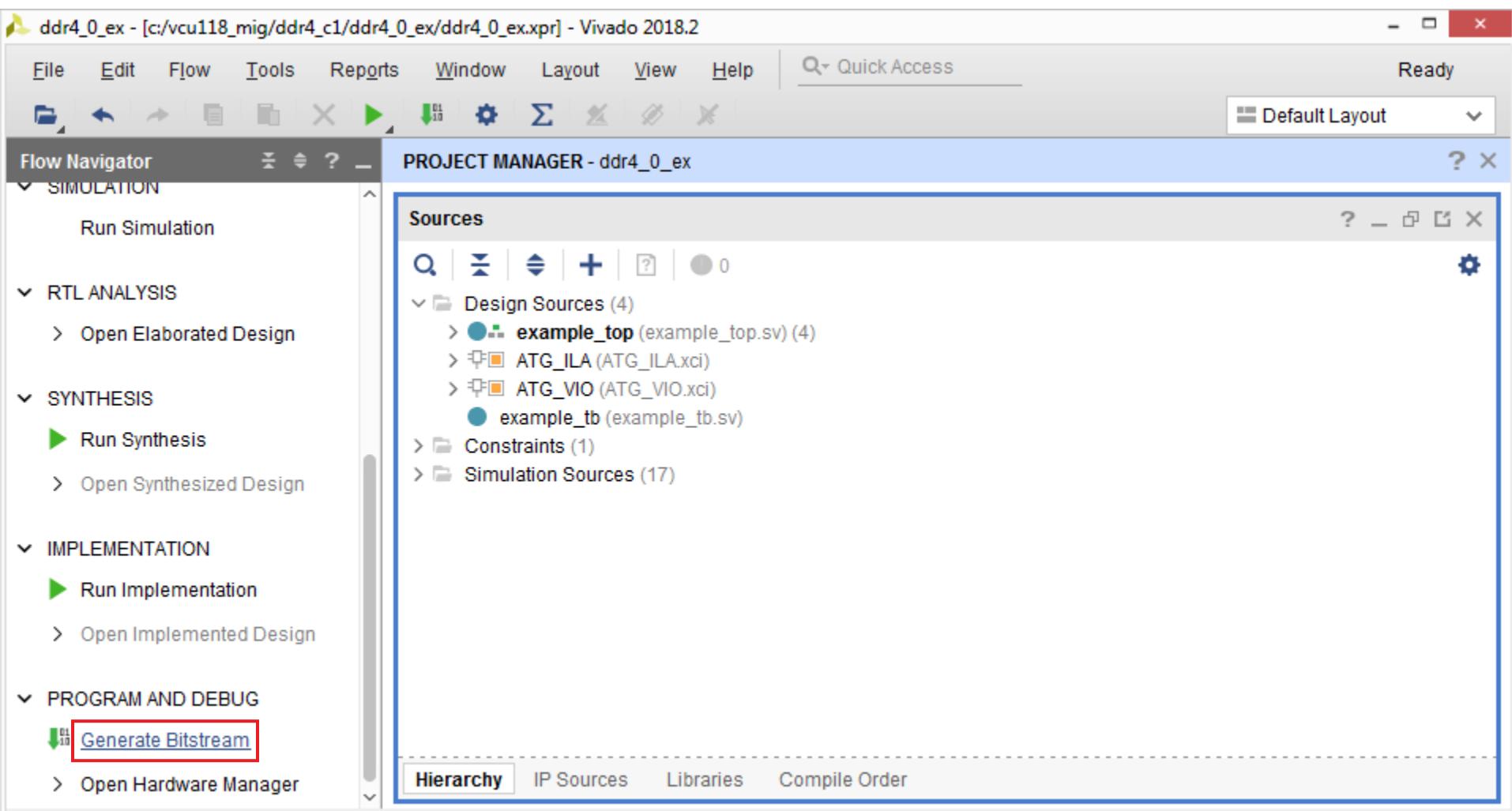
- > Tcl commands completed successfully

The screenshot shows the Vivado 2018.2 interface with the project "ddr4_0_ex" open. The left sidebar contains the Project Manager, IP Integrator, Simulation, and RTL Analysis sections. The main area is the PROJECT MANAGER - ddr4_0_ex window, which includes tabs for Tcl Console, Messages, Log, Reports, and Design Runs. The Tcl Console tab is active, displaying the following command history:

```
INFO: [exportsim-Tcl-29] Script generated: 'C:/vcu118_mig/ddr4_c1/ddr4_0_ex/ddr4_0_ex.ip_user_files.tcl'
INFO: [exportsim-Tcl-35] Exporting simulation files for "XCELIUM" (Cadence Xcelium Parallel)
WARNING: [Vivado 12-3672] The is_managed property should only be queried on the file object
WARNING: [Vivado 12-3670] The generate_synth_checkpoint property should only be queried on the ip object
INFO: [exportsim-Tcl-29] Script generated: 'C:/vcu118_mig/ddr4_c1/ddr4_0_ex/ddr4_0_ex.ip_user_files.tcl'
export_ip_user_files: Time (s): cpu = 00:00:51 ; elapsed = 00:00:53 . Memory (MB): peak = 1000
INFO: [open_example_project] Open Example Project completed
update_compile_order -fileset sources_1
add_files -norecurse C:/vcu118_mig/ddr4_c1/ddr4_0_ex/imports/led_display_driver.v
C:/vcu118_mig/ddr4_c1/ddr4_0_ex/imports/led_display_driver.v
create_ip -name vio -vendor xilinx.com -library ip -version 3.0 -module_name vio_leds
c:/vcu118_mig/ddr4_c1/ddr4_0_ex/ddr4_0_ex.srcs/sources_1/ip/vio_leds/vio_leds.xci
set_property -dict [list CONFIG.C_PROBE_IN0_WIDTH {4}] [get_ips vio_leds]
0
update_compile_order -fileset sources_1
```

Compile Example Design

- > Click on Generate Bitstream



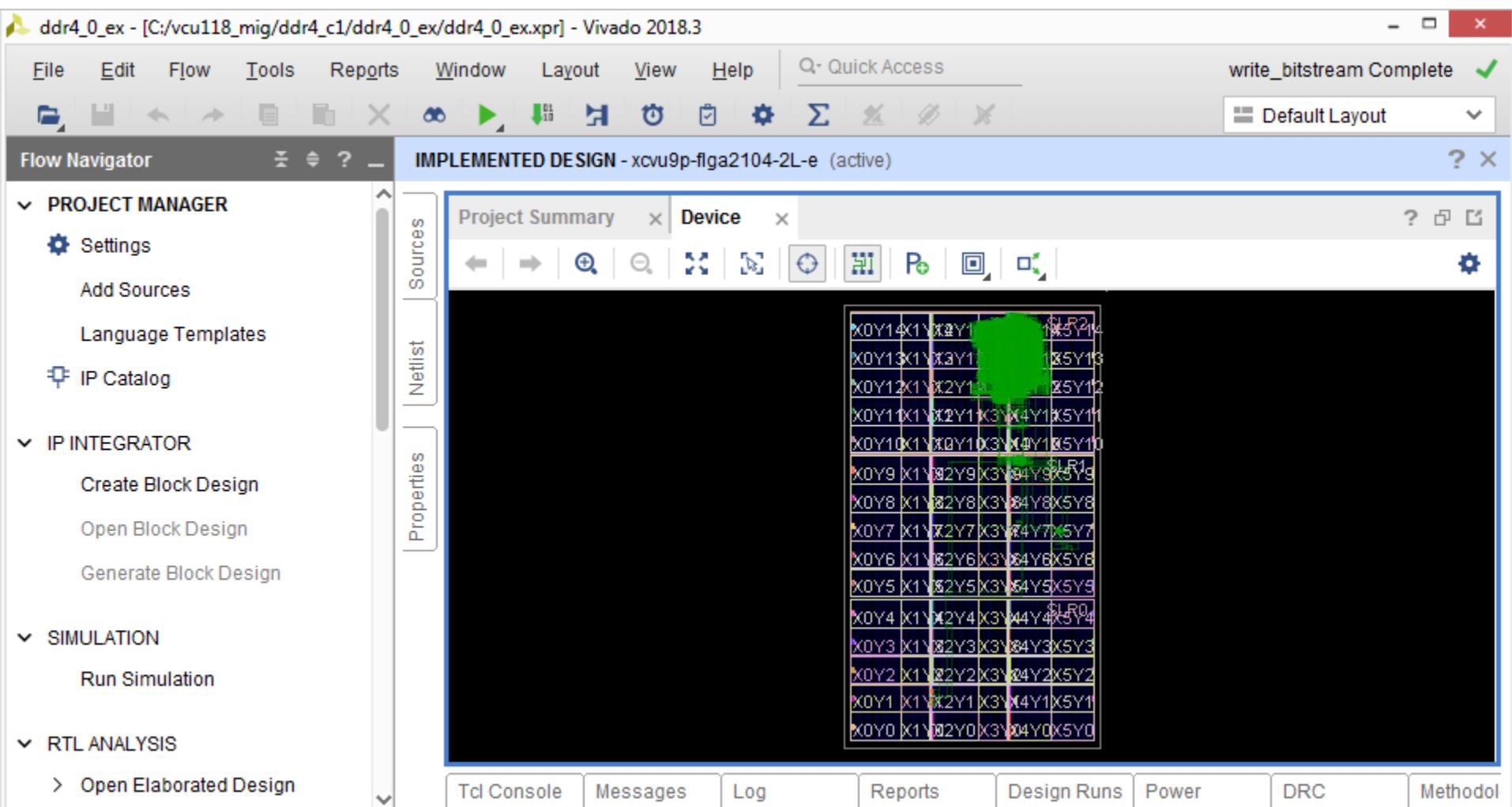
Generate a programming file after implementation

Note: Presentation applies to the VCU118

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Compile Example Design

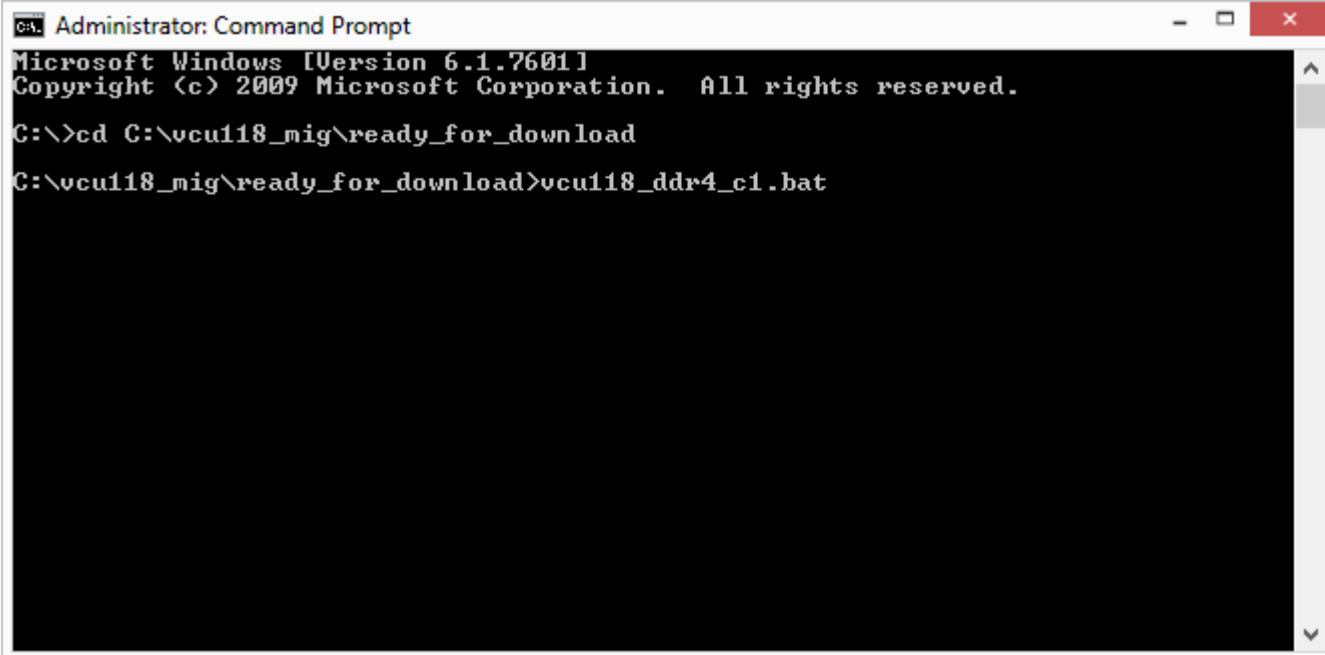
- > Open and view the Implemented Design



Run MIG Example Design

- > From a Command Prompt, type:

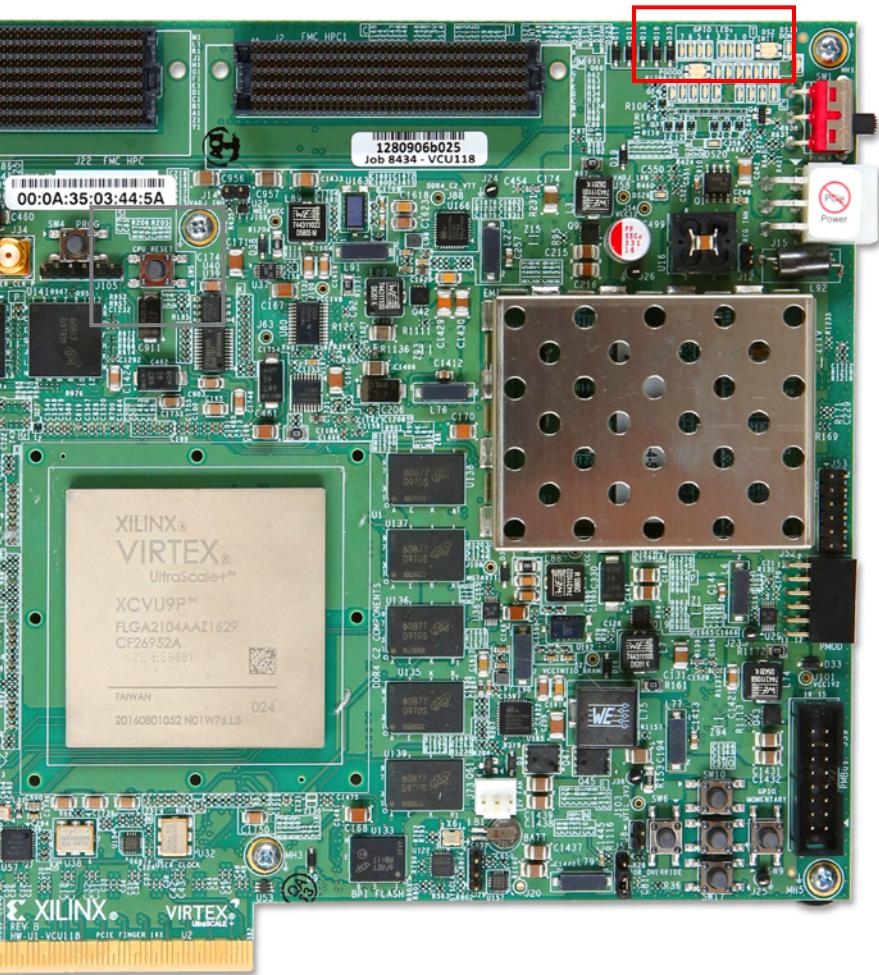
```
cd C:\vcu118_mig\ready_for_download  
vcu118_ddr4_c1.bat
```



The screenshot shows a Windows Command Prompt window titled "Administrator: Command Prompt". The window is running on Microsoft Windows [Version 6.1.7601]. It displays the following command sequence:

```
Microsoft Windows [Version 6.1.7601]  
Copyright <c> 2009 Microsoft Corporation. All rights reserved.  
  
C:>cd C:\vcu118_mig\ready_for_download  
C:\vcu118_mig\ready_for_download>vcu118_ddr4_c1.bat
```

Run MIG Example Design



- > After bitstream loads, LED 0 (right most LED) will be lit, and LED1 will be blinking
- > LED 3 will light and stay on
 - » This indicates Calibration has completed
- > If an error occurs, LED 0 will go out and LED 2 will light
 - » The “CPU_RESET” button, SW5, is the reset

Generate MIG DDR4 C2 Example Design

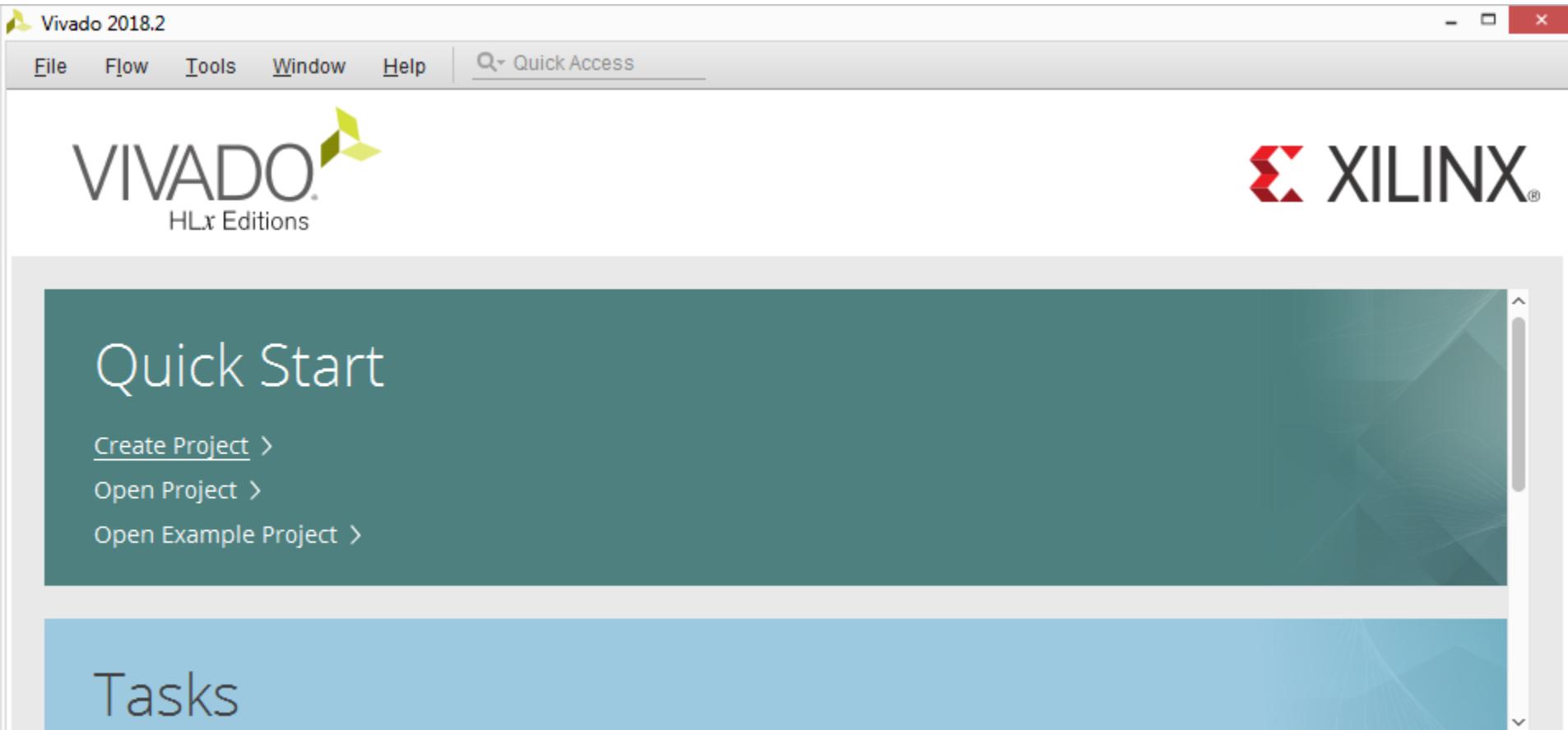


Generate MIG DDR4 C2 Example Design

> Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2019.1 → Vivado

> Select Create Project



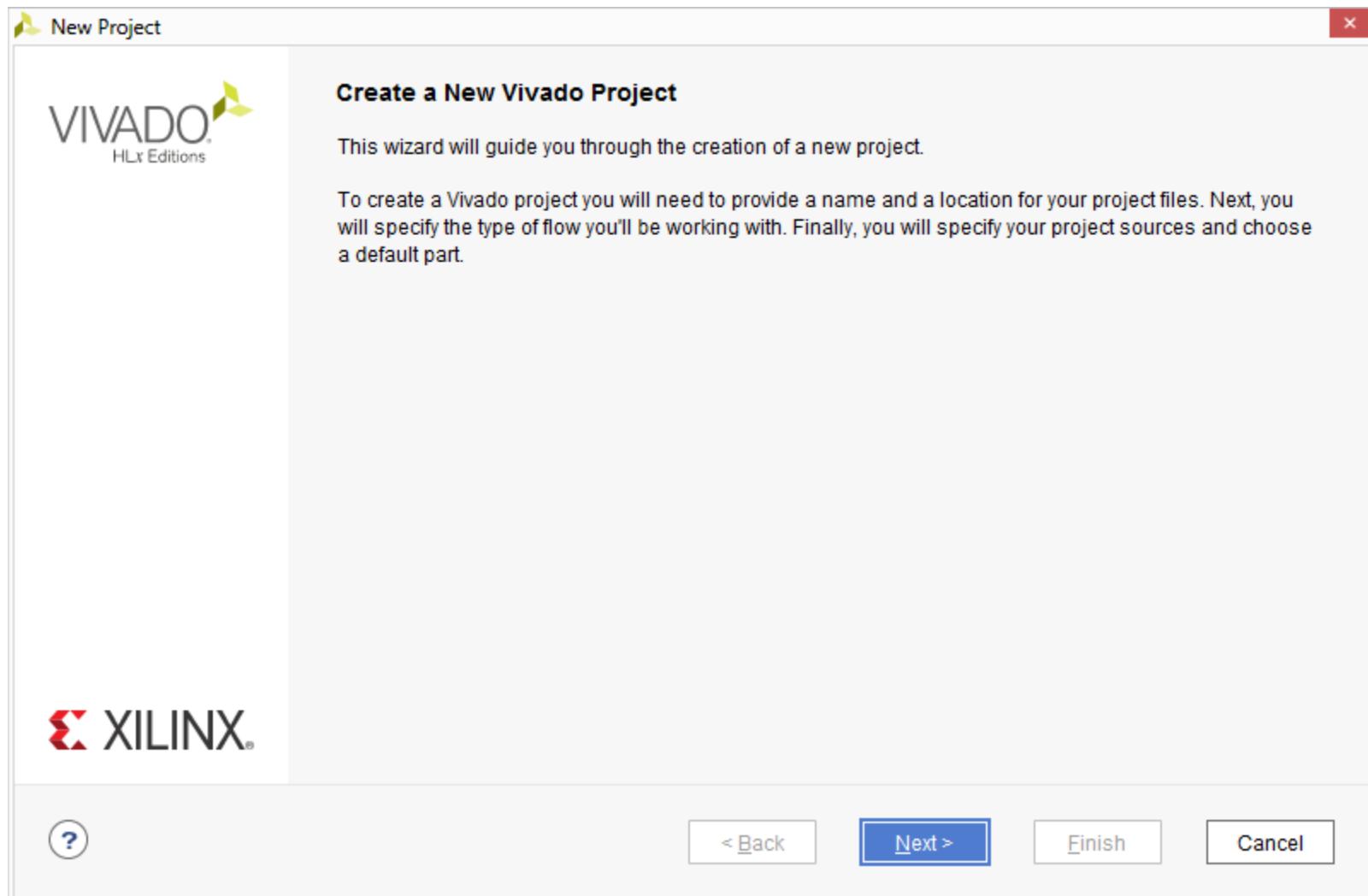
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Note: Presentation applies to the VCU118

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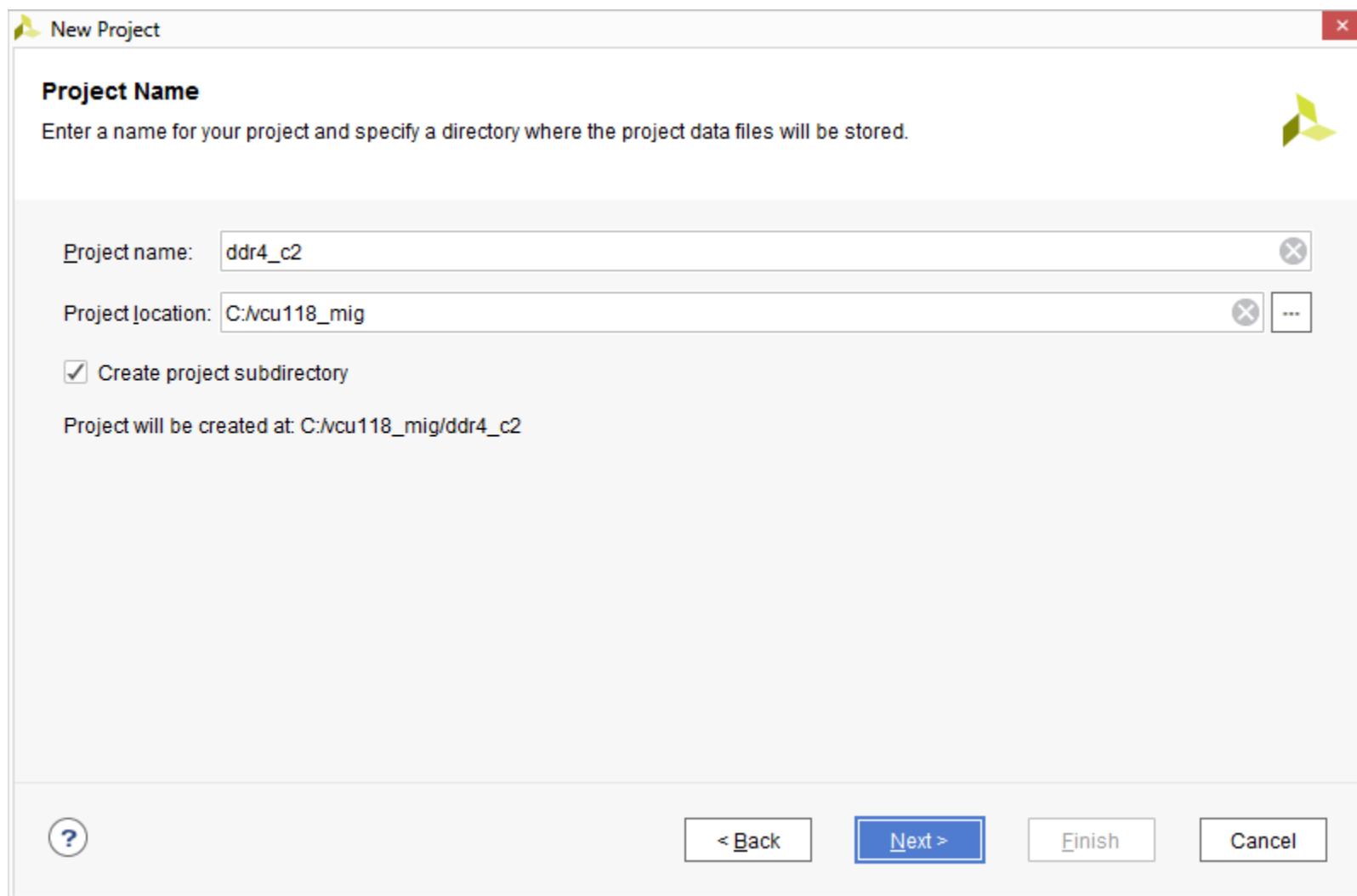
Generate MIG DDR4 C2 Example Design

> Click Next



Generate MIG DDR4 C2 Example Design

- > Set the Project name to ddr4_c2 and location to C:/vcu118_mig
 - » Check Create project subdirectory



Note: Vivado generally requires forward slashes in paths

Generate MIG DDR4 C2 Example Design

> Select RTL Project

» Select Do not specify sources at this time

New Project X

Project Type
Specify the type of project to create.



RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
 Do not specify sources at this time

Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.
 Do not specify sources at this time

I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.

Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.

Example Project
Create a new Vivado project from a predefined template.

? < Back Next > Finish Cancel

Generate MIG DDR4 C2 Example Design

- > Under Boards, select the VCU118 Rev 2.0

New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Parts | Boards

Reset All Filters

Vendor: All Name: All

Search:

Display Name	Preview	Vendor	File V
Virtex UltraScale+ VCU118 Evaluation Platform		xilinx.com	2.0
Virtex UltraScale+ VCU1525 Acceleration Development Board		xilinx.com	1.1

< >

?

< Back

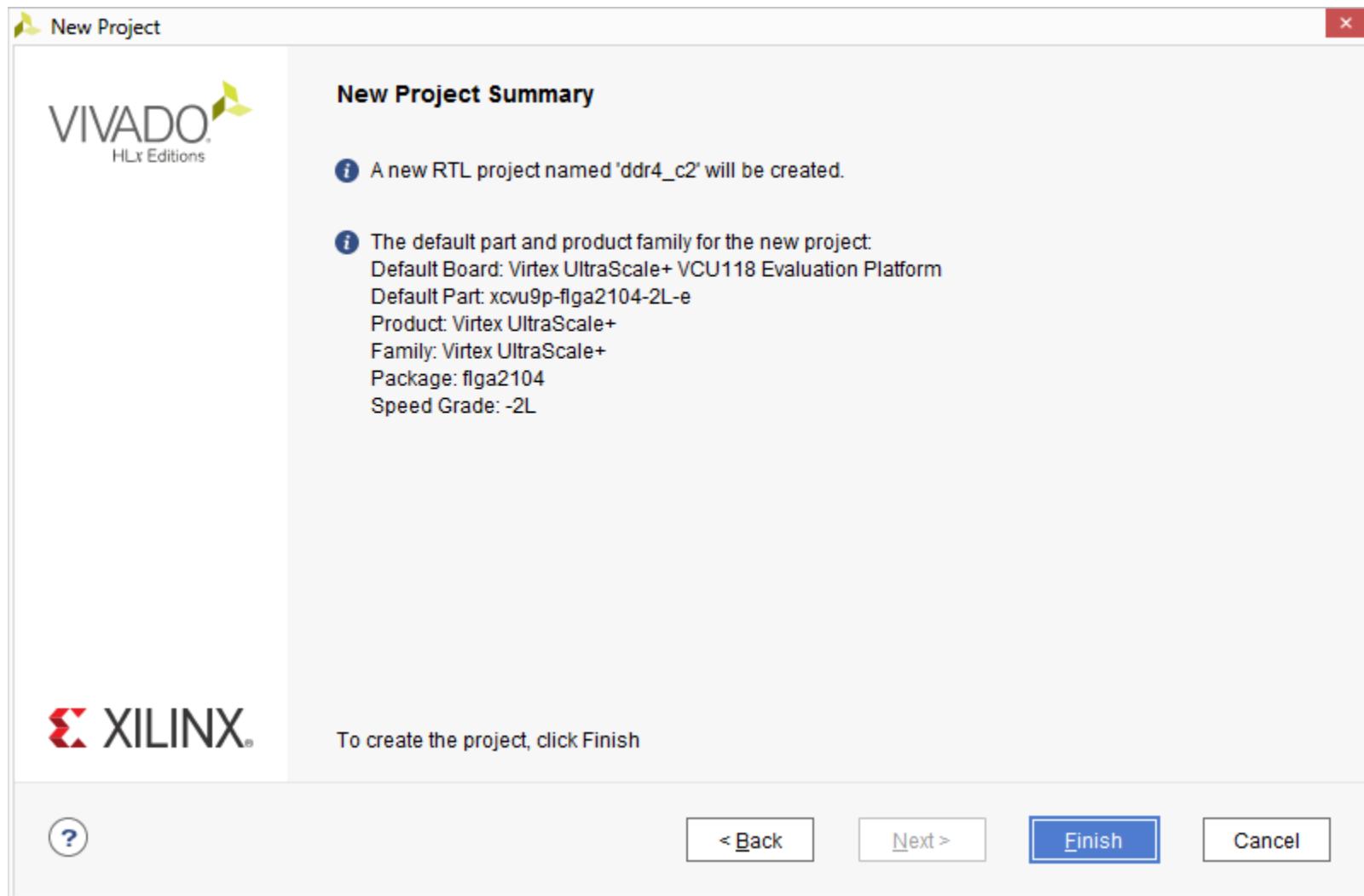
Next >

Finish

Cancel

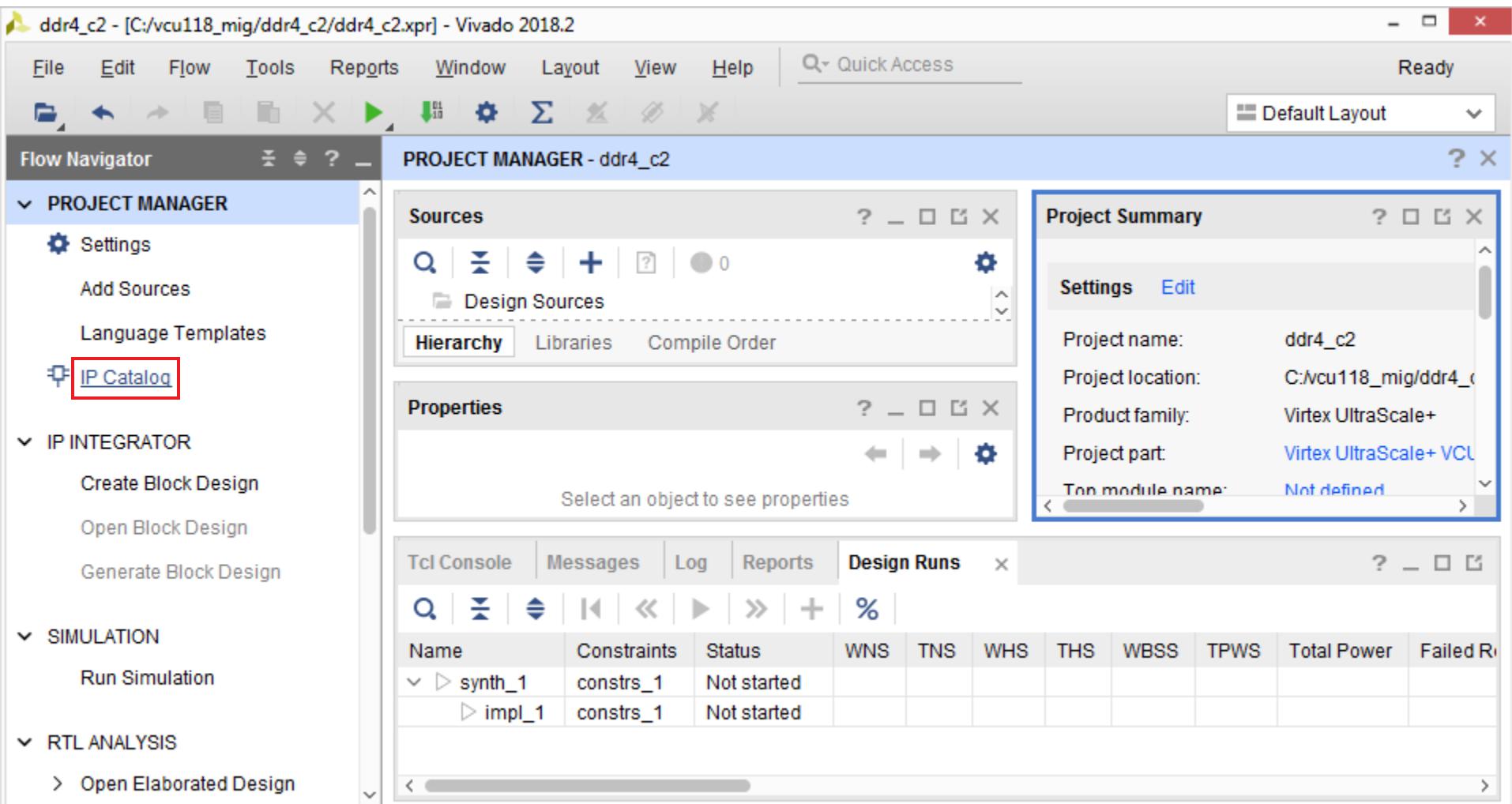
Generate MIG DDR4 C2 Example Design

> Click Finish



Generate MIG DDR4 C2 Example Design

> Click on IP Catalog



Generate MIG DDR4 C2 Example Design

> Select DDR4 SDRAM (MIG), v2.2

The screenshot shows the Vivado 2018.2 interface with the project "ddr4_c2" open. The left sidebar contains the "PROJECT MANAGER" section with options like Settings, Add Sources, Language Templates, and IP Catalog. The "IP Catalog" option is selected. The main area displays the "IP Catalog" window with tabs for Project Summary and IP Catalog. The IP Catalog tab shows a list of cores and interfaces. Under "Memories & Storage Elements", the "DDR4 SDRAM (MIG)" item is selected and highlighted with a blue border. Below the table, the "Details" section shows the selected item's name and version.

Name	Type	Status	License	VLM
AXI4	Production	Included	xilinx	
ECC	Production	Included	xilinx	
External Memory Interface	Production	Included	xilinx	
DDR3 SDRAM (MIG)	AXI4	Production	Included	xilinx
DDR4 SDRAM (MIG)	AXI4	Production	Included	xilinx
LPDDR3 SDRAM (MIG)	Production	Included	xilinx	
DDRII SDRAM (MIG)	Production	Included	xilinx	

Details:

- Name: DDR4 SDRAM (MIG)
- Version: 2.2 (Rev. 5)

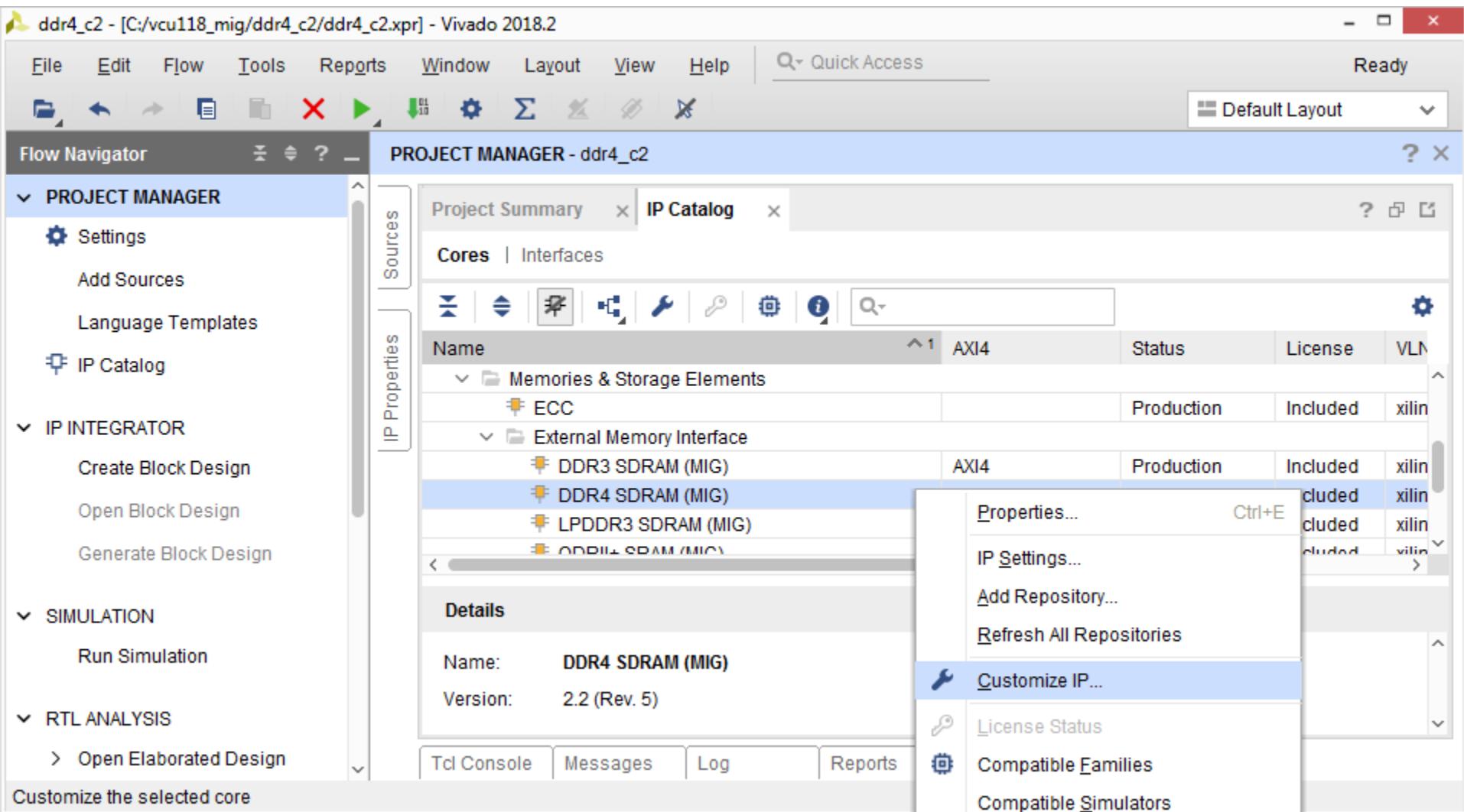
Note: Presentation applies to the VCU118

 XILINX

Generate MIG DDR4 C2 Example Design

- > Right click on DDR4 SDRAM (MIG)

- » Select Customize IP

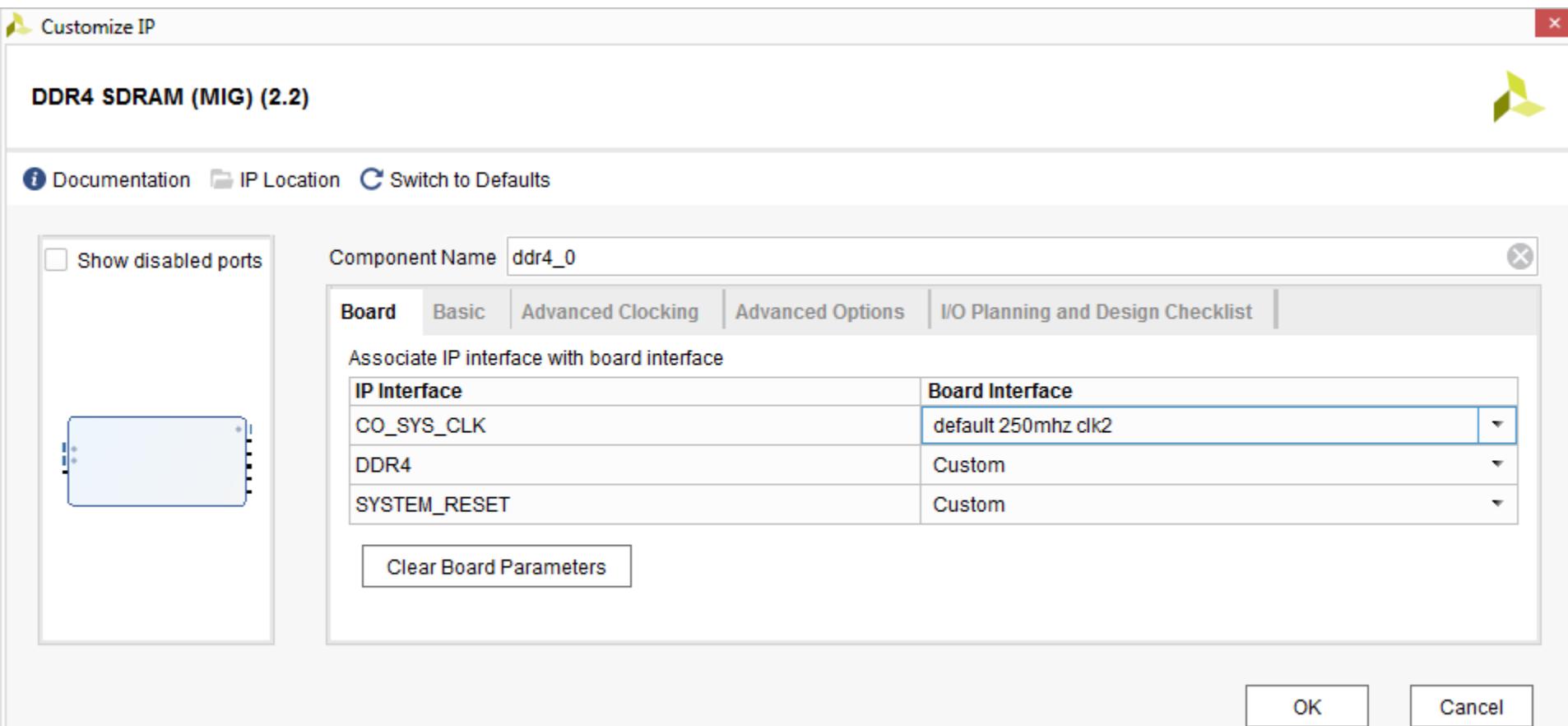


Note: Presentation applies to the VCU118

Generate MIG DDR4 C2 Example Design

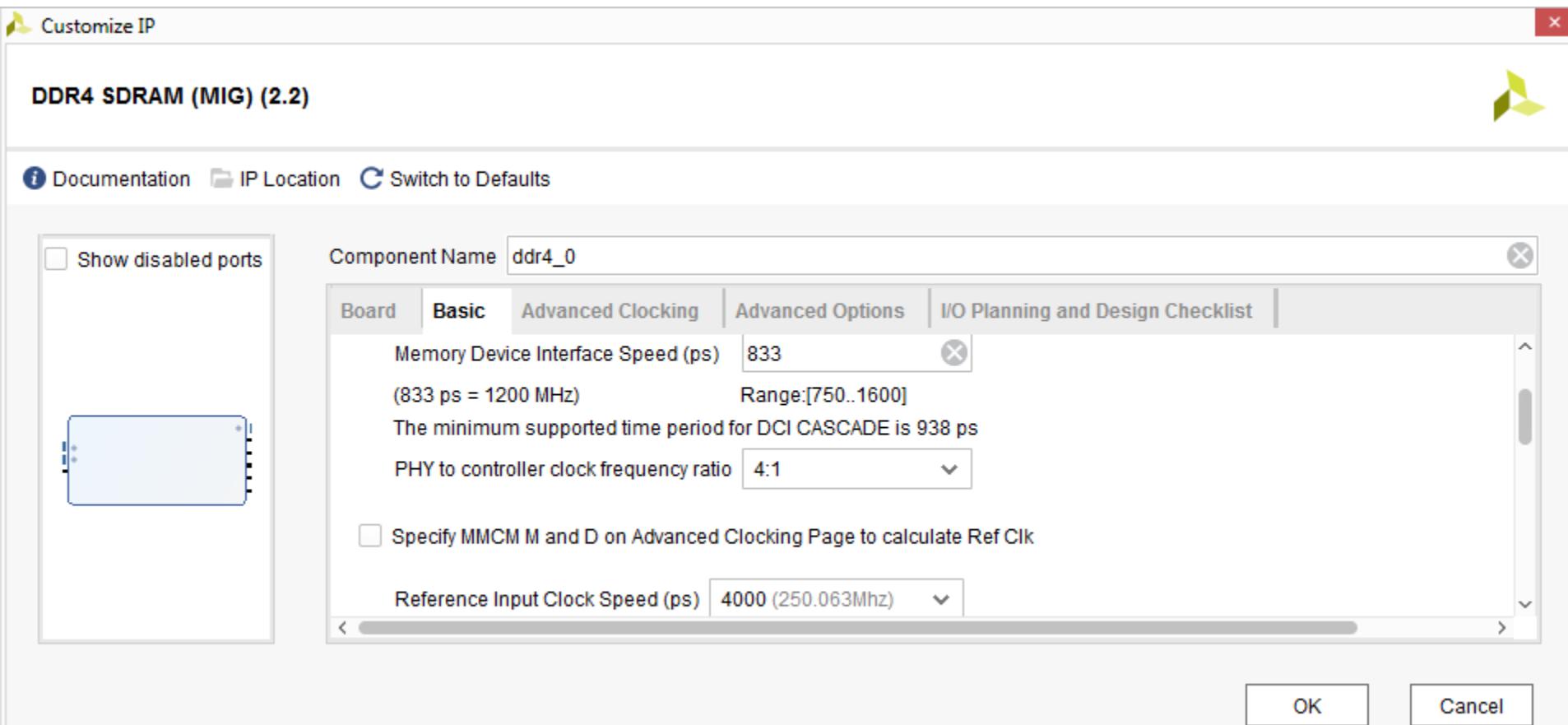
> Under the Board tab, set the DDR4 interfaces

- » Set CO_SYS_CLK to default 250mhz clk2
- » Set CO_DDR4 to Custom
- » Set SYSTEM_RESET to Custom



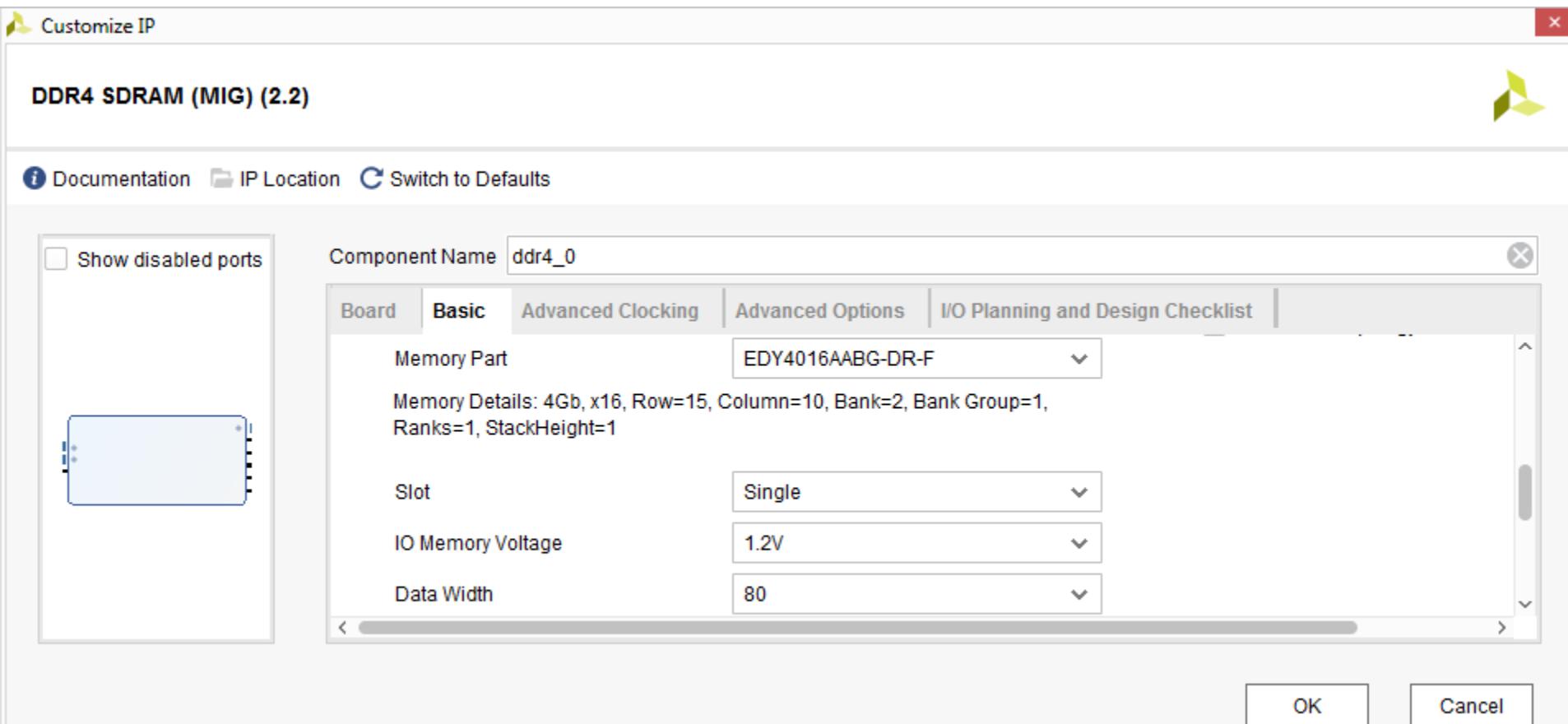
Generate MIG DDR4 C2 Example Design

- > Set Clock period to 833 for 2400 Mb/s operation.
- > Set the Input Clock to 4000 ps for 250 MHz
- > Scroll down



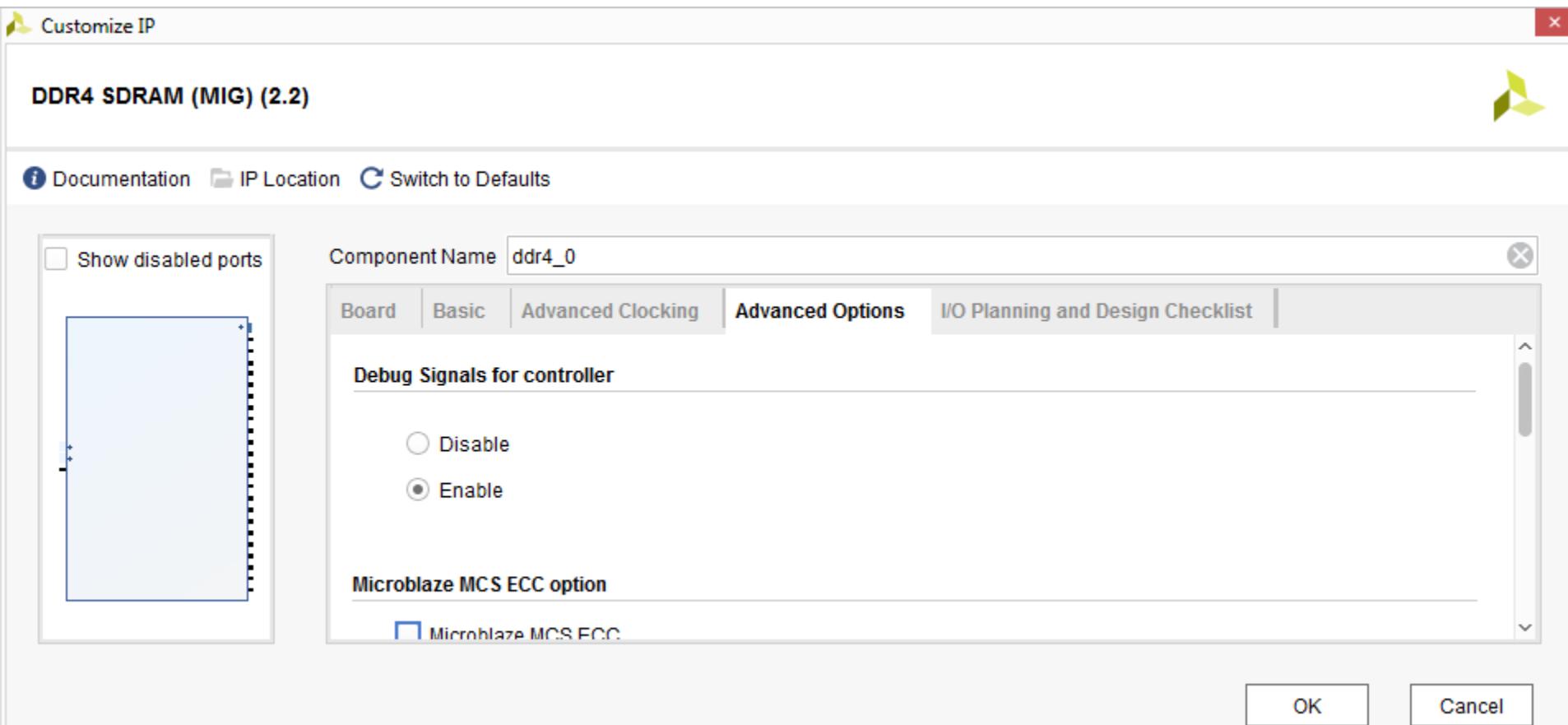
Generate MIG DDR4 C2 Example Design

- > Select the part EDY4016AABG-DR-F
 - » Note: this part is equivalent to the MT40A256M16GE-083E used on the VCU118
- > Set the Data Width to 80 and click the Advanced Options tab



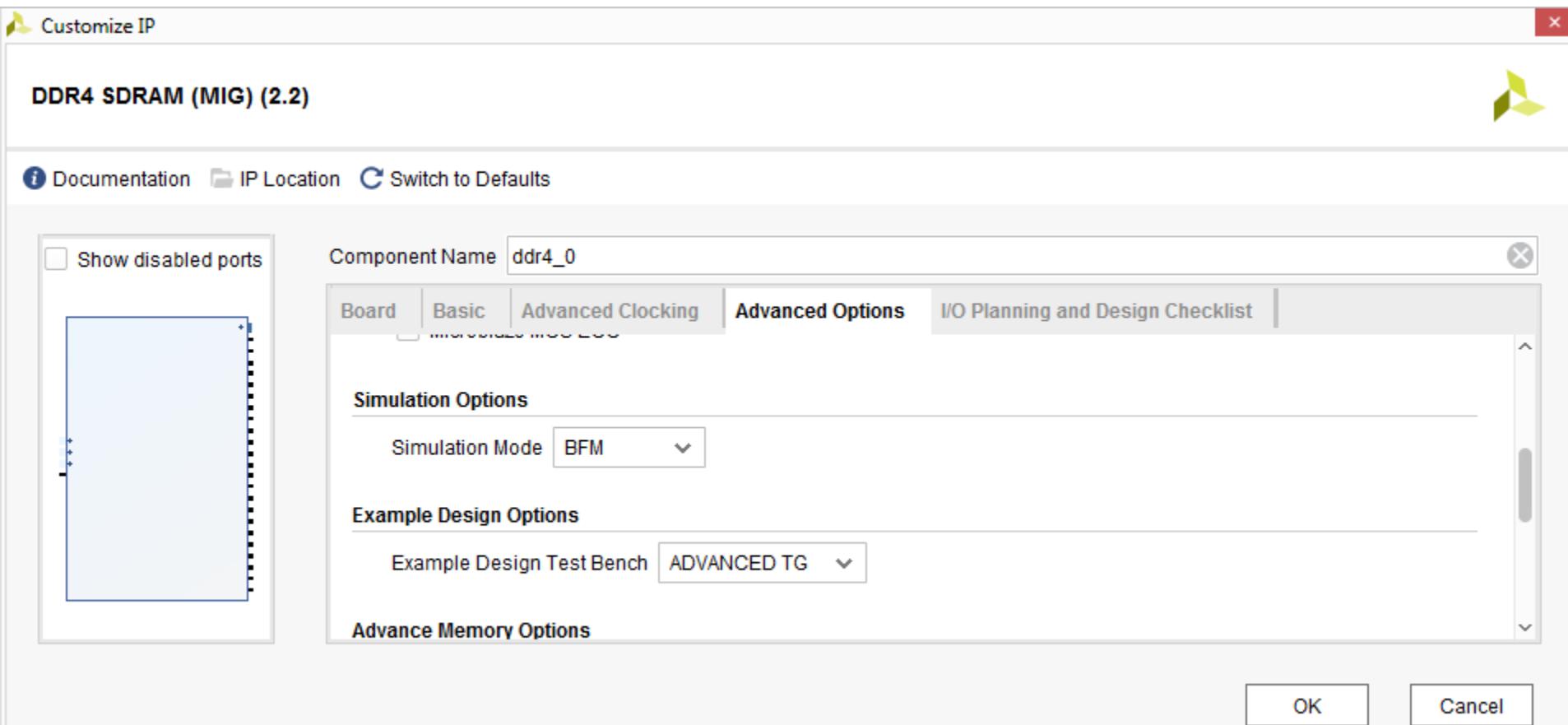
Generate MIG DDR4 C2 Example Design

- > Set the Debug Signals to Enable
- > Scroll down



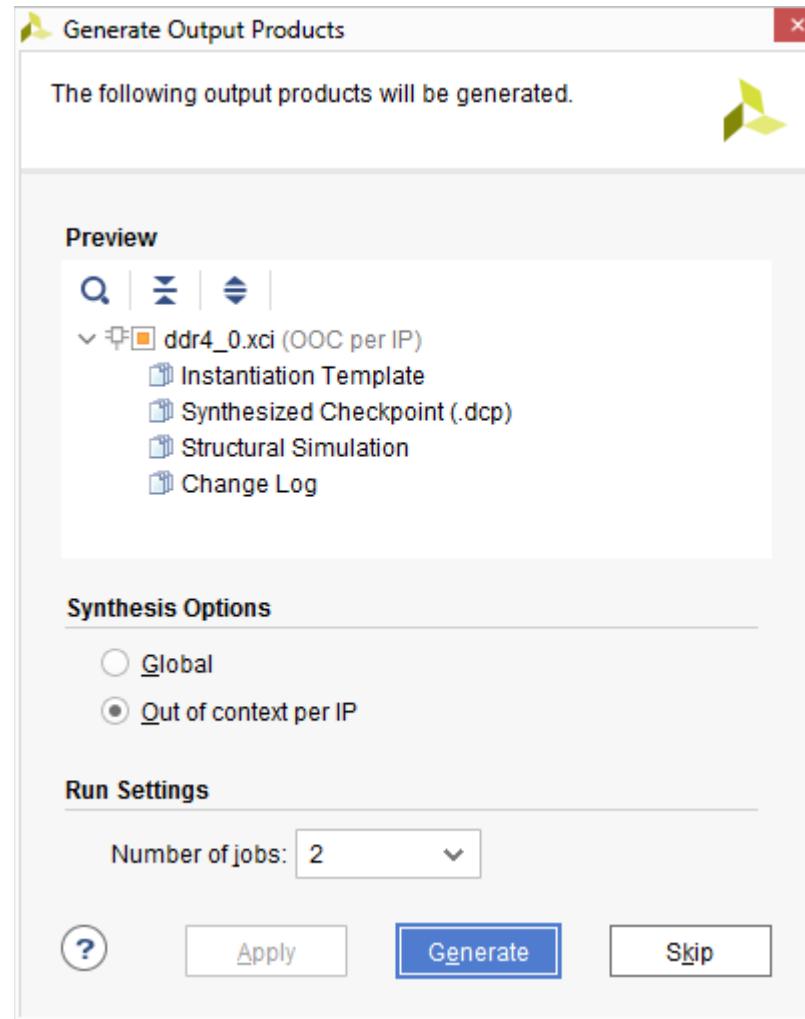
Generate MIG DDR4 C2 Example Design

- > Set the Example Design Test Bench to ADVANCED TG
- > Click OK



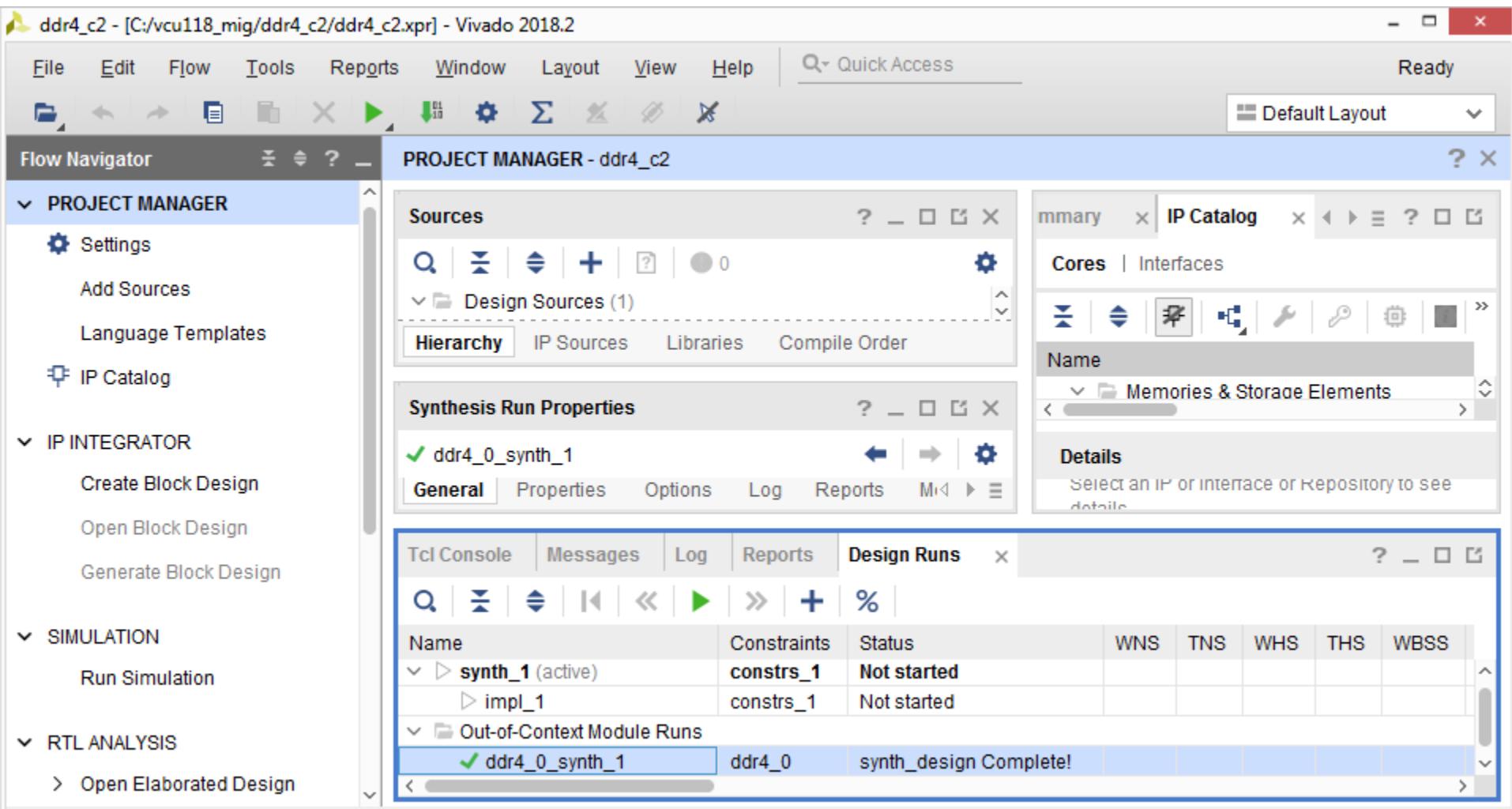
Generate MIG DDR4 C2 Example Design

> Click Generate



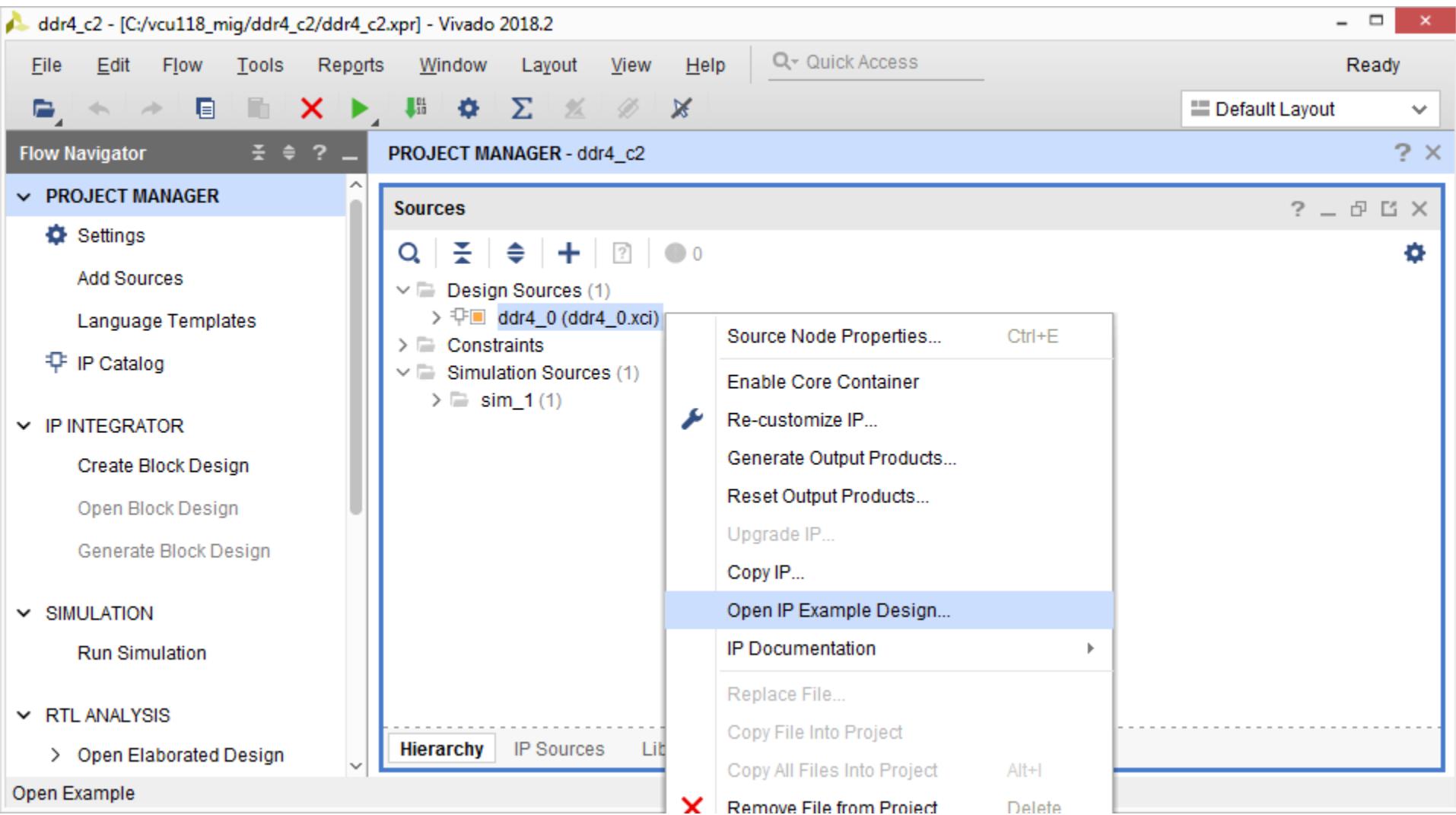
Generate MIG DDR4 C2 Example Design

- > Wait until checkmark appears on ddr4_0_synth_1



Compile Example Design

- > Right click on ddr4_0 and select Open IP Example Design...

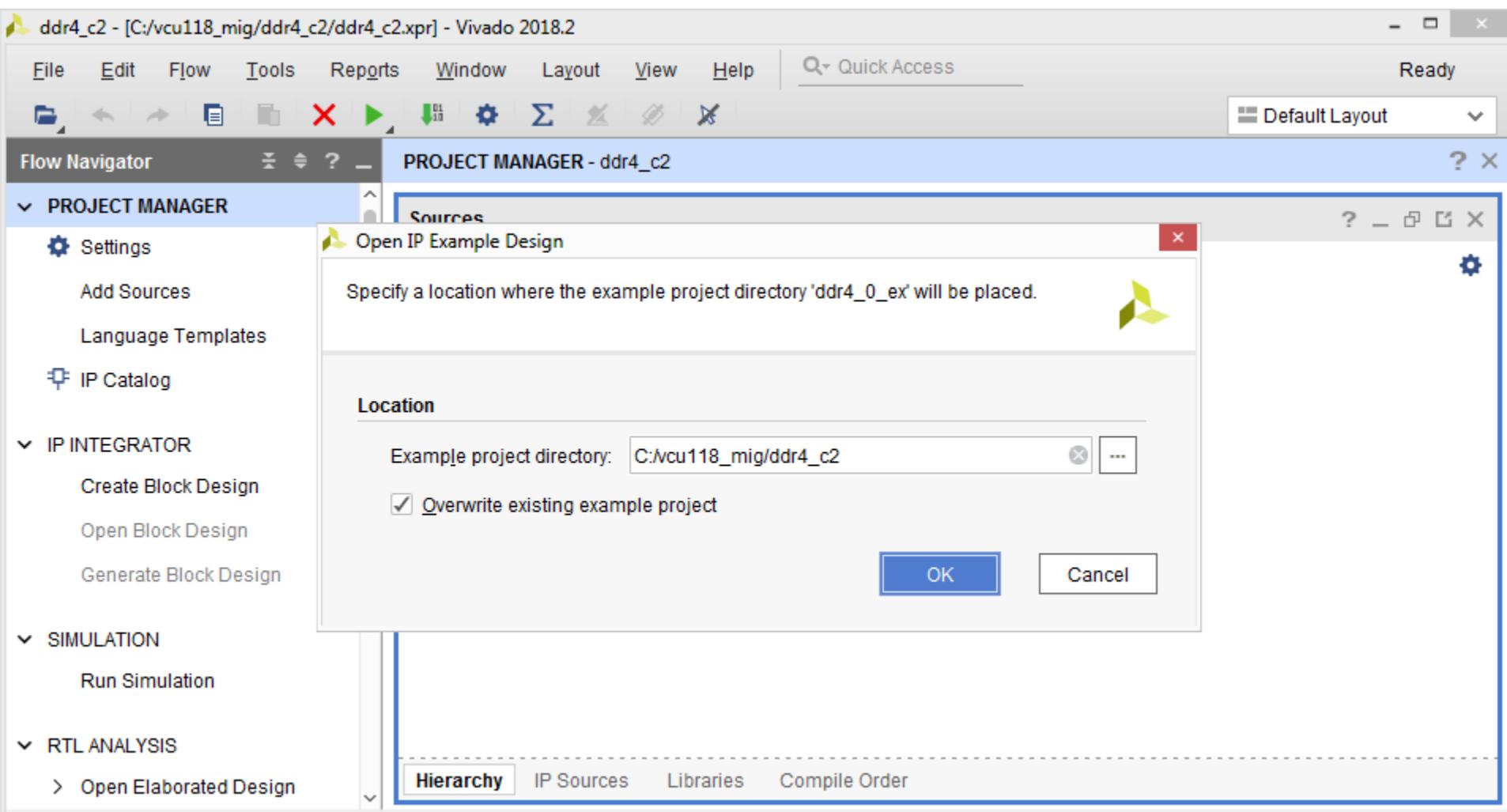


Note: Presentation applies to the VCU118

 XILINX

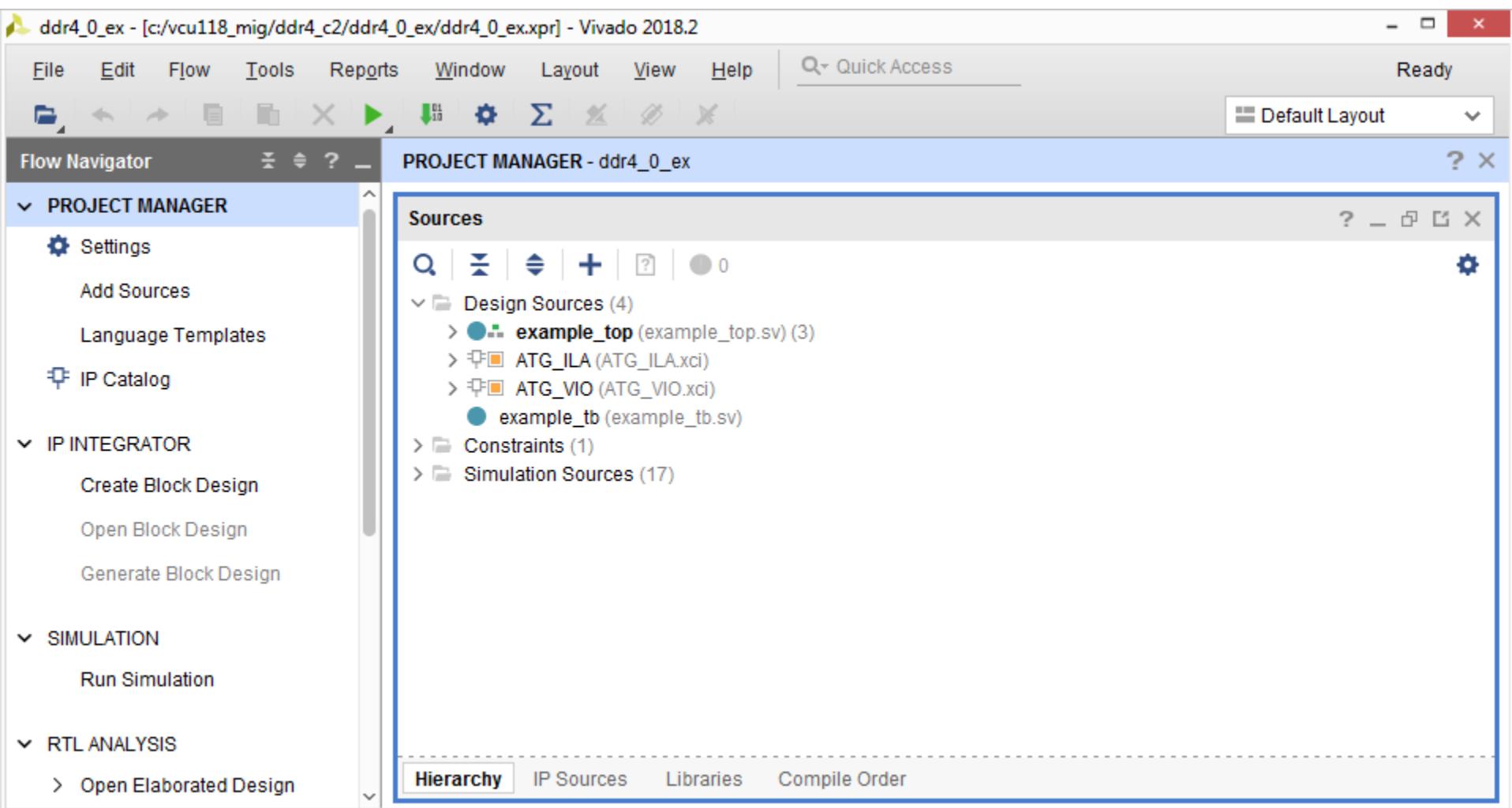
Compile Example Design

- > Set the location to C:/vcu118_mig/ddr4_c2 and click OK



Compile Example Design

- > A new project is created under <design path>/

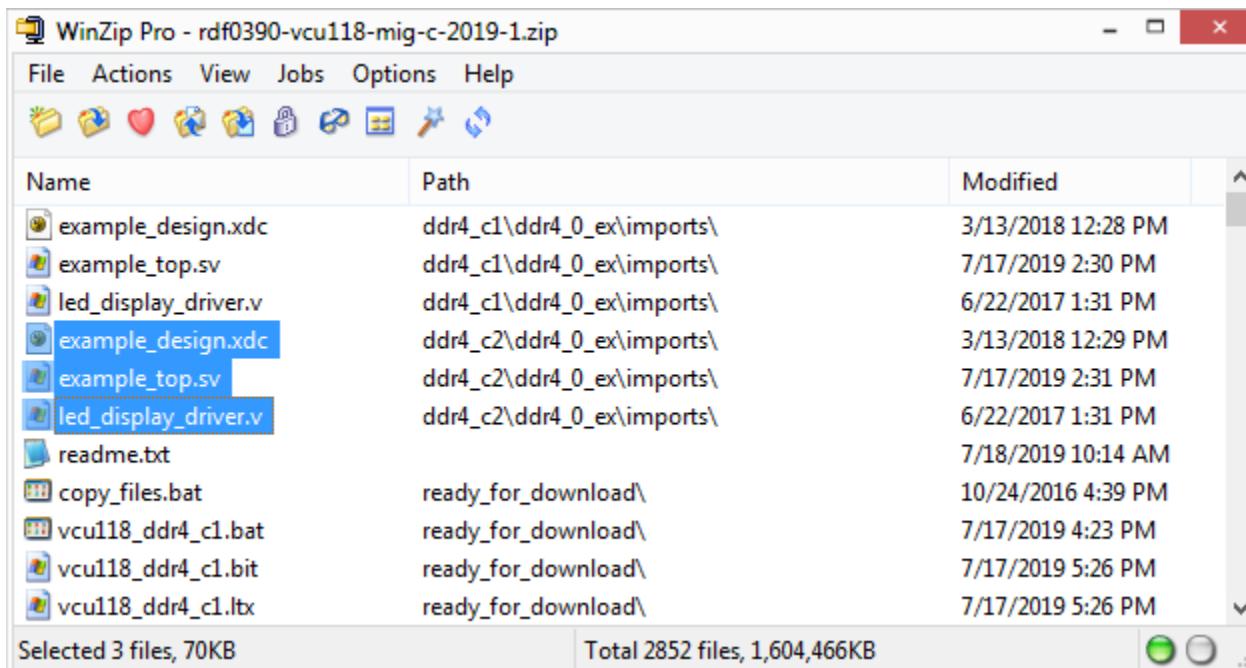


Note: The original project window can be closed

Modifications to Example Design

> From the RDF0390 - VCU118 MIG Design Files (2019.1 C) ZIP file

- » Extract the ddr4_c2 files, example_design.xdc, example_top.sv, and led_display_driver.v
- » Overwrite these three existing files in your ddr4_c2 MIG design
- » Do this after creating the Example Design; changes only affect the Example Design



Modifications to Example Design

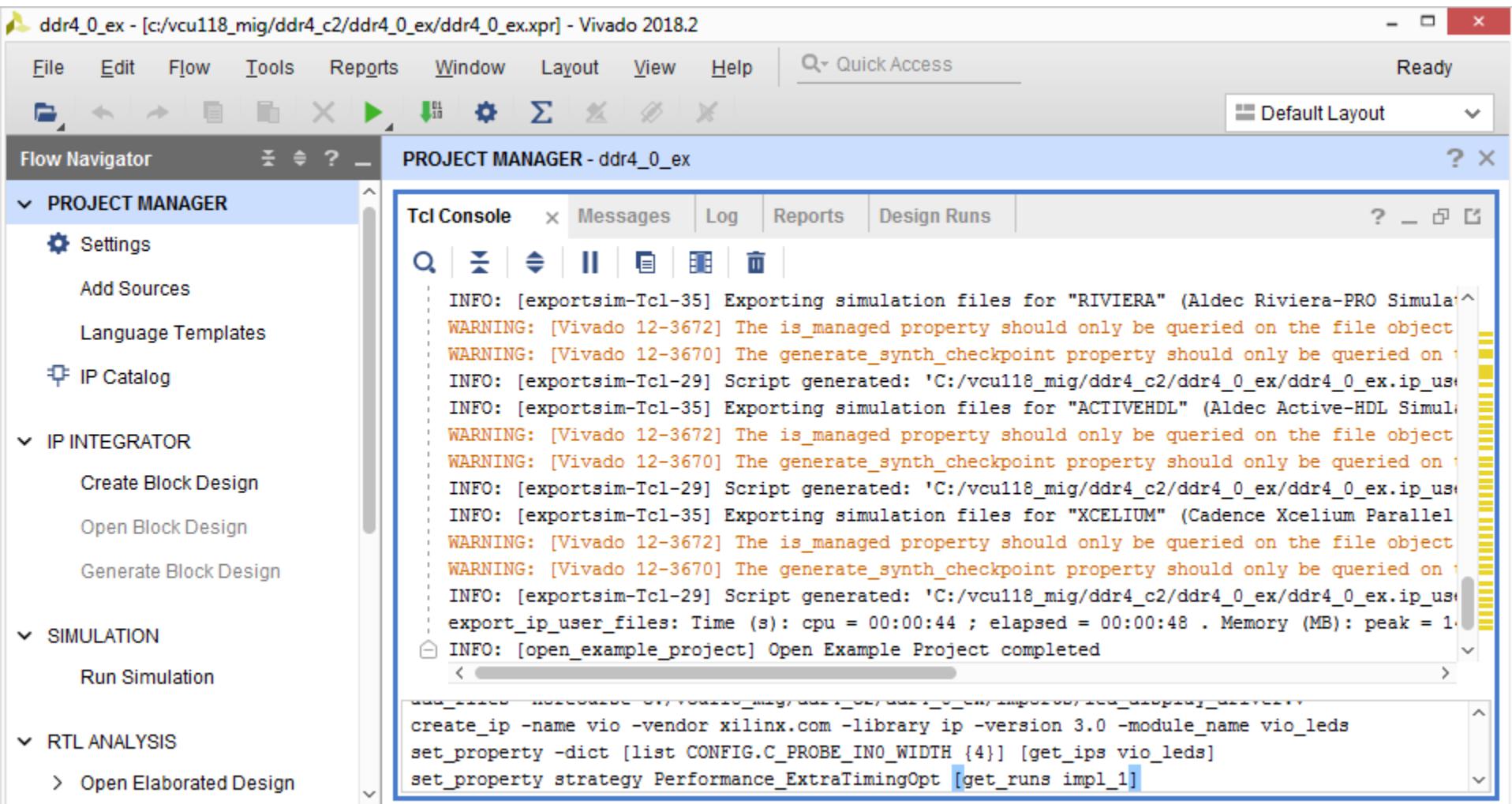
> Modifications to the example design

- » Added RTL and XDC modifications to drive LEDs
- » The following commands will add the led_display_driver.v and create the required VIO IP
- » From the Tcl Console, run these commands:

```
add_files -norecurse  
C:/vcu118_mig/ddr4_c2/ddr4_0_ex/imports/led_display_driver.v  
create_ip -name vio -vendor xilinx.com -library ip -version 3.0 -module_name  
vio_leds  
set_property -dict [list CONFIG.C_PROBE_IN0_WIDTH {4}] [get_ips vio_leds]  
set_property strategy Performance_ExtraTimingOpt [get_runs impl_1]
```

Modifications to Example Design

- > Press enter after entering Tcl commands



Modifications to Example Design

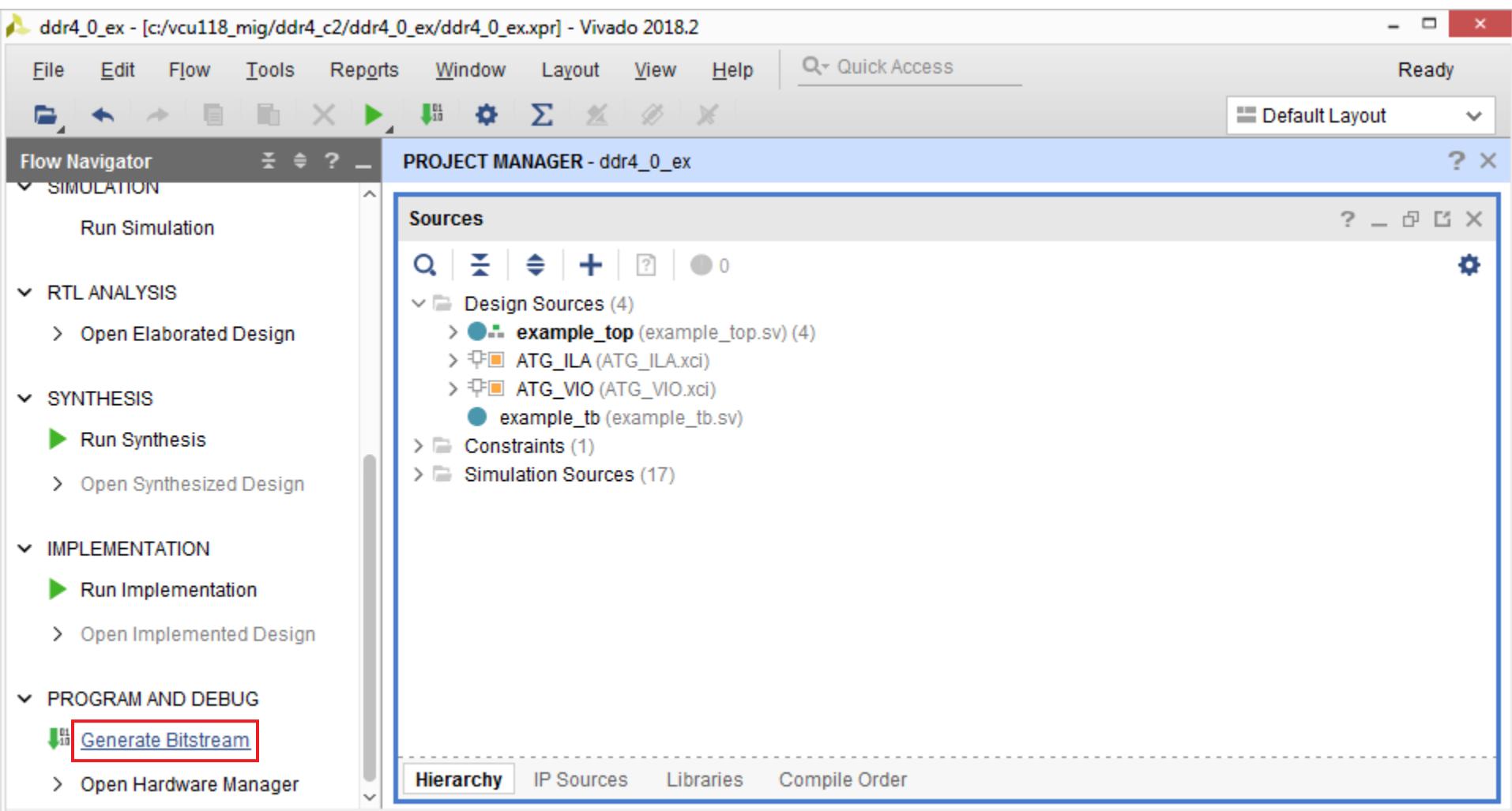
- > Tcl commands completed successfully

The screenshot shows the Vivado 2018.2 interface with the project 'ddr4_0_ex' open. The left sidebar contains sections for PROJECT MANAGER, IP INTEGRATOR, SIMULATION, and RTL ANALYSIS. The PROJECT MANAGER section is expanded, showing options like Settings, Add Sources, Language Templates, and IP Catalog. The central area is the PROJECT MANAGER - ddr4_0_ex window, which has tabs for Tcl Console, Messages, Log, Reports, and Design Runs. The Tcl Console tab is selected, displaying a series of command-line entries and their outputs. The outputs include informational messages about exporting simulation files for XCELIUM, warnings about managed properties, and details about the generated script and its execution time. The console also shows commands for opening the example project, updating compile orders, adding files, creating IP blocks, and setting properties for the 'vio_leds' module.

```
INFO: [exportsim-Tcl-35] Exporting simulation files for "XCELIUM" (Cadence Xcelium Parallel)
WARNING: [Vivado 12-3672] The is_managed property should only be queried on the file object
WARNING: [Vivado 12-3670] The generate_synth_checkpoint property should only be queried on t
INFO: [exportsim-Tcl-29] Script generated: 'C:/vcu118_mig/ddr4_c2/ddr4_0_ex/ddr4_0_ex.ip_us
export_ip_user_files: Time (s): cpu = 00:00:44 ; elapsed = 00:00:48 . Memory (MB): peak = 1
INFO: [open_example_project] Open Example Project completed
update_compile_order -fileset sources_1
add_files -norecurse C:/vcu118_mig/ddr4_c2/ddr4_0_ex/imports/led_display_driver.v
C:/vcu118_mig/ddr4_c2/ddr4_0_ex/imports/led_display_driver.v
create_ip -name vio -vendor xilinx.com -library ip -version 3.0 -module_name vio_leds
c:/vcu118_mig/ddr4_c2/ddr4_0_ex/ddr4_0_ex.srcs/sources_1/ip/vio_leds/vio_leds.xci
set_property -dict [list CONFIG.C_PROBE_IN0_WIDTH {4}] [get_ips vio_leds]
0
set_property strategy Performance_ExtraTimingOpt [get_runs impl_1]
update_compile_order -fileset sources_1
```

Compile Example Design

- > Click on Generate Bitstream

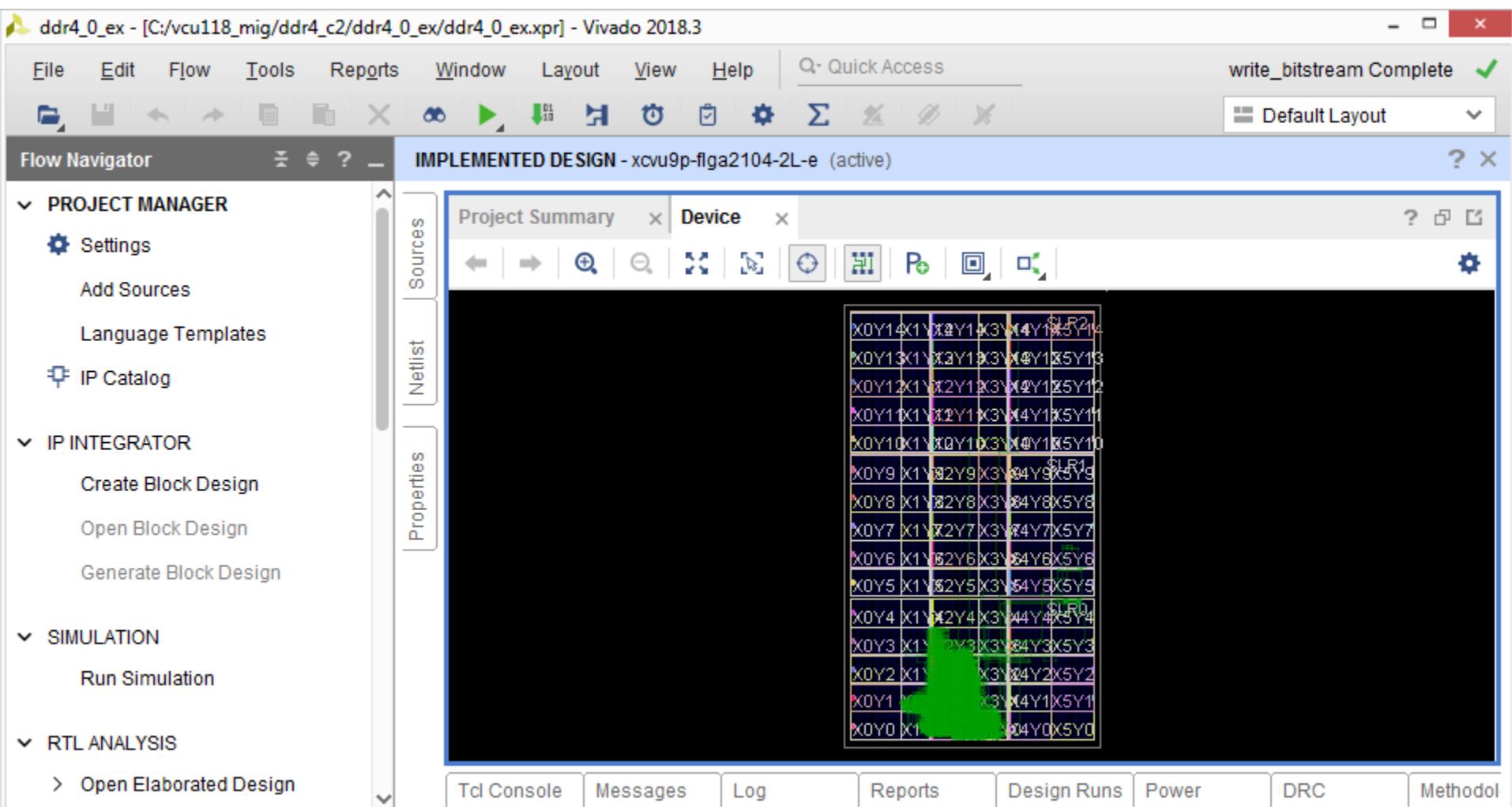


Generate a programming file after implementation

Note: Presentation applies to the VCU118

Compile Example Design

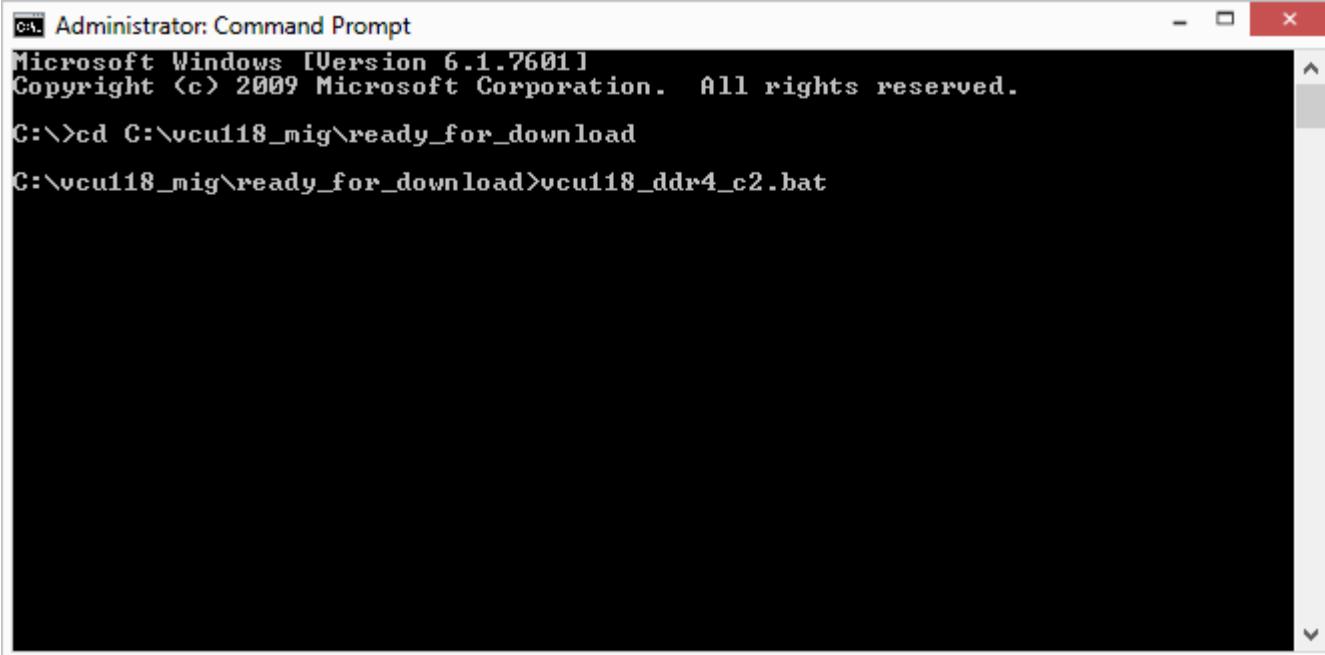
- > Open and view the Implemented Design



Run MIG Example Design

- > From a Command Prompt, type:

```
cd C:\vcu118_mig\ready_for_download  
vcu118_ddr4_c2.bat
```

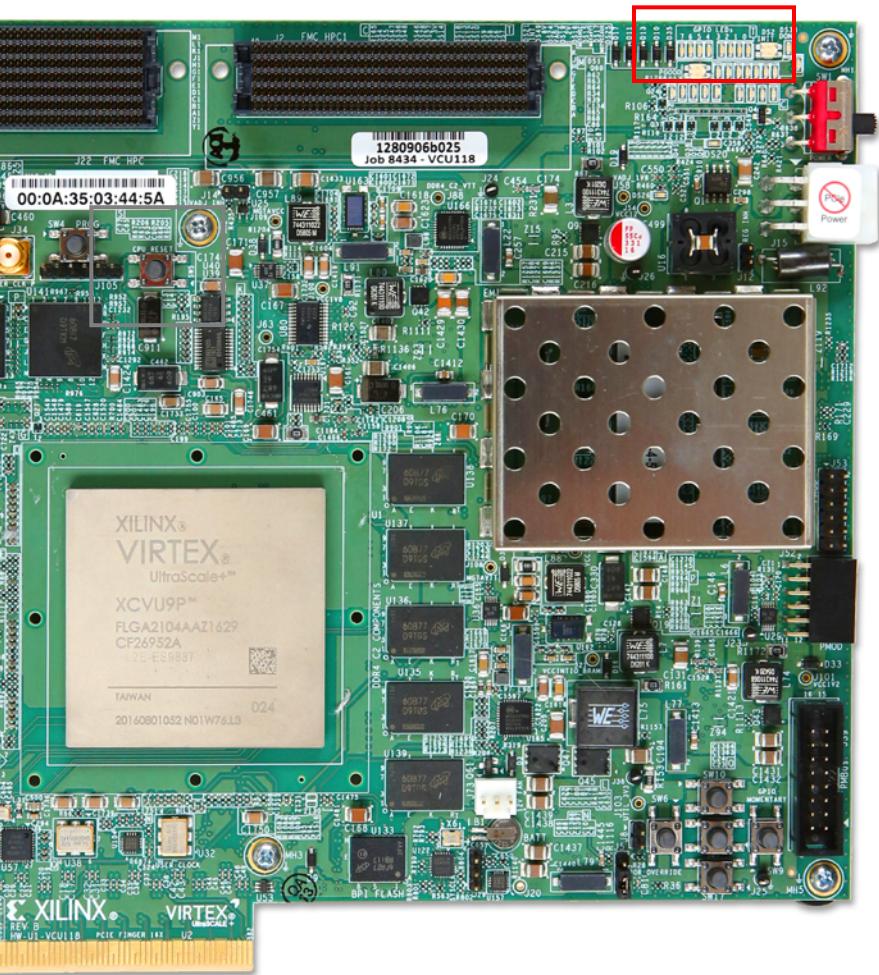


The screenshot shows a Windows Command Prompt window titled "Administrator: Command Prompt". The window displays the following text:

```
Microsoft Windows [Version 6.1.7601]
Copyright <c> 2009 Microsoft Corporation. All rights reserved.

C:>cd C:\vcu118_mig\ready_for_download
C:\vcu118_mig\ready_for_download>vcu118_ddr4_c2.bat
```

Run MIG Example Design



- > After bitstream loads, LED 0 (right most LED) will be lit, and LED1 will be blinking
- > LED 3 will light and stay on
 - » This indicates Calibration has completed
- > If an error occurs, LED 0 will go out and LED 2 will light
 - » The “CPU_RESET” button, SW5, is the reset

Generate MIG RLD3 C3 Example Design

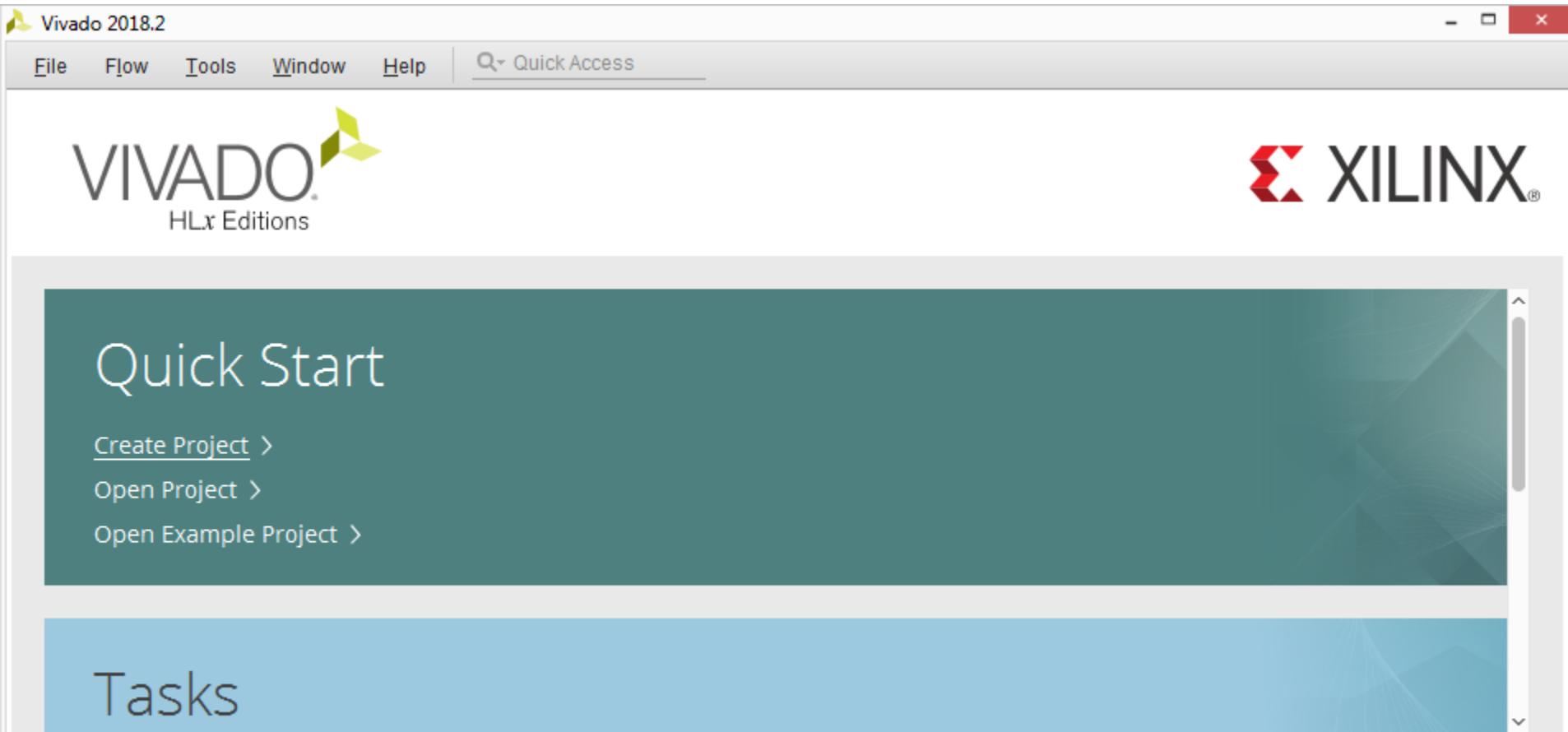


Generate MIG RLD3 C3 Example Design

> Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2019.1 → Vivado

> Select Create Project



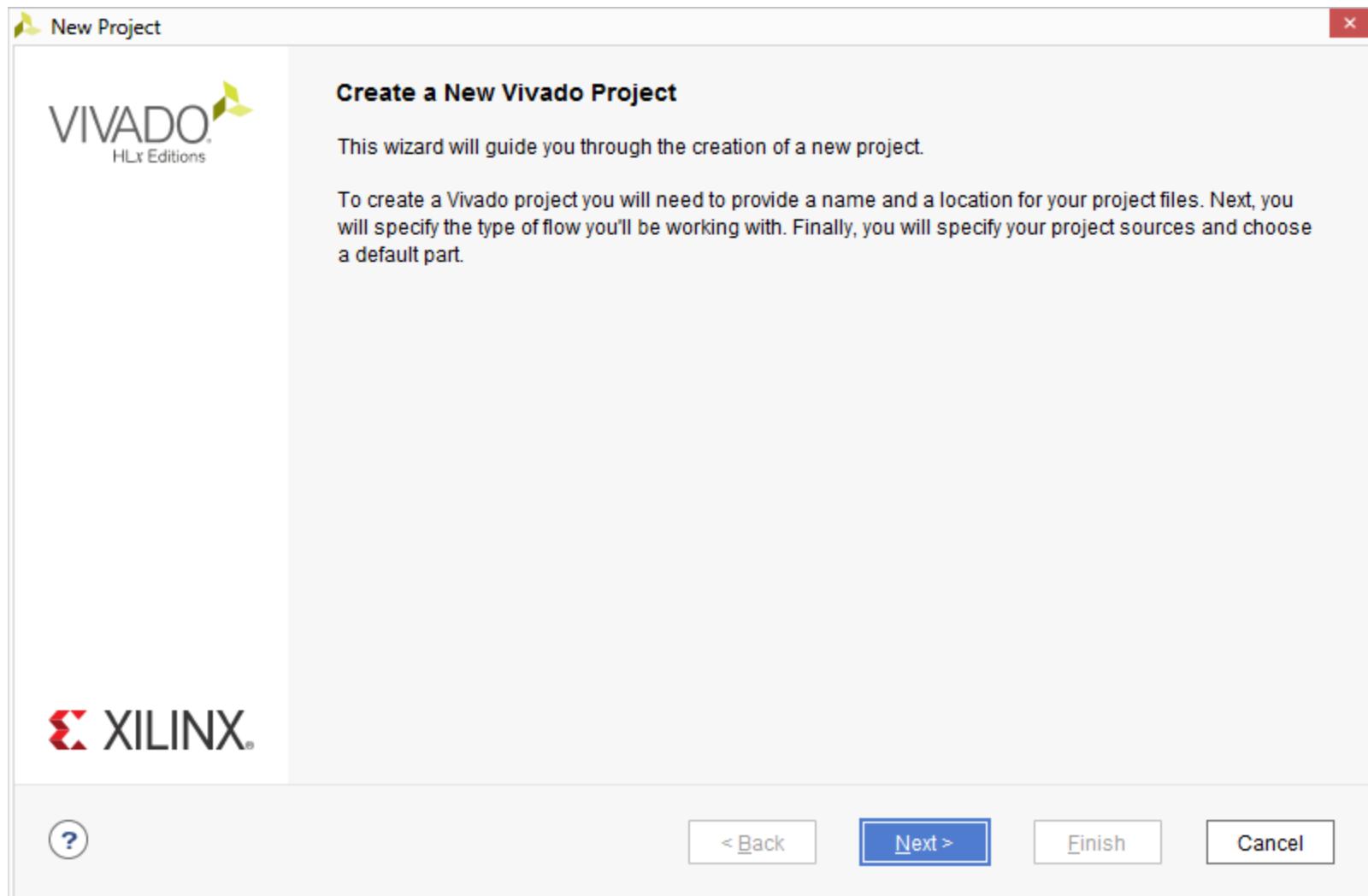
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Note: Presentation applies to the VCU118

XILINX

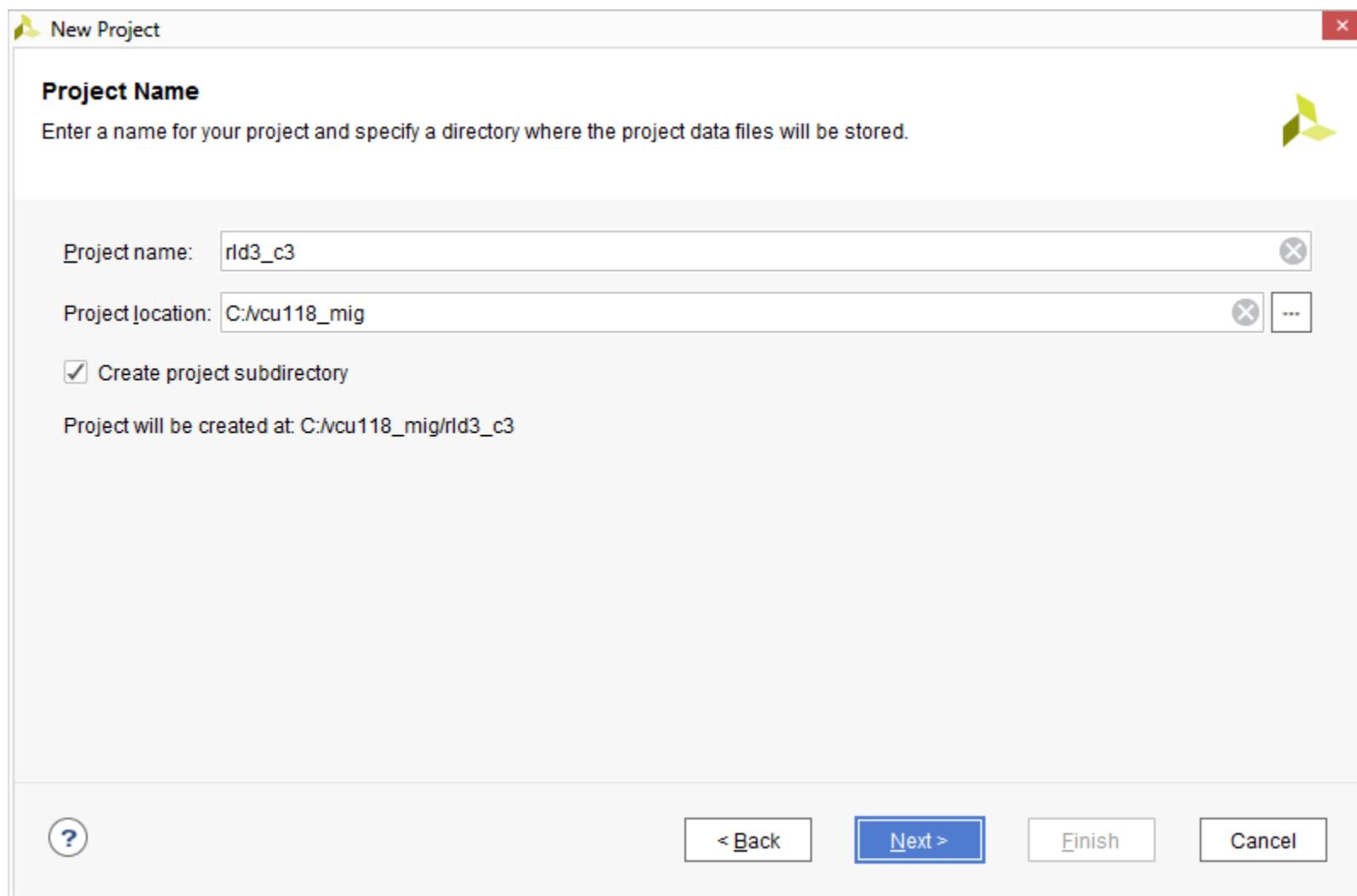
Generate MIG RLD3 C3 Example Design

> Click Next



Generate MIG RLD3 C3 Example Design

- > Set the Project name to rld3_c3 and location to C:/vcu118_mig
 - » Check Create project subdirectory

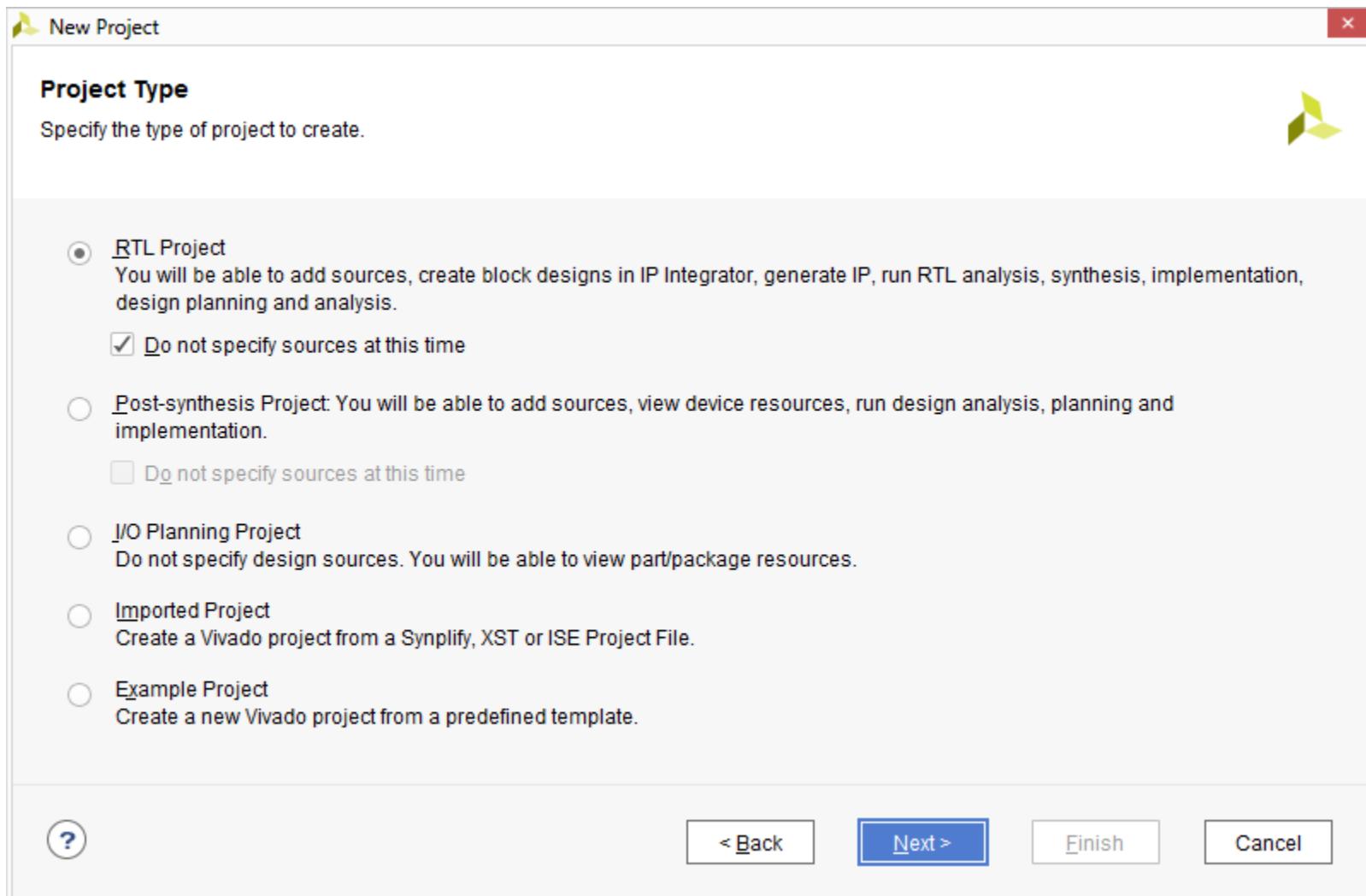


Note: Vivado generally requires forward slashes in paths

Generate MIG RLD3 C3 Example Design

> Select RTL Project

» Select Do not specify sources at this time



Generate MIG RLD3 C3 Example Design

- > Under Boards, select the VCU118 Rev 2.0

New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Parts | Boards

Reset All Filters

Vendor: All Name: All

Search:

Display Name	Preview	Vendor	File V
Virtex UltraScale+ VCU118 Evaluation Platform		xilinx.com	2.0
Virtex UltraScale+ VCU1525 Acceleration Development Board		xilinx.com	1.1

< >

?

< Back

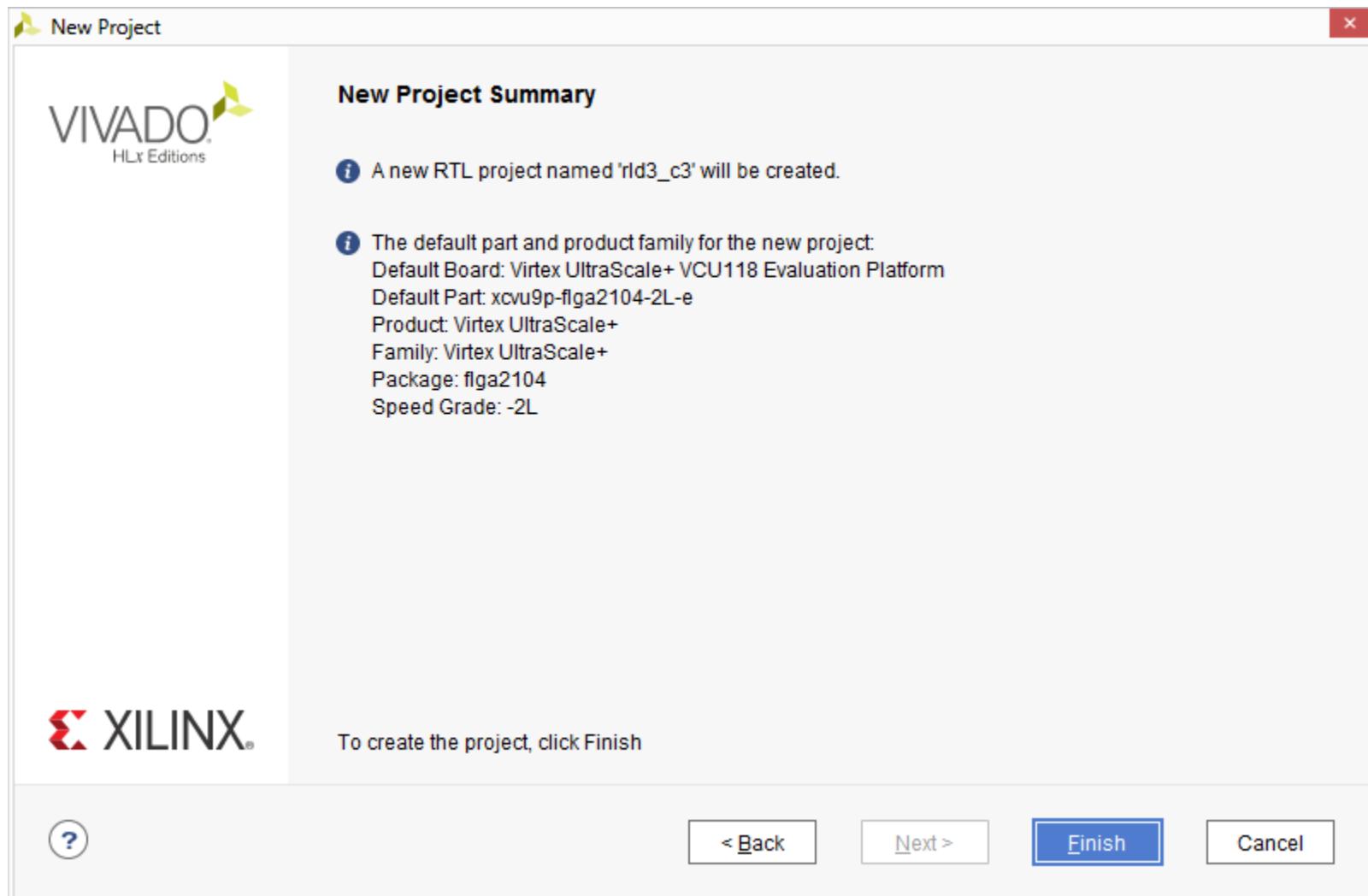
Next >

Finish

Cancel

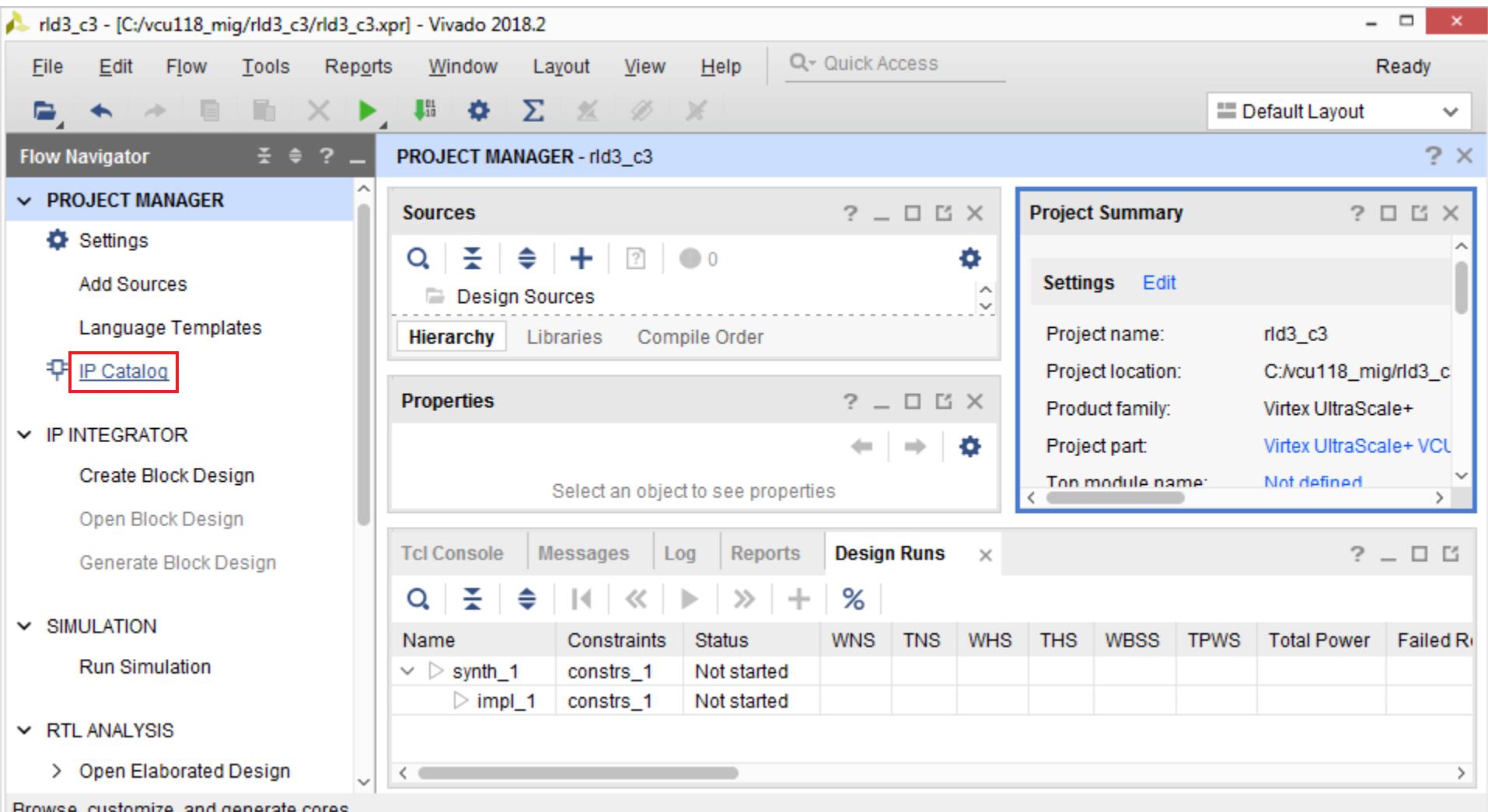
Generate MIG RLD3 C3 Example Design

> Click Finish



Generate MIG RLD3 C3 Example Design

> Click on IP Catalog



Generate MIG RLD3 C3 Example Design

> Select RLDRAM3 (MIG), v1.4

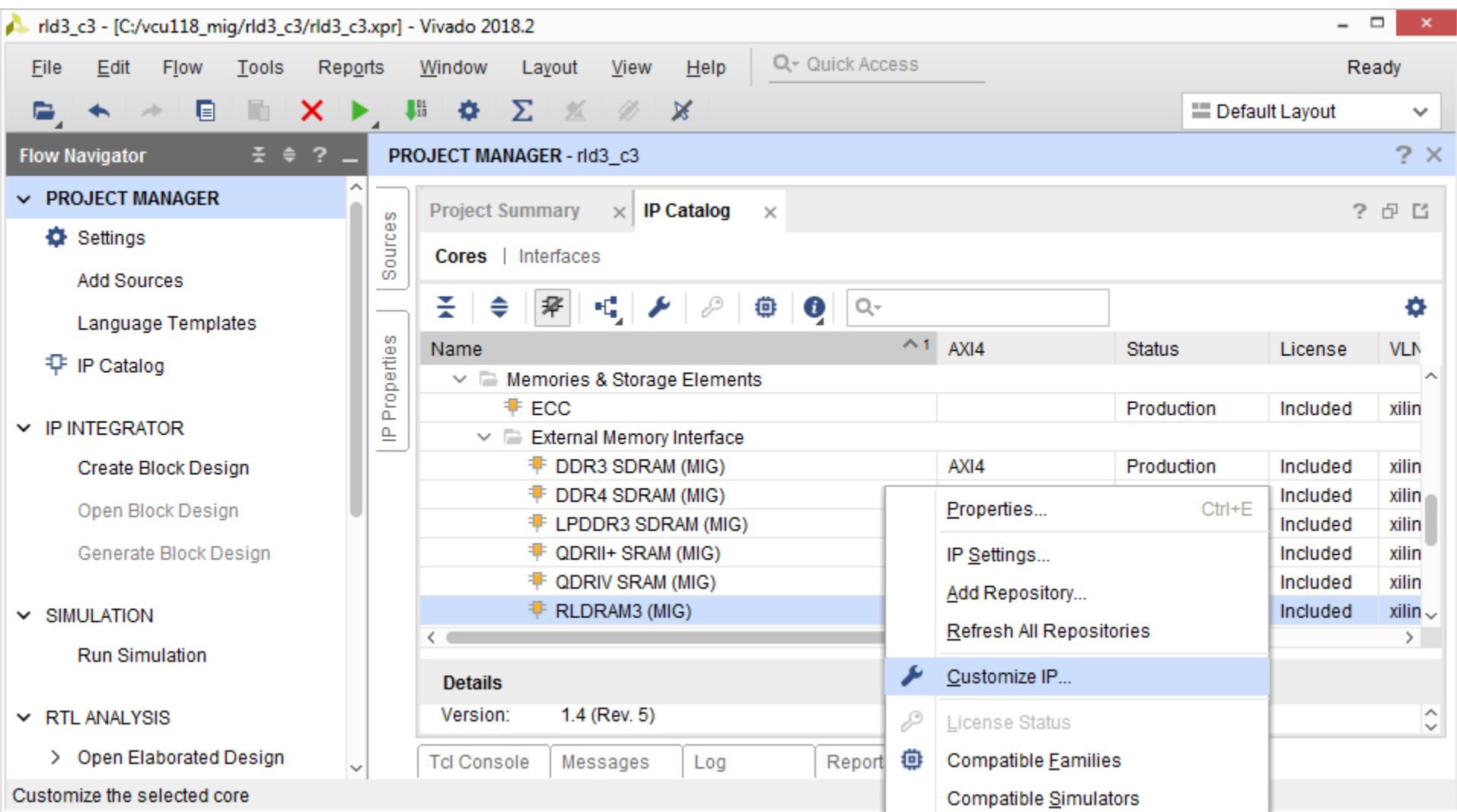
The screenshot shows the Vivado 2018.2 interface with the project "rld3_c3" open. The left sidebar contains sections for PROJECT MANAGER, IP INTEGRATOR, SIMULATION, and RTL ANALYSIS. The IP INTEGRATOR section is expanded, showing options like Create Block Design, Open Block Design, and Generate Block Design. The central area is the PROJECT MANAGER, with the IP Catalog tab selected. The IP Catalog window displays a table of available IP cores. The table has columns for Name, Status, License, and VLM. The "Memories & Storage Elements" category is expanded, showing sub-options for ECC, External Memory Interface, and various DDR variants. The "RLDRAM3 (MIG)" option is highlighted with a blue selection bar. Below the table, a "Details" section shows the version as 1.4 (Rev. 5). The bottom navigation bar includes tabs for Tcl Console, Messages, Log, Reports, and Design Runs.

Name	Status	License	VLM	
ECC	Production	Included	xilinx	
External Memory Interface	AXI4	Production	Included	xilinx
DDR3 SDRAM (MIG)	AXI4	Production	Included	xilinx
DDR4 SDRAM (MIG)	AXI4	Production	Included	xilinx
LPDDR3 SDRAM (MIG)		Production	Included	xilinx
QDRII+ SRAM (MIG)		Production	Included	xilinx
QDRIV SRAM (MIG)		Production	Included	xilinx
RLDRAM3 (MIG)	Production	Included	xilinx	

Generate MIG RLD3 C3 Example Design

> Right click on RLDRAM3 (MIG)

» Select Customize IP

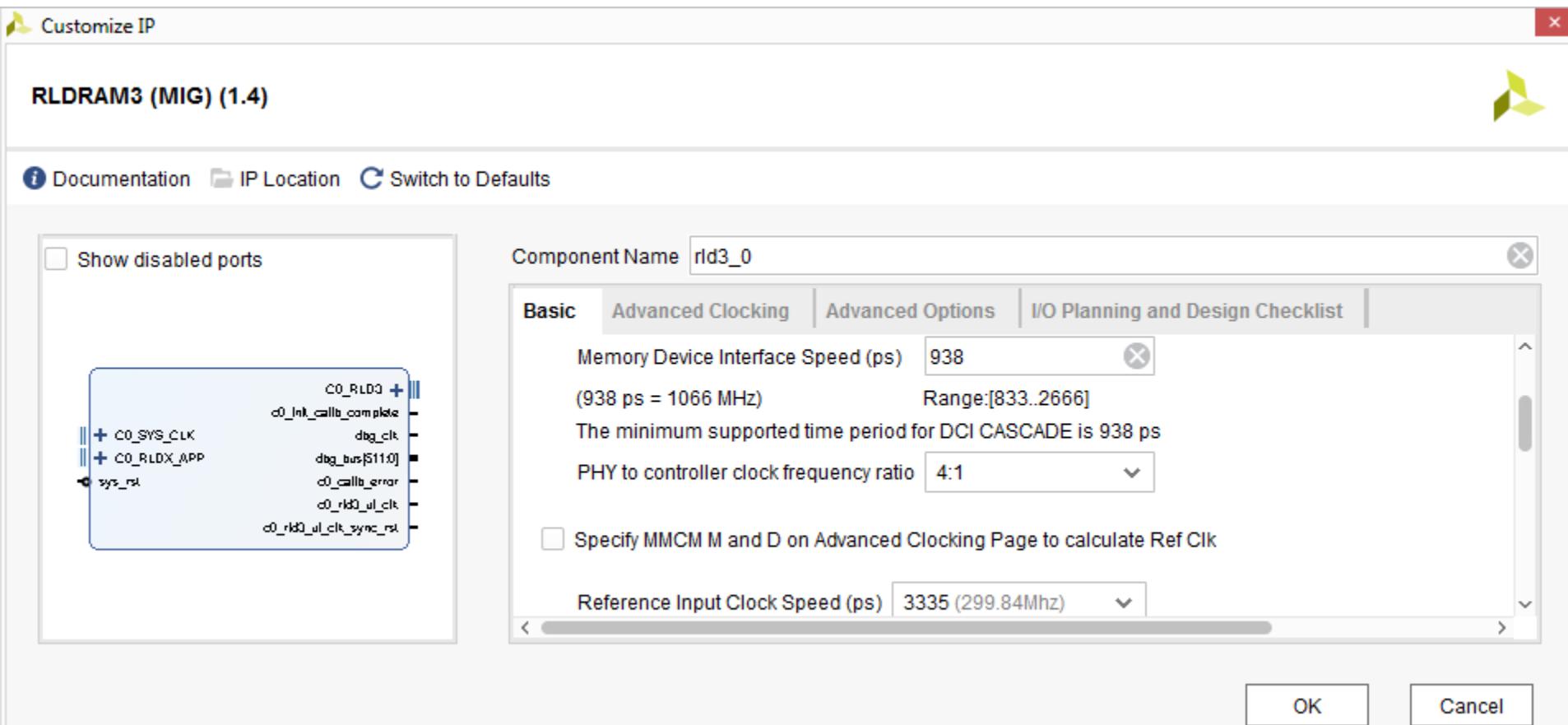


Note: Presentation applies to the VCU118

XILINX

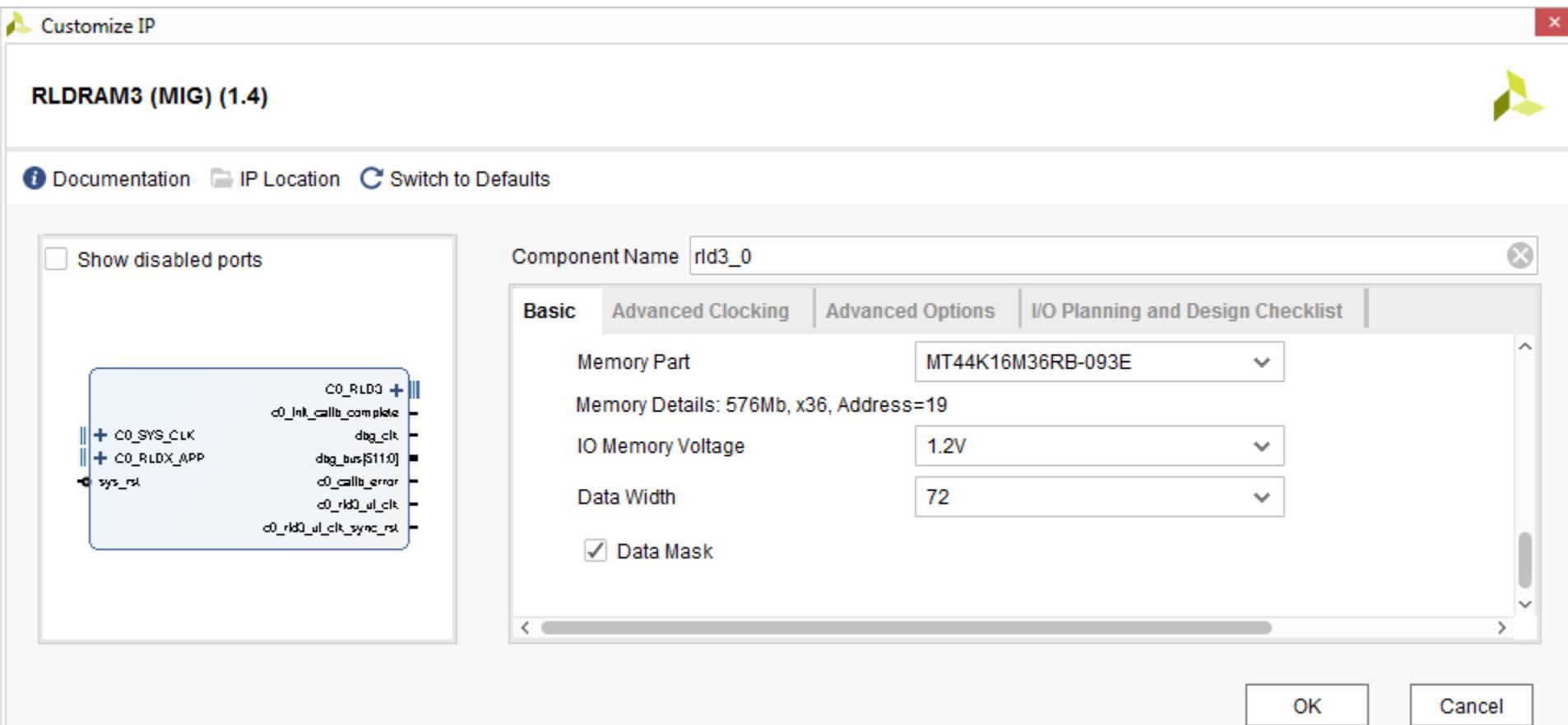
Generate MIG RLD3 C3 Example Design

- > Set Clock period to 938 for 2133 Mb/s operation.
- > Set the Input Clock to 3335 ps for 300 MHz
- > Scroll down



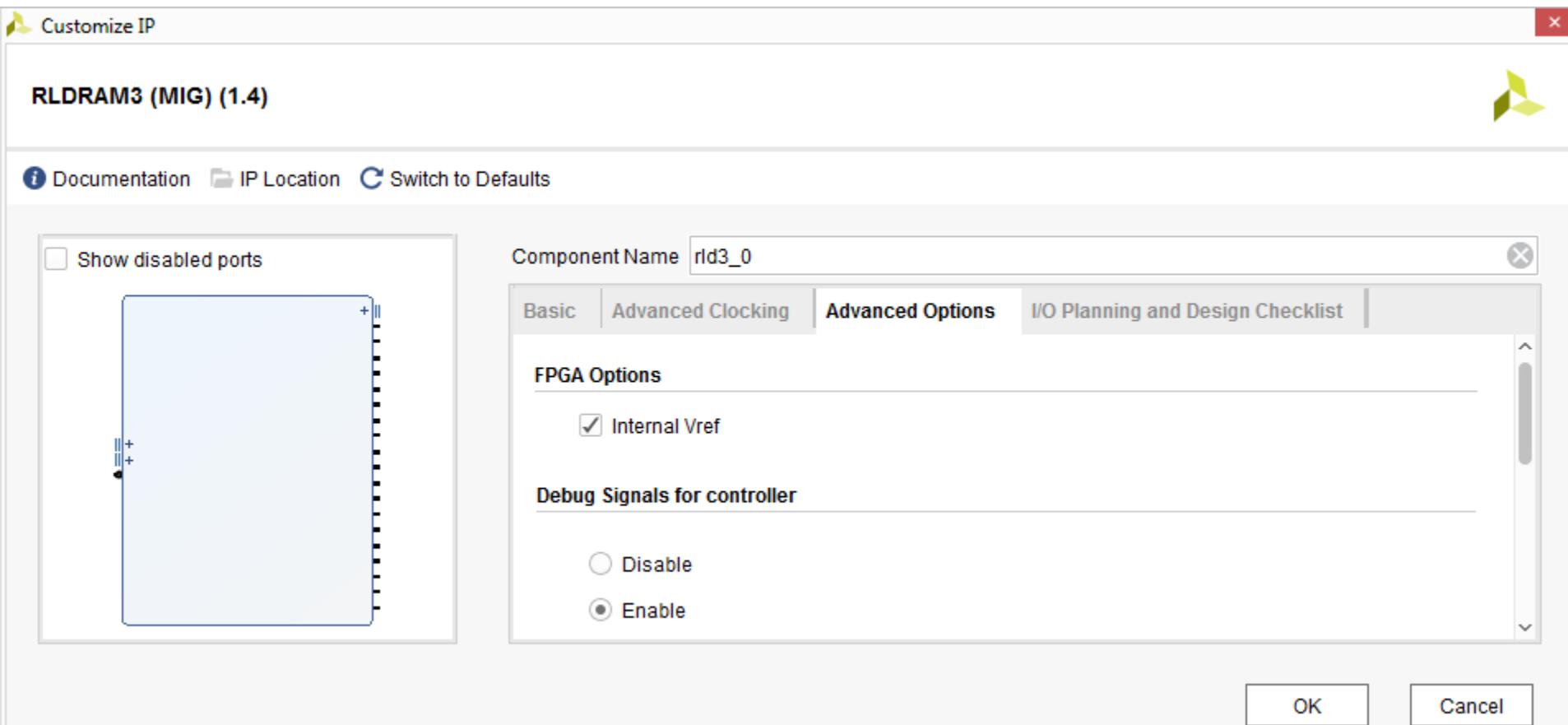
Generate MIG RLD3 C3 Example Design

- > Select the part MT44K16M36RB-093E
- > Set the Data Width to 72 and click the Advanced Options Tab



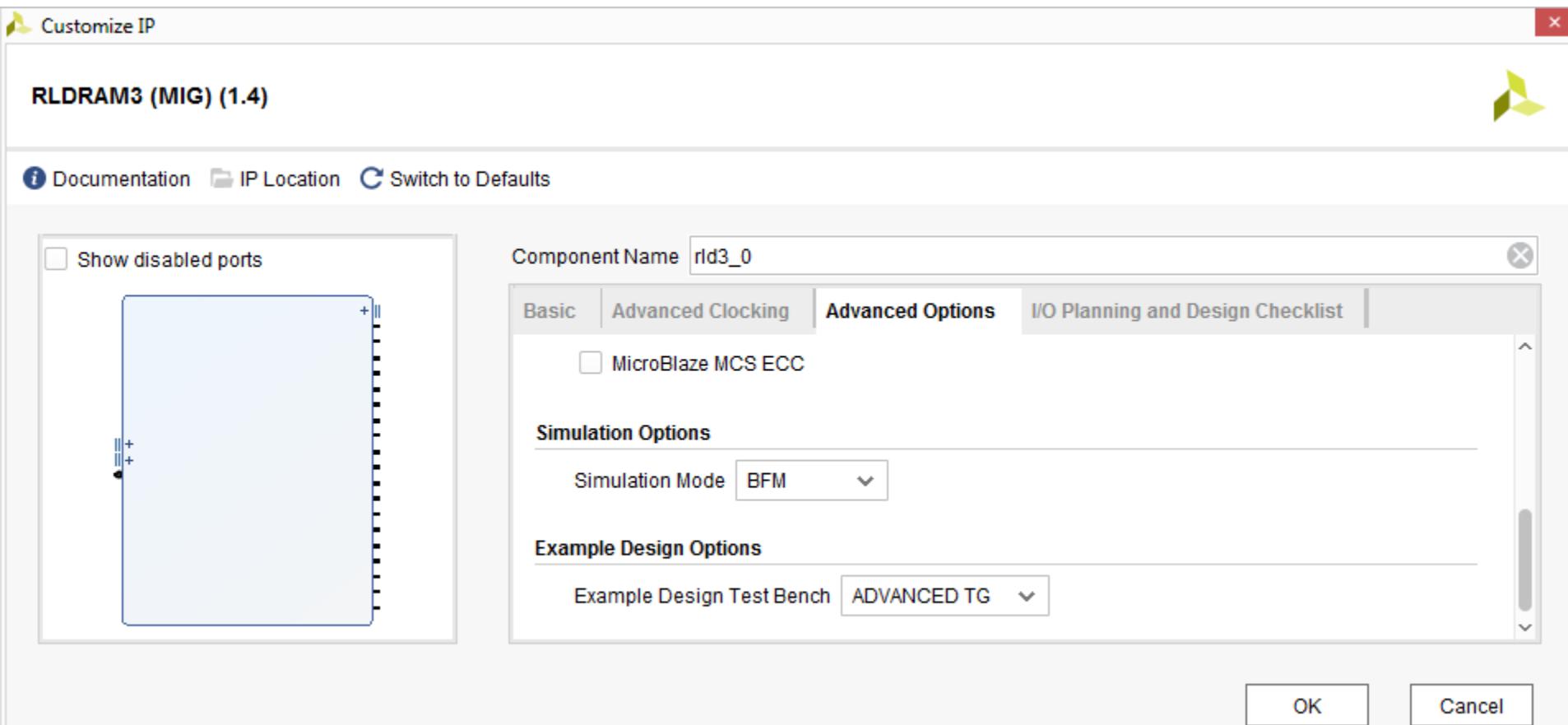
Generate MIG RLD3 C3 Example Design

- > Set the Debug Signals to Enable
- > Scroll down



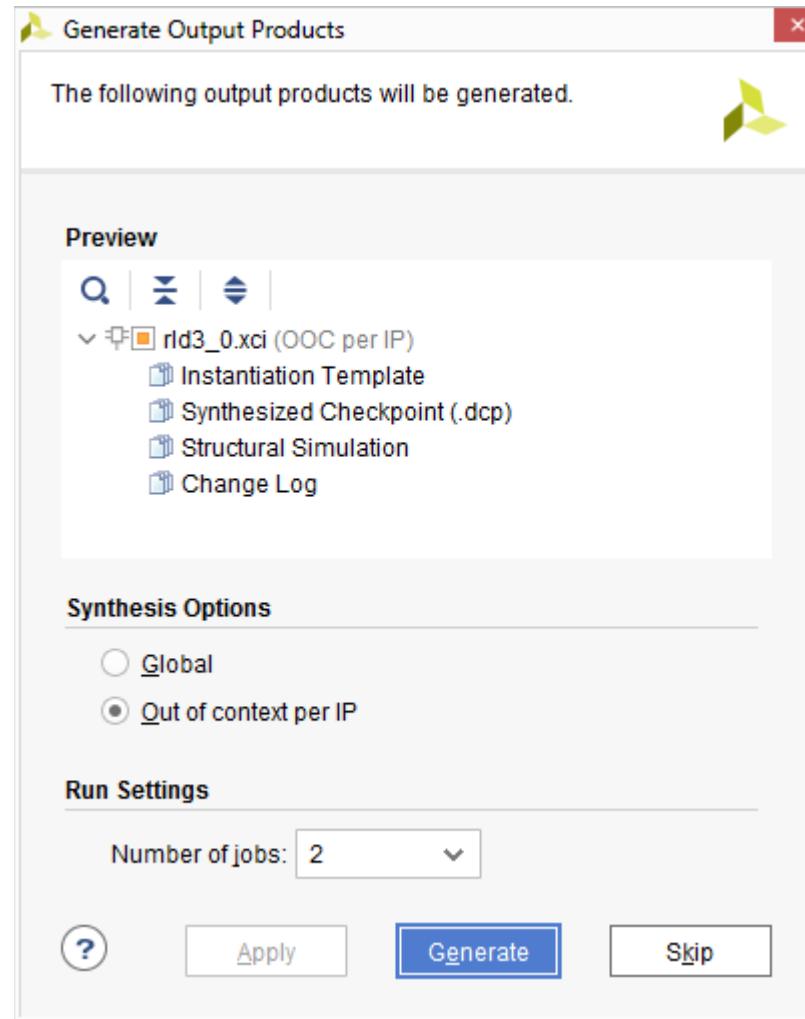
Generate MIG RLD3 C3 Example Design

- > Set the Example Design Test Bench to ADVANCED TG
- > Click OK



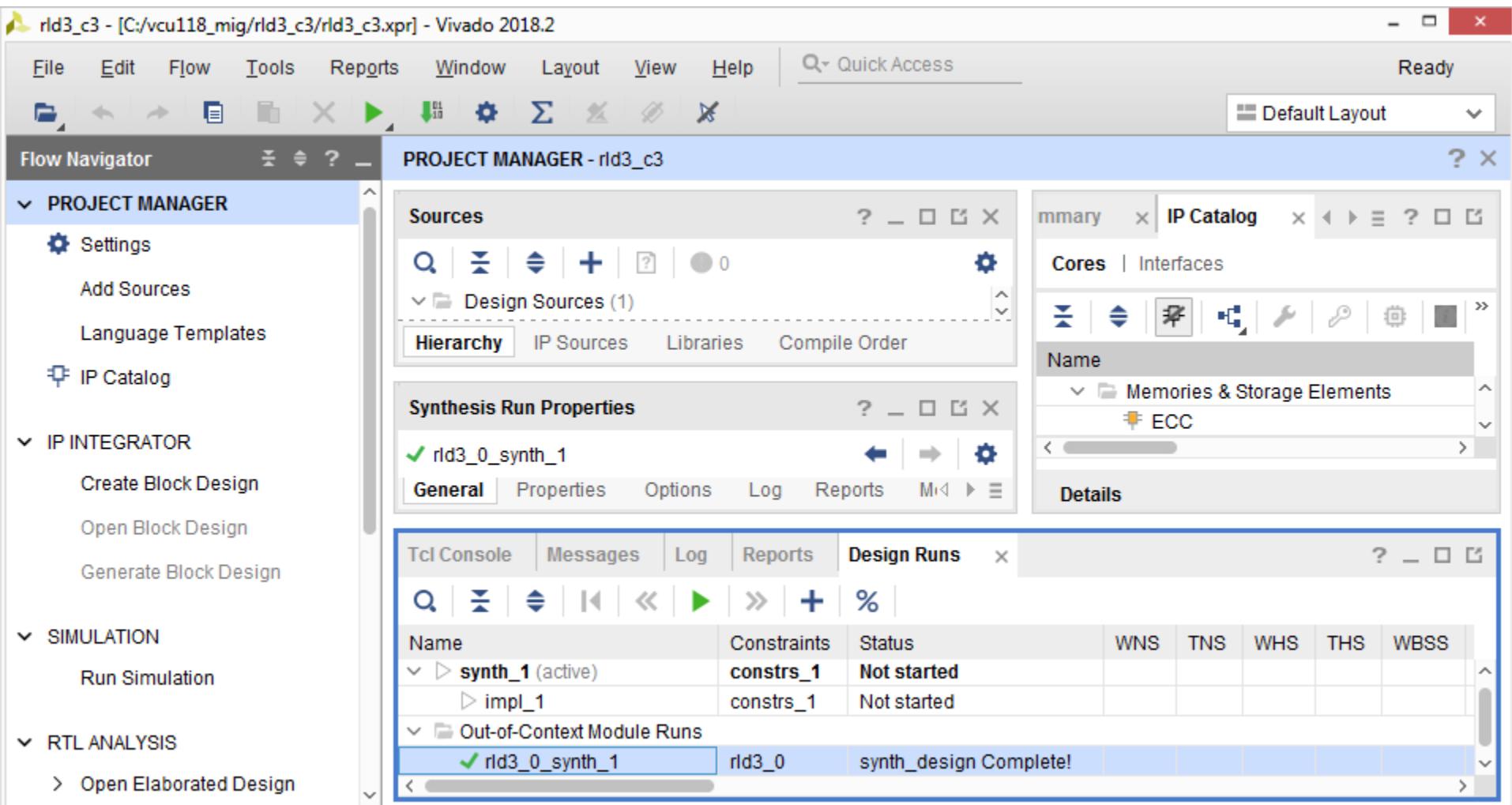
Generate MIG RLD3 C3 Example Design

> Click Generate



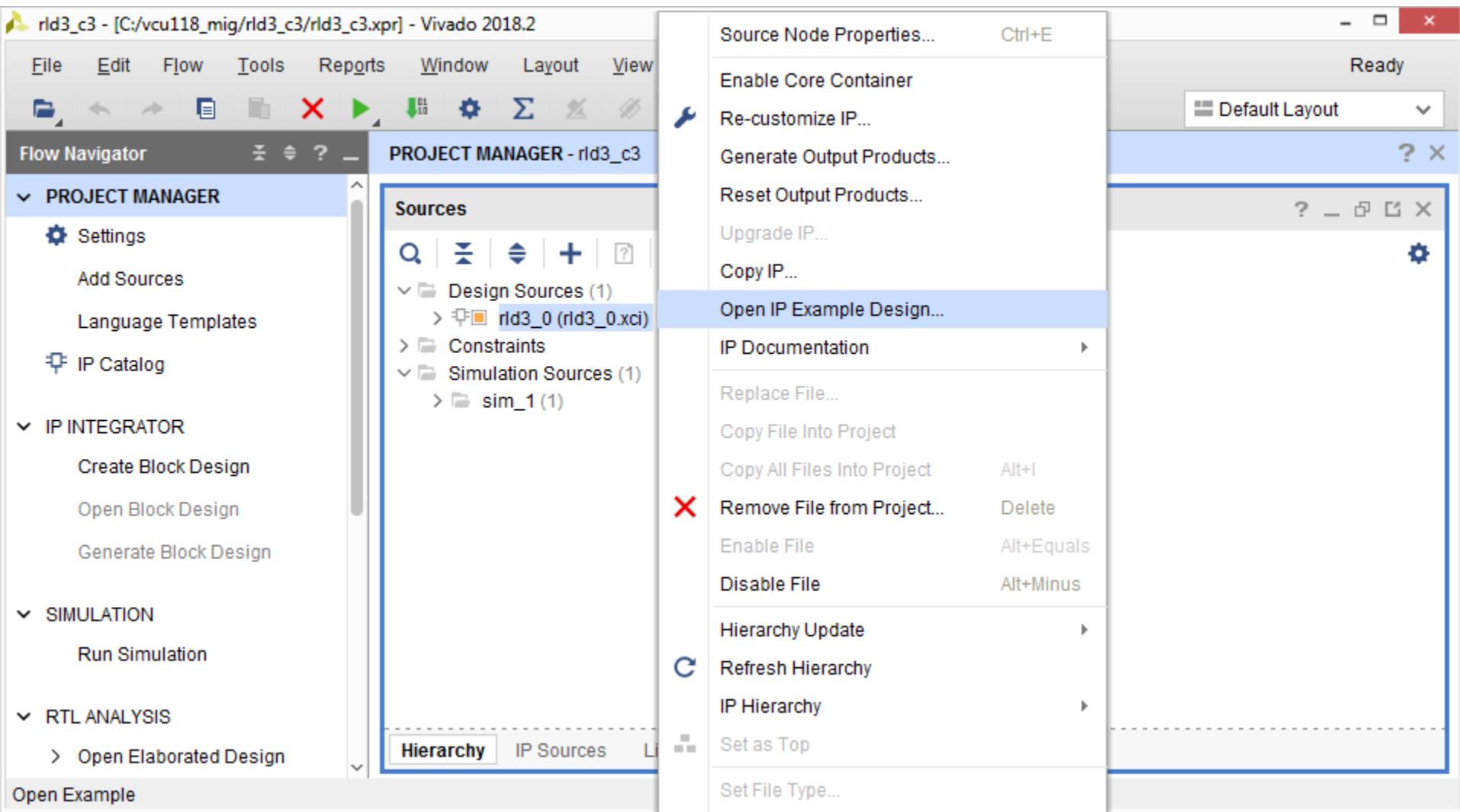
Generate MIG RLD3 C3 Example Design

- > Wait until checkmark appears on rld3_0_synth_1



Compile Example Design

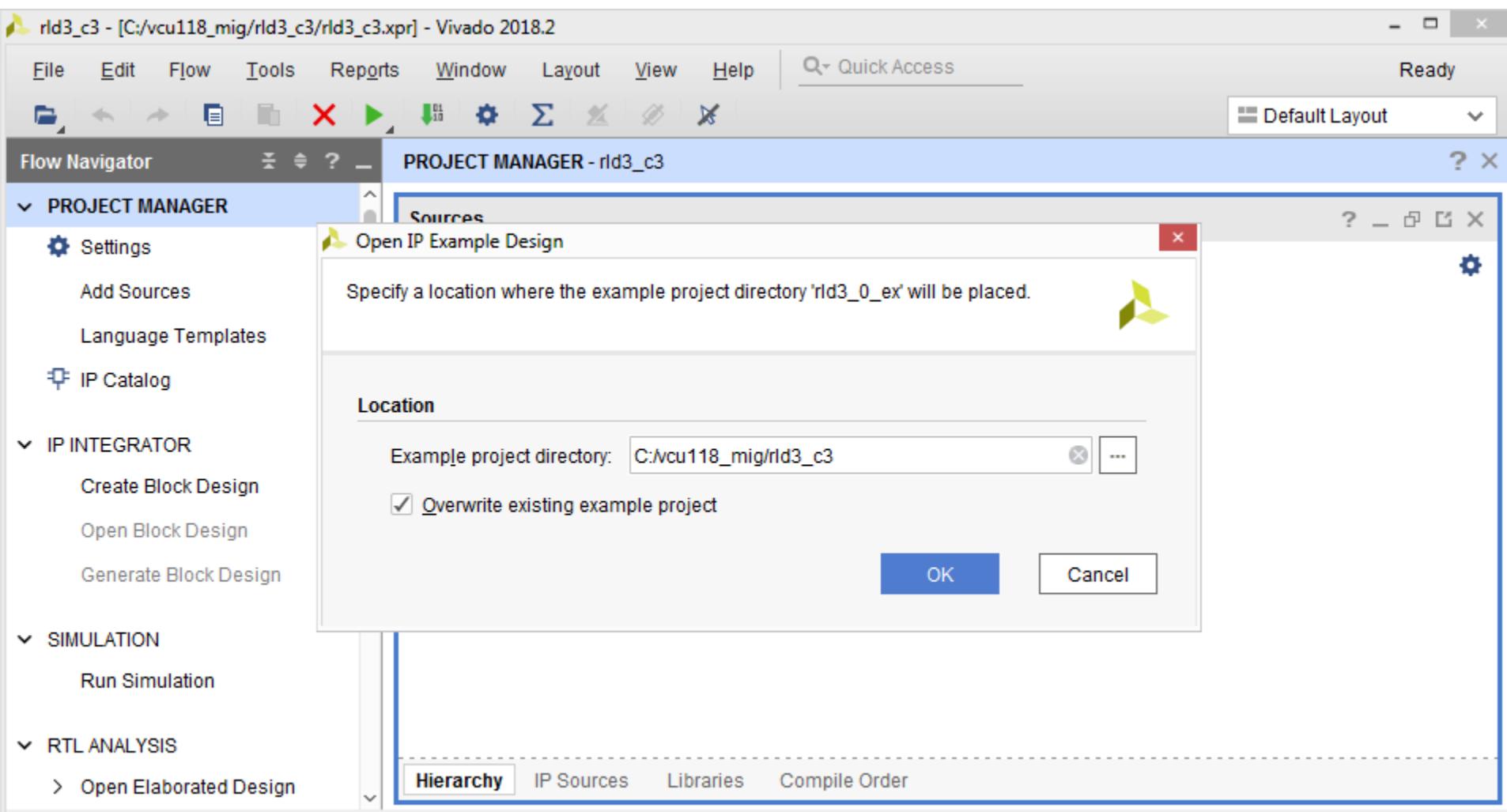
- > Right click on rld3_0 and select Open IP Example Design...



Note: Presentation applies to the VCU118

Compile Example Design

- > Set the location to C:/vcu118_mig/rld3_c3 and click OK



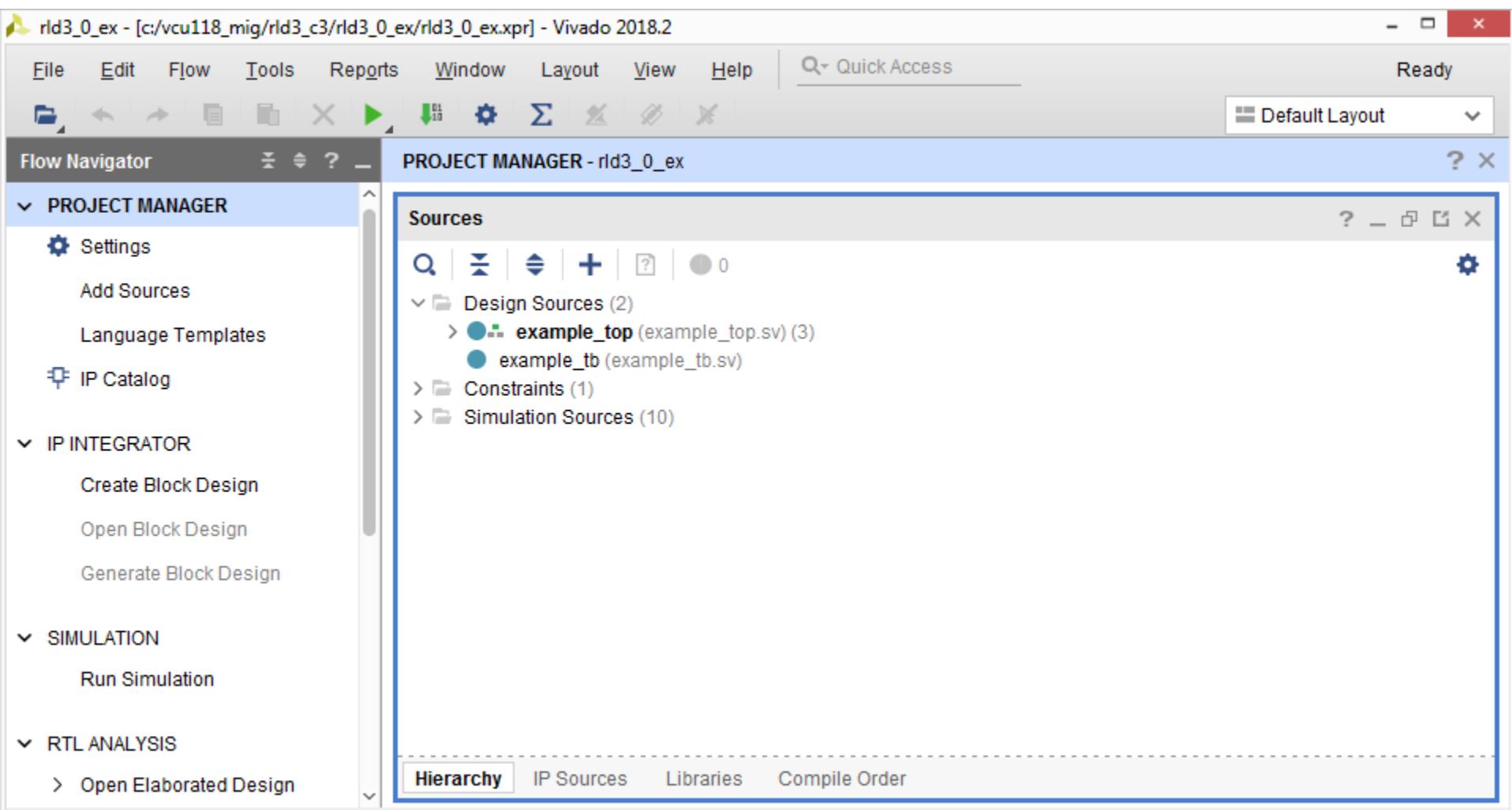
Open Example

Note: Presentation applies to the VCU118

 XILINX

Compile Example Design

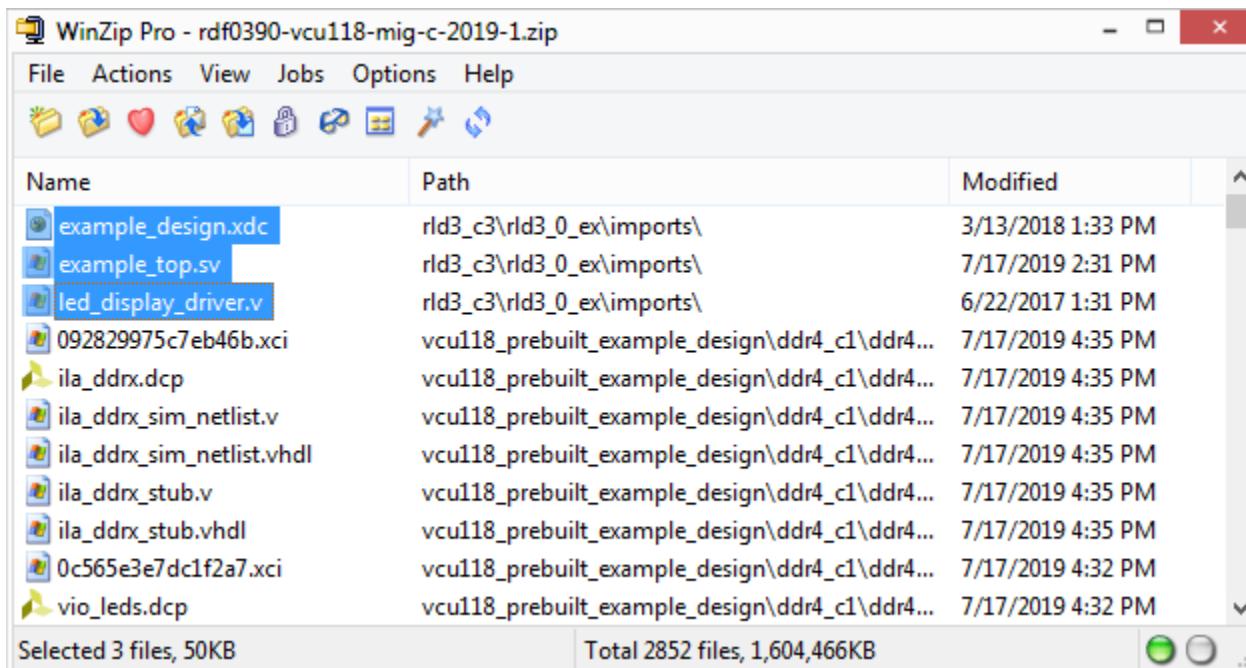
- > A new project is created under <design path>/



Note: The original project window can be closed

Modifications to Example Design

- > From the **RDF0390 - VCU118 MIG Design Files (2019.1 C) ZIP file**
 - » Extract the rld3_c3 files, example_design.xdc, example_top.sv, and led_display_driver.v
 - » Overwrite these three existing files in your rld3_c3 MIG design
 - » Do this after creating the Example Design; changes only affect the Example Design



Modifications to Example Design

> Modifications to the example design

- » Added RTL and XDC modifications to drive LEDs and AR66800
- » The following commands will add the led_display_driver.v and create the required VIO IP
- » From the Tcl Console, run these commands:

```
add_files -norecurse
```

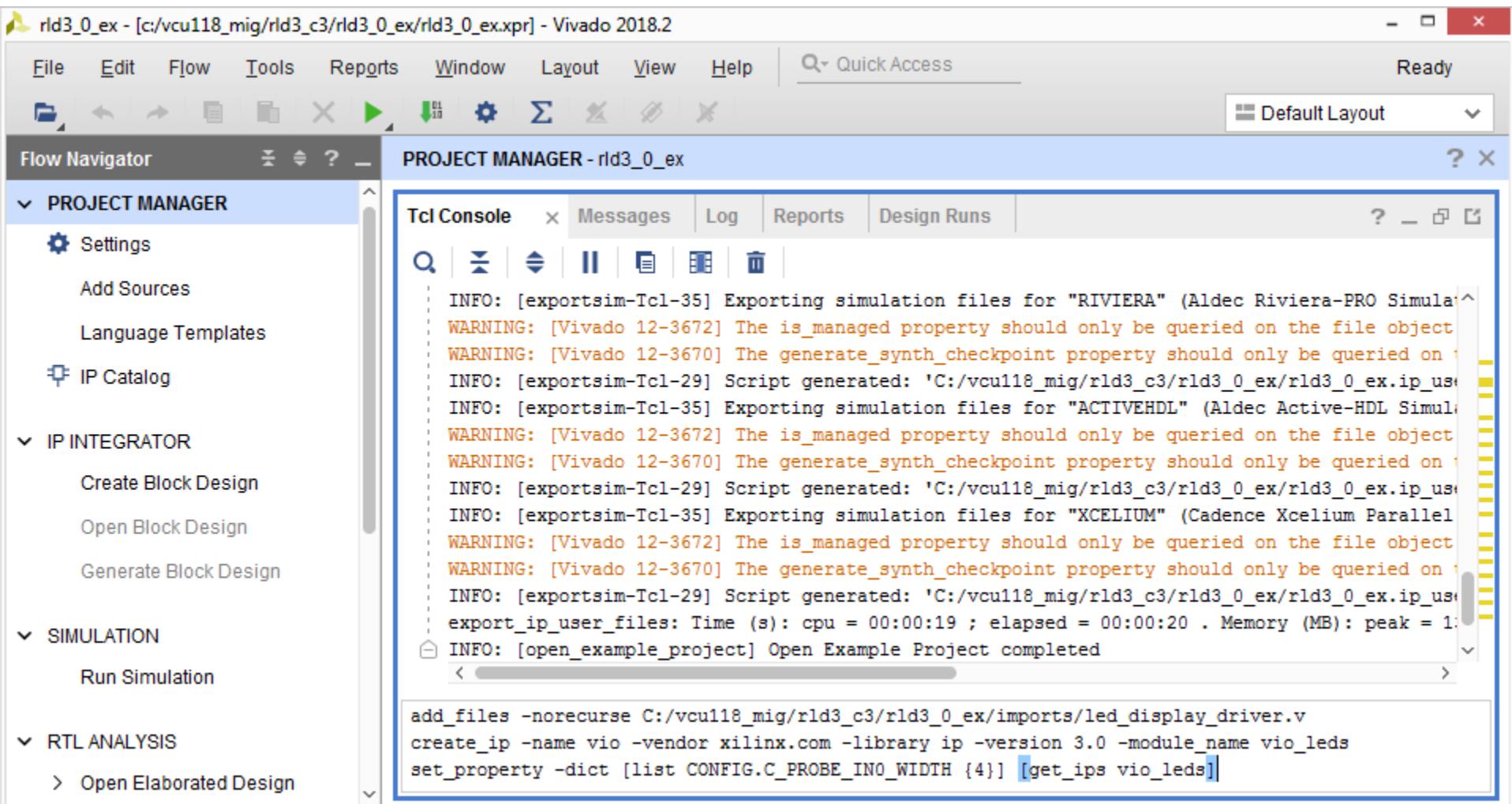
```
C:/vcu118_mig/rld3_c3/rld3_0_ex/imports/led_display_driver.v
```

```
create_ip -name vio -vendor xilinx.com -library ip -version 3.0 -module_name  
vio_leds
```

```
set_property -dict [list CONFIG.C_PROBE_IN0_WIDTH {4}] [get_ips vio_leds]
```

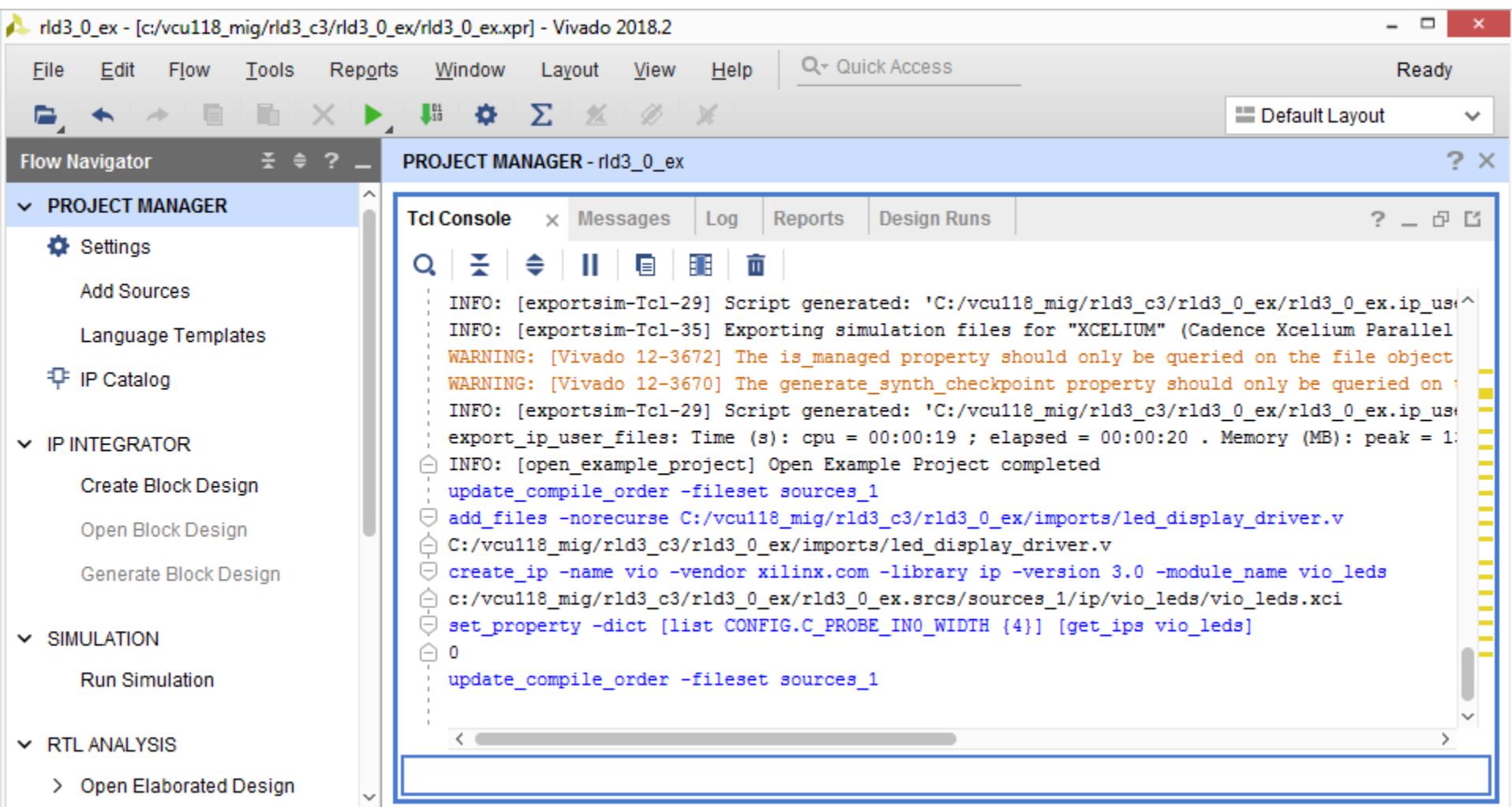
Modifications to Example Design

- > Press enter after entering Tcl commands



Modifications to Example Design

- > Tcl commands completed successfully

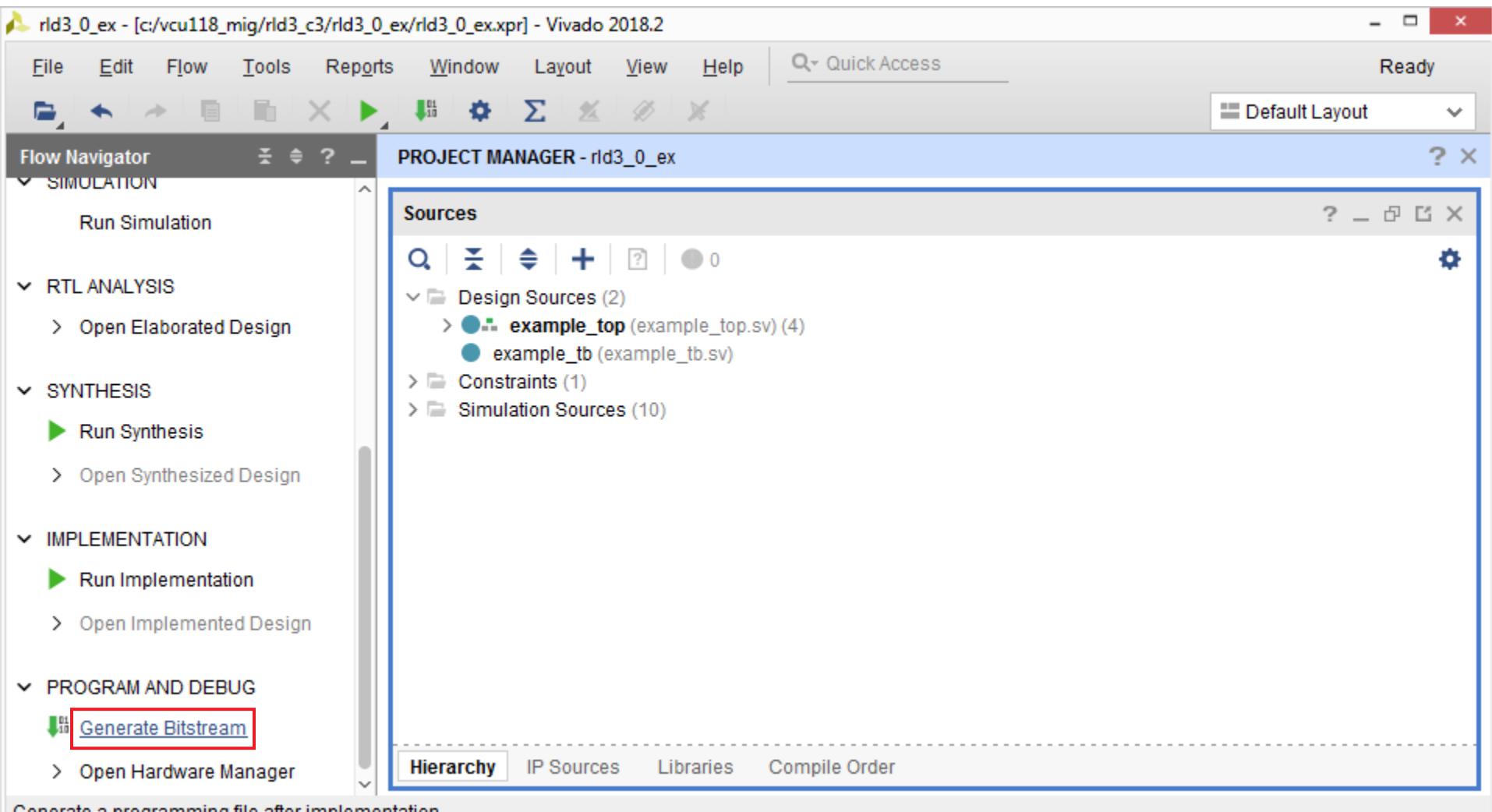


The screenshot shows the Vivado 2018.2 interface with the project "rld3_0_ex" open. The left sidebar contains the Project Manager, IP Integrator, Simulation, and RTL Analysis sections. The main area is the PROJECT MANAGER - rld3_0_ex window, which includes tabs for Tcl Console, Messages, Log, Reports, and Design Runs. The Tcl Console tab is active, displaying the following command history:

```
INFO: [exportsim-Tcl-29] Script generated: 'C:/vcu118_mig/rld3_c3/rld3_0_ex/rld3_0_ex.ip_user_files'
INFO: [exportsim-Tcl-35] Exporting simulation files for "XCELIUM" (Cadence Xcelium Parallel)
WARNING: [Vivado 12-3672] The is_managed property should only be queried on the file object
WARNING: [Vivado 12-3670] The generate_synth_checkpoint property should only be queried on t
INFO: [exportsim-Tcl-29] Script generated: 'C:/vcu118_mig/rld3_c3/rld3_0_ex/rld3_0_ex.ip_user_files'
export_ip_user_files: Time (s): cpu = 00:00:19 ; elapsed = 00:00:20 . Memory (MB): peak = 1
INFO: [open_example_project] Open Example Project completed
update_compile_order -fileset sources_1
add_files -norecurse C:/vcu118_mig/rld3_c3/rld3_0_ex/imports/led_display_driver.v
C:/vcu118_mig/rld3_c3/rld3_0_ex/imports/led_display_driver.v
create_ip -name vio -vendor xilinx.com -library ip -version 3.0 -module_name vio_leds
c:/vcu118_mig/rld3_c3/rld3_0_ex/rld3_0_ex.srcs/sources_1/ip/vio_leds/vio_leds.xci
set_property -dict [list CONFIG.C_PROBE_IN0_WIDTH {4}] [get_ips vio_leds]
0
update_compile_order -fileset sources_1
```

Compile Example Design

- > Click on Generate Bitstream

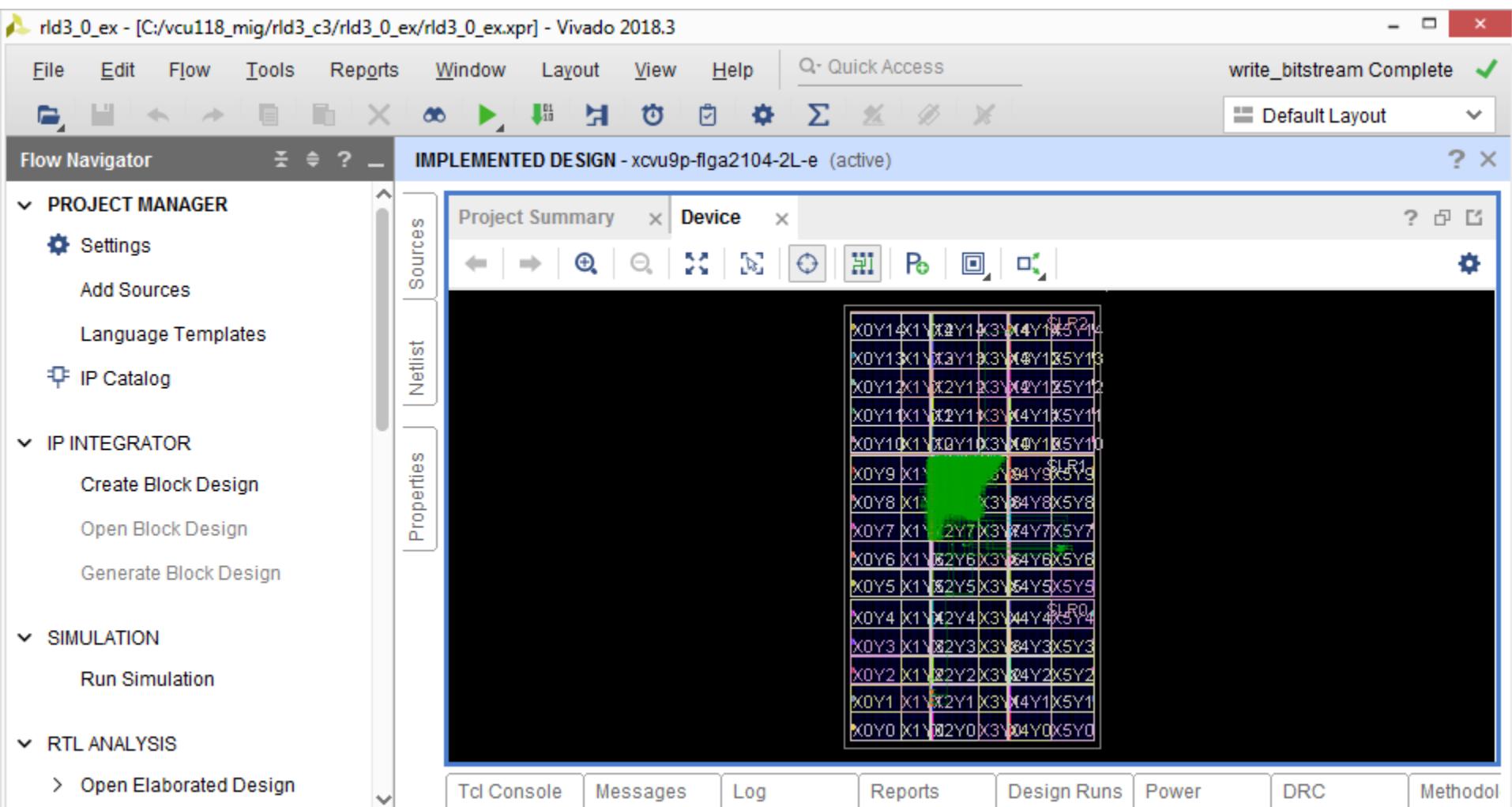


Generate a programming file after implementation

Note: Presentation applies to the VCU118

Compile Example Design

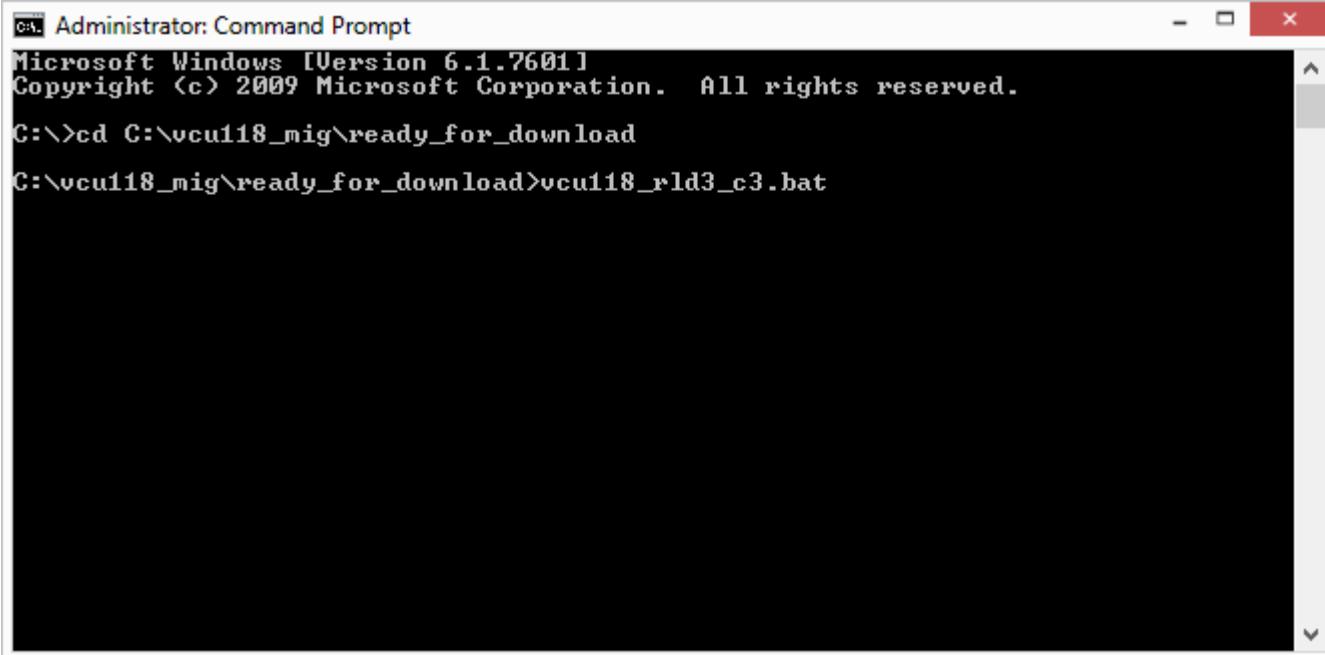
- > Open and view the Implemented Design



Run MIG Example Design

- > From a Command Prompt, type:

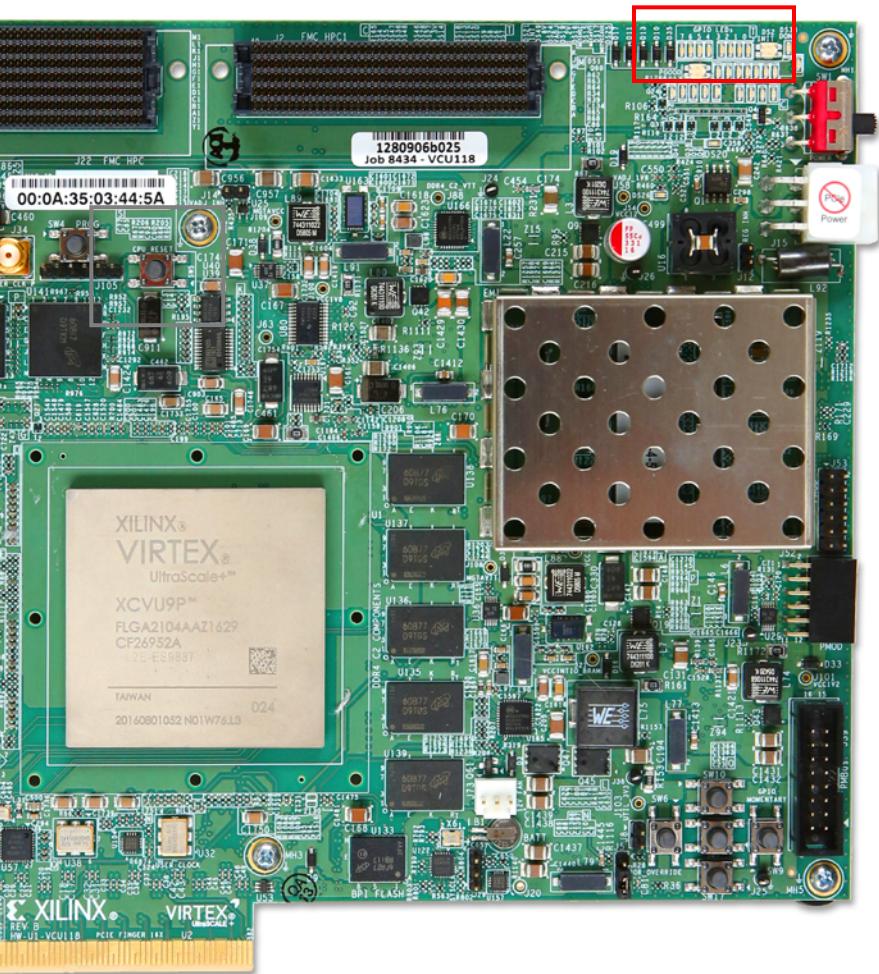
```
cd C:\vcu118_mig\ready_for_download  
vcu118_rld3_c3.bat
```



The screenshot shows a Windows Command Prompt window titled "Administrator: Command Prompt". The window is running on Microsoft Windows [Version 6.1.7601]. The user has navigated to the directory C:\vcu118_mig\ready_for_download and executed the batch file vcu118_rld3_c3.bat. The command history in the window shows:

```
C:\>cd C:\vcu118_mig\ready_for_download  
C:\vcu118_mig\ready_for_download>vcu118_rld3_c3.bat
```

Run MIG Example Design



- > After bitstream loads, LED 0 (right most LED) will be lit, and LED1 will be blinking
- > LED 3 will light and stay on
 - » This indicates Calibration has completed
- > If an error occurs, LED 0 will go out and LED 2 will light
 - » The “CPU_RESET” button, SW5, is the reset

References



References

> Virtex UltraScale Memory

- » UltraScale FPGA Memory Interface Solutions Product Guide – PG150
 - https://www.xilinx.com/support/documentation/ip_documentation/ultrascale_memory_ip/v1_4/pg150-ultrascale-memory-ip.pdf

> Vivado Release Notes

- » Vivado Design Suite User Guide - Release Notes – UG973
 - https://www.xilinx.com/support/documentation/sw_manuals/xilinx2019_1/ug973-vivado-release-notes-install-license.pdf
- » Vivado Design Suite 2019 - Vivado Known Issues
 - <https://www.xilinx.com/support/answers/72162.html>

> Vivado Programming and Debugging

- » Vivado Design Suite Programming and Debugging User Guide – UG908
 - https://www.xilinx.com/support/documentation/sw_manuals/xilinx2019_1/ug908-vivado-programming-debugging.pdf

Documentation



Documentation

- > **Virtex UltraScale+**
 - » Virtex UltraScale+ FPGA Family
 - <https://www.xilinx.com/products/silicon-devices/fpga/virtex-ultrascale-plus.html>
- > **VCU118 Documentation**
 - » Virtex UltraScale+ FPGA VCU118 Evaluation Kit
 - <https://www.xilinx.com/products/boards-and-kits/vcu118.html>
 - » VCU118 Board User Guide – UG1224
 - https://www.xilinx.com/support/documentation/boards_and_kits/vcu118/ug1224-vcu118-eval-bd.pdf
 - » VCU118 Evaluation Kit Quick Start Guide User Guide – XTP453
 - https://www.xilinx.com/support/documentation/boards_and_kits/vcu118/xtp453-vcu118-quickstart.pdf
 - » VCU118 - Known Issues and Release Notes Master Answer Record
 - <https://www.xilinx.com/support/answers/68268.html>