

VCU118 PCIe Design Creation

May 2019



Revision History

Date	Version	Description
05/29/19	9.0	Updated for 2019.1. Some screenshots not updated.
12/10/18	8.0	Updated for 2018.3. Some screenshots not updated.
06/18/18	7.0	Updated for 2018.2.
04/09/18	6.0	Updated for 2018.1.
12/20/17	5.0	Updated for 2017.4.
10/26/17	4.0	Updated for 2017.3.1. For Rev 2.0, with Production Silicon, and QSPI Flash devices.
06/20/17	3.0	Updated for 2017.2.
04/19/17	2.0	Updated for 2017.1.
12/19/16	1.0	Initial version for 2016.4.

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Overview

- > **Virtex UltraScale PCIe x16 Gen 3 Capability**
- > **Xilinx VCU118 Board**
- > **Software Requirements**
- > **VCU118 Setup**
- > **Generate x16 Gen 3 PCIe Core**
 - » Modify PCIe Core
 - » Compile Example Design
 - » Generate PCIe MCS File
 - » Program QSPI Flash with PCIe Design
- > **Running the PCIe x16 Gen 3 Design**
- > **References**

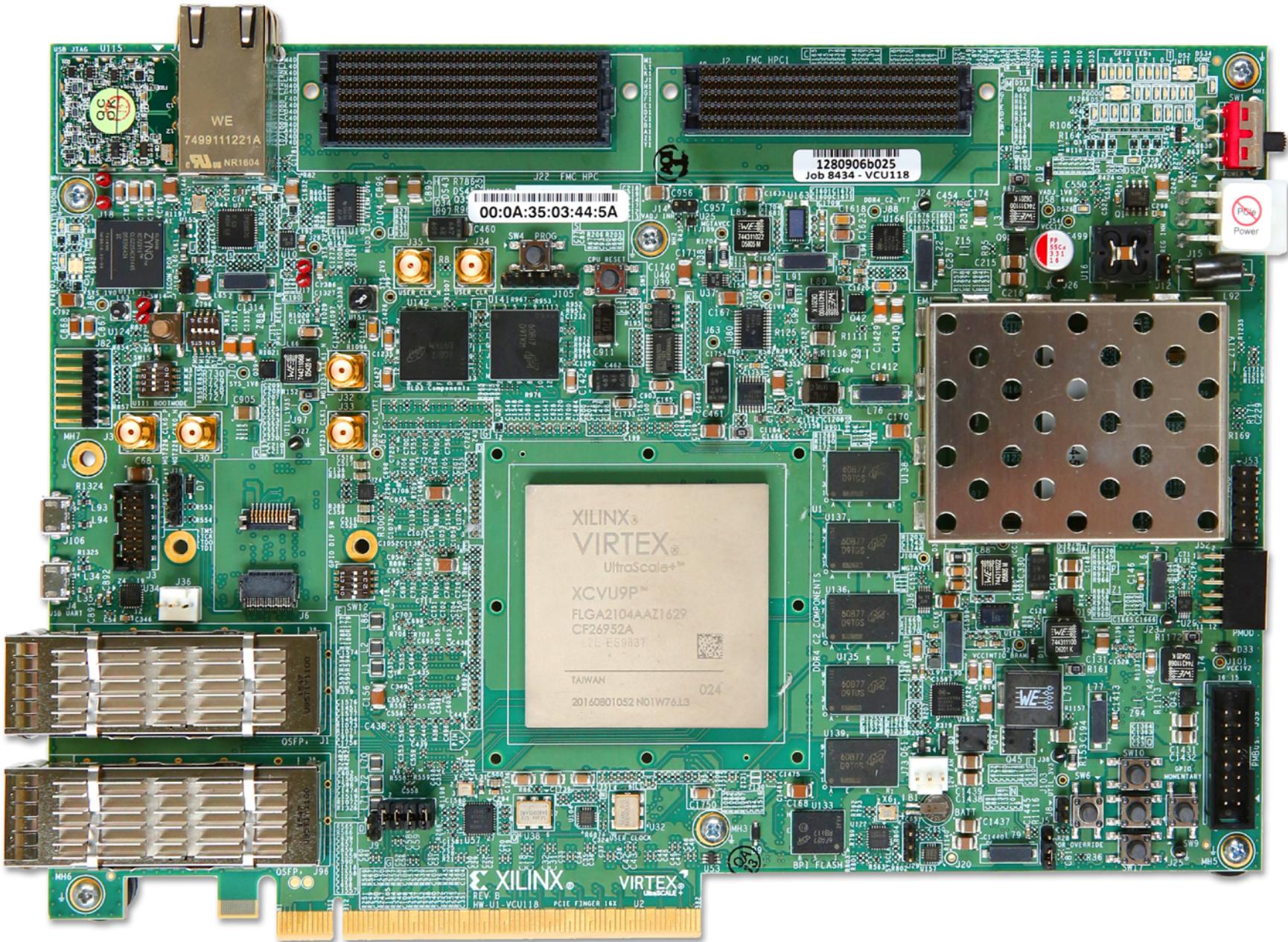
Virtex UltraScale PCIe x16 Gen 3 Capability

- > **VCU118 Supports PCIe Gen1, Gen2, and Gen3 Capability**
 - » x16, x8, x4, x2, or x1 in Gen1, Gen2, and Gen3 lane widths
 - » As per [PG213](#) for -2L speed grade
 - » Note: Gen3 x16 requires VCCINT set to 0.85 V; VCU118 Rev 2.x boards are shipped with VCCINT set to 0.85 V
- > **LogiCORE PIO Example Design**
 - » RDF0392 - VCU118 PCIe Design Files (2019.1 C) ZIP file
- > **UltraScale Integrated Block for PCI Express**
 - » See [PG213](#) for details

Virtex UltraScale PCIe x16 Gen 3 Capability

- > **Integrated Block for PCI Express**
 - » PCI Express 3.0 Specification
- > **Configurable for Endpoint or Root Port Applications**
 - » VCU118 configured for Endpoint Applications
- > **GTH Transceivers implement a fully compliant PHY**
- > **Large range of maximum payload size**
 - » 128 / 256 / 512 / 1024 bytes
- > **Configurable BAR spaces**
 - » Up to 6 x 32 bit, 3 x 64 bit, or a combination
 - » Memory or IO
 - » BAR and ID filtering
- > **Management and Statistics Interface**

Xilinx VCU118 Board



VCU118 Software Install and Board Setup

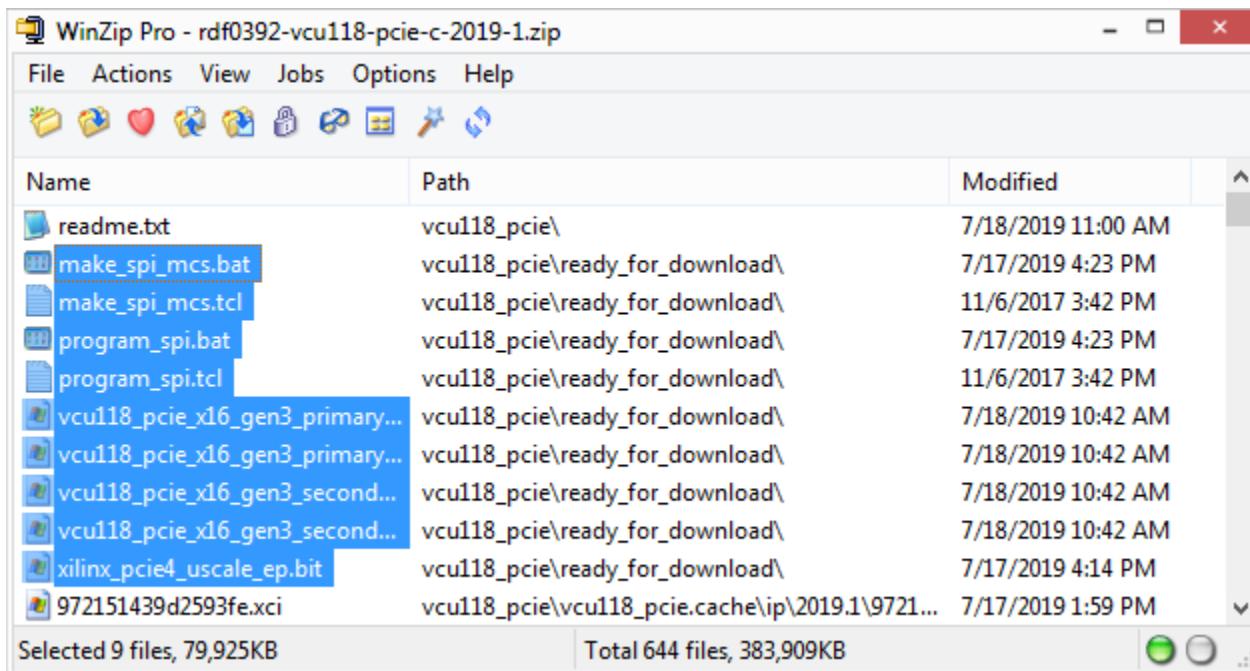
- > Complete setup steps in XTP449 – VCU118 Software Install and Board Setup:

- » Software Requirements
- » VCU118 Board Setup
- » UART Driver Install
- » Optional Hardware Setup



Files needed for PCIe design

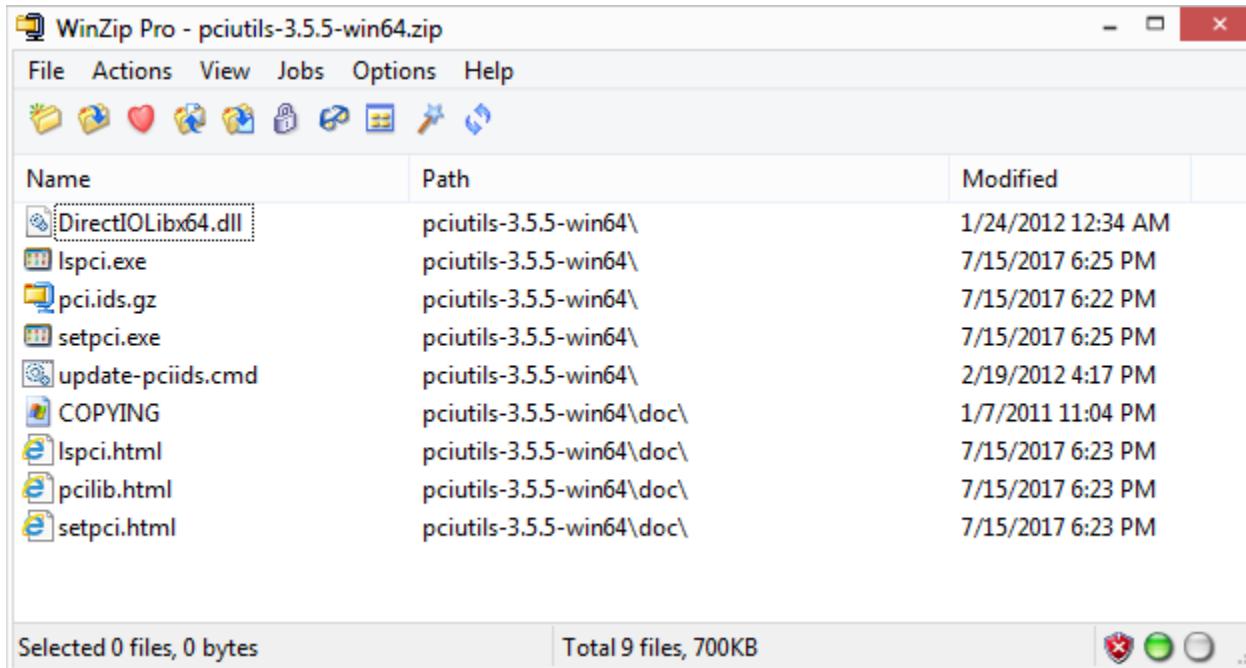
- > Open the VCU118 PCIe Design Files (2019.1 C) ZIP file, and extract these files to your C:\ drive:
 - » vcu118_PCIE\ready_for_download*



Ispci Software Requirement

> Ispci for Windows

- » Free [download](#)
- » Unzip to the C:\ drive of the test PC



Generate x16 Gen 3 PCIe Core

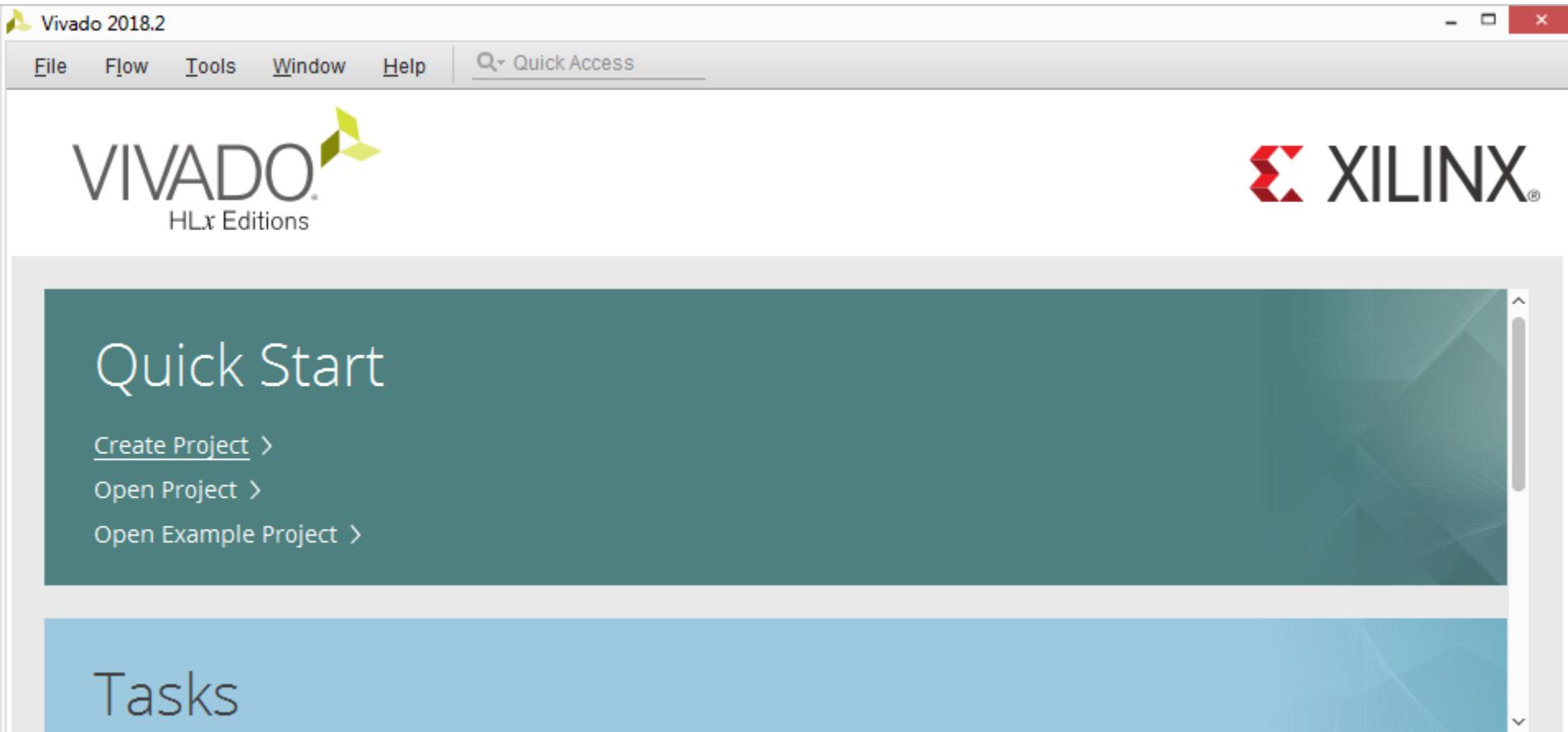


Generate x16 Gen 3 PCIe Core

> Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2019.1 → Vivado

> Select Create Project



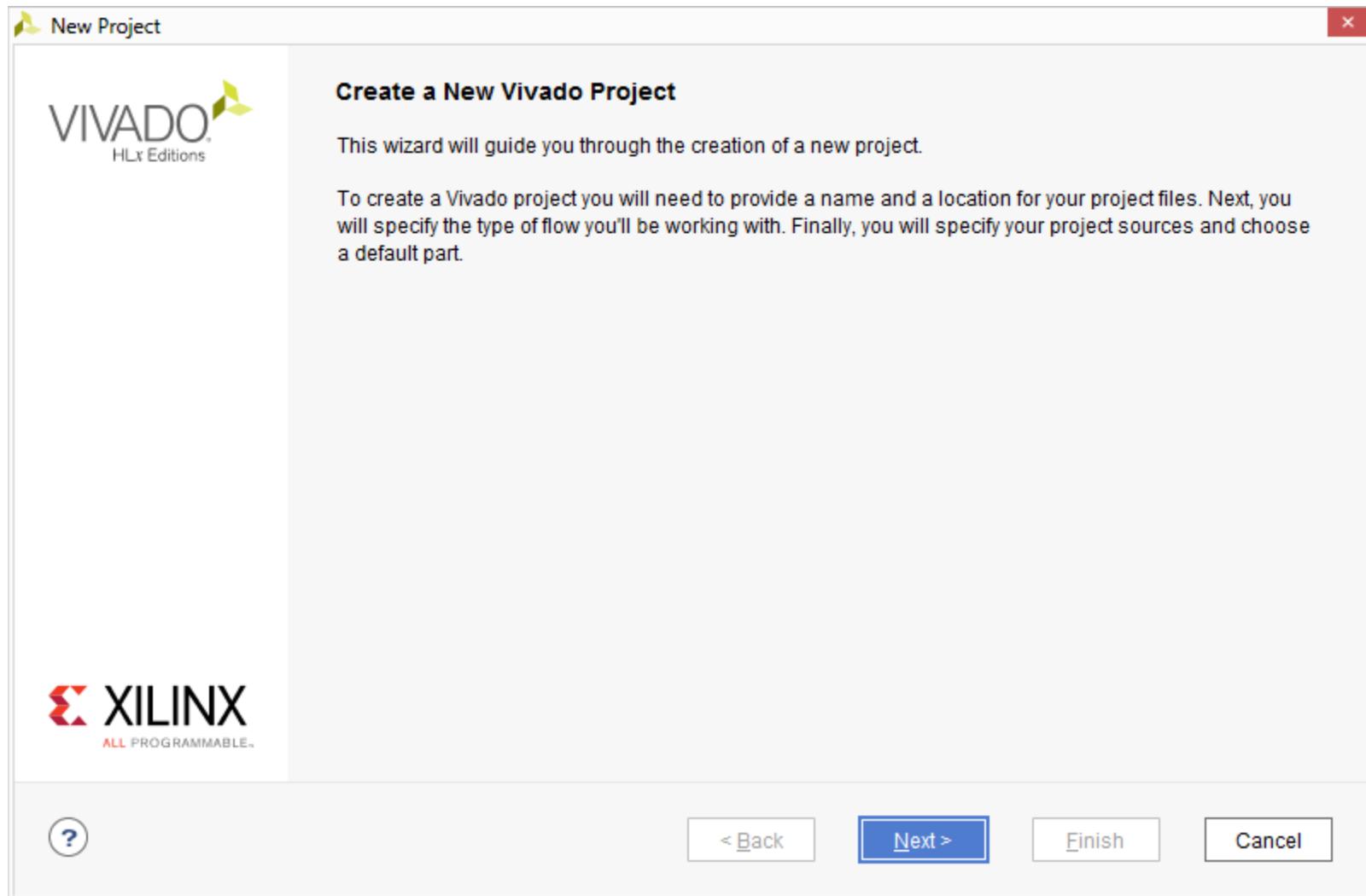
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Note: Presentation applies to the VCU118

XILINX

Generate x16 Gen 3 PCIe Core

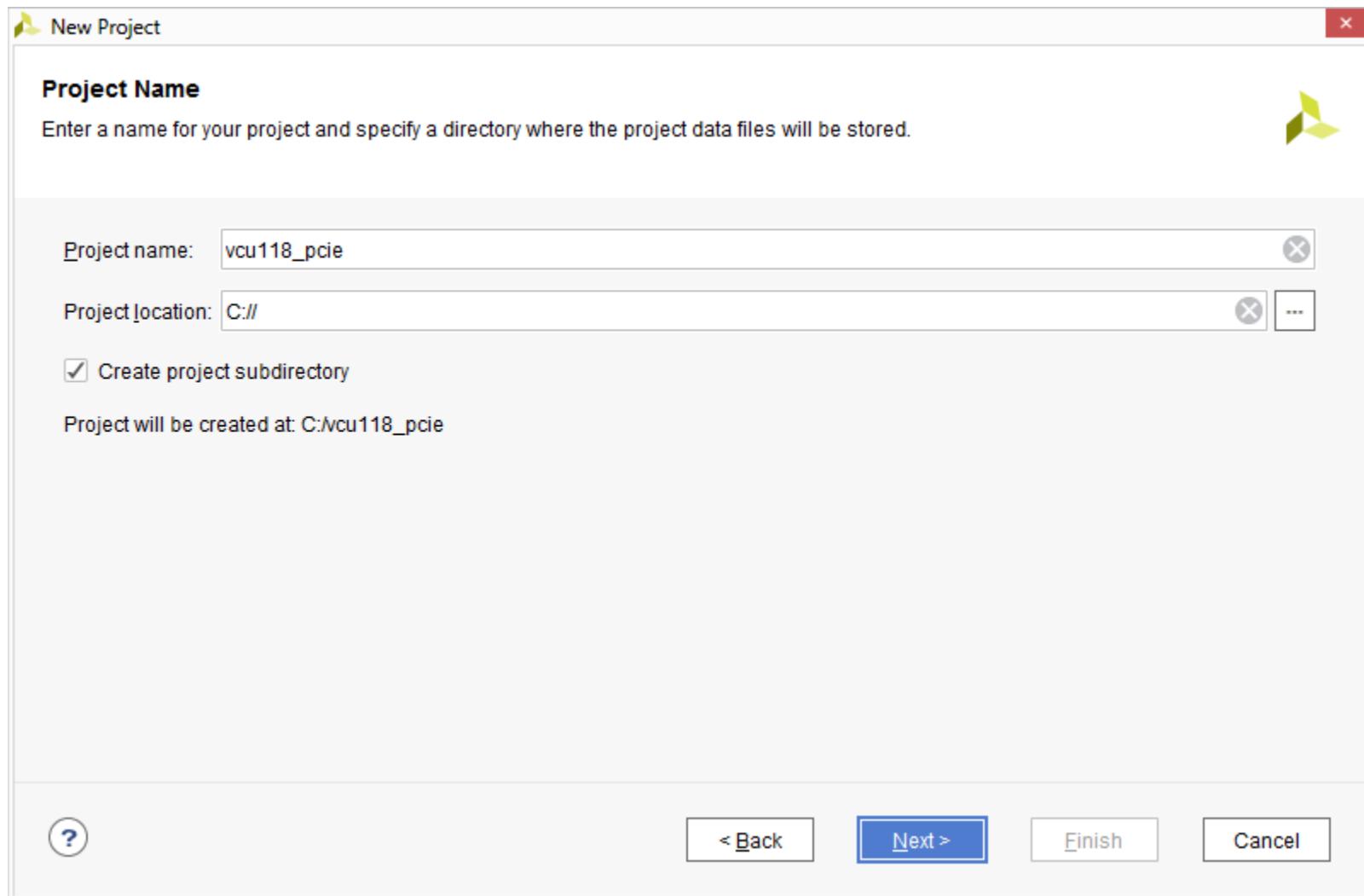
> Click Next



Generate x16 Gen 3 PCIe Core

- > Set the Project name and location to vcu118_pcie and C:\

- » Check Create project subdirectory



Note: Vivado generally requires forward slashes in paths

Generate x16 Gen 3 PCIe Core

> Select RTL Project

» Select Do not specify sources at this time

New Project X

Project Type
Specify the type of project to create.

RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
 Do not specify sources at this time

Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.
 Do not specify sources at this time

I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.

Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.

Example Project
Create a new Vivado project from a predefined template.

? < Back Next > Finish Cancel

Generate x16 Gen 3 PCIe Core

- > Under Boards, select the VCU118 Evaluation Platform

New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Parts | Boards

Reset All Filters

Vendor: All Name: All

Search:

Display Name	Preview	Vendor	File V
Virtex UltraScale+ VCU118 Evaluation Platform		xilinx.com	2.0
Virtex UltraScale+ VCU1525 Acceleration Development Board		xilinx.com	1.1

< >

?

< Back

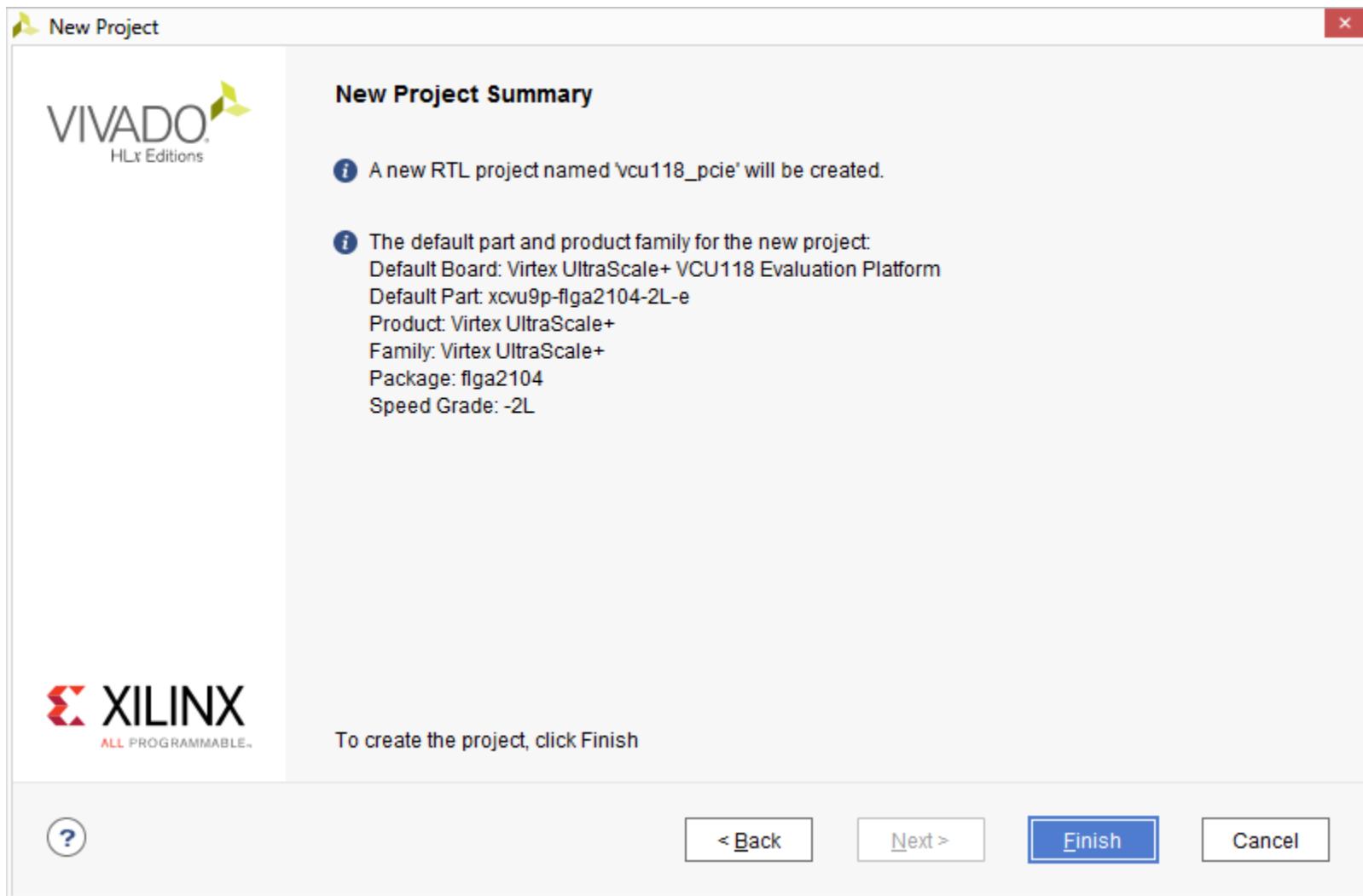
Next >

Finish

Cancel

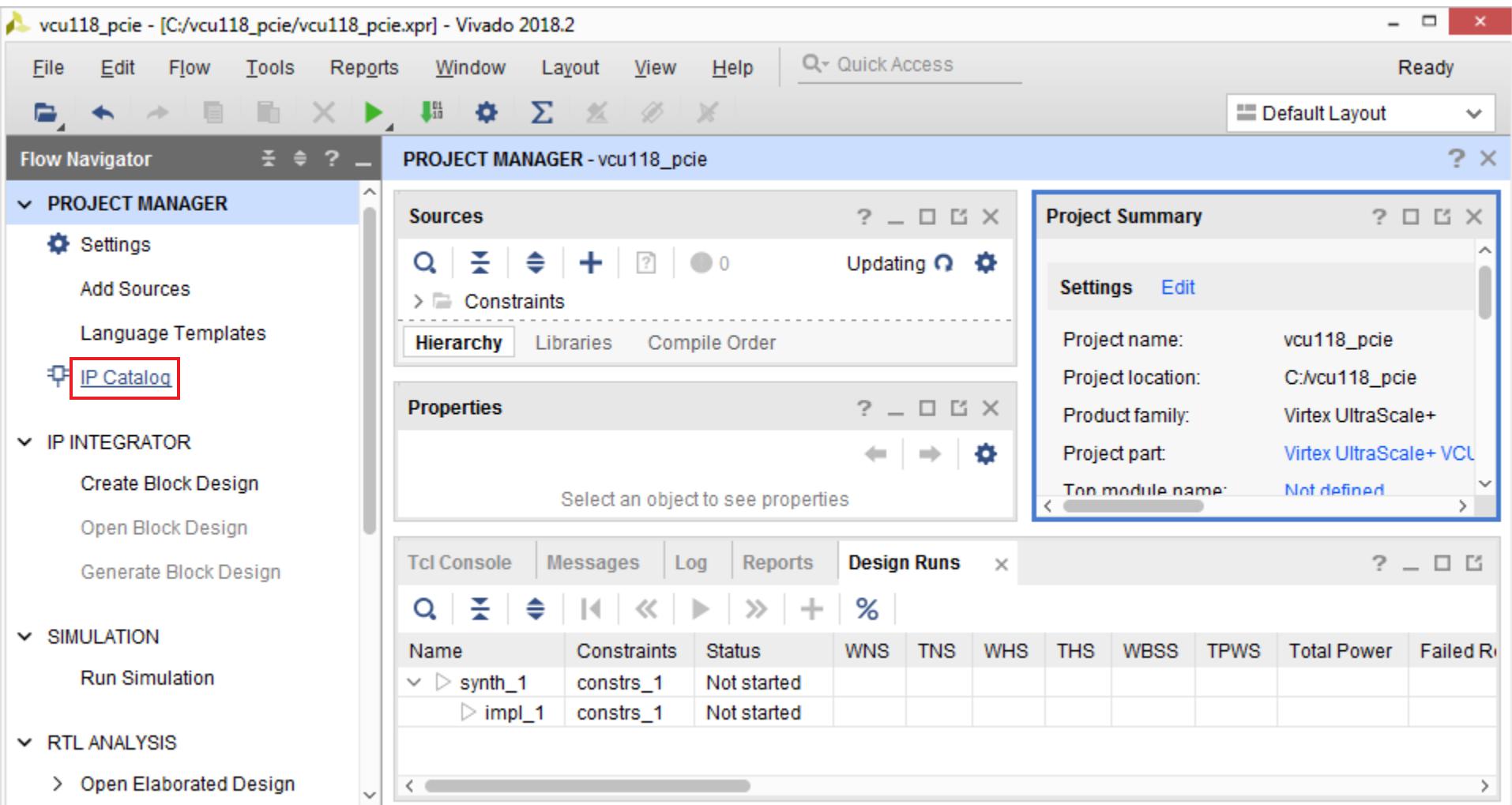
Generate x16 Gen 3 PCIe Core

> Click Finish



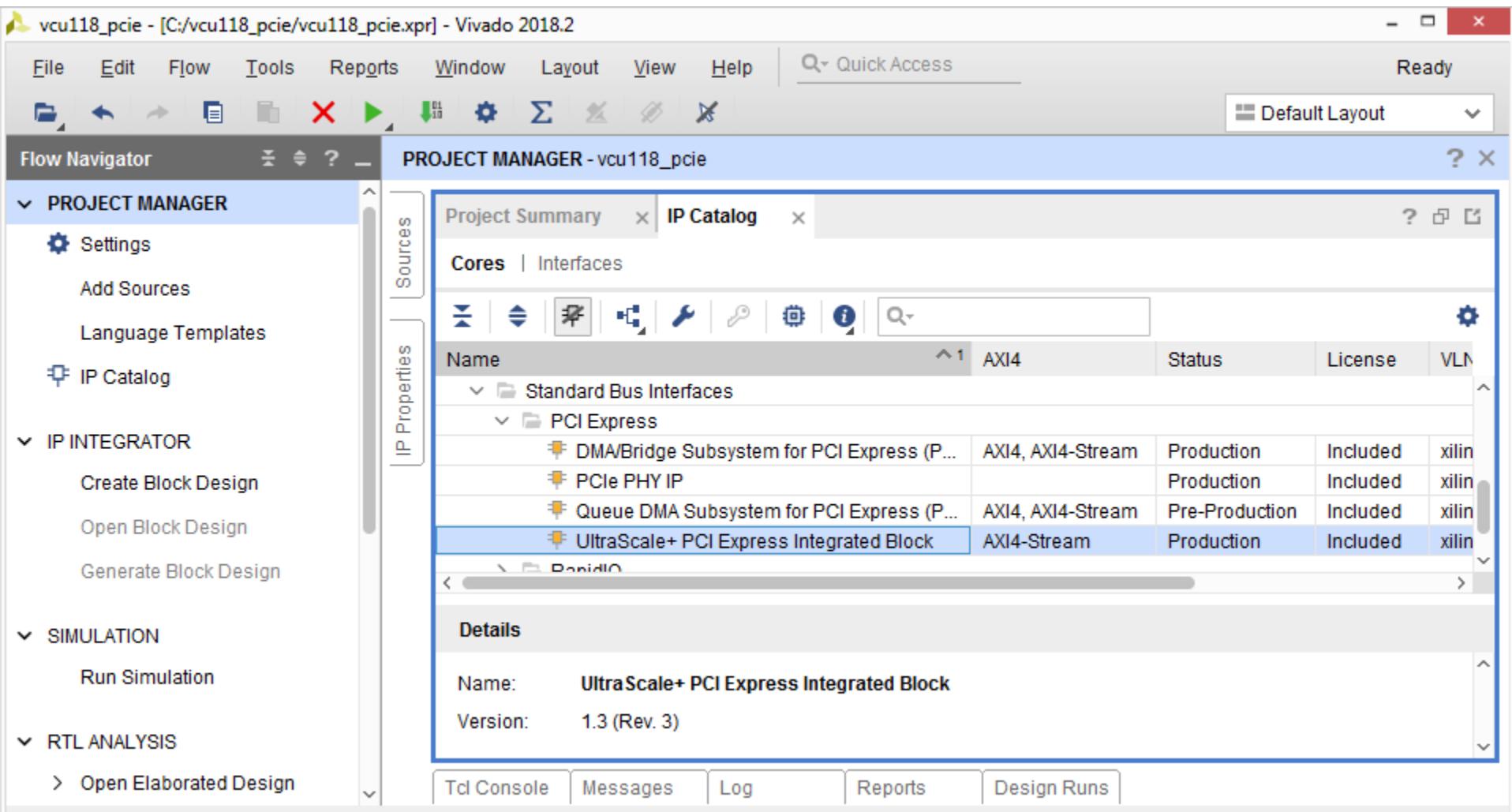
Generate x16 Gen 3 PCIe Core

> Click on IP Catalog



Generate x16 Gen 3 PCIe Core

- > Select UltraScale+ PCI Express Integrated Block, v1.3 under Standard Bus Interfaces

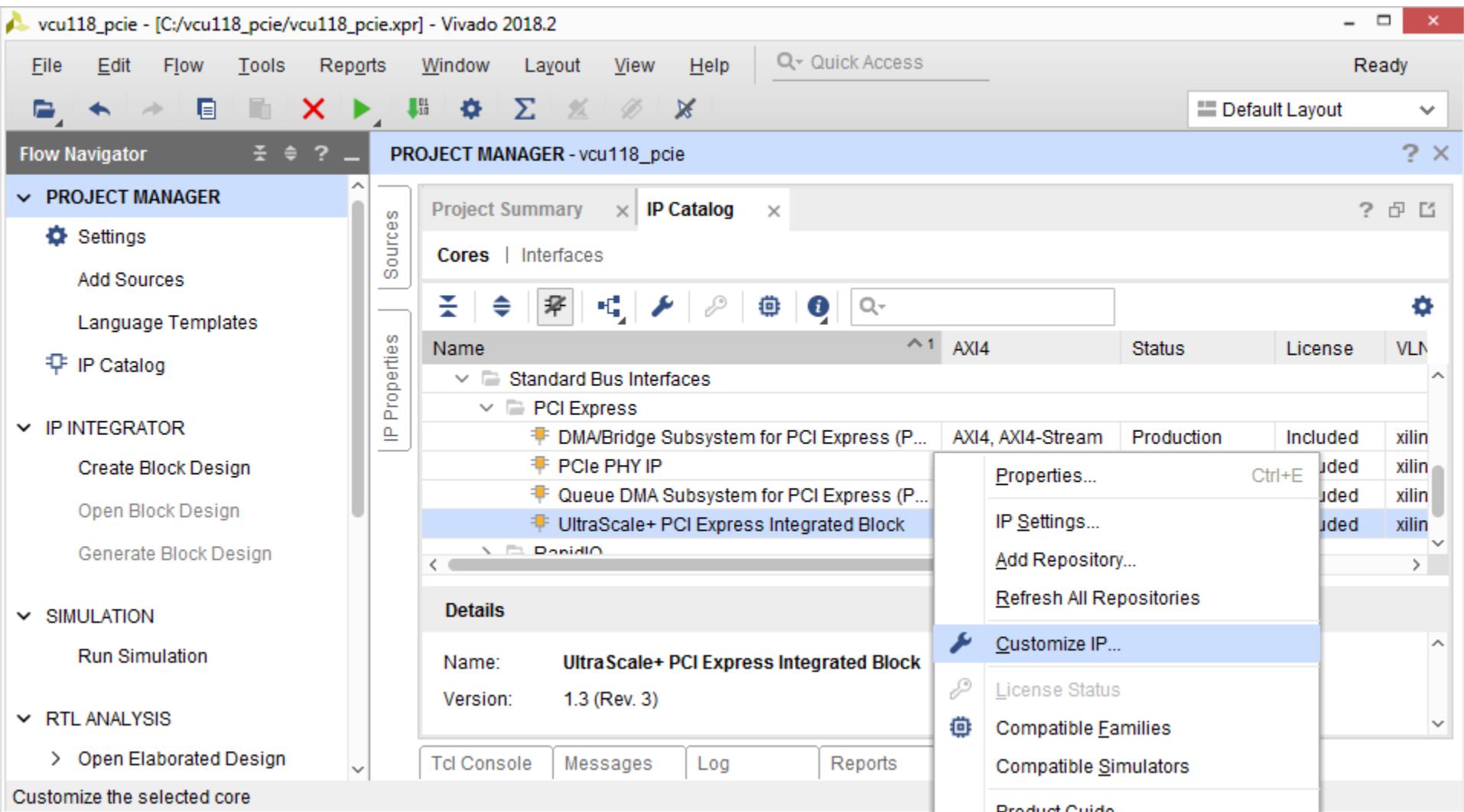


IP: UltraScale+ PCI Express Integrated Block

Note: Presentation applies to the VCU118

Generate x16 Gen 3 PCIe Core

- > Right click on UltraScale+ PCI Express Integrated Block and select Customize IP...

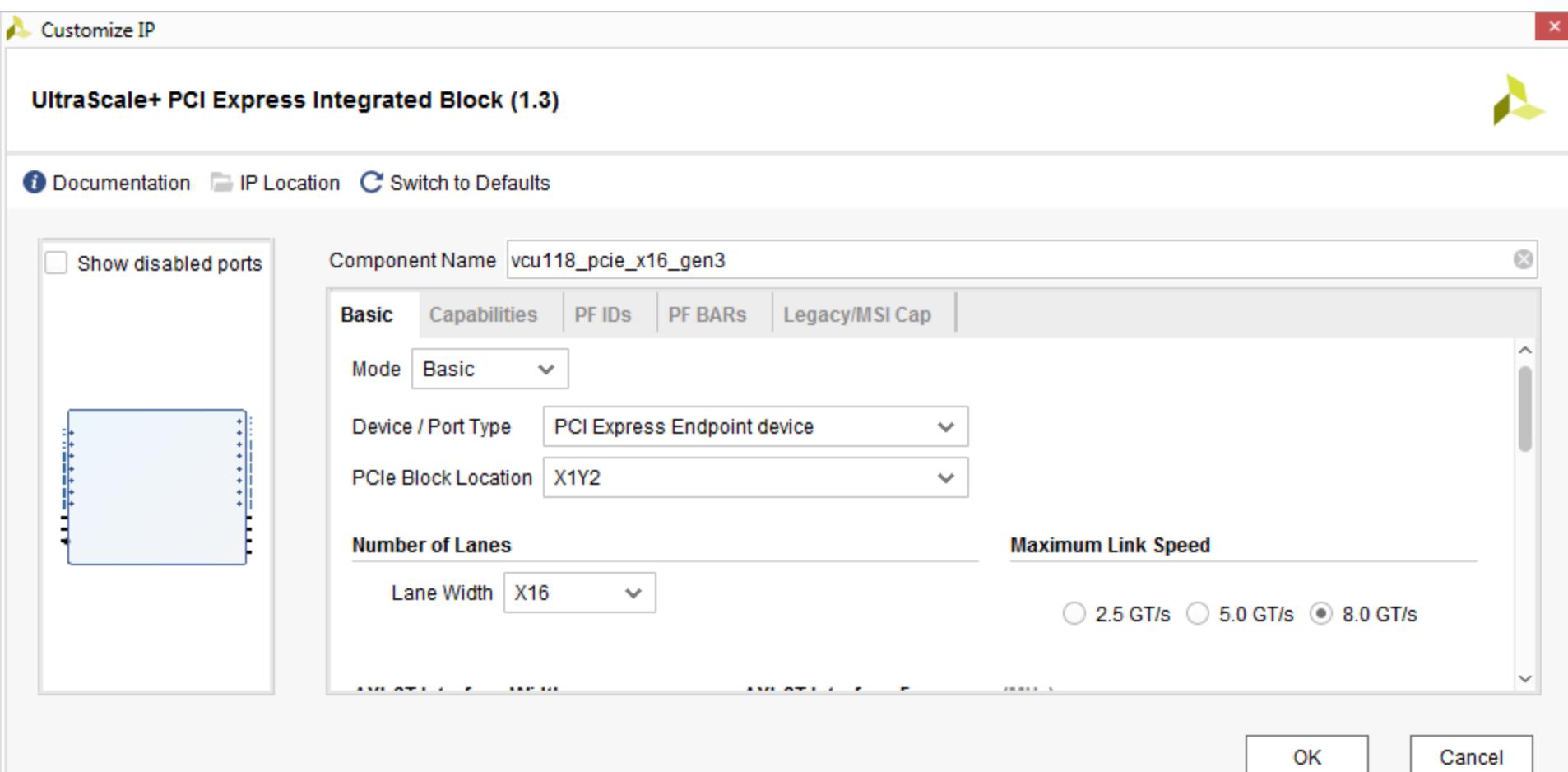


Note: Presentation applies to the VCU118

Generate x16 Gen 3 PCIe Core

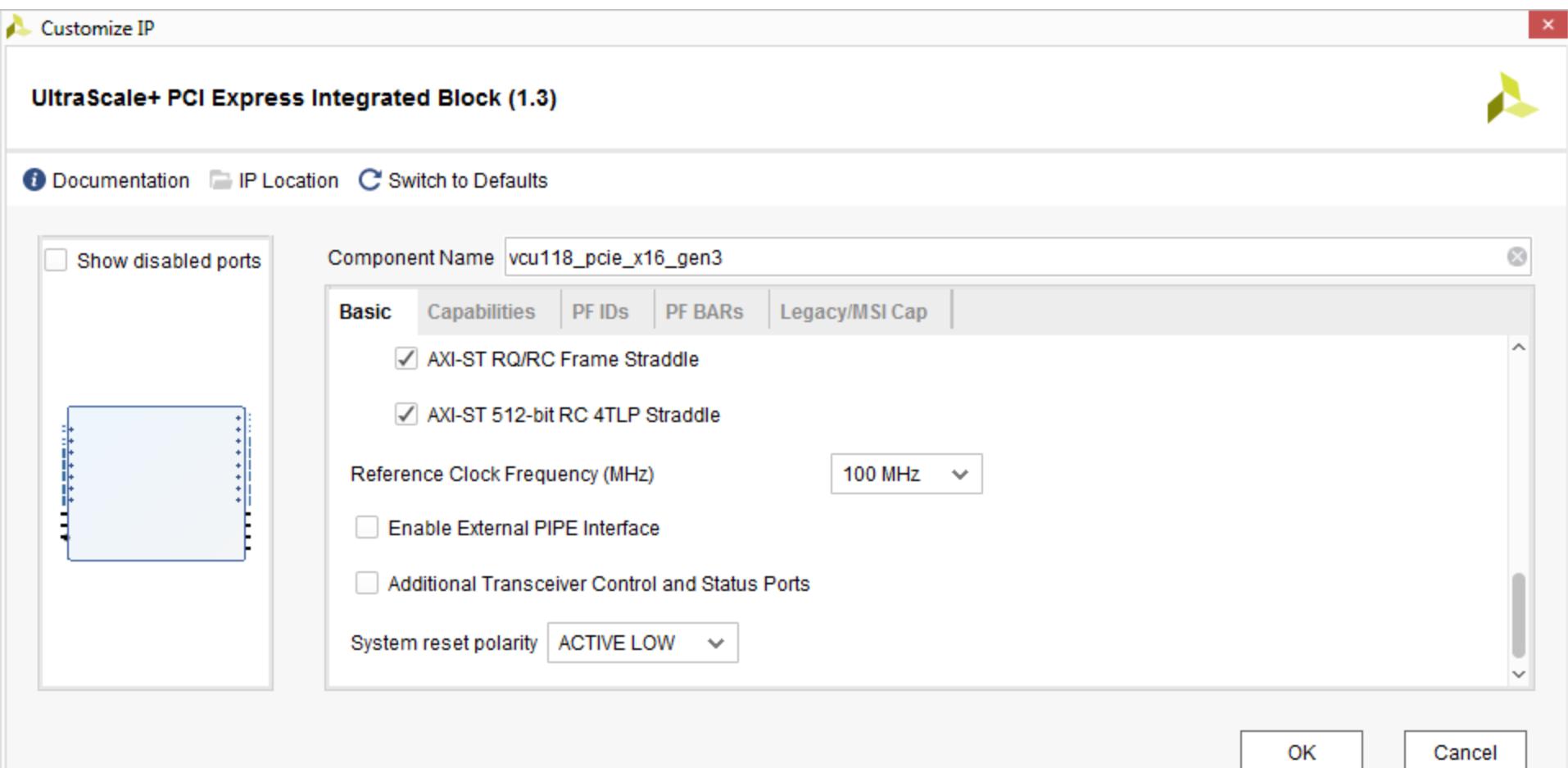
> Under the Basic tab,

- » Set Component name to **vcu118_pcie_x16_gen3**
- » Set the PCIe Block Location to **X1Y2**
- » Set the Max Link Speed to **8.0 GT/s**; set the Lane Width to **X16** and scroll down



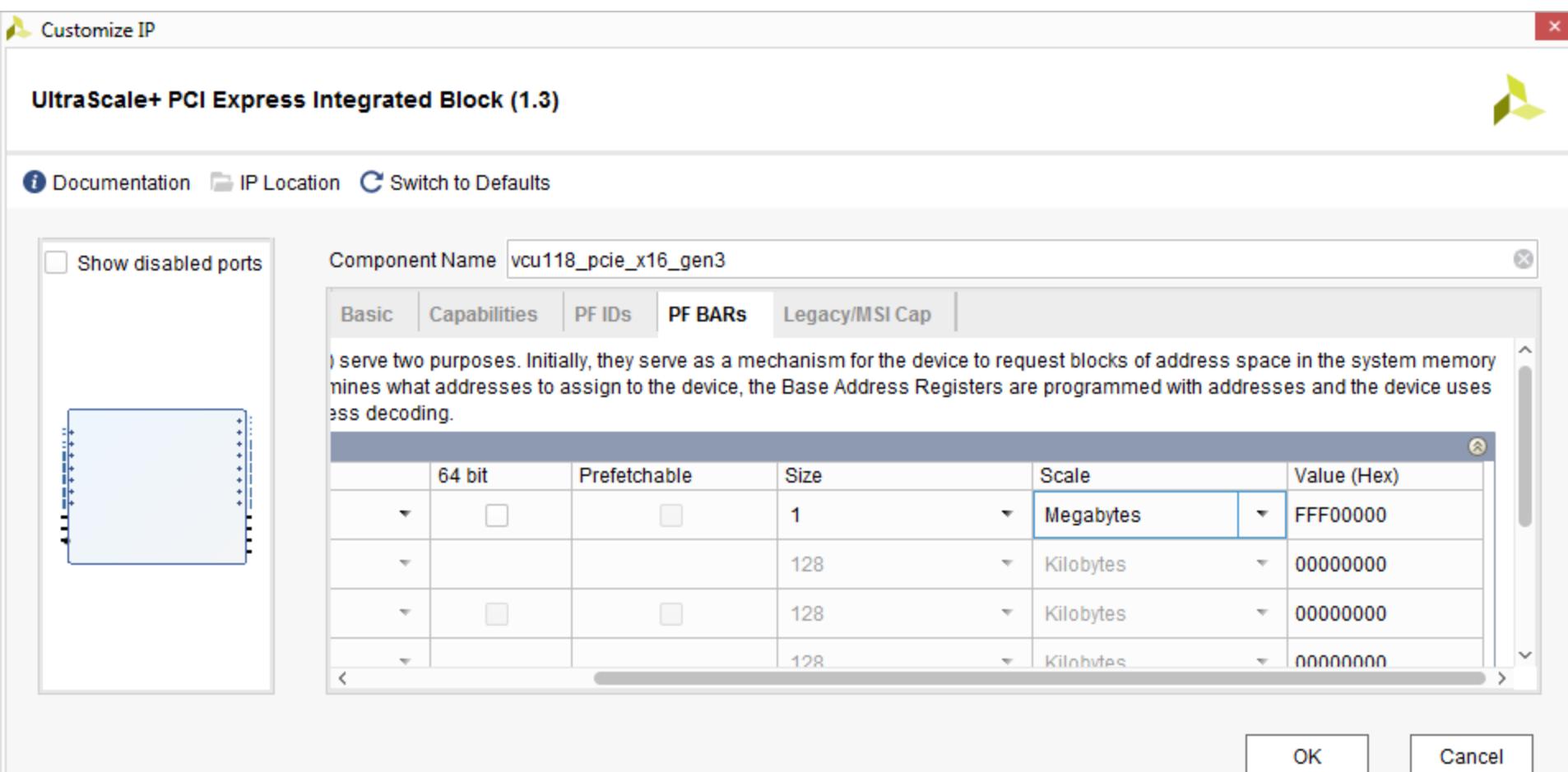
Generate x16 Gen 3 PCIe Core

- > Under the Basic tab,
 - » Set the Reference Clock to **100 MHz**
 - » Set the System reset polarity to **ACTIVE LOW**



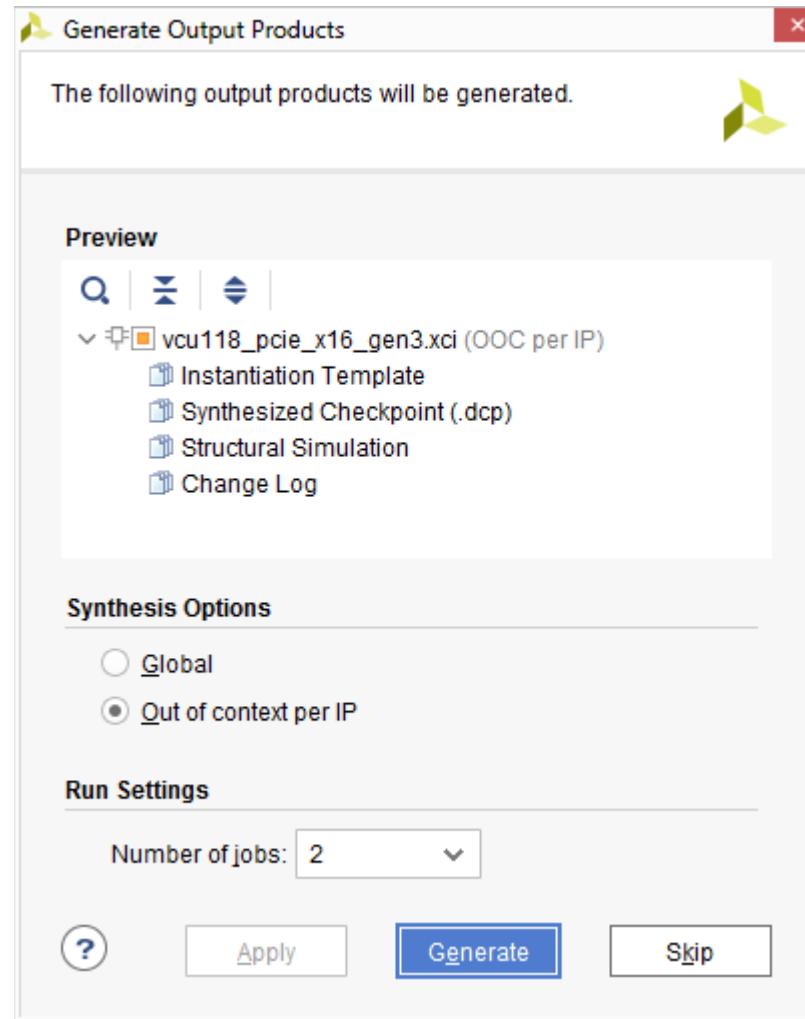
Generate x16 Gen 3 PCIe Core

- > Under the PF BAR tab, set the first Bar
 - » Set to 1 Megabytes
- > Click OK



Generate x16 Gen 3 PCIe Core

> Click Generate

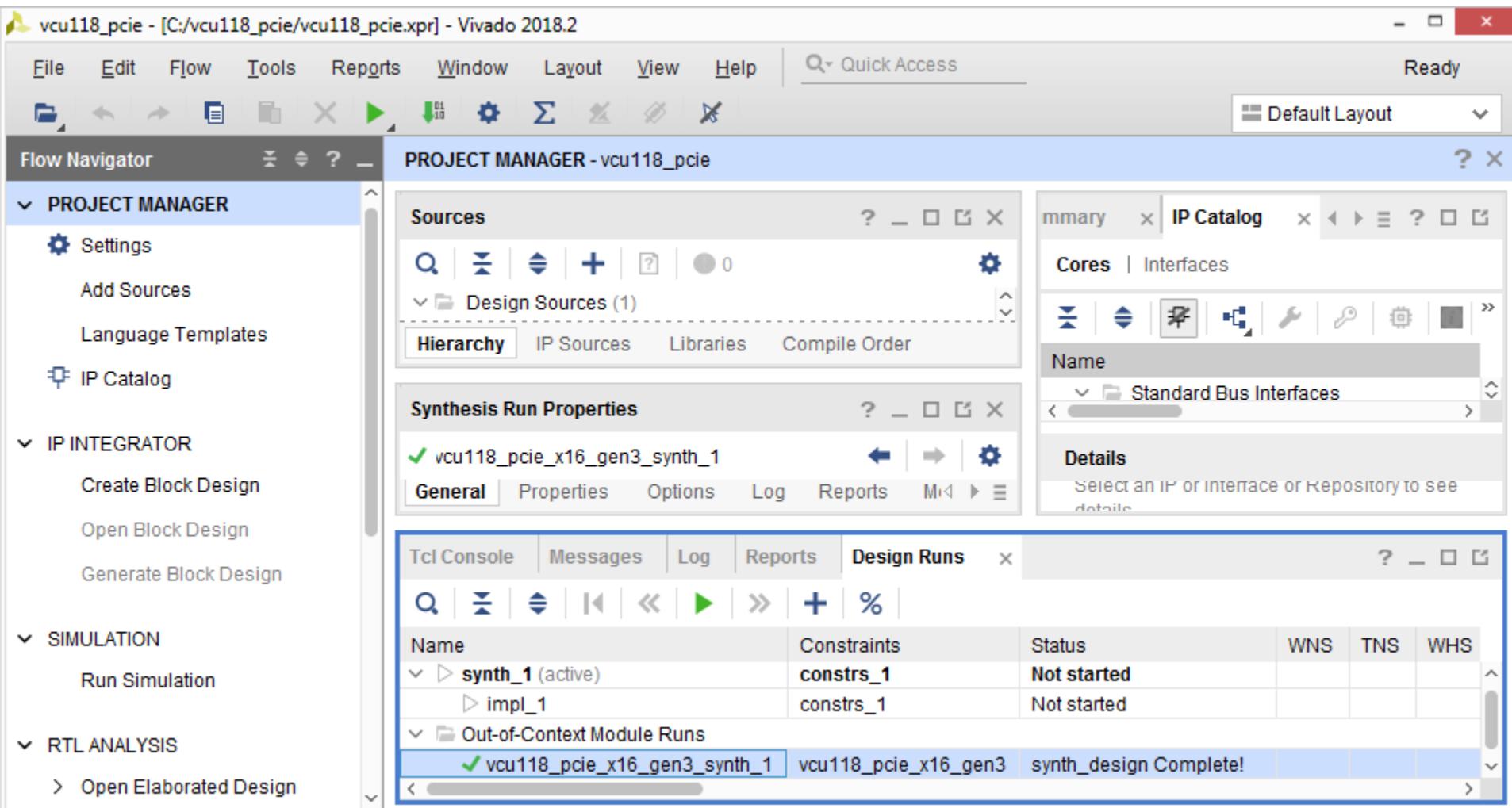


Note: This step will take about 9 minutes

Generate x16 Gen 3 PCIe Core

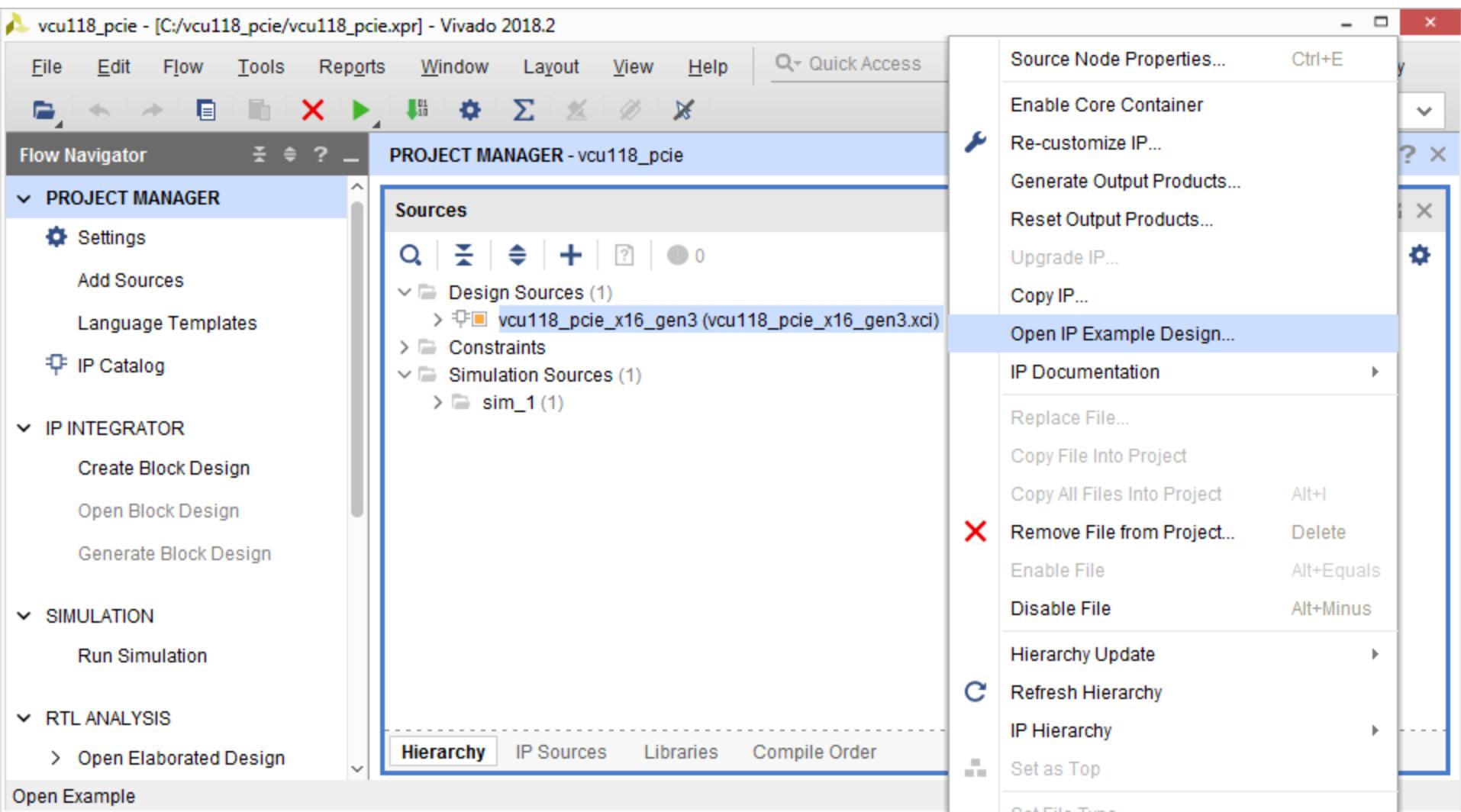
> PCIe design appears in Design Sources

» Wait until checkmark appears on `vcu118_pcnie_x16_gen3_synth_1` in Design Runs



Generate x16 Gen 3 PCIe Core

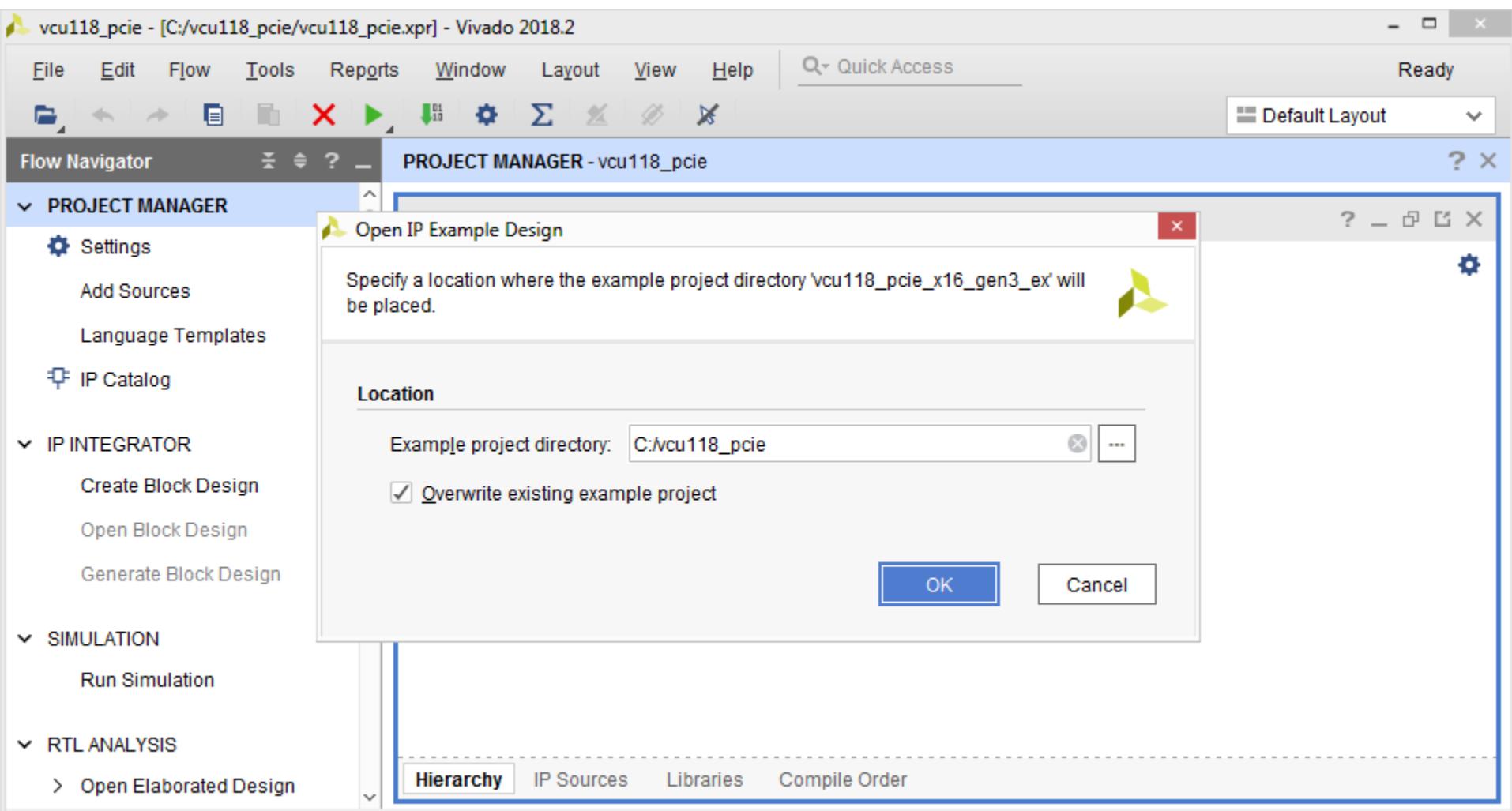
- > Right-click on vcu118_pcie_x16_gen3 and select Open IP Example Design...



Note: Presentation applies to the VCU118

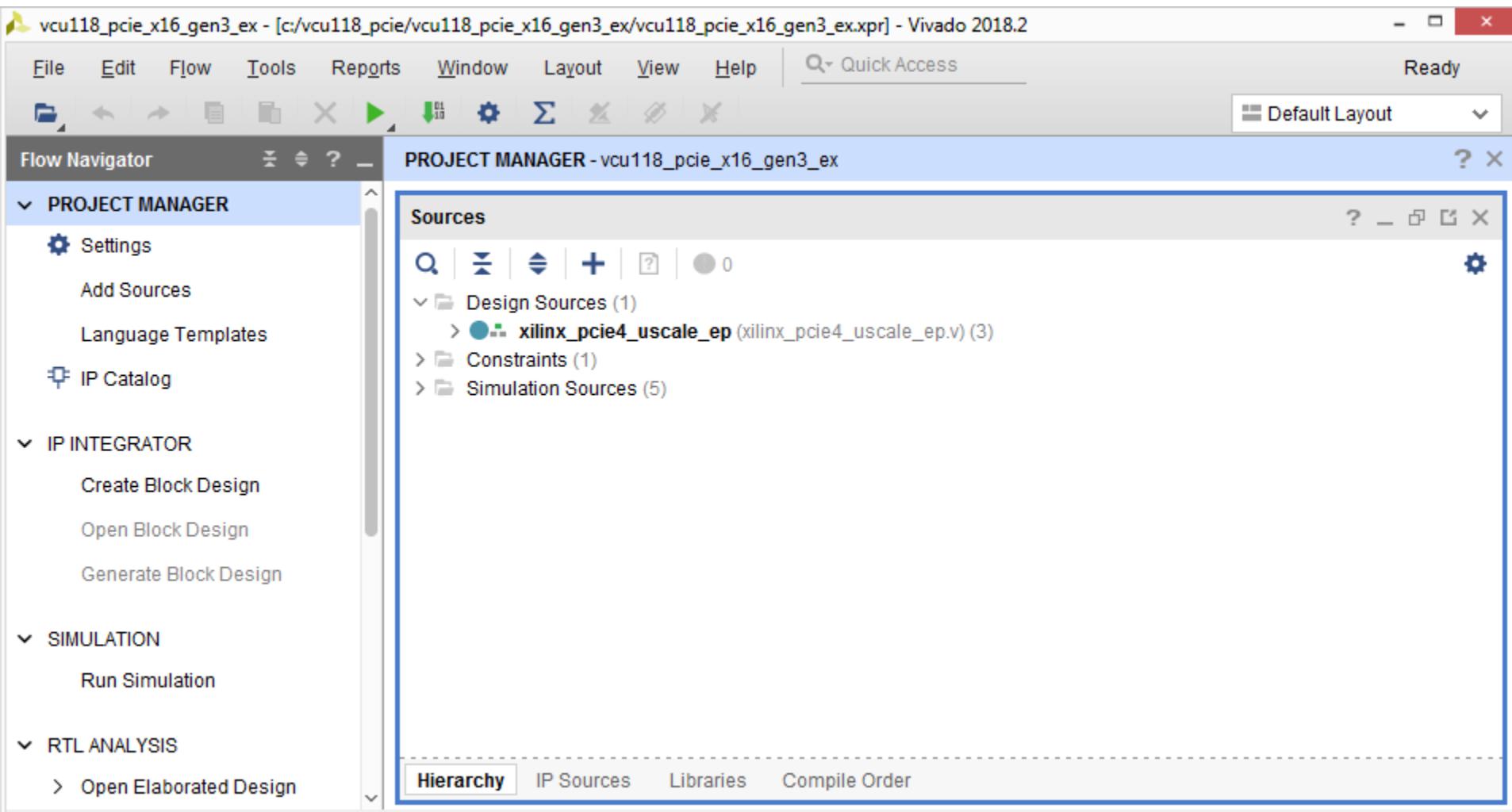
Generate x16 Gen 3 PCIe Core

- > Set the location to C:/vcu118_PCIE and click OK



Generate x16 Gen 3 PCIe Core

- > A new project is created under C:\vcu118_PCIE_x16_gen3_ex



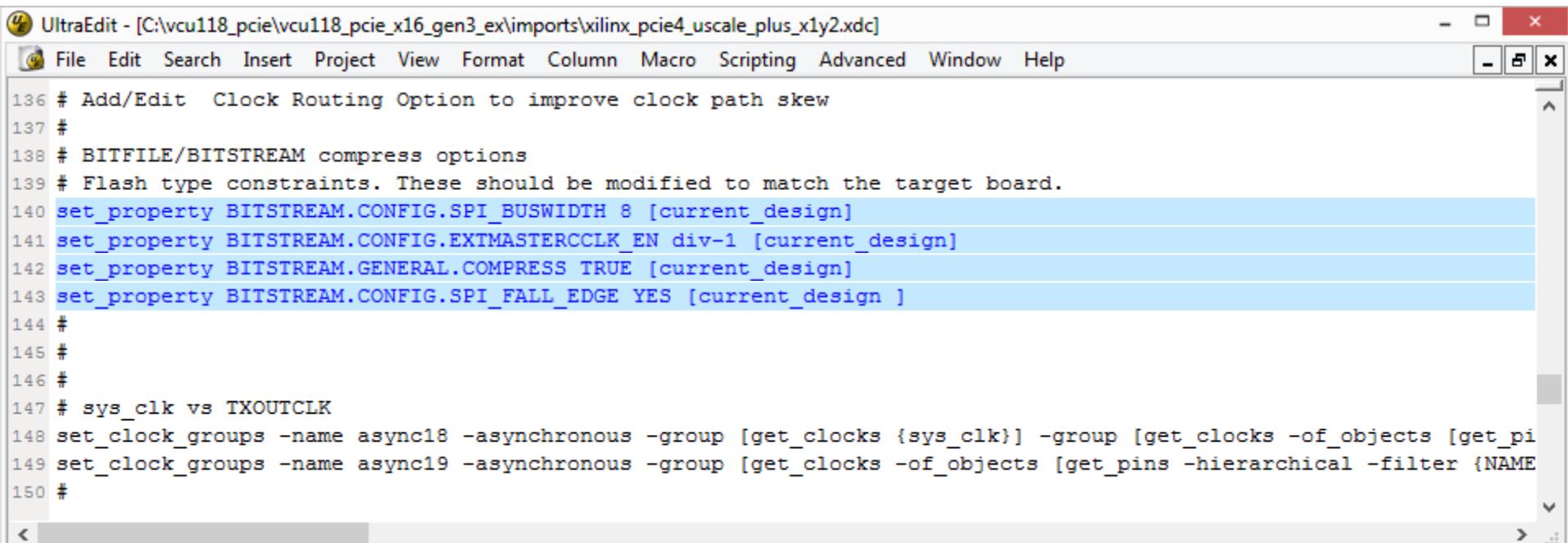
Note: The original project window can be closed

Modify PCIe Core

- > As per [UG570](#), [UG949](#), and [N25Q256 Flash](#) specifications

- » In the XDC file, xilinx_pcnie4_uscale_plus_x1y2.xdc, add these lines:

```
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 8 [current_design]
set_property BITSTREAM.CONFIG.EXTMMASTERCCLK_EN div-1 [current_design]
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design]
```



The screenshot shows a code editor window titled "UltraEdit - [C:\vcu118_pcnie\vcu118_pcnie_x16_gen3_ex\imports\xilinx_pcnie4_uscale_plus_x1y2.xdc]". The menu bar includes File, Edit, Search, Insert, Project, View, Format, Column, Macro, Scripting, Advanced, Window, and Help. The code in the editor is as follows:

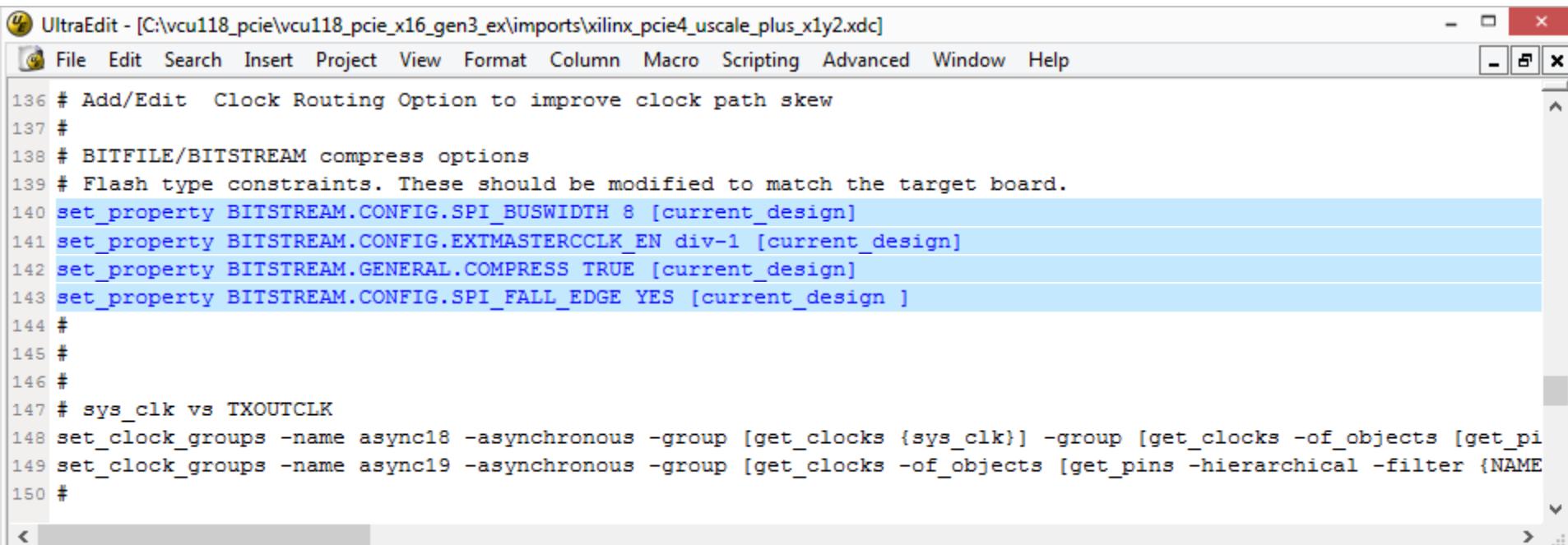
```
136 # Add/Edit Clock Routing Option to improve clock path skew
137 #
138 # BITFILE/BITSTREAM compress options
139 # Flash type constraints. These should be modified to match the target board.
140 set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 8 [current_design]
141 set_property BITSTREAM.CONFIG.EXTMMASTERCCLK_EN div-1 [current_design]
142 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
143 set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design ]
144 #
145 #
146 #
147 # sys_clk vs TXOUTCLK
148 set_clock_groups -name async18 -asynchronous -group [get_clocks {sys_clk}] -group [get_clocks -of_objects [get_pins -hierarchical -filter {NAME
149 set_clock_groups -name async19 -asynchronous -group [get_clocks -of_objects [get_pins -hierarchical -filter {NAME
150 #
```

The lines from 140 to 143 are highlighted in blue, indicating they are the new properties added to the XDC file.

Modify PCIe Core

> Details on the XDC constraints:

- » N25Q256 Maximum Frequency: 108 MHz; KCU105 EMCCLK Freq: 90 MHz
- » BITSTREAM.CONFIG.SPI_BUSWIDTH 8: For Dual Quad SPI
- BITSTREAM.CONFIG.EXTMMASTERCCLK_EN div-1: Sets the EMCCLK in the FPGA to divide by 1
- » BITSTREAM.GENERAL.COMPRESS TRUE: Shrinks the bitstream
- » BITSTREAM.CONFIG.SPI_FALL_EDGE YES: Improves SPI loading speed

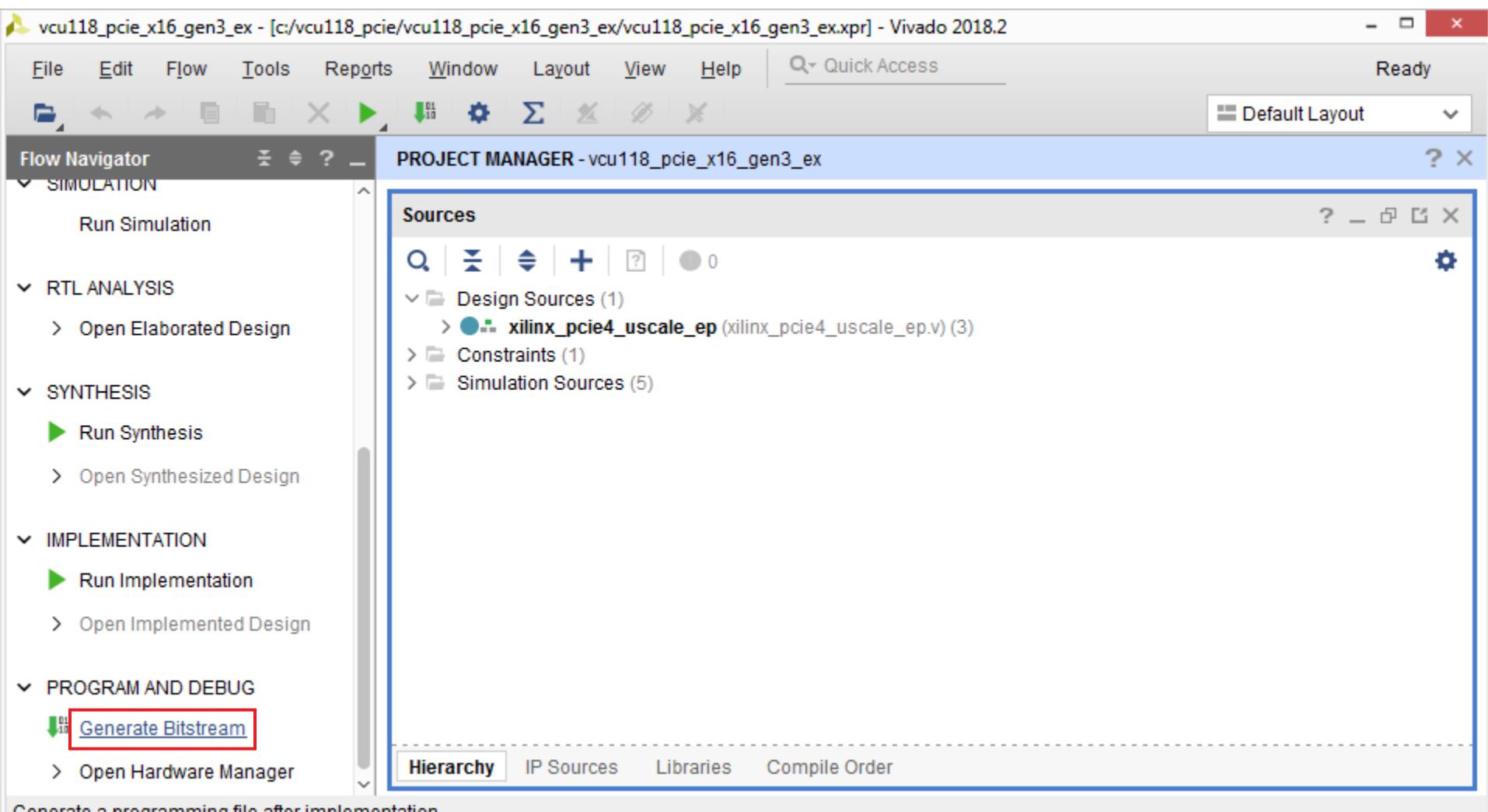


The screenshot shows a Windows application window titled "UltraEdit - [C:\vcu118_pcie\vcu118_pcie_x16_gen3_ex\imports\xilinx_pcie4_uscale_plus_x1y2.xdc]". The menu bar includes File, Edit, Search, Insert, Project, View, Format, Column, Macro, Scripting, Advanced, Window, and Help. The main text area displays an XDC (Xilinx Design Constraints) file with the following content:

```
136 # Add/Edit Clock Routing Option to improve clock path skew
137 #
138 # BITFILE/BITSTREAM compress options
139 # Flash type constraints. These should be modified to match the target board.
140 set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 8 [current_design]
141 set_property BITSTREAM.CONFIG.EXTMMASTERCCLK_EN div-1 [current_design]
142 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
143 set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design ]
144 #
145 #
146 #
147 # sys_clk vs TXOUTCLK
148 set_clock_groups -name async18 -asynchronous -group [get_clocks {sys_clk}] -group [get_clocks -of_objects [get_pins -hierarchical -filter {NAME
149 set_clock_groups -name async19 -asynchronous -group [get_clocks -of_objects [get_pins -hierarchical -filter {NAME
150 #
```

Compile Example Design

- > Click on Generate Bitstream

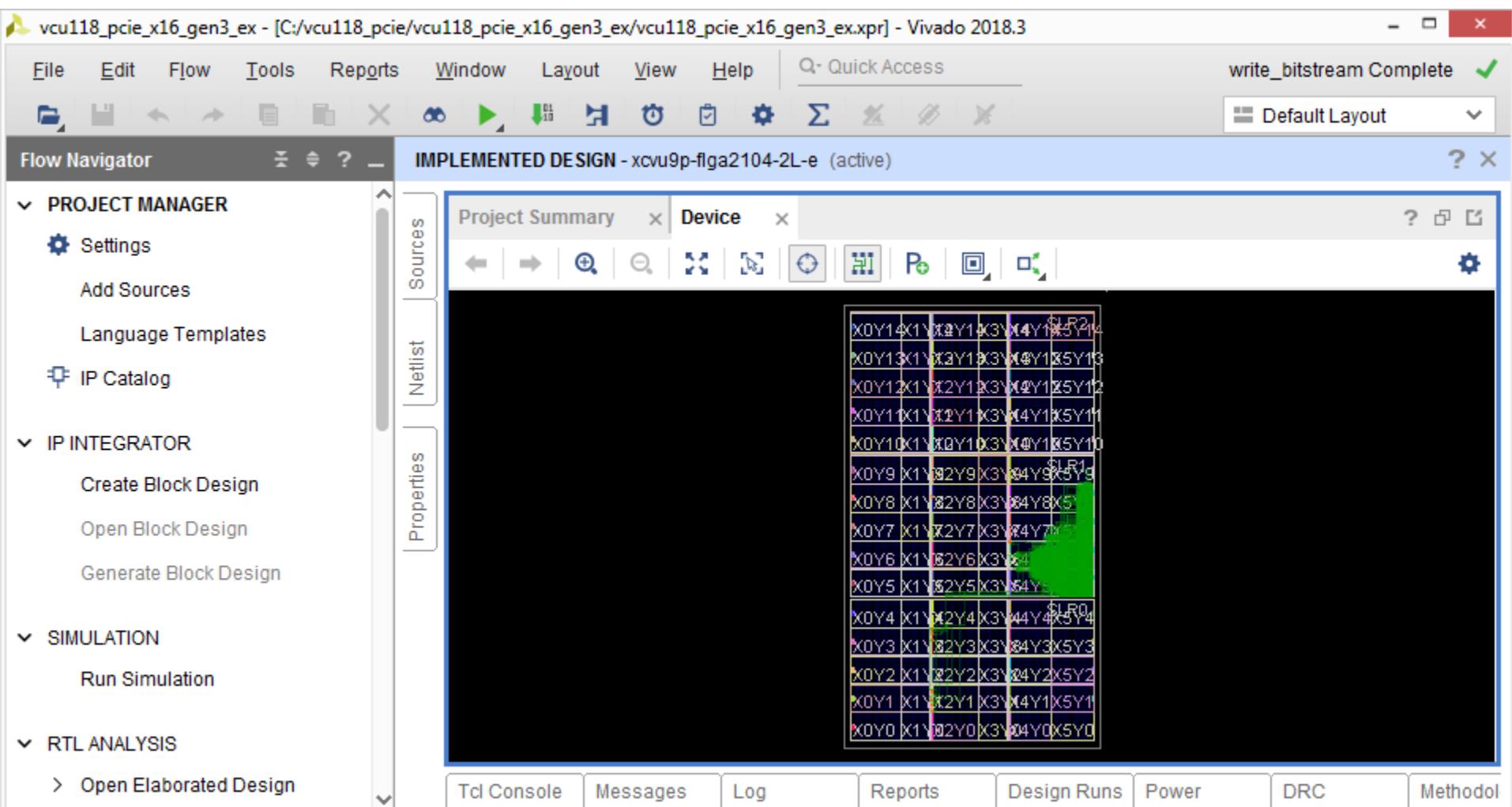


Note: Presentation applies to the VCU118

 XILINX

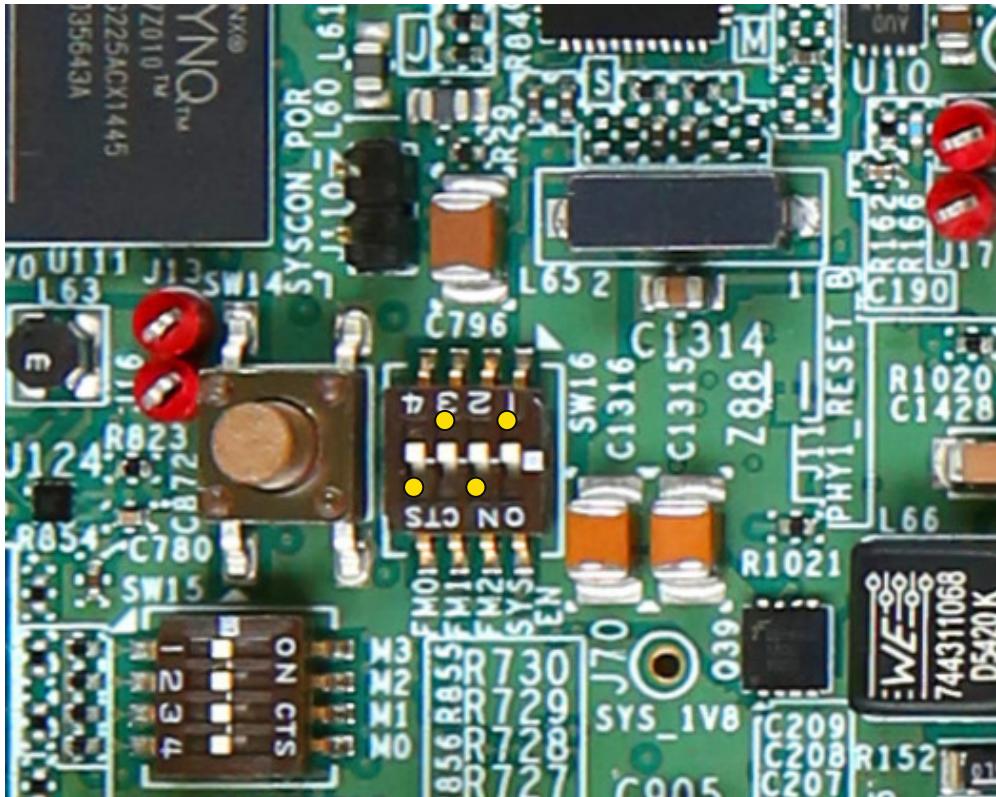
Compile Example Design

- > Open and view the Implemented Design



Setup for the VCU118 PCIe Designs

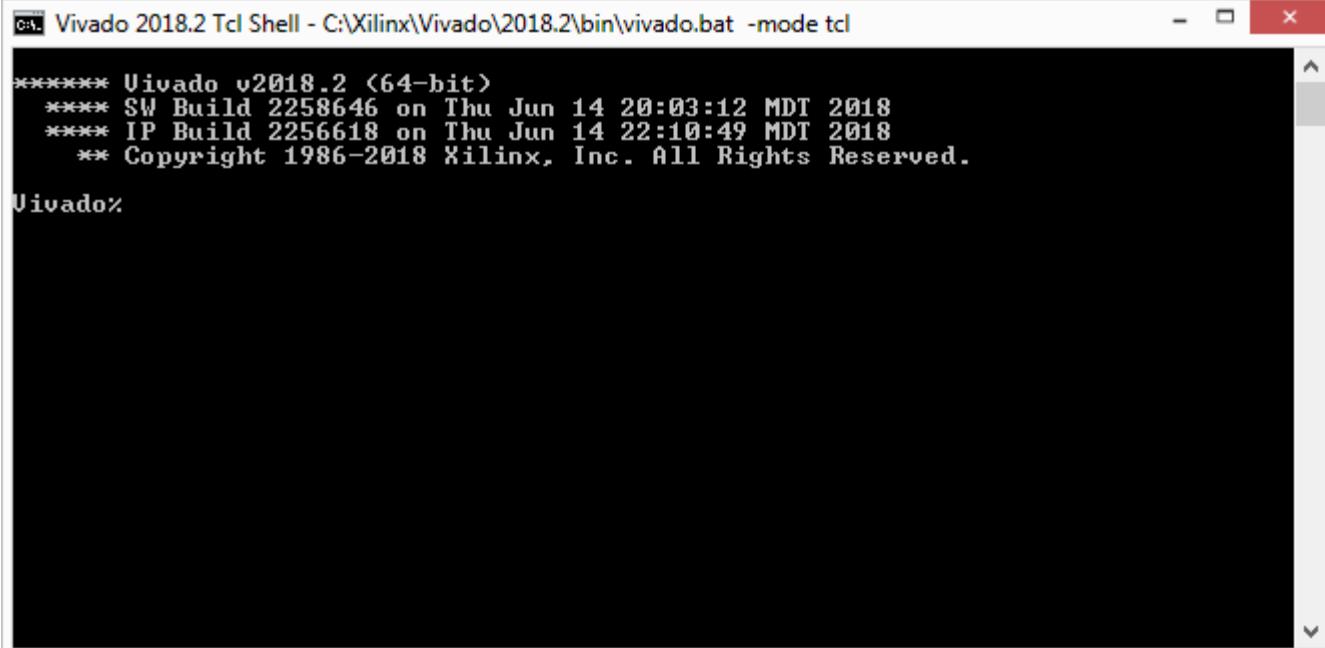
- > Set JTAG mode ($M[2:0] = 101$) to program QSPI Flash
- > Disable System Controller booting (Position 1 off)
- > Set SW16 to 0101 (1 = on, Position 1 \rightarrow Position 4)



Generate PCIe MCS File

> Open a Vivado Tcl Shell:

Start → All Programs → Xilinx Design Tools → Vivado 2019.1 →
Vivado 2019.1 Tcl Shell



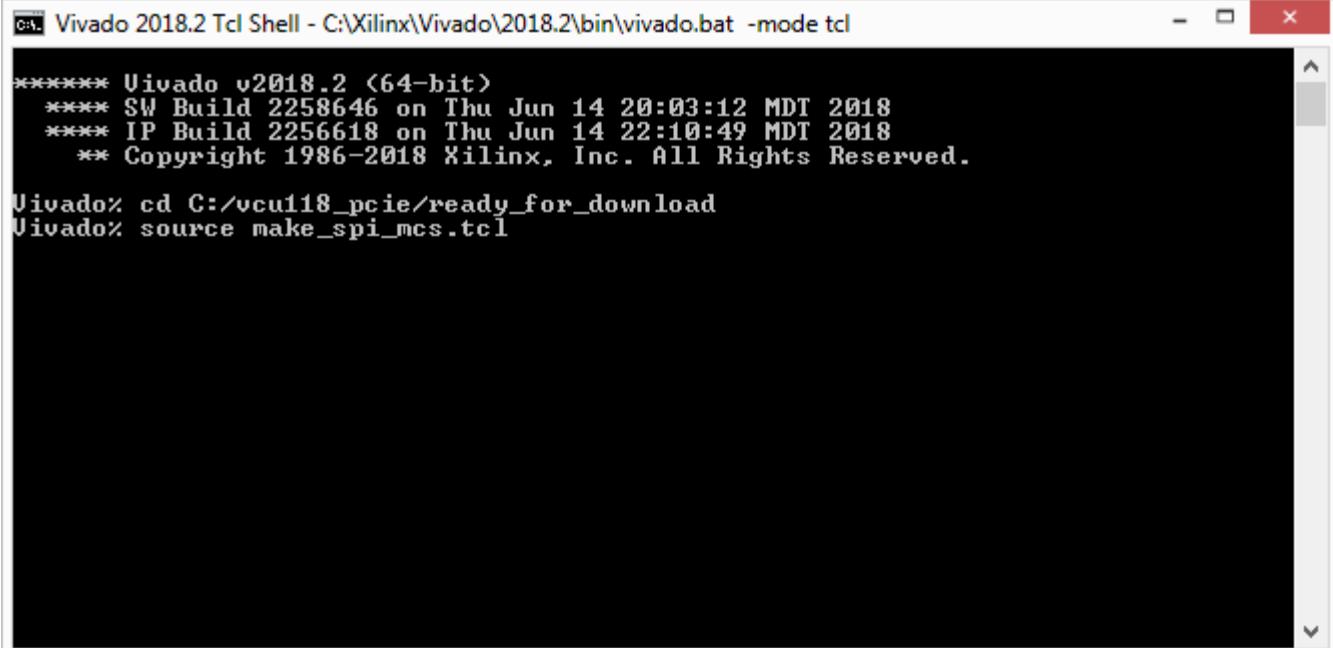
```
Vivado 2018.2 (64-bit)
 **** SW Build 2258646 on Thu Jun 14 20:03:12 MDT 2018
 **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
 ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

Vivado>
```

Generate PCIe MCS File

- > Create the PCIe MCS file
- > In the Vivado Tcl Shell type:

```
cd C:/vcu118_pcie/ready_for_download  
source make_spi_mcs.tcl
```



The screenshot shows a Windows command-line interface window titled "Vivado 2018.2 Tcl Shell - C:\Xilinx\Vivado\2018.2\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2018.2 (64-bit)  
***** SW Build 2258646 on Thu Jun 14 20:03:12 MDT 2018  
***** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018  
** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.  
  
Vivado> cd C:/vcu118_pcie/ready_for_download  
Vivado> source make_spi_mcs.tcl
```

Program QSPI Flash with PCIe Design

- > Program the QSPI Flash device
- > In the Vivado Tcl Shell type:
`source program_spi.tcl`

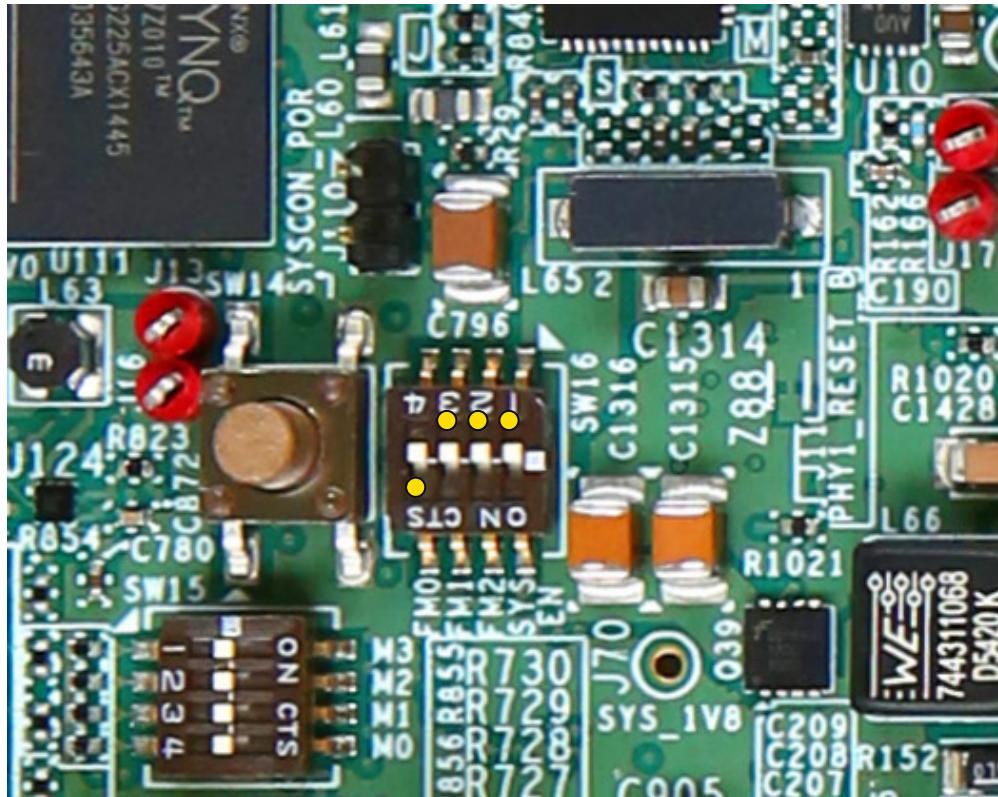
```
C:\ Vivado 2018.2 Tcl Shell - C:\Xilinx\Vivado\2018.2\bin\vivado.bat -mode tcl
File Format      MCS
Interface        SPIx8
Size             16M
Start Address    0x00000000
End Address      0x00FFFFFF

Addr1           Addr2           Date          File(s)
0x00000000     0x00814C59   Sep 9 15:07:55 2018  xilinx_pcie4_uscale_ep.bit
Writing log file ./vcu118_pcie_x16_gen3_secondary.prm
=====
Configuration Memory information
=====
File Format      MCS
Interface        SPIx8
Size             16M
Start Address    0x00000000
End Address      0x00FFFFFF

Addr1           Addr2           Date          File(s)
0x00000000     0x00814C59   Sep 9 15:07:55 2018  xilinx_pcie4_uscale_ep.bit
0 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
write_cfmem completed successfully
write_cfmem: Time <s>: cpu = 00:00:26 ; elapsed = 00:00:27 . Memory <MB>: peak
= 407.746 ; gain = 147.395
Vivado% source program_spi.tcl
```

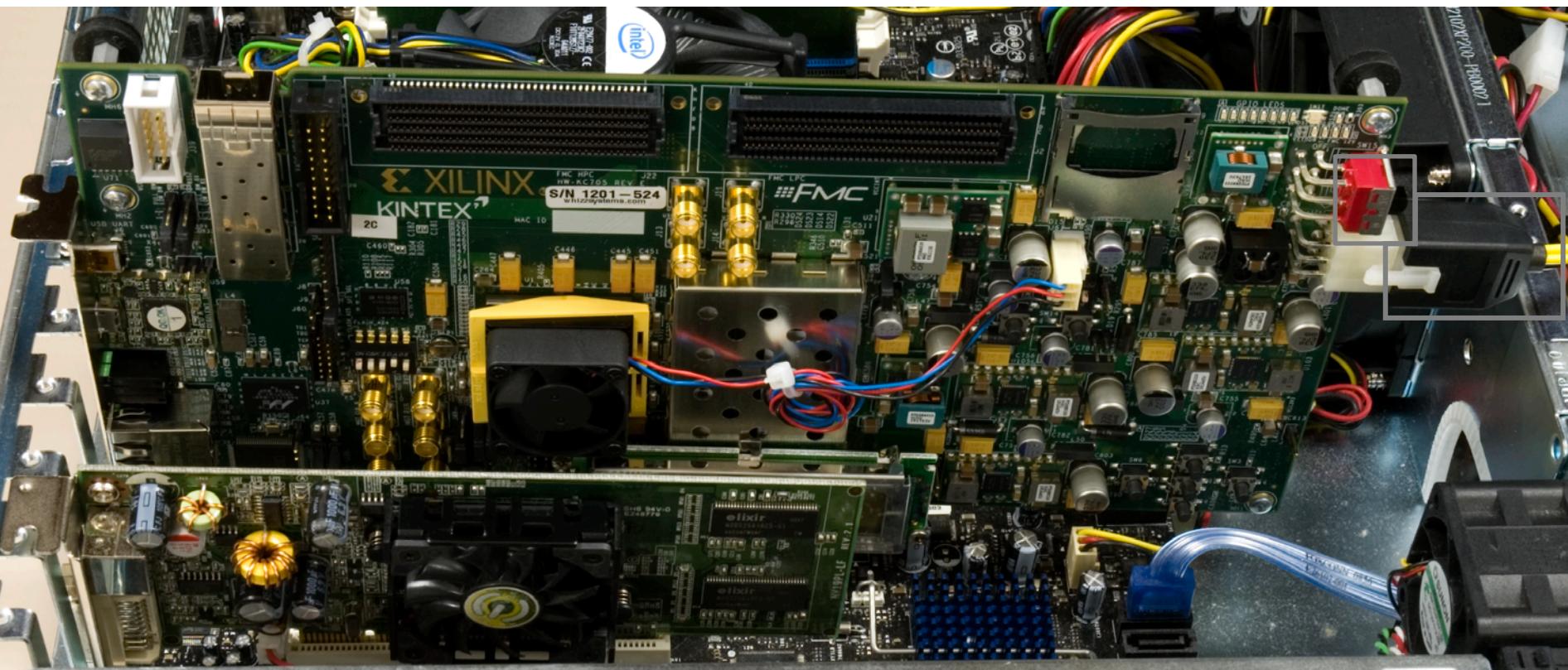
Setup for the VCU118 PCIe Designs

- > Set QSPI mode ($M[2:0] = 001$) to load FPGA from Flash
- > Disable System Controller booting (Position 1 off)
- > Set SW16 to 0001 (1 = on, Position 1 → Position 4)



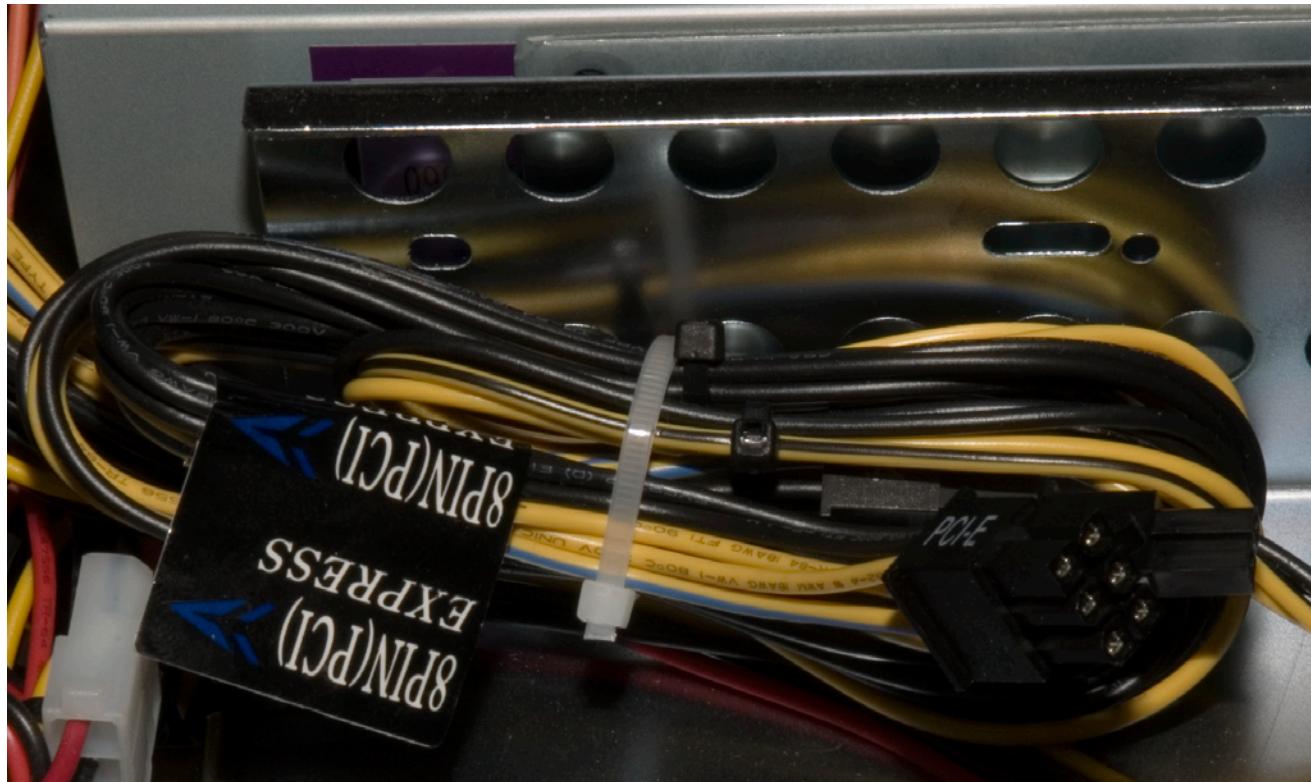
Hardware Setup

- > Insert the VCU118 Board into a x16 PCIe slot (KC705 shown)
 - » Use the included PC Power adapter; turn on Power Switch



Hardware Setup

- > Do not use the PCIe connector from the PC power supply

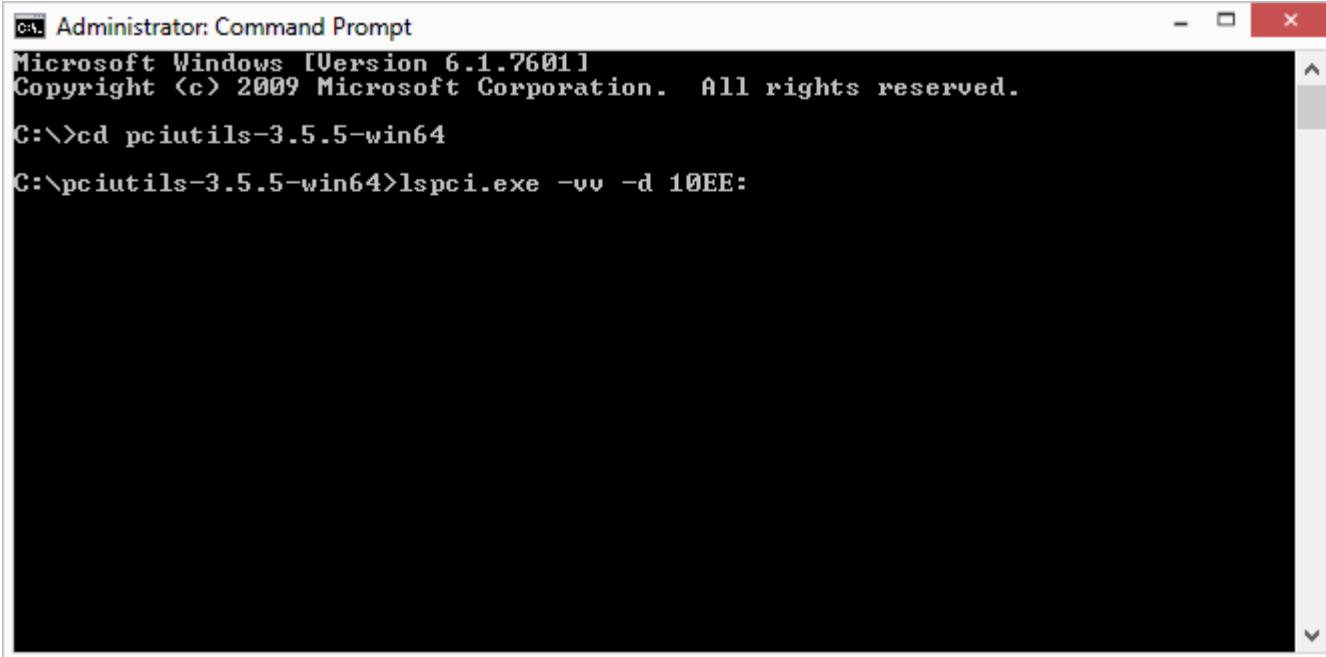


Running the PCIe x16 Gen3 Design

- > Power on the PC
- > Open an Administrator command prompt and type:

```
cd pciutils-3.5.5-win64
```

```
lspci.exe -vv -d 10EE:
```



The screenshot shows a Windows Command Prompt window titled "Administrator: Command Prompt". The window title bar includes the text "Administrator: Command Prompt", the window icon, and standard window control buttons (minimize, maximize, close). The main area of the window displays the following text:

```
Microsoft Windows [Version 6.1.7601]
Copyright (c) 2009 Microsoft Corporation. All rights reserved.

C:\>cd pciutils-3.5.5-win64
C:\pciutils-3.5.5-win64>lspci.exe -vv -d 10EE:
```

The command entered was "lspci.exe -vv -d 10EE:", which is intended to list PCI devices with detailed output for device ID 10EE. The output is currently blank, indicating no results were found or displayed.

Note: Modify path to match your version of the PCI Utils

Running the PCIe x16 Gen3 Design

- > Shown here on Linux, Xilinx at 8GT/s (Gen3) and Width x16

```
xilinx@localhost:/home/xilinx
File Edit View Search Terminal Help
[root@localhost xilinx]# lspci -vv -d 10EE:
01:00.0 Memory controller: Xilinx Corporation Device 903f
    Subsystem: Xilinx Corporation Device 0007
    Control: I/O+ Mem+ BusMaster+ SpecCycle- MemWINV- VGASnoop- ParErr- Stepping- SERR- FastB2B- DisINTx-
    Status: Cap+ 66MHz- UDF- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbsor- <MAbort- >SERR- <PERR- INTx-
    Latency: 0
    Region 0: Memory at df900000 (32-bit, non-prefetchable) [size=1M]
    Capabilities: [40] Power Management version 3
        Flags: PMEClk- DSI- D1- D2- AuxCurrent=0mA PME(D0-,D1-,D2-,D3hot--,D3cold-)
        Status: D0 NoSoftRst+ PME-Enable- DSel=0 DScale=0 PME-
    Capabilities: [48] MSI: Enable- Count=1/1 Maskable- 64bit+
        Address: 0000000000000000 Data: 0000
    Capabilities: [70] Express (v2) Endpoint, MSI 00
        DevCap: MaxPayload 1024 bytes, PhantFunc 0, Latency L0s <64ns, L1 <1us
            ExtTag+ AttnBtn- AttnInd- PwrInd- RBE+ FLReset-
        DevCtl: Report errors: Correctable- Non-Fatal- Fatal- Unsupported-
            RLxd0Rd+ ExtTag+ PhantFunc- AuxPwr- NoSnoop+
            MaxPayload 128 bytes, MaxReadReq 512 bytes
        DevSta: CorrErr+ UncorrErr- FatalErr- UnsuppReq+ AuxPwr- TransPend-
        LnkCap: Port #0, Speed 8GT/s, Width x16, ASPM not supported, Exit Latency L0s unlimited, L1 unlimited
            ClockPM- Surprise- LLActRep- BwNot- ASPMOptComp+
        LnkCtl: ASPM Disabled; RCB 64 bytes Disabled- CommClk+
            ExtSynch- ClockPM- AutWidDis- BWInt- AutBWInt-
        LnkSta: Speed 8GT/s, Width x16, TrErr- Train- SlotClk+ DLActive- BWMgmt- ABWMgmt-
        DevCap2: Completion timeout: Range BC, TimeoutDis+, LTR-, OBFF Not Supported
        DevCtl2: Completion Timeout: 50us to 50ms, TimeoutDis-, LTR-, OBFF Disabled
        LnkCtl2: Target Link Speed: 8GT/s, EnterCompliance- SpeedDis-
            Transmit Margin: Normal Operating Range, EnterModifiedCompliance- ComplianceSOS-
            Compliance De-emphasis: -6dB
        LnkSta2: Current De-emphasis Level: -6dB, EqualizationComplete+, EqualizationPhase1+
            EqualizationPhase2-, EqualizationPhase3-, LinkEqualizationRequest-
    Capabilities: [100 v1] Advanced Error Reporting
        UESta: DLP- SDES- TLP- FCP- CmpltAbrt- UnxCmplt- RxOF- MalfTLP- ECRC- UnsupReq- ACSViol-
        UEMsk: DLP- SDES- TLP- FCP- CmpltAbrt- UnxCmplt- RxOF- MalfTLP- ECRC- UnsupReq- ACSViol-
        UESvrt: DLP+ SDES+ TLP+ FCP+ CmpltAbrt- UnxCmplt- RxOF+ MalfTLP+ ECRC- UnsupReq- ACSViol-
        CESta: RxErr- BadTLP- BadDLLP- Rollover- Timeout- NonFatalErr+
        CEMsk: RxErr- BadTLP- BadDLLP- Rollover- Timeout- NonFatalErr+
        AERCap: First Error Pointer: 00, GenCap- CGenEn- ChkCap- ChkEn-
    Capabilities: [1c0 v1] #19
[root@localhost xilinx]#
```

References



References

> PCIe Base Specification

- » PCI SIG Web Site
 - <http://pcisig.com>

> Xilinx PCI Express

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