

VCU118 Software Install and Board Setup

May 2019



Revision History

Date	Version	Description
05/29/19	9.0	Updated for 2019.1.
12/10/18	8.0	Updated for 2018.3.
06/18/18	7.0	Updated for 2018.2.
04/09/18	6.0	Updated for 2018.1.
12/20/17	5.0	Updated for 2017.4.
10/26/17	4.0	Updated for 2017.3.1. For Rev 2.0, with Production Silicon, and QSPI Flash devices.
06/20/17	3.0	Updated for 2017.2.
04/19/17	2.0	Updated for 2017.1. Updated to match kit contents. Added AR69402.
01/16/17	1.1	Updated SW16 settings.
12/19/16	1.0	Initial version for 2016.4.

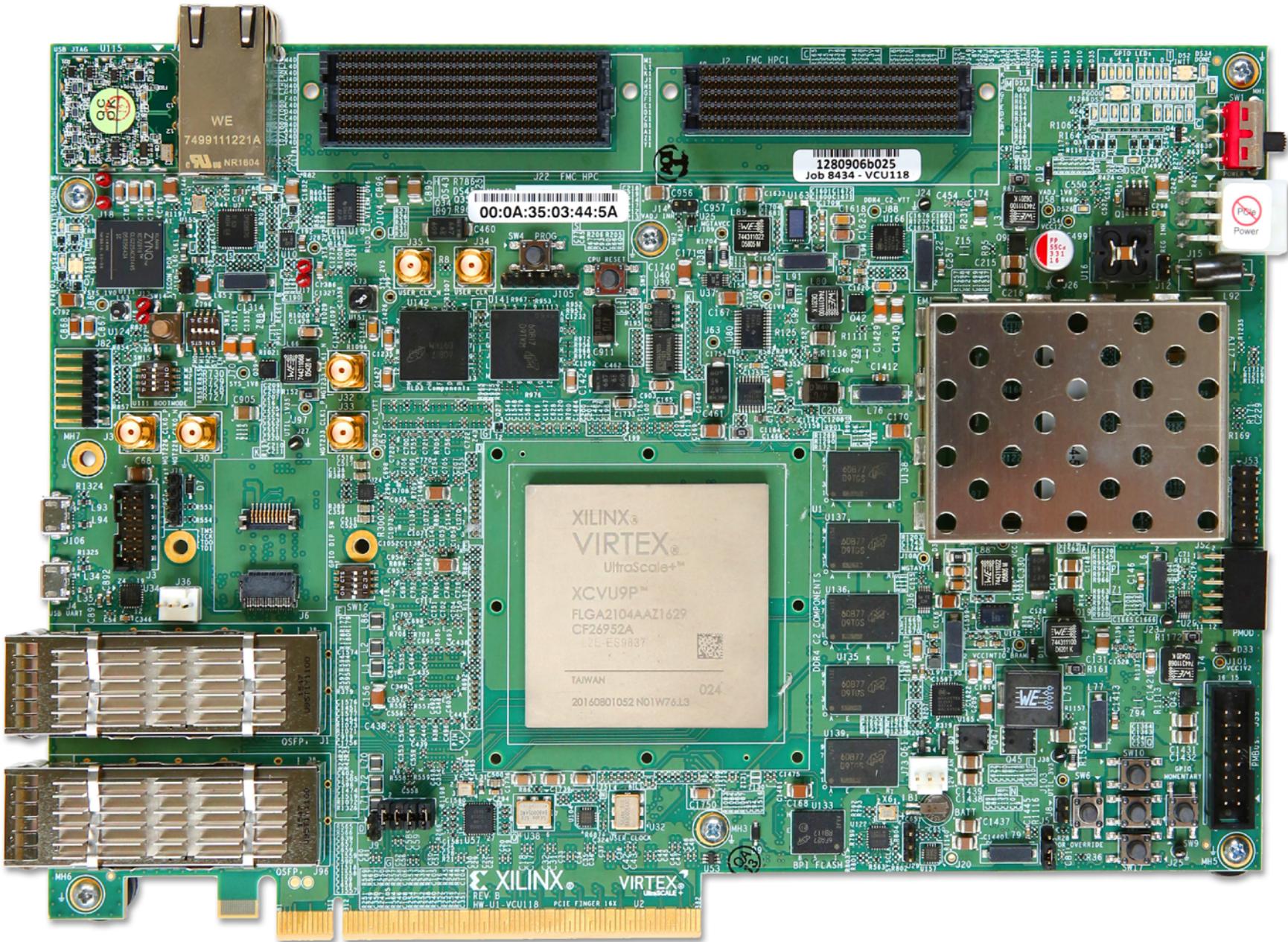
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VCU118 Software Install and Board Setup

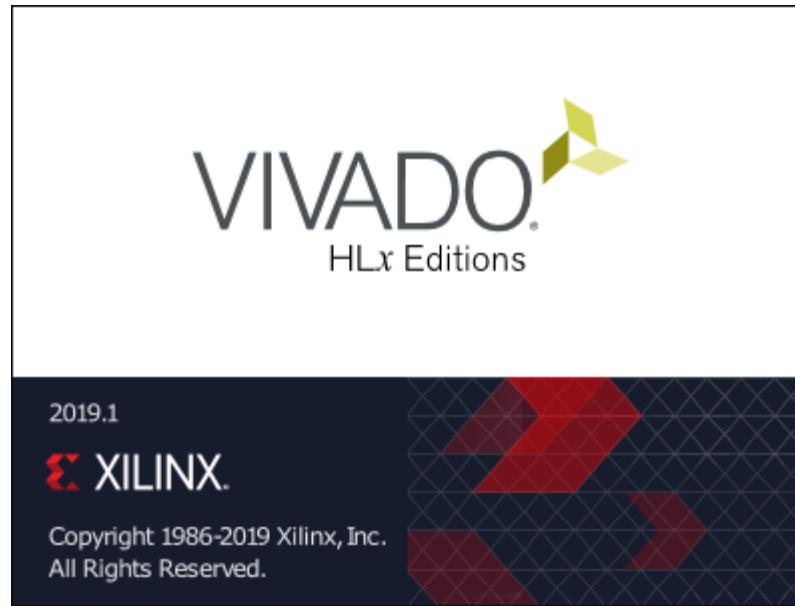
- > **Xilinx VCU118 Board**
- > **Software Requirements**
- > **VCU118 Hardware Setup**
- > **UART Driver Install**
- > **Clock Setup**
- > **Ethernet Setup**
- > **Optional Hardware Setup**
- > **References**

Xilinx VCU118 Board



Software Requirements

- > Xilinx Vivado Design Suite 2019.1, HL System Edition with SDK



Software Requirements

- > The Rev. 2.0 VCU118 board has a -2 Production device and VCCINT is set to 0.85 V
- > DS923 notes in this case, the speed grade is considered to -2LE

Table 17: Speed Grade Designations by Device

Device	Speed Grade, Temperature Ranges, and V _{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCVU3P	-3E (V _{CCINT} = 0.90V) -2LE (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V) ⁽¹⁾		-2I (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V) -1I (V _{CCINT} = 0.85V)
XCVU5P	-3E (V _{CCINT} = 0.90V) -2I (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V) ⁽¹⁾		
XCVU7P	-3E (V _{CCINT} = 0.90V) -2I (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V) ⁽¹⁾		
XCVU9P	-3E (V _{CCINT} = 0.90V) -2I (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V) ⁽¹⁾		
XCVU11P	-3E (V _{CCINT} = 0.90V) -2I (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.72V) ⁽¹⁾		
XCVU13P	-3E (V _{CCINT} = 0.90V) -2I (V _{CCINT} = 0.85V), -2LE (V _{CCINT} = 0.85V) -1E (V _{CCINT} = 0.85V), -1I (V _{CCINT} = 0.85V) -2LE (V _{CCINT} = 0.72V) ⁽¹⁾		

Notes:

1. The lowest power -2L devices, where V_{CCINT} = 0.72V, are listed in the Vivado Design Suite as -2LV.

VCU118 Hardware Setup

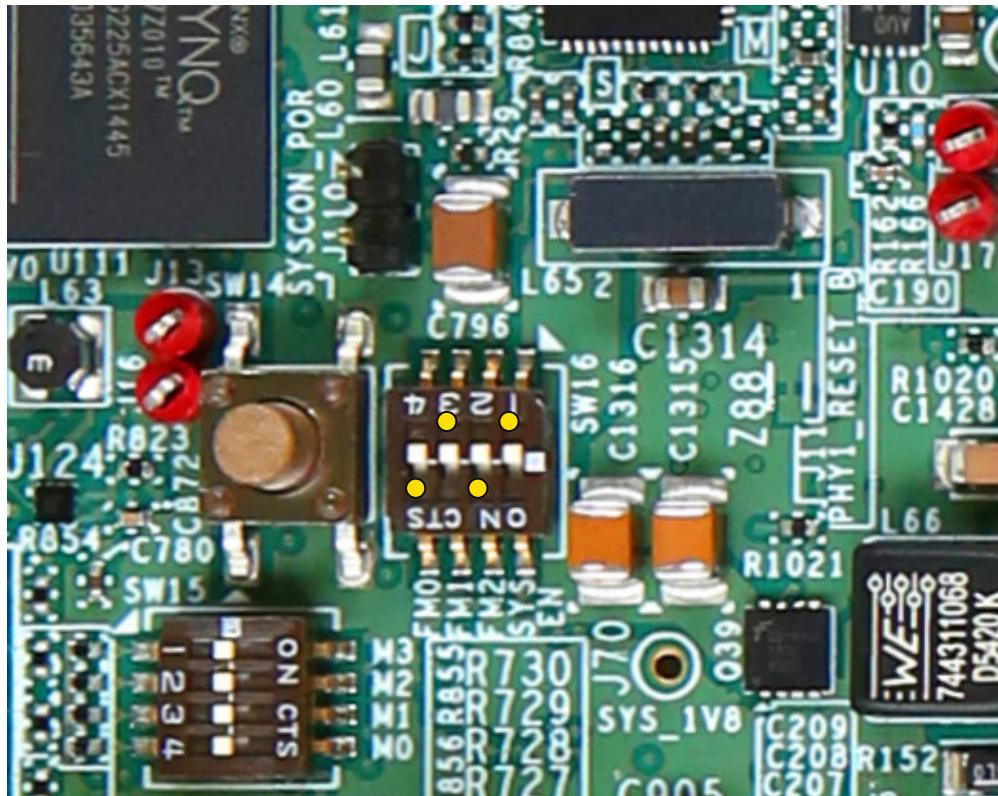
> Kit Hardware contents

- >> VCU118 Board
- >> QSFP+ Loopback
- >> FMC+ Loopback
- >> Samtec FireFly Loopback
- >> XM107 FMC Loopback
- >> PCIe Loopback board
- >> Ethernet cable
- >> Three Micro USB cables
- >> Power supply



Hardware Setup

- > Set JTAG mode ($M[2:0] = 101$) for downloading
- > Disable System Controller booting (Position 1 off)
- > Set SW16 to 0101 (1 = on, Position 1 → Position 4)



Note: JTAG mode is required for downloading bitstreams

VCU118 Hardware Setup

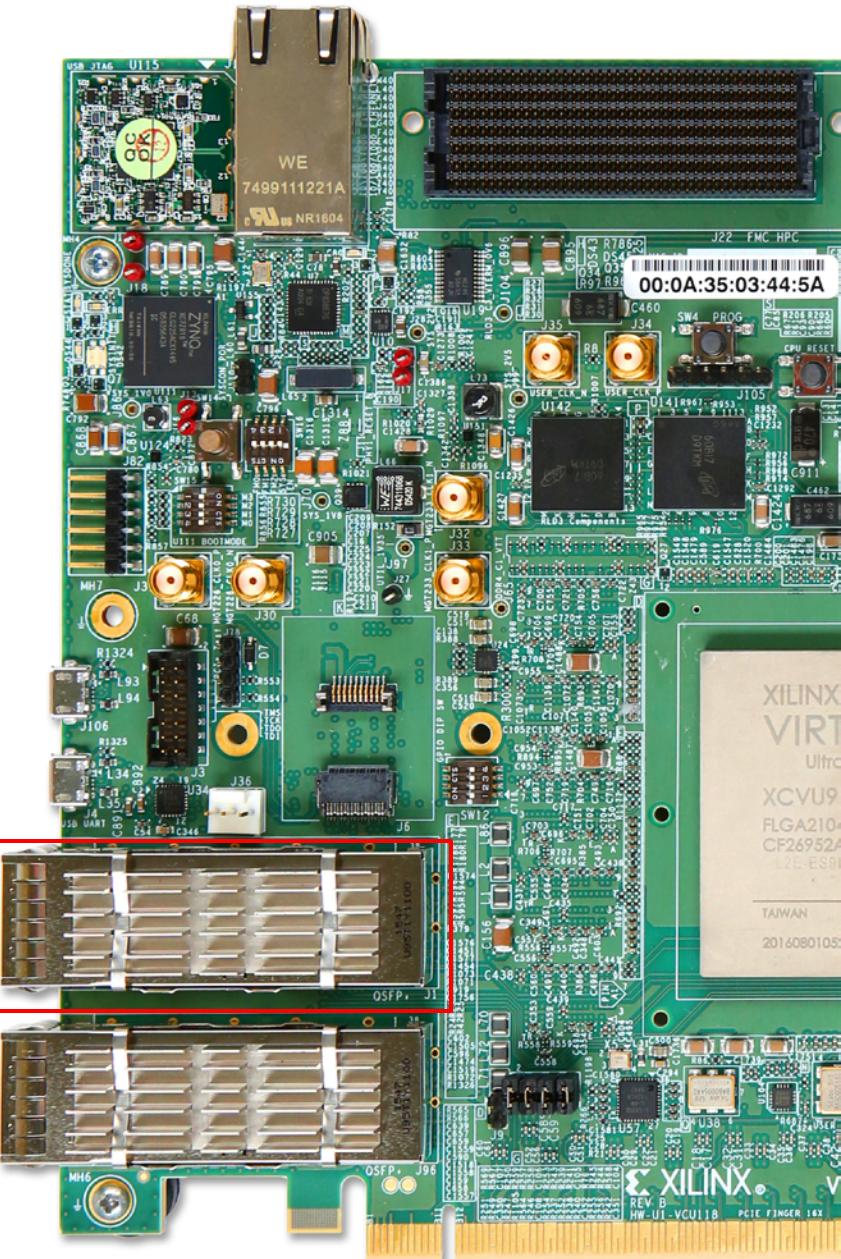
> QSFP Loopback Adapter

> <http://www.molex.com>

> QSFP+ Universal Loopback Adapter, 0dB

> Part # [74763-0020](#)

> Insert this adapter into the Top QSFP cage (J1) on the VCU118



Note: Presentation applies to the VCU118

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VCU118 Hardware Setup

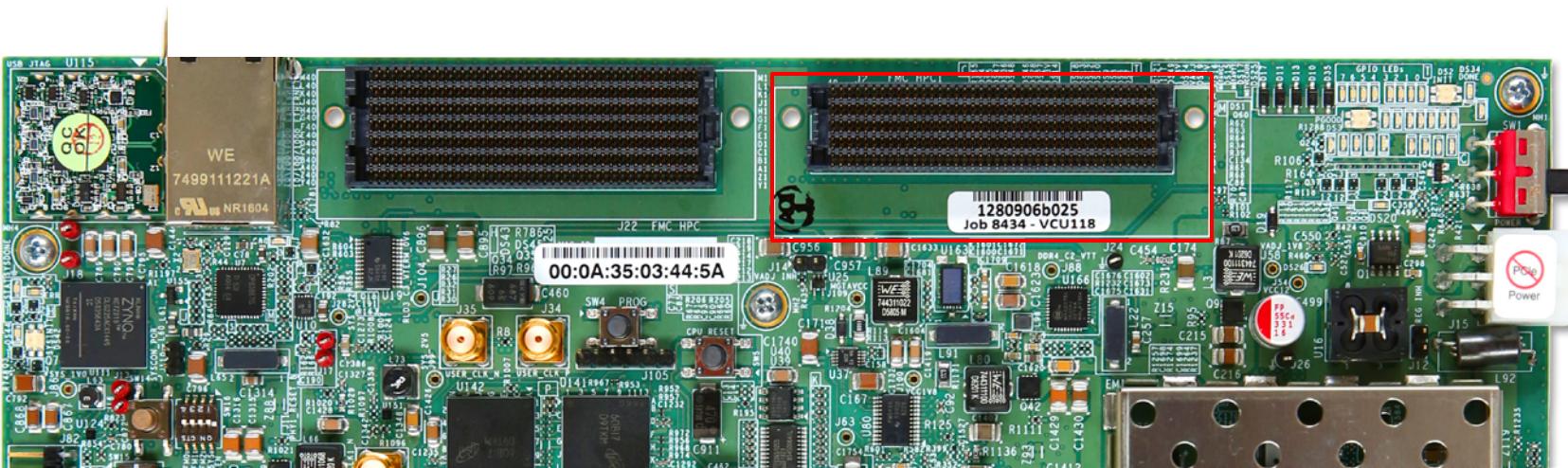
- > Connect a Micro USB cable to the PCIe Loopback card for power
 - » Connect this cable to your PC
- > Attach to the PCIe connector (U2) on the VCU118



Note: KCU105 board shown

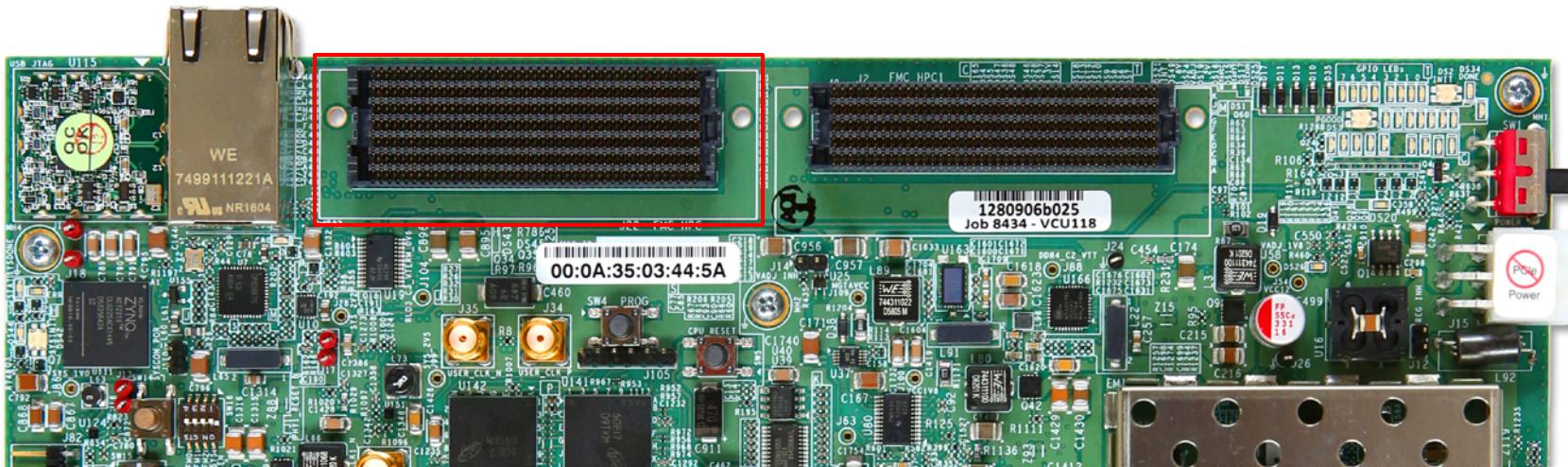
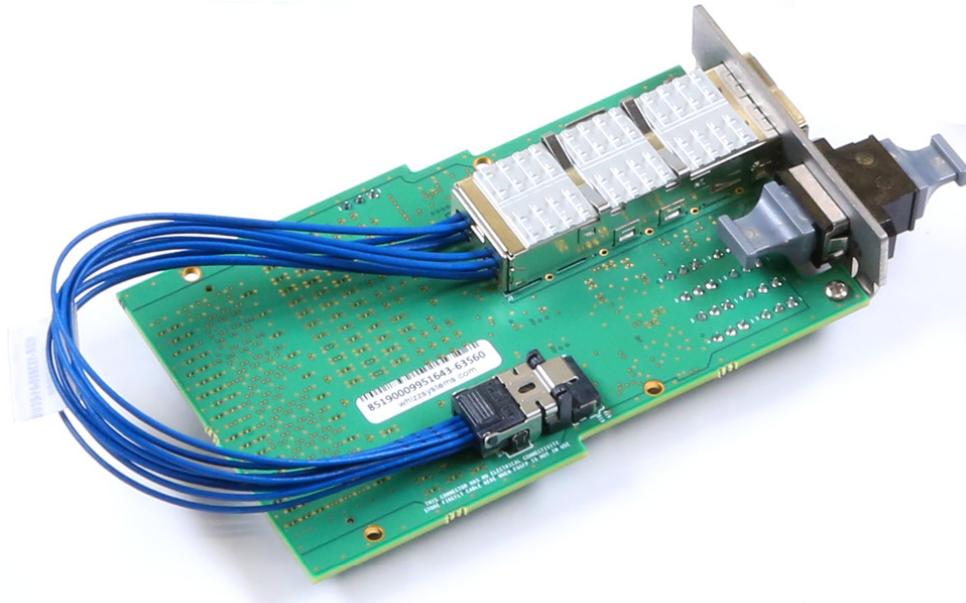
VCU118 Hardware Setup

- > Attach the FMC XM107 board to the J2 HPC1 FMC connector



VCU118 Hardware Setup

- > Attach the FMC+ Loopback board to the J22 HPC FMC+ connector

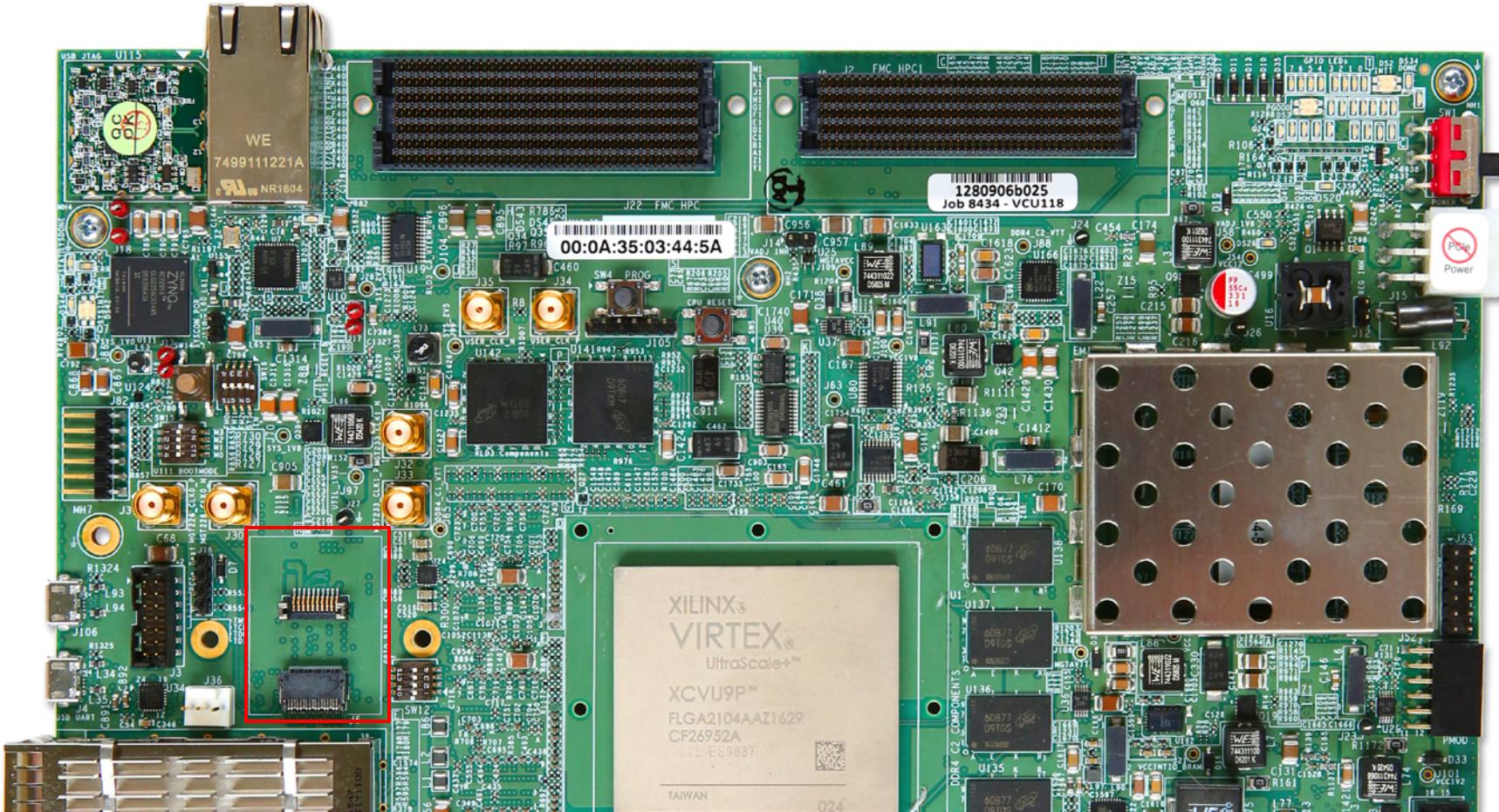


VCU118 Hardware Setup

> Samtec FireFly Loopback

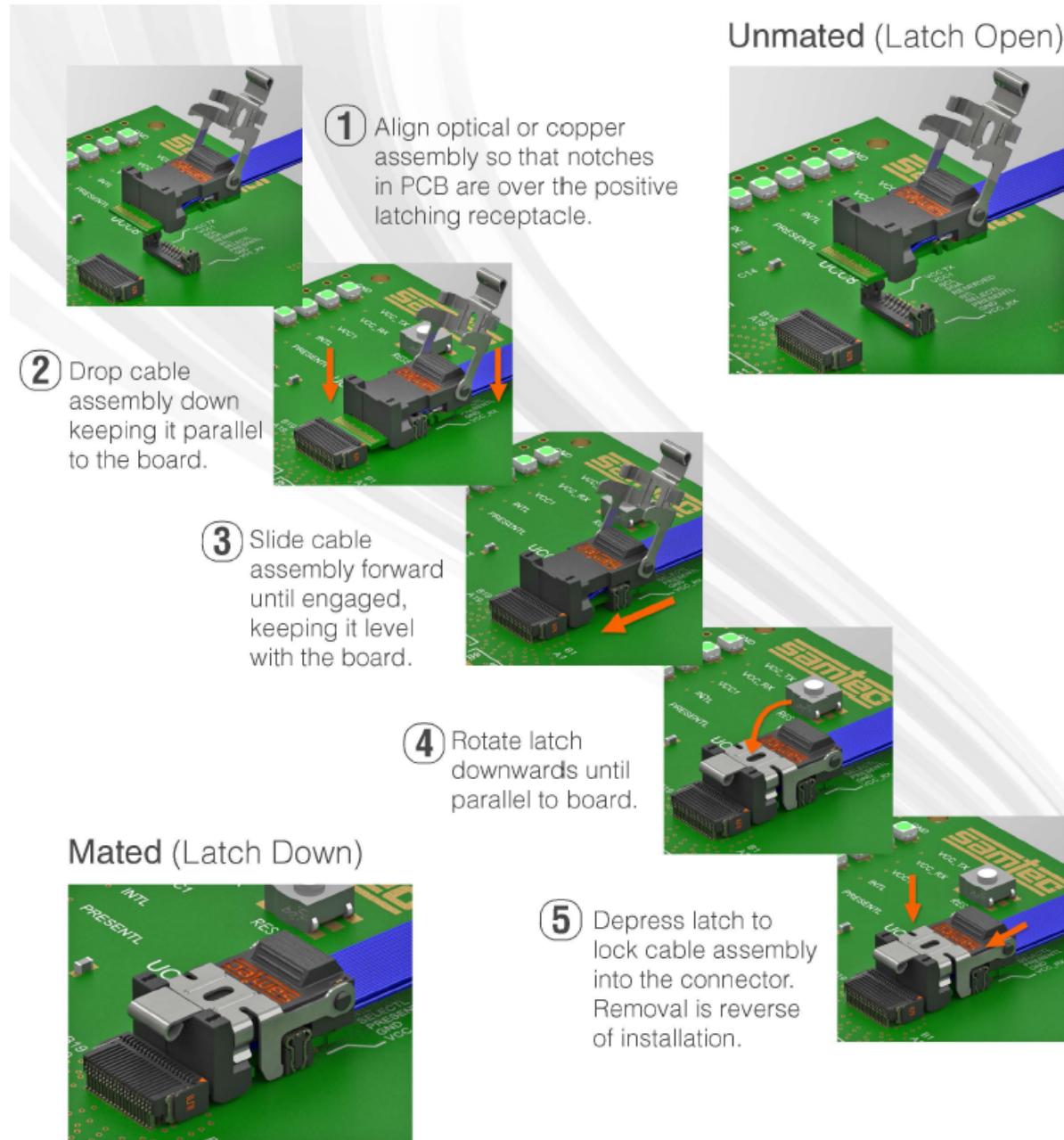
- > <https://www.samtec.com/optics/optical-cable/mid-board/firefly>
- > Part # [HDR-190945-01-ECUE](#)

> Attach the Samtec FireFly Loopback

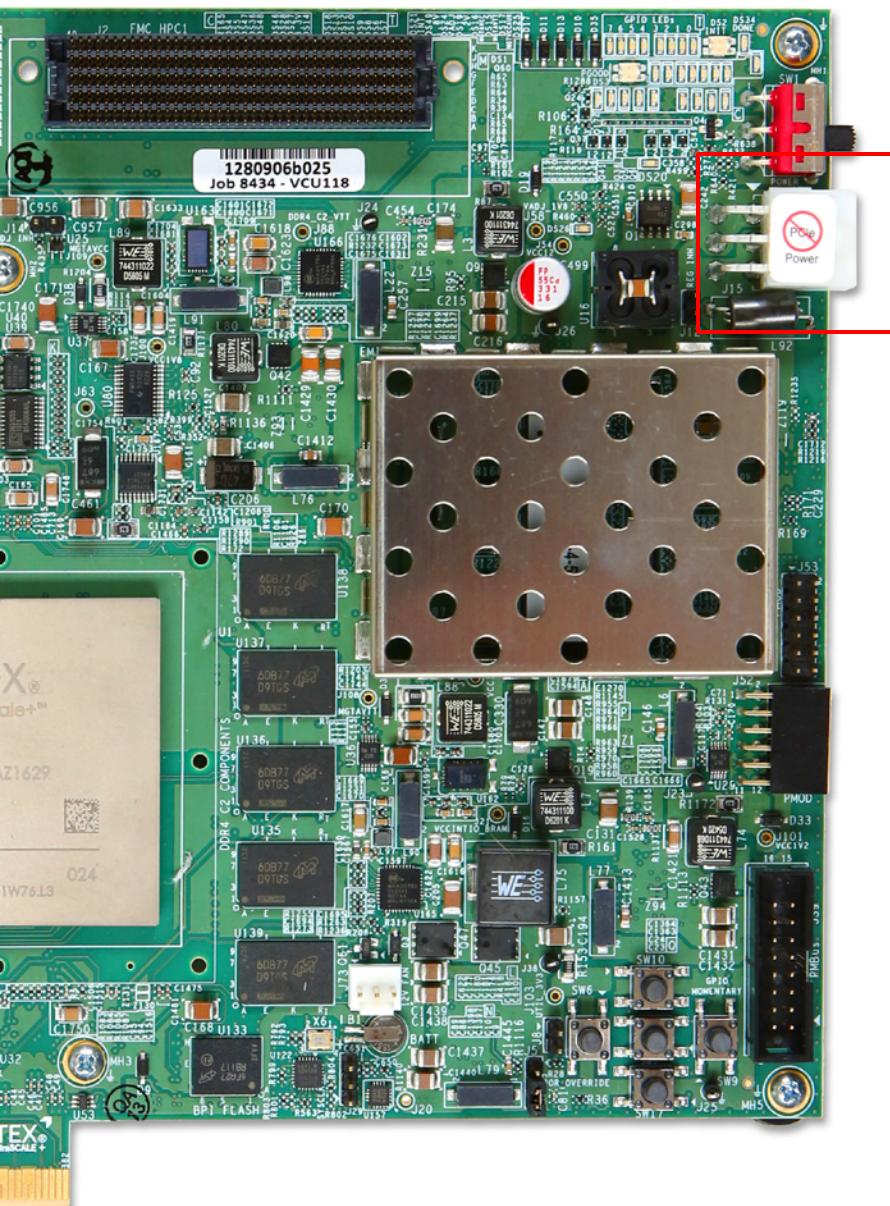


FireFly Insertion and Removal

- > From Samtec PDF:
 - » [FireFly Mating](#)



VCU118 Hardware Setup

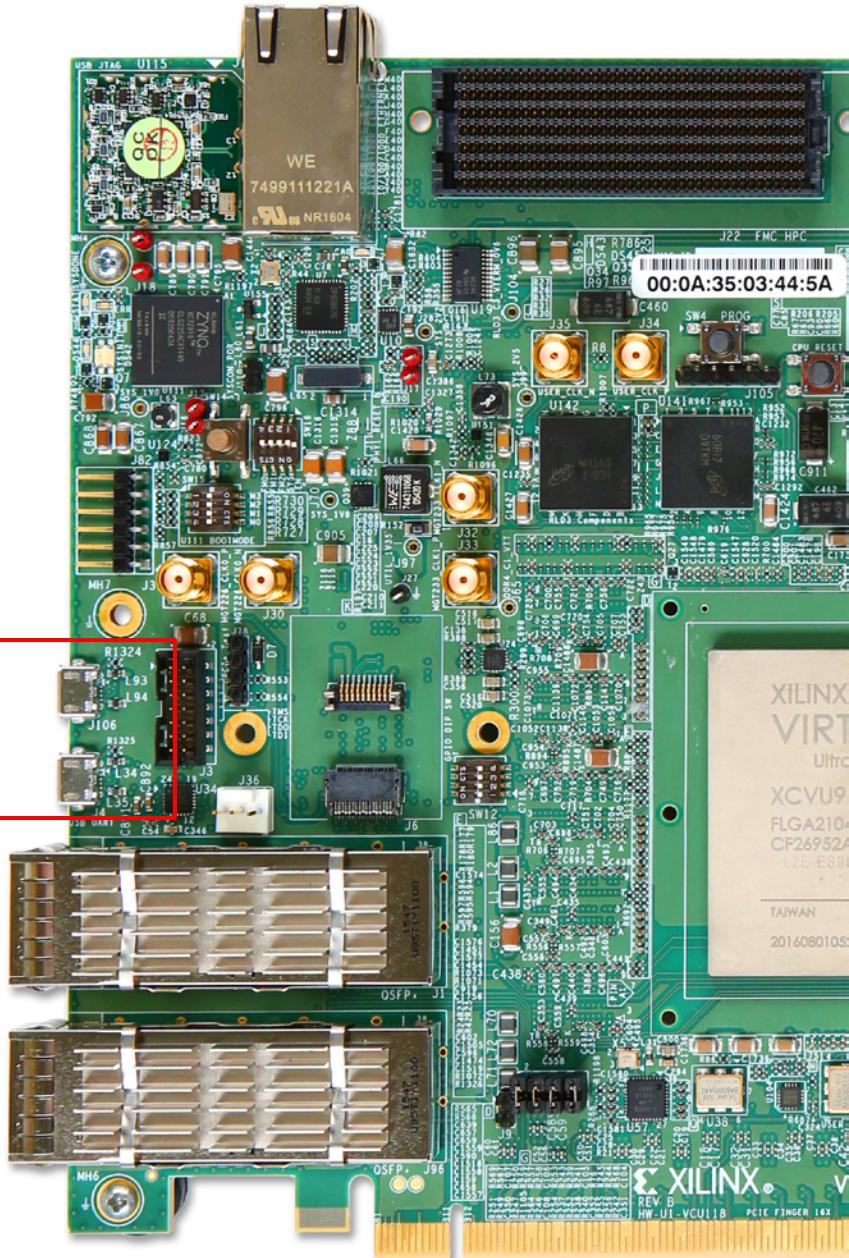


> Connect the power supply to the VCU118 (J15)

» Connect this cable to a power outlet

Hardware Setup

- > Connect USB Type-A to Micro-B cables to the USB JTAG (Digilent) and to the USB UART connectors on the VCU118 board
 - > Connect these cables to your PC
 - > Power on the VCU118 board for the UART driver installation

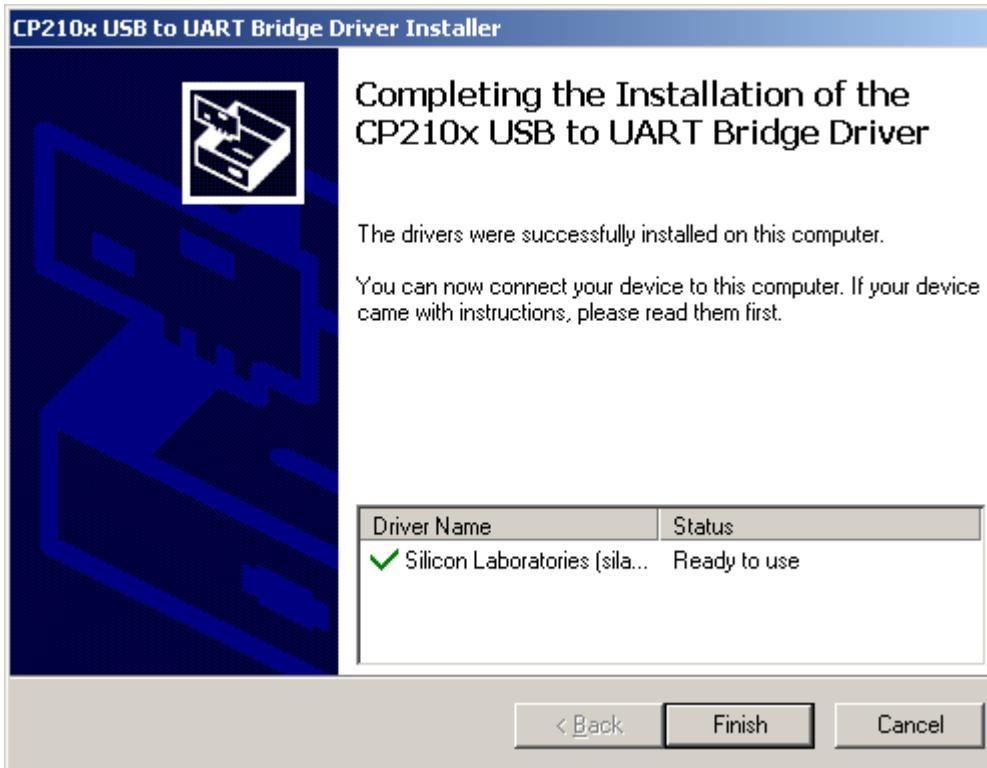


Note: Presentation applies to the VCU118

UART Driver Install

> Install Si Labs CP210x USB UART Drivers

» Refer to [UG1033](#) for details on installing the USB to UART Drivers



UART Driver Install

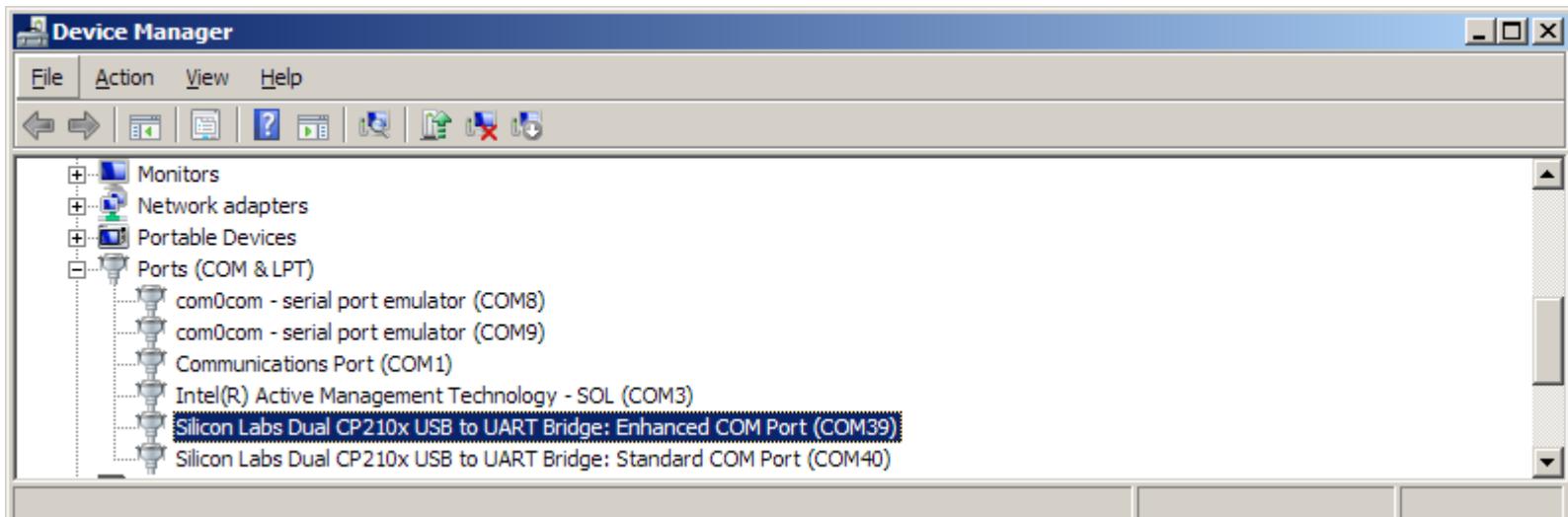
> Determine the COM Port numbers for your system

> Open the Device manager

Control Panel → System → Device Manager

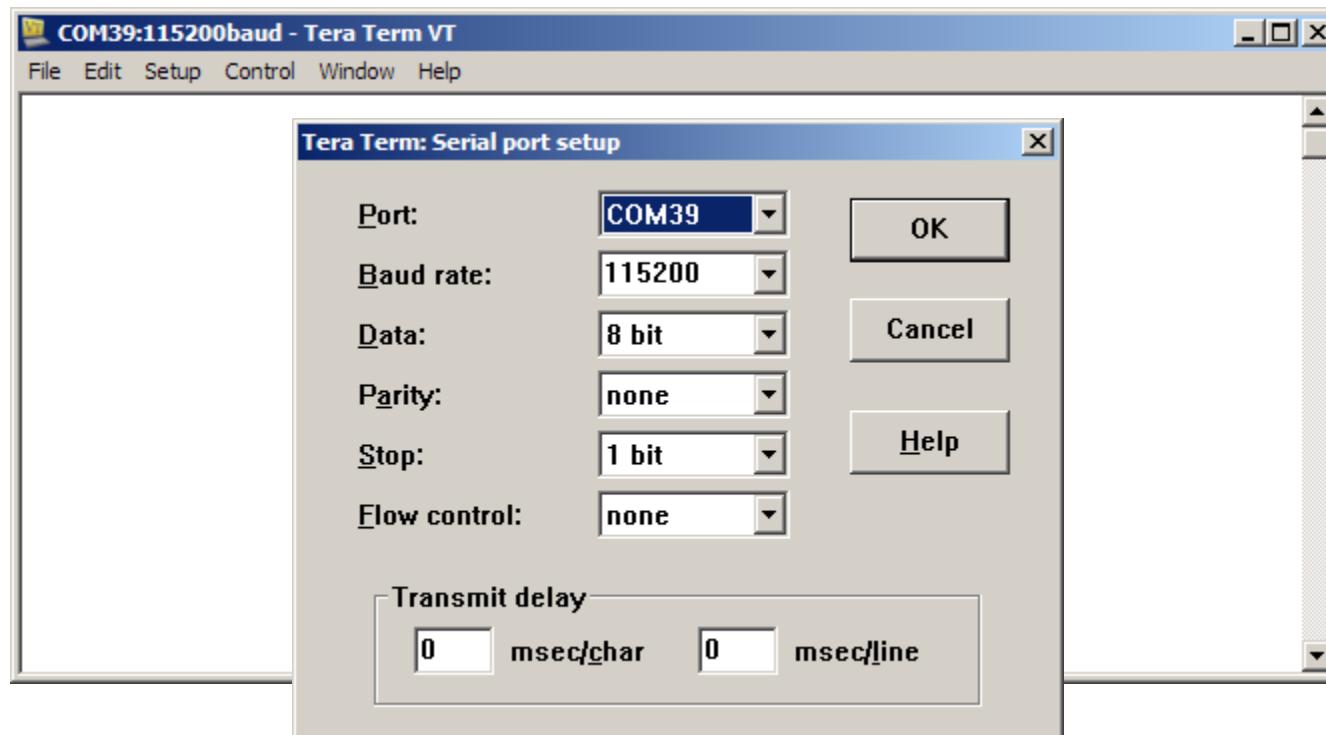
- » There will be two “Silicon Labs Dual CP210x” COM ports, Standard and Enhanced
- » The Standard COM Port is the FPGA UART COM Port
- » The Enhanced COM Port is the System Controller COM Port
- » The COM Port numbers will vary from system to system

> These COM Port Numbers will be used in several of the tutorials



Terminal Setup

- > Refer to [UG1036](#) regarding Tera Term installation
- > Board Power must be on before starting Tera Term
- > Start the Terminal Program
 - » Select your USB Com Port
 - » Set the baud to 115200

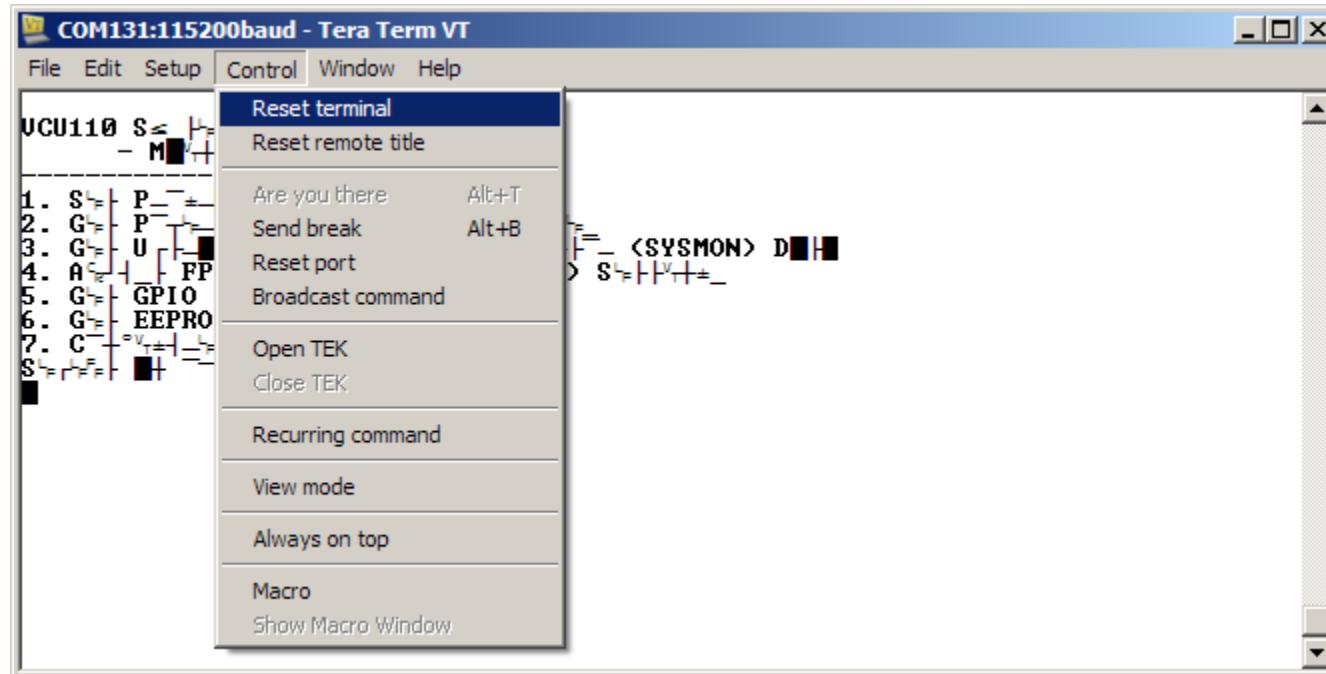


Note: See AR63771 regarding SDK Terminal Program

Terminal Setup

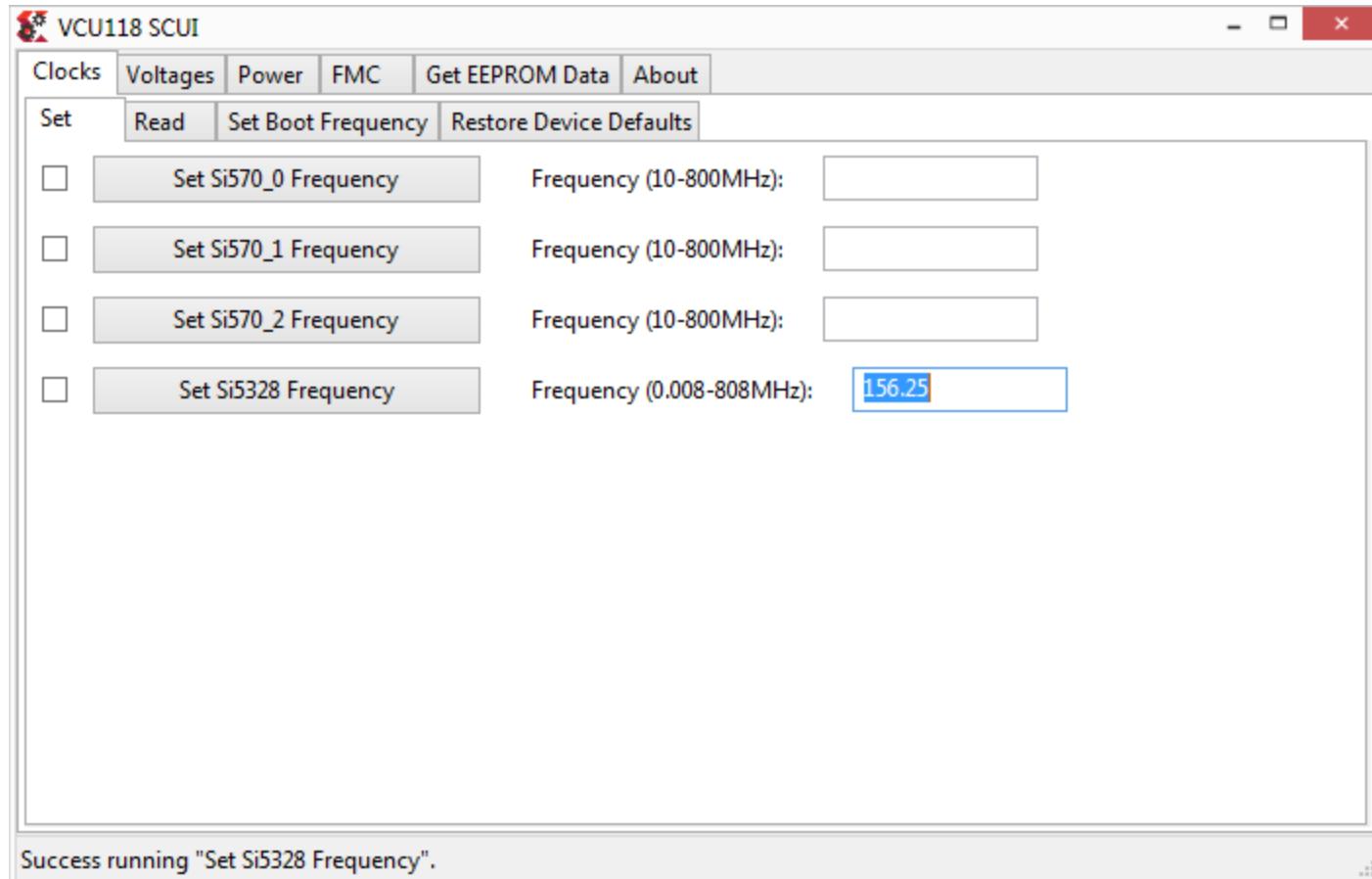
- > If 115200 UART output occurs while set to 9600, you may need to reset Tera Term. From the menu select:

Control -> Reset Terminal



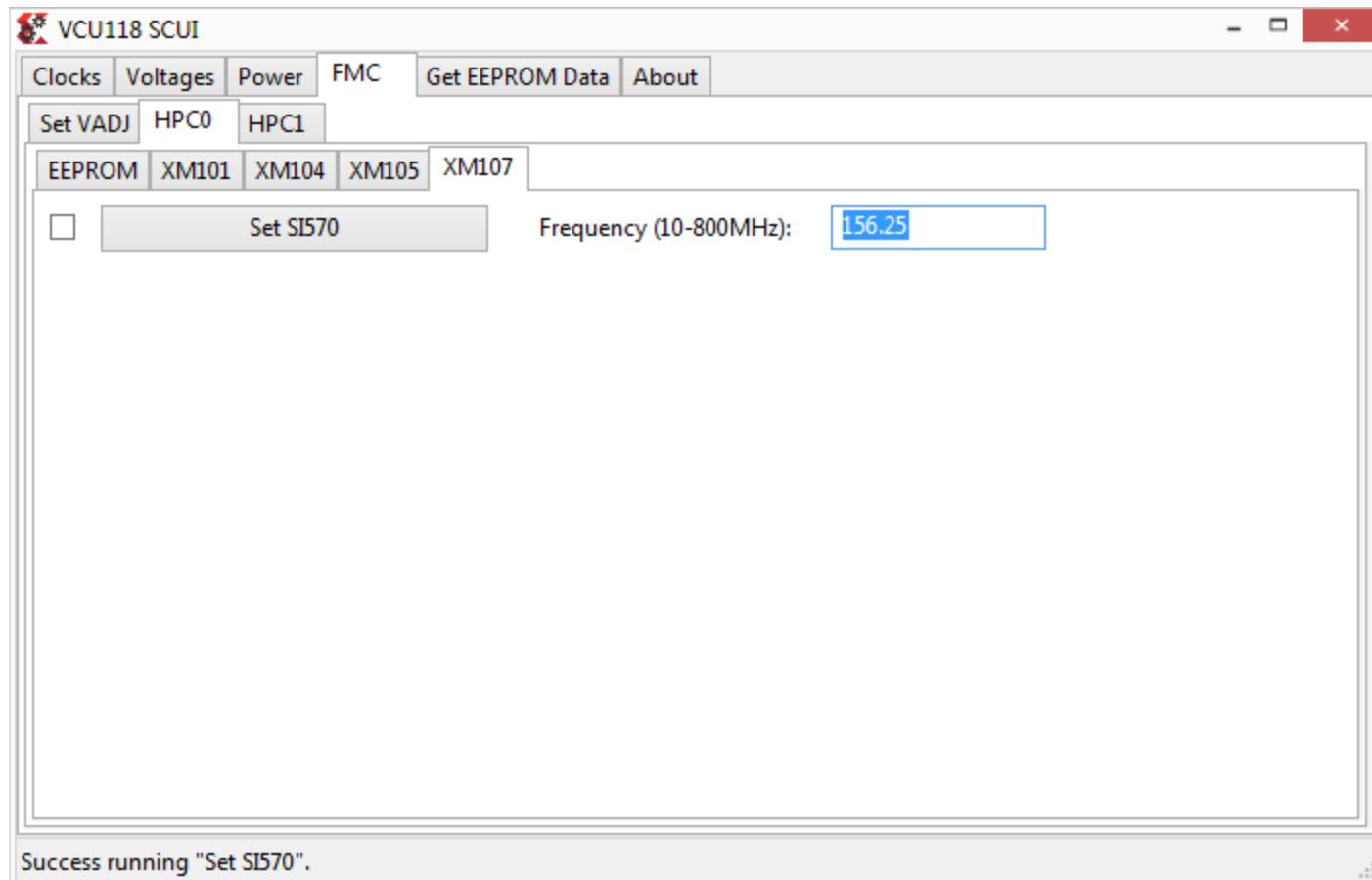
Setting the clocks with the System Controller GUI

- > See XTP447 for details on using the System Controller GUI
- > Select the Set tab underneath the Clocks tab
- > Enter 156.25 for the Si5328 and click Set Si5328 Frequency



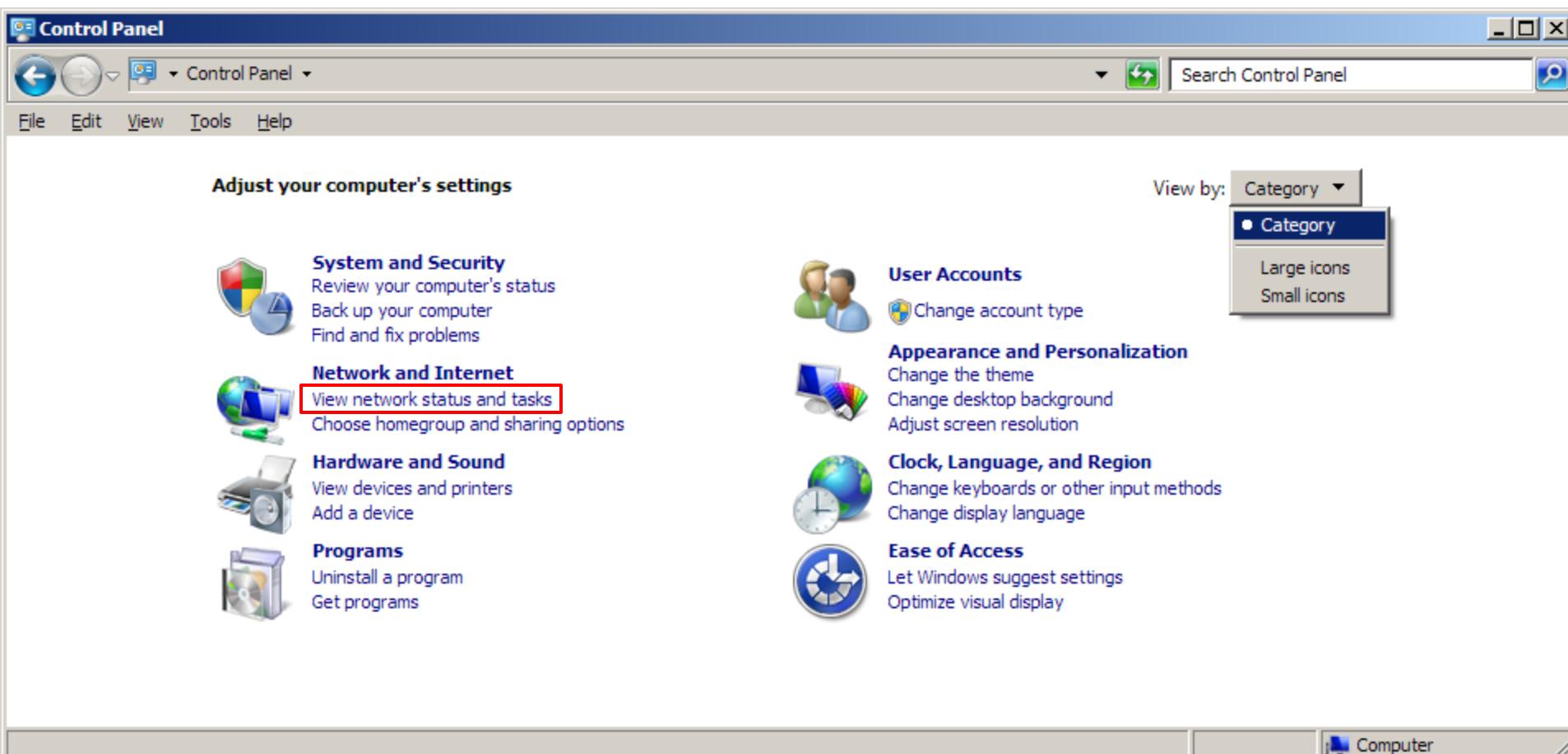
Setting FMC HPC clock

- > With the FMC+ Loopback card attached, select the XM107 tab
- > For the IBERT FMC+ testing, set 156.25, and click Set SI570



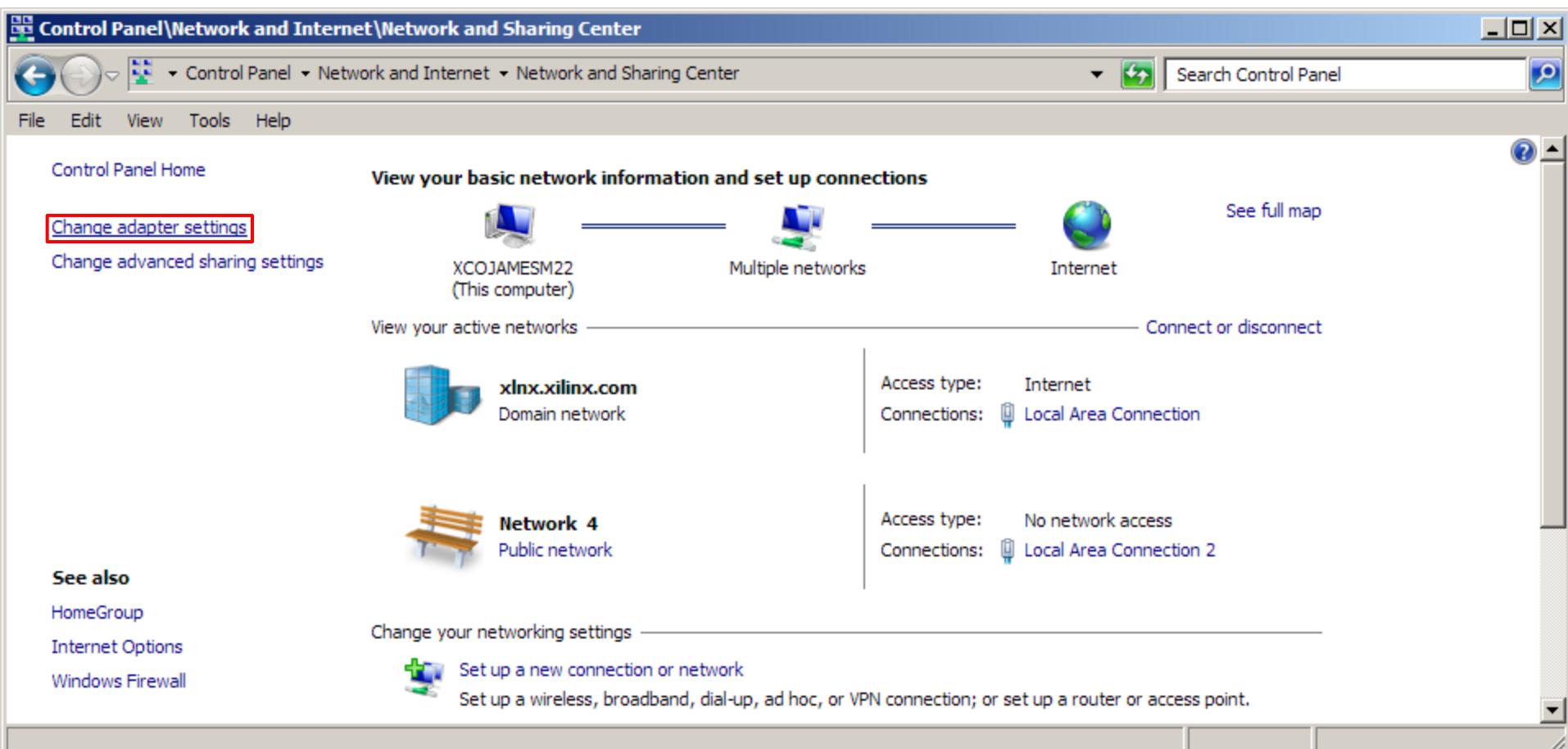
Ethernet Setup

- > Open the Windows Control Panel
 - » Set to View by Category
- > Click on “View network status and tasks”



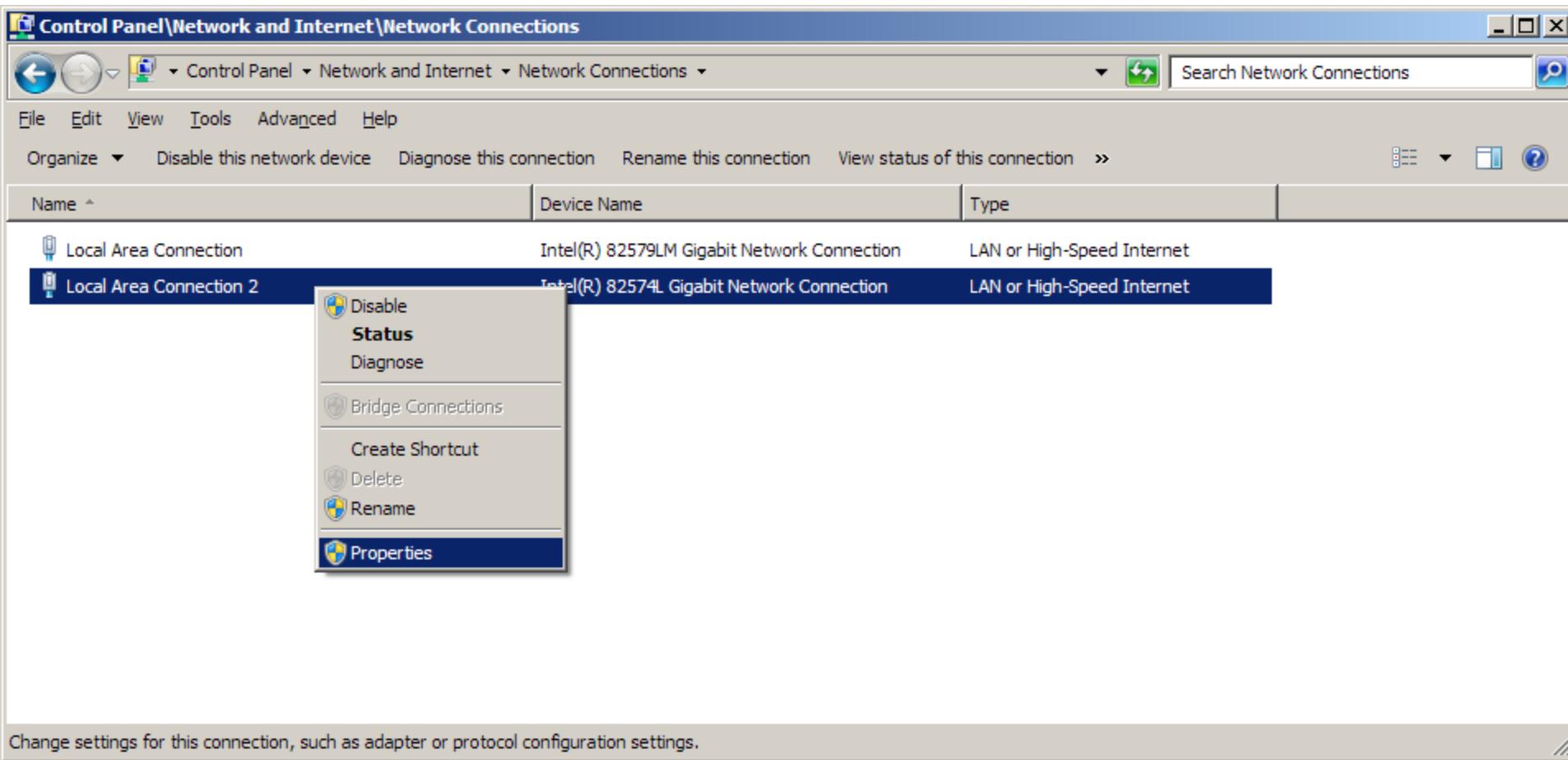
Ethernet Setup

- > Click on “Change adapter settings”



Ethernet Setup

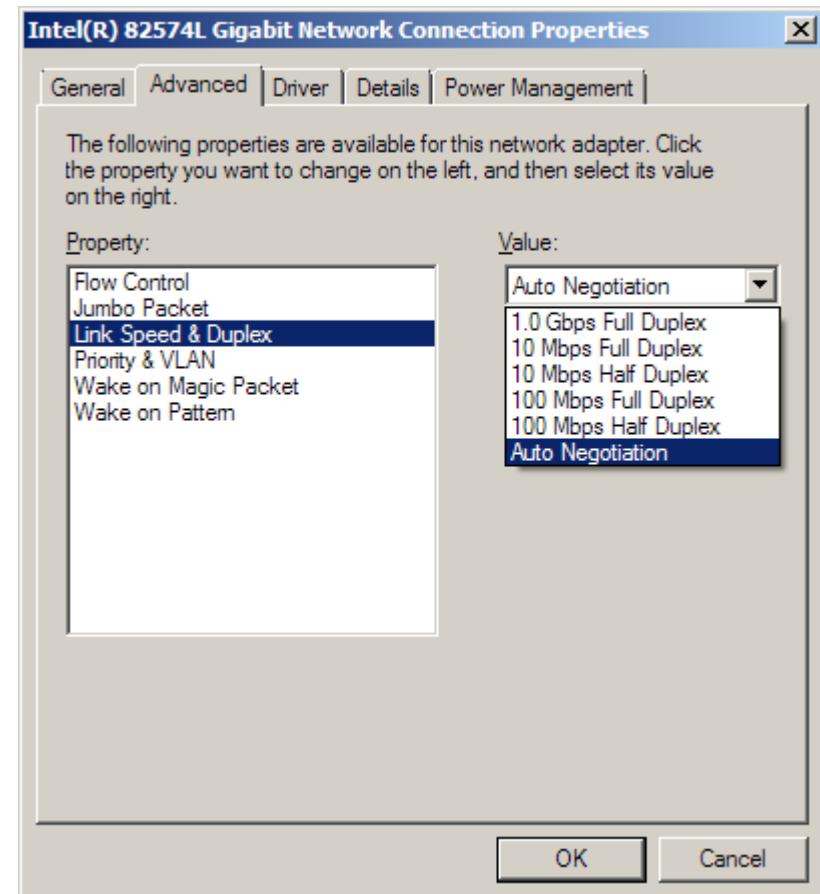
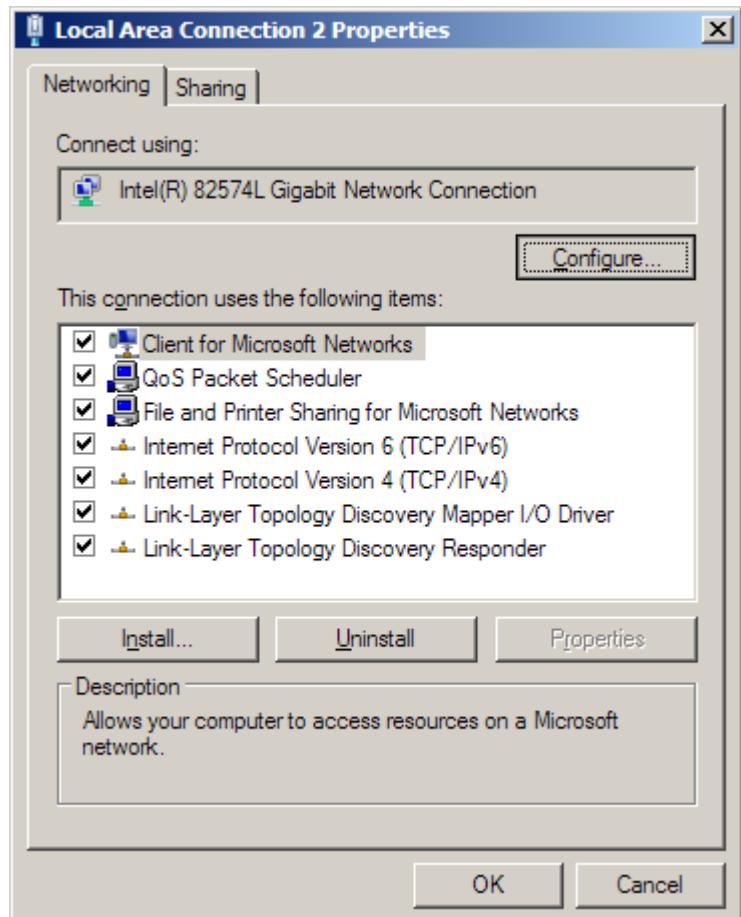
- > Right-click on the Gigabit Ethernet Adapter that you will be using for this test and select Properties



Ethernet Setup

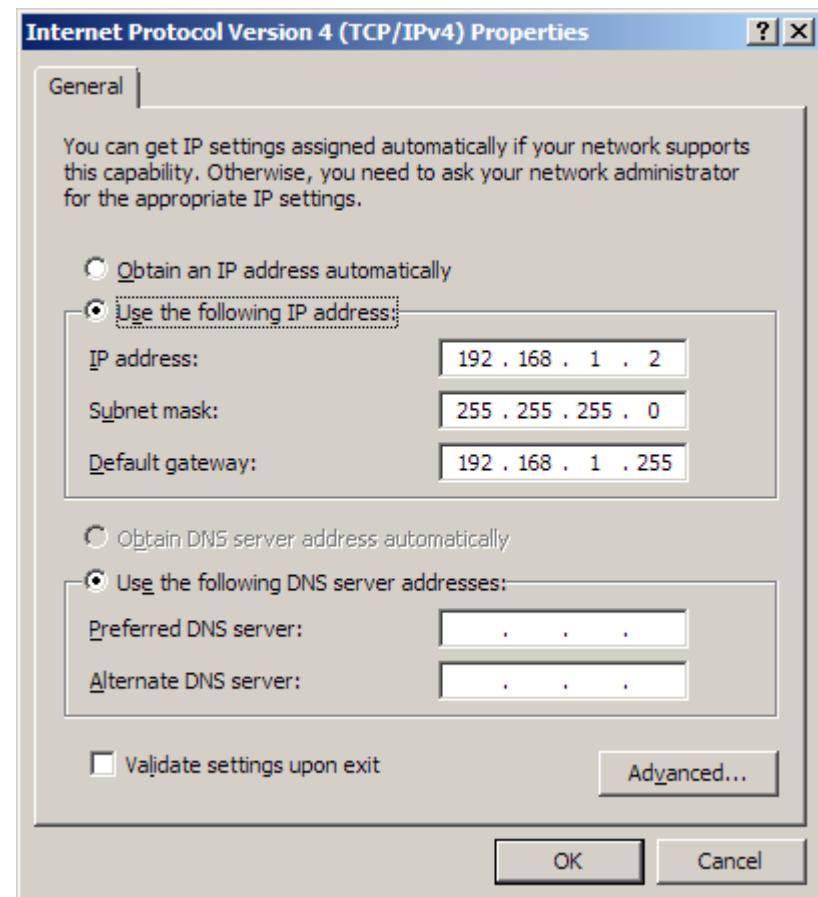
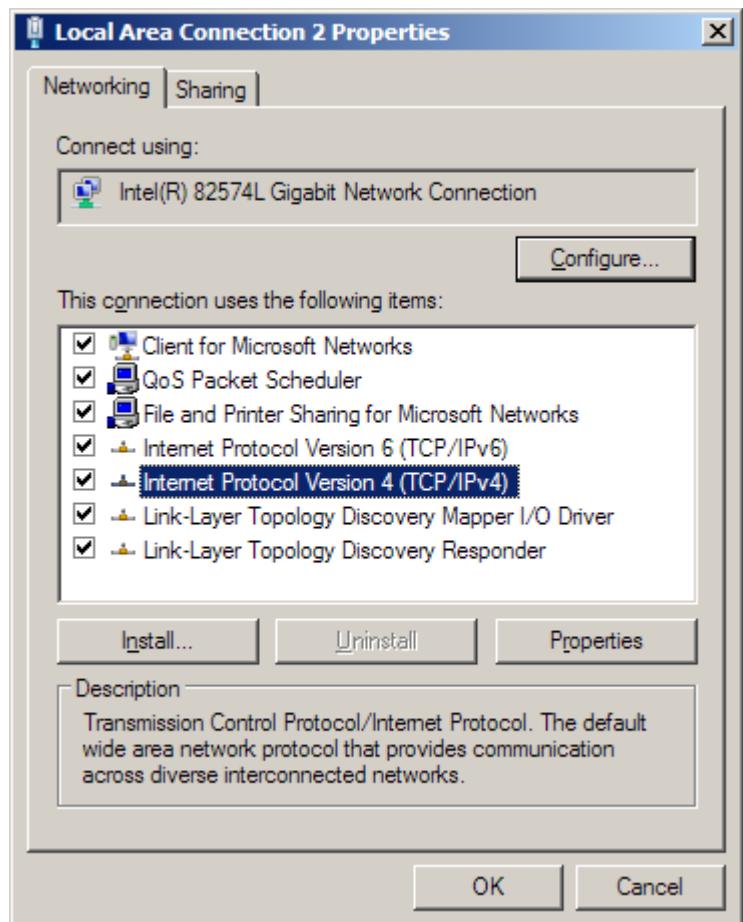
> Click Configure

- » Set the Link Speed & Duplex to Auto Negotiation then click OK



Ethernet Setup

- > Reopen the properties after the last step
- > Double-click the Internet Protocol Version 4
- > Set your host (PC) to this IP Address:



Note: Remember to restore your IP settings when finished

Optional Hardware Setup

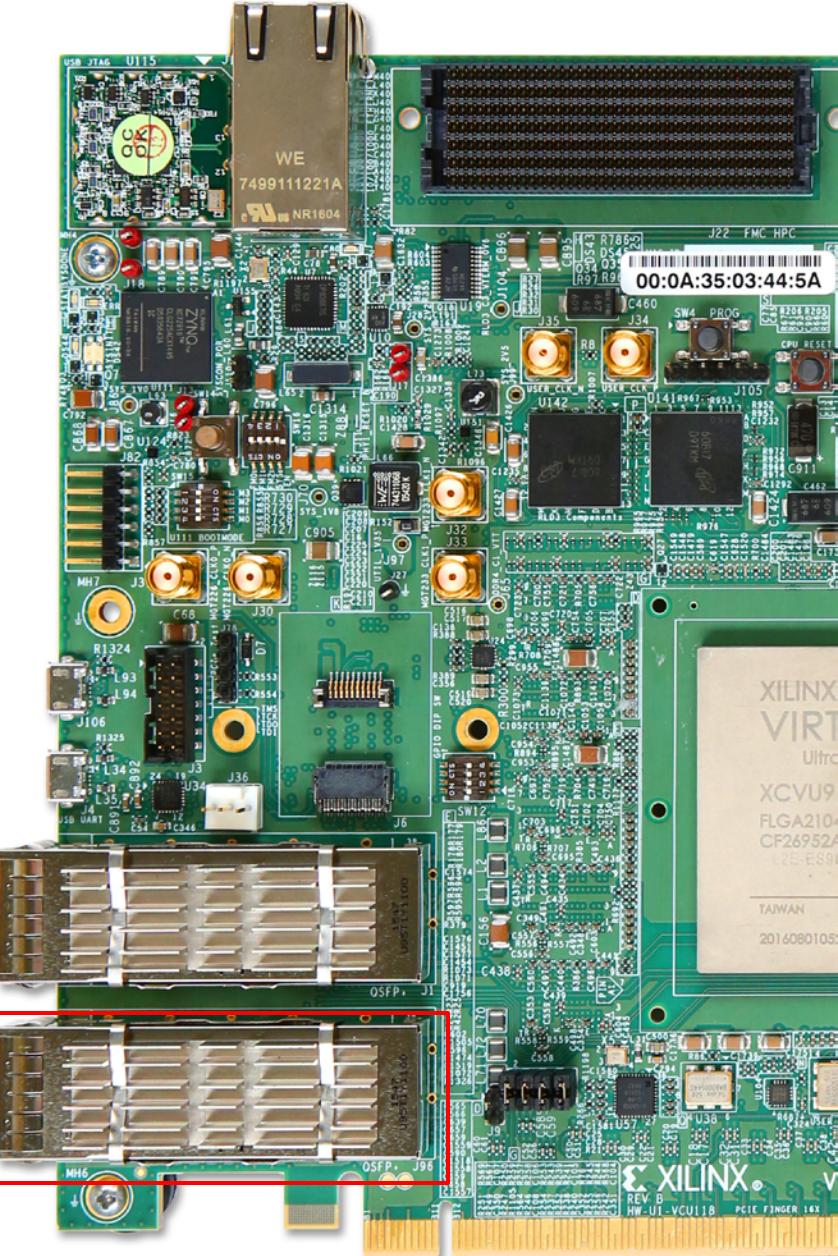
> A second QSFP Loopback Adapter

> <http://www.molex.com>

> QSFP+ Universal Loopback Adapter, 5dB

> Part # [74763-0025](#)

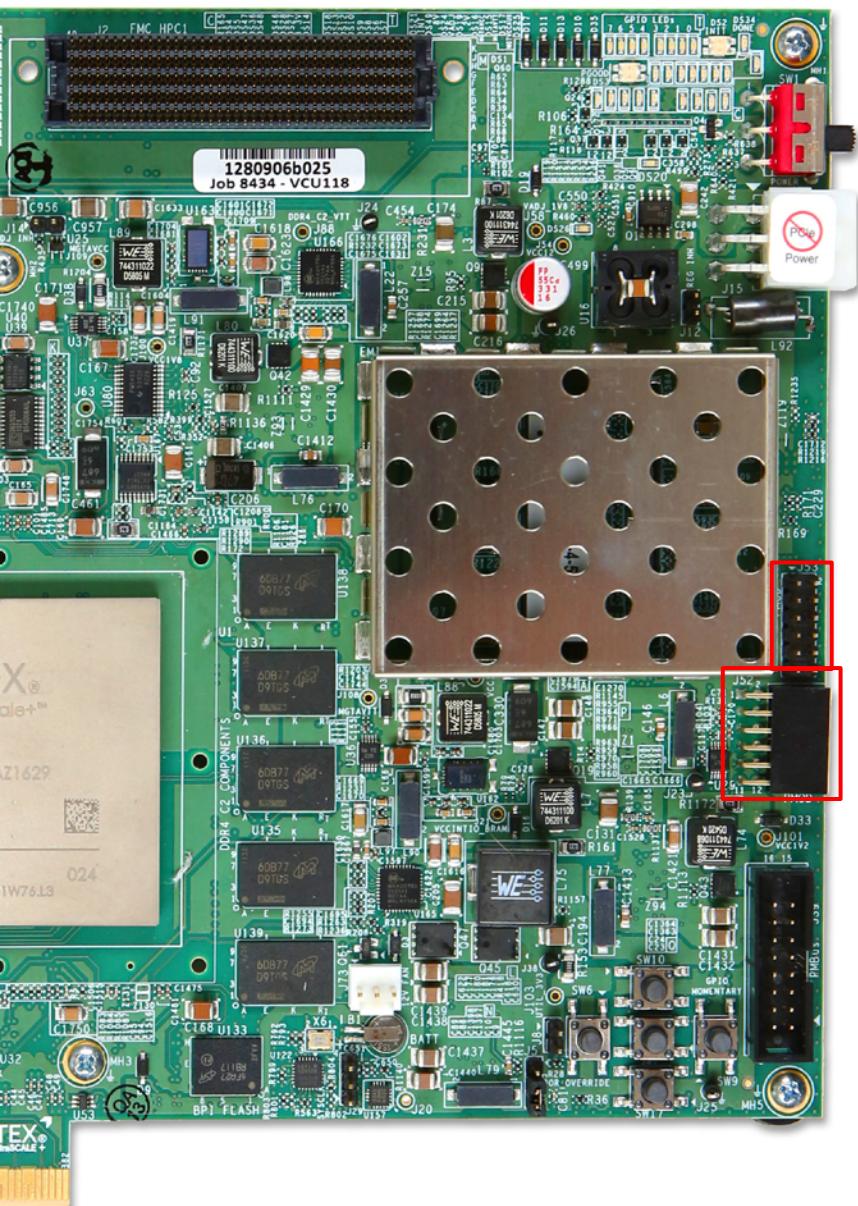
> Insert this adapter into the Bottom QSFP cage (J96) on the VCU118



Note: Presentation applies to the VCU118

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Optional Hardware Setup



- > Connect PMOD headers
 - >> 1 to 2
 - >> 3 to 4
 - >> 5 to 6
 - >> 7 to 8
- > Both J52 and J53:

Note: Presentation applies to the VCU118

Optional Hardware Setup

> SMA Cables

- » www.rosenbergerna.com
- » Part number:
72D-32S1-32S1-00610A



> Optional: SMA Quick connects

- » RADIALL
- » Part number: R125791501
- » Available [here](#) or [here](#)



> SMA Blocking Capacitors

- » Required for MGT226 and MGT233 SMA connections
- » Not needed on Rev 2.0 boards
- » www.minicircuits.com
- » Part number: [BLK-18-S+](#)



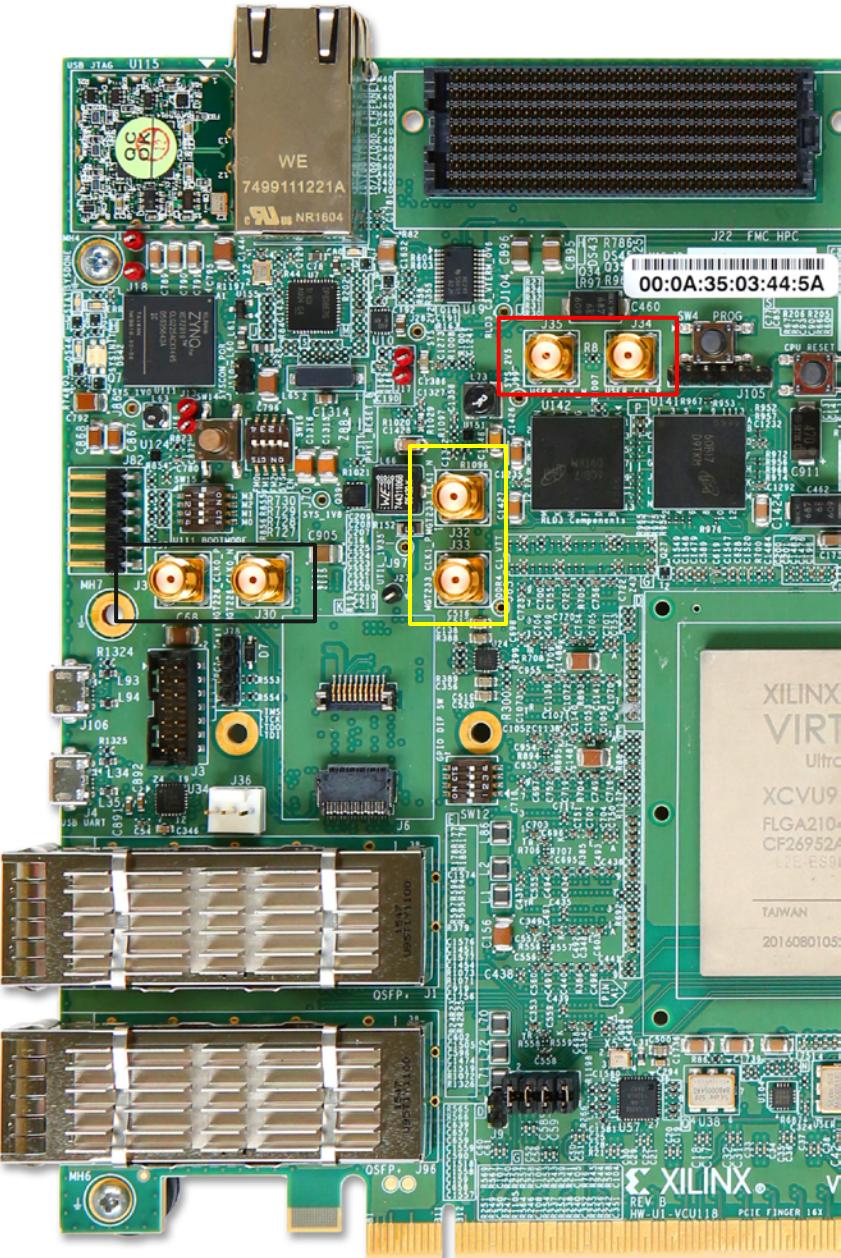
> Optional: Splitters

- » www.minicircuits.com
- » Part number: [ZFRSC-42-S+](#)



Optional Hardware Setup

- > Connect a 156.25 MHz clock source to these SMA inputs:
 - > MGT226_CLK0, J30, J31 (Black)
 - > MGT233_CLK0, J32, J33 (Yellow)
 - > USER_CLK, J34, J35 (Red)
- > **MGT226 and MGT233 require DC Blocking Capacitors**
 - > On all VCU118 boards through Rev 1.1
- > Use splitters if desired



Note: Presentation applies to the VCU118

References



References

> Vivado Release Notes

- » Vivado Design Suite User Guide - Release Notes – UG973
 - https://www.xilinx.com/support/documentation/sw_manuals/xilinx2019_1/ug973-vivado-release-notes-install-license.pdf
- » Vivado Design Suite 2019 - Vivado Known Issues
 - <https://www.xilinx.com/support/answers/72162.html>

> Vivado Programming and Debugging

- » Vivado Design Suite Programming and Debugging User Guide – UG908
 - https://www.xilinx.com/support/documentation/sw_manuals/xilinx2019_1/ug908-vivado-programming-debugging.pdf

Documentation



Documentation

- > **Virtex UltraScale+**
 - » Virtex UltraScale+ FPGA Family
 - <https://www.xilinx.com/products/silicon-devices/fpga/virtex-ultrascale-plus.html>
- > **VCU118 Documentation**
 - » Virtex UltraScale+ FPGA VCU118 Evaluation Kit
 - <https://www.xilinx.com/products/boards-and-kits/vcu118.html>
 - » VCU118 Board User Guide – UG1224
 - https://www.xilinx.com/support/documentation/boards_and_kits/vcu118/ug1224-vcu118-eval-bd.pdf
 - » VCU118 Evaluation Kit Quick Start Guide User Guide – XTP453
 - https://www.xilinx.com/support/documentation/boards_and_kits/vcu118/xtp453-vcu118-quickstart.pdf
 - » VCU118 - Known Issues and Release Notes Master Answer Record
 - <https://www.xilinx.com/support/answers/68268.html>