

# VCU118 GT IBERT Design Creation

May 2019



XTP440

# Revision History

Date	Version	Description
05/29/19	9.0	Updated for 2019.1. Some screenshots not updated.
12/10/18	8.0	Updated for 2018.3. Some screenshots not updated.
06/18/18	7.0	Updated for 2018.2.
04/09/18	6.0	Updated for 2018.1.
12/20/17	5.0	Updated for 2017.4.
10/26/17	4.0	Updated for 2017.3.1. For Rev 2.0, with Production Silicon.
06/20/17	3.0	Updated for 2017.2.
04/19/17	2.0	Updated for 2017.1.
12/19/16	1.0	Initial version for 2016.4.

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# VCU118 IBERT Overview

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  - » Testing IBERT QSFP
  - » Testing IBERT Firefly
- > Create IBERT Design
  - » Compile Example Design
  - » Run IBERT Example Design
- > References

# VCU118 IBERT Overview

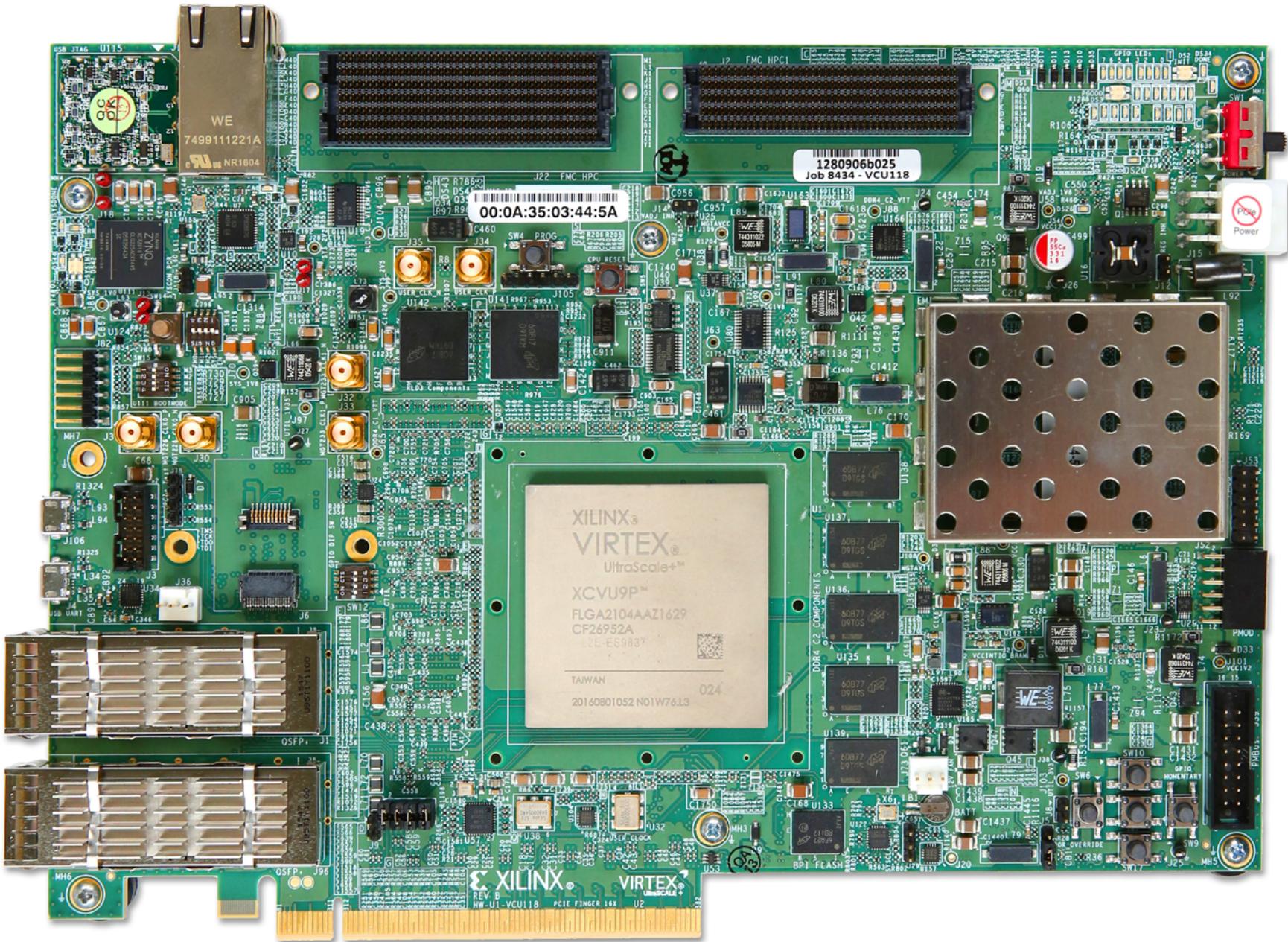
## > Description

- » The LogiCORE Integrated Bit Error Ratio (IBERT) core is used to create a pattern generation and verification design to exercise the UltraScale Virtex GTY transceivers. A graphical user interface is provided through the Vivado Hardware Manager.

## > Reference Design IP

- » LogiCORE UltraScale IBERT GTY Example Designs

# Xilinx VCU118 Board



# VCU118 Software Install and Board Setup

- > Complete setup steps in XTP449 – VCU118 Software Install and Board Setup:

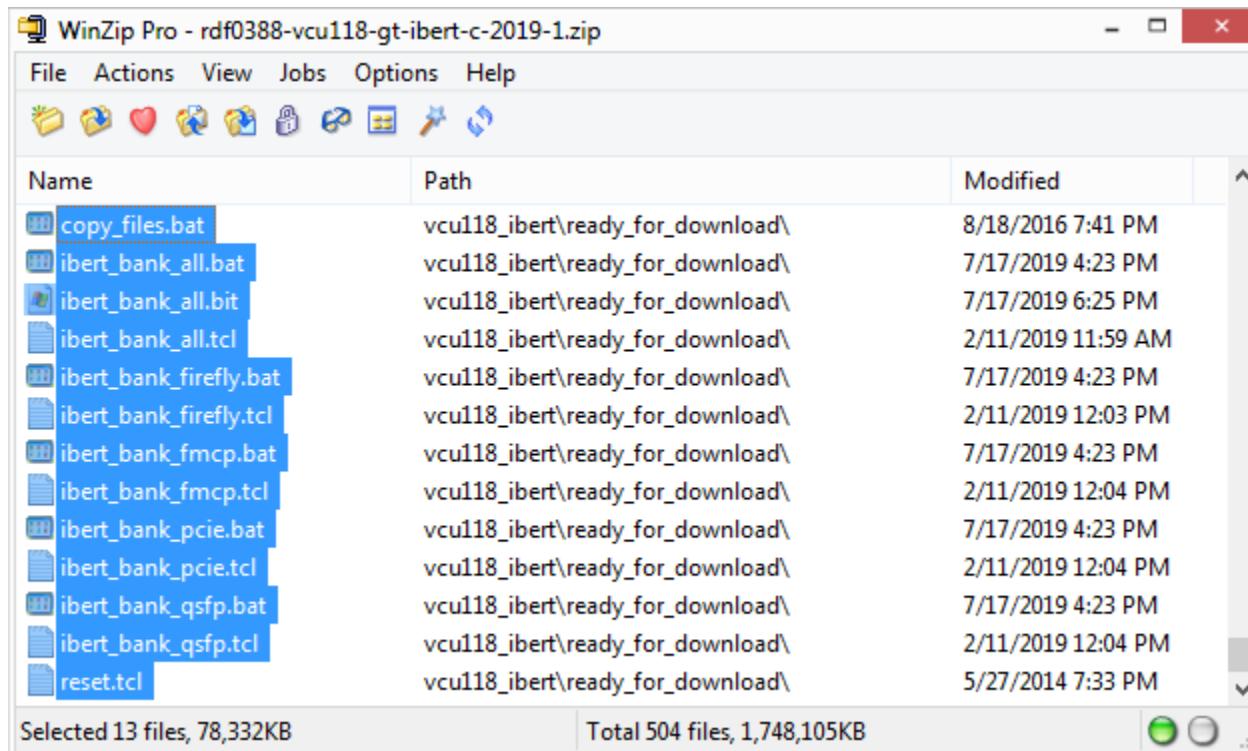
- » Software Requirements
- » VCU118 Board Setup
- » UART Driver Install
- » Clock Setup
- » IBERT Loopbacks
- » Optional Hardware Setup



Note: Clock Setup must be completed for IBERT testing

# VCU118 Setup

- > Open the RDF0388 - VCU118 GT IBERT Design Files (2019.1 C) ZIP file, and extract the “ready\_for\_download” files to your C:\ drive:



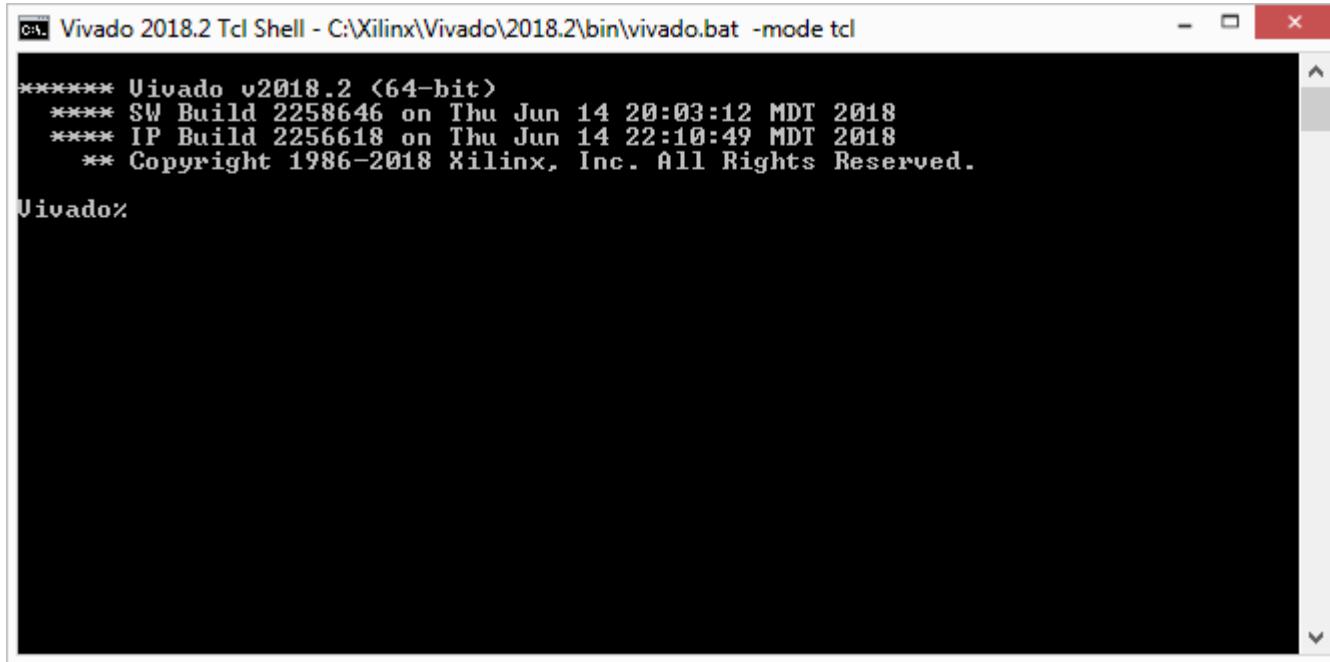
# Testing IBERT FMC+



# Testing IBERT FMC+

## > Open a Vivado Tcl Shell:

Start → All Programs → Xilinx Design Tools → Vivado 2019.1 →  
Vivado 2019.1 Tcl Shell



Vivado 2018.2 Tcl Shell - C:\Xilinx\Vivado\2018.2\bin\vivado.bat -mode tcl

```
***** Vivado v2018.2 (64-bit)
***** SW Build 2258646 on Thu Jun 14 20:03:12 MDT 2018
***** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.
```

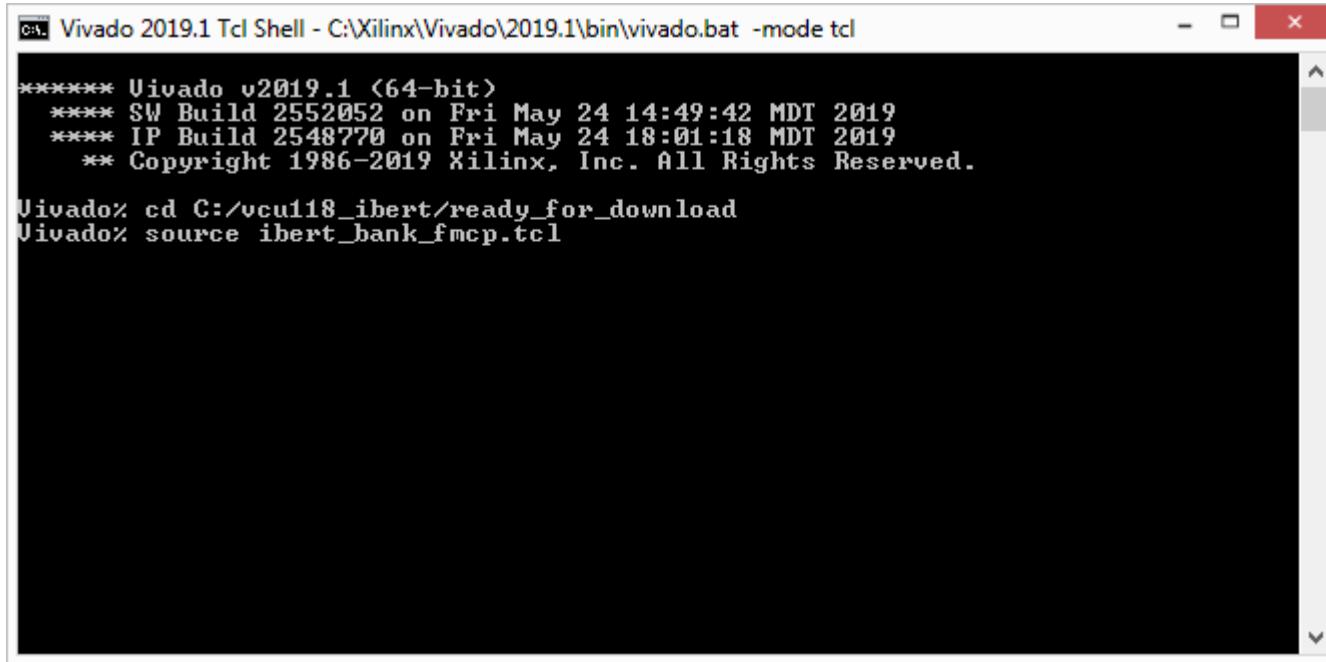
Vivado>

The screenshot shows a Windows command-line interface window titled "Vivado 2018.2 Tcl Shell". The title bar also includes the path "C:\Xilinx\Vivado\2018.2\bin\vivado.bat -mode tcl". The window contains the startup text for Vivado 2018.2, which includes the software version, build date and time, and copyright information. Below this text, there is a single command prompt line starting with "Vivado>" followed by a blank line for input.

# Testing IBERT FMC+

- > In the Vivado Tcl Shell type:

```
cd C:/vcu118_ibert/ready_for_download  
source ibert_bank_fmcpl.tcl
```

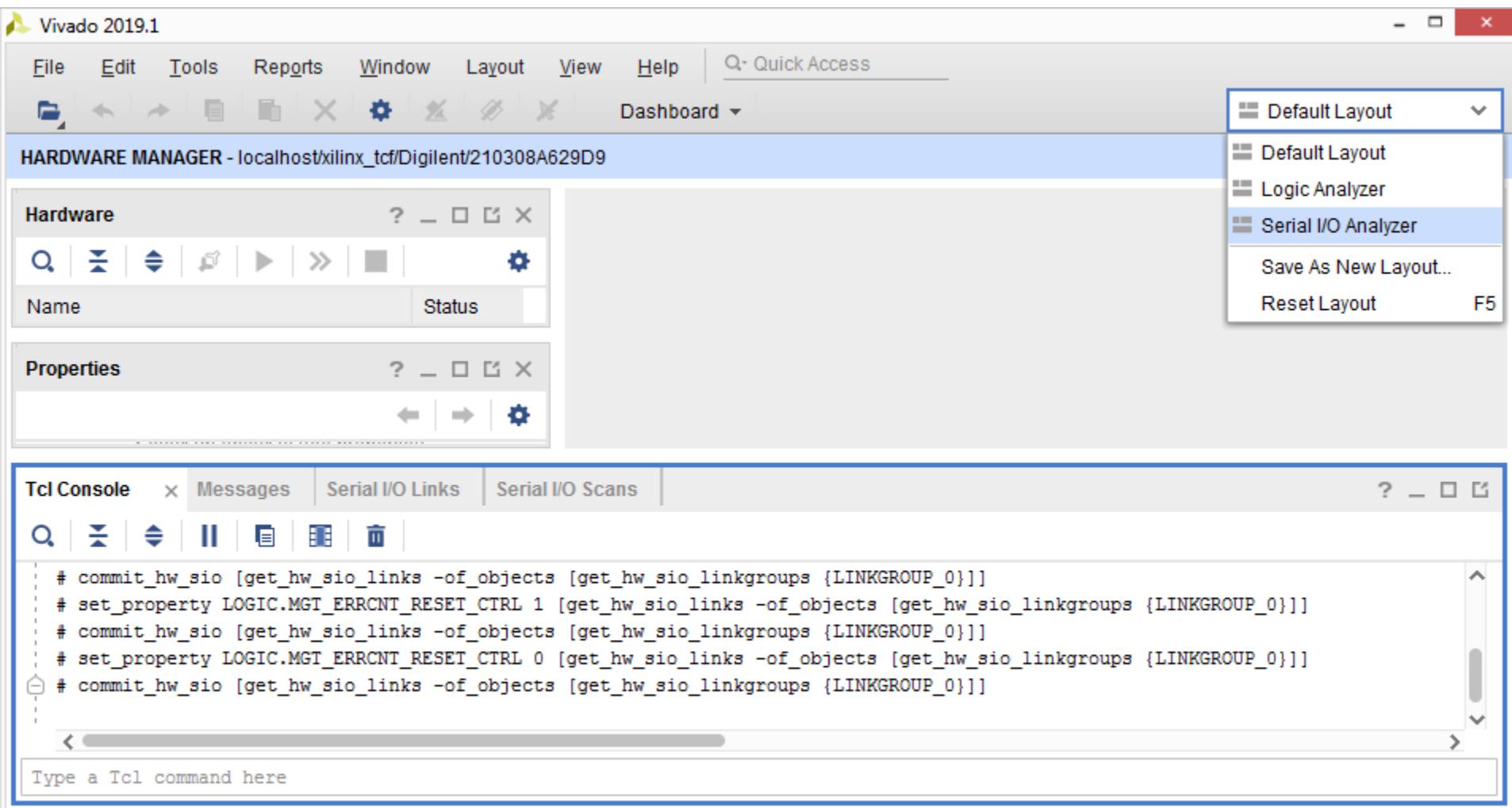


The screenshot shows a Windows command-line interface window titled "Vivado 2019.1 Tcl Shell - C:\Xilinx\Vivado\2019.1\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2019.1 (64-bit)  
***** SW Build 2552052 on Fri May 24 14:49:42 MDT 2019  
***** IP Build 2548770 on Fri May 24 18:01:18 MDT 2019  
** Copyright 1986-2019 Xilinx, Inc. All Rights Reserved.  
  
Vivado> cd C:/vcu118_ibert/ready_for_download  
Vivado> source ibert_bank_fmcpl.tcl
```

# Testing IBERT FMC+

- > If needed, set Vivado GUI Layout to Serial I/O Analyzer



# Testing IBERT FMC+

- > FMC+ line rate is 25 Gbps
- > Close Vivado GUI and Tcl Shell when finished viewing

Serial I/O Links									
Name	TX	RX	Status	Bits	Errors	BER	BERT Re...	TX Pattern	RX Pattern
Link 0	MGT_X0Y4/TX	MGT_X0Y4/RX	25.000 Gbps	4.525E12	0E0	2.21E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 1	MGT_X0Y5/TX	MGT_X0Y5/RX	24.982 Gbps	4.524E12	0E0	2.21E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 2	MGT_X0Y6/TX	MGT_X0Y6/RX	25.000 Gbps	4.524E12	0E0	2.21E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 3	MGT_X0Y7/TX	MGT_X0Y7/RX	25.001 Gbps	4.524E12	0E0	2.21E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 4	MGT_X0Y8/TX	MGT_X0Y8/RX	25.000 Gbps	4.524E12	0E0	2.21E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 5	MGT_X0Y9/TX	MGT_X0Y9/RX	24.983 Gbps	4.524E12	0E0	2.211E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 6	MGT_X0Y10/TX	MGT_X0Y10/RX	25.000 Gbps	4.524E12	0E0	2.211E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 7	MGT_X0Y11/TX	MGT_X0Y11/RX	24.985 Gbps	4.524E12	0E0	2.211E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 8	MGT_X0Y12/TX	MGT_X0Y12/RX	25.028 Gbps	4.524E12	0E0	2.211E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 9	MGT_X0Y13/TX	MGT_X0Y13/RX	25.000 Gbps	4.524E12	0E0	2.211E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 10	MGT_X0Y14/TX	MGT_X0Y14/RX	24.998 Gbps	4.524E12	0E0	2.21E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 11	MGT_X0Y15/TX	MGT_X0Y15/RX	25.000 Gbps	4.524E12	0E0	2.21E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 12	MGT_X0Y24/TX	MGT_X0Y24/RX	25.003 Gbps	4.524E12	0E0	2.21E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 13	MGT_X0Y25/TX	MGT_X0Y25/RX	25.000 Gbps	4.524E12	0E0	2.21E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 14	MGT_X0Y26/TX	MGT_X0Y26/RX	25.000 Gbps	4.524E12	0E0	2.21E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 15	MGT_X0Y27/TX	MGT_X0Y27/RX	25.007 Gbps	4.524E12	0E0	2.21E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 16	MGT_X0Y28/TX	MGT_X0Y28/RX	24.995 Gbps	4.524E12	0E0	2.21E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 17	MGT_X0Y29/TX	MGT_X0Y29/RX	24.968 Gbps	4.524E12	0E0	2.21E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 18	MGT_X0Y30/TX	MGT_X0Y30/RX	25.025 Gbps	4.524E12	0E0	2.21E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 19	MGT_X0Y31/TX	MGT_X0Y31/RX	24.980 Gbps	4.524E12	0E0	2.21E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 20	MGT_X0Y32/TX	MGT_X0Y32/RX	25.000 Gbps	4.524E12	0E0	2.21E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 21	MGT_X0Y33/TX	MGT_X0Y33/RX	25.049 Gbps	4.524E12	0E0	2.21E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 22	MGT_X0Y34/TX	MGT_X0Y34/RX	25.021 Gbps	4.524E12	0E0	2.21E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit
Link 23	MGT_X0Y35/TX	MGT_X0Y35/RX	25.000 Gbps	4.524E12	0E0	2.21E-13	Reset	PRBS 31-bit	▼ PRBS 31-bit

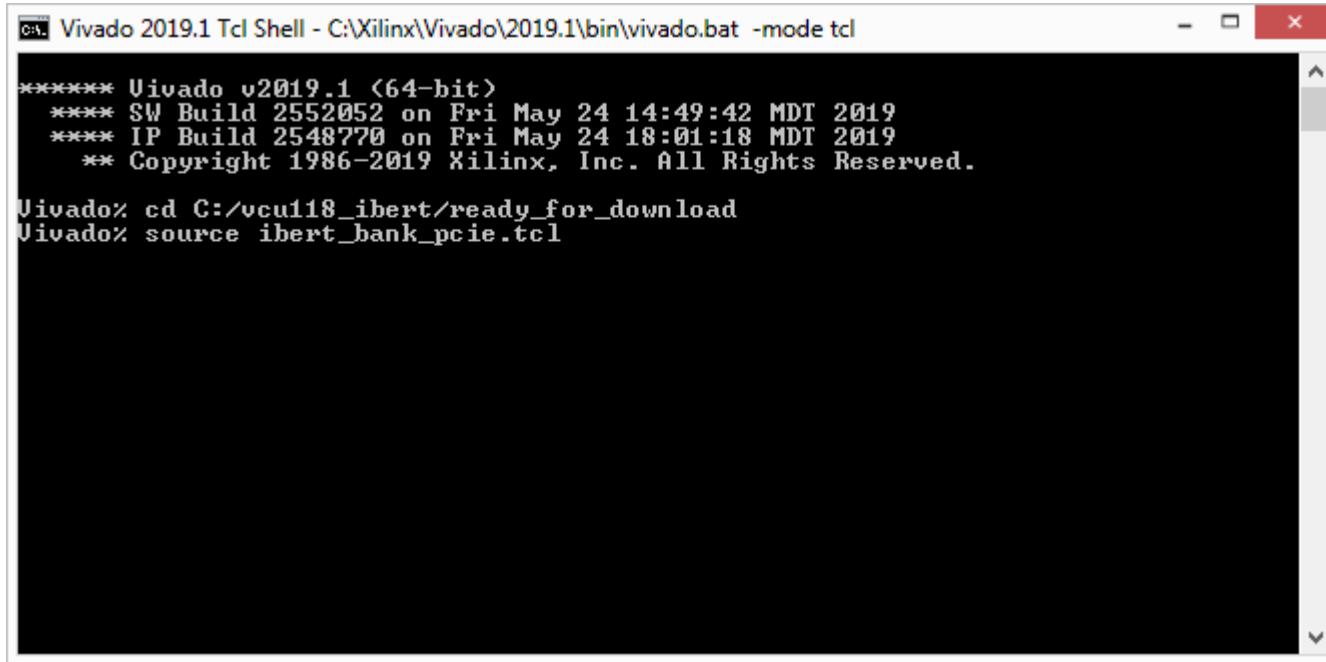
# Testing IBERT PCIe



# Testing IBERT PCIe

- > In a Vivado Tcl Shell type:

```
cd C:/vcu118_ibert/ready_for_download  
source ibert_bank_pcie.tcl
```



The screenshot shows a Windows command-line interface window titled "Vivado 2019.1 Tcl Shell - C:\Xilinx\Vivado\2019.1\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2019.1 (64-bit)  
***** SW Build 2552052 on Fri May 24 14:49:42 MDT 2019  
***** IP Build 2548770 on Fri May 24 18:01:18 MDT 2019  
** Copyright 1986-2019 Xilinx, Inc. All Rights Reserved.  
  
Vivado> cd C:/vcu118_ibert/ready_for_download  
Vivado> source ibert_bank_pcie.tcl
```

# Testing IBERT PCIe

> 8 Gbps for PCIe; close Vivado GUI and Tcl Shell when finished

Vivado 2019.1

File Edit Tools Reports Window Layout View Help Quick Access

Dashboard Serial I/O Analyzer

HARDWARE MANAGER - localhost/xilinx\_tcf/Digilent/210308A629D9

Tcl Console Messages Serial I/O Links Serial I/O Scans

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern
Ungrouped Links (0)									
Link Group 0 (16)							Reset	PRBS 31-bit	PRBS 31-bit
Link 0	MGT_X1Y20/TX	MGT_X1Y20/RX	8.000 Gbps	1.67E12	0E0	5.987E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 1	MGT_X1Y21/TX	MGT_X1Y21/RX	8.000 Gbps	1.67E12	0E0	5.989E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 2	MGT_X1Y22/TX	MGT_X1Y22/RX	7.992 Gbps	1.67E12	0E0	5.988E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 3	MGT_X1Y23/TX	MGT_X1Y23/RX	8.000 Gbps	1.67E12	0E0	5.988E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 4	MGT_X1Y24/TX	MGT_X1Y24/RX	8.012 Gbps	1.67E12	0E0	5.988E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 5	MGT_X1Y25/TX	MGT_X1Y25/RX	8.000 Gbps	1.67E12	0E0	5.988E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 6	MGT_X1Y26/TX	MGT_X1Y26/RX	8.000 Gbps	1.67E12	0E0	5.988E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 7	MGT_X1Y27/TX	MGT_X1Y27/RX	8.000 Gbps	1.67E12	0E0	5.988E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 8	MGT_X1Y28/TX	MGT_X1Y28/RX	8.000 Gbps	1.67E12	0E0	5.988E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 9	MGT_X1Y29/TX	MGT_X1Y29/RX	8.009 Gbps	1.67E12	0E0	5.988E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 10	MGT_X1Y30/TX	MGT_X1Y30/RX	8.000 Gbps	1.67E12	0E0	5.988E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 11	MGT_X1Y31/TX	MGT_X1Y31/RX	8.000 Gbps	1.67E12	0E0	5.988E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 12	MGT_X1Y32/TX	MGT_X1Y32/RX	8.000 Gbps	1.67E12	0E0	5.988E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 13	MGT_X1Y33/TX	MGT_X1Y33/RX	8.000 Gbps	1.67E12	0E0	5.988E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 14	MGT_X1Y34/TX	MGT_X1Y34/RX	8.013 Gbps	1.67E12	0E0	5.988E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 15	MGT_X1Y35/TX	MGT_X1Y35/RX	8.000 Gbps	1.67E12	0E0	5.988E-13	Reset	PRBS 31-bit	PRBS 31-bit

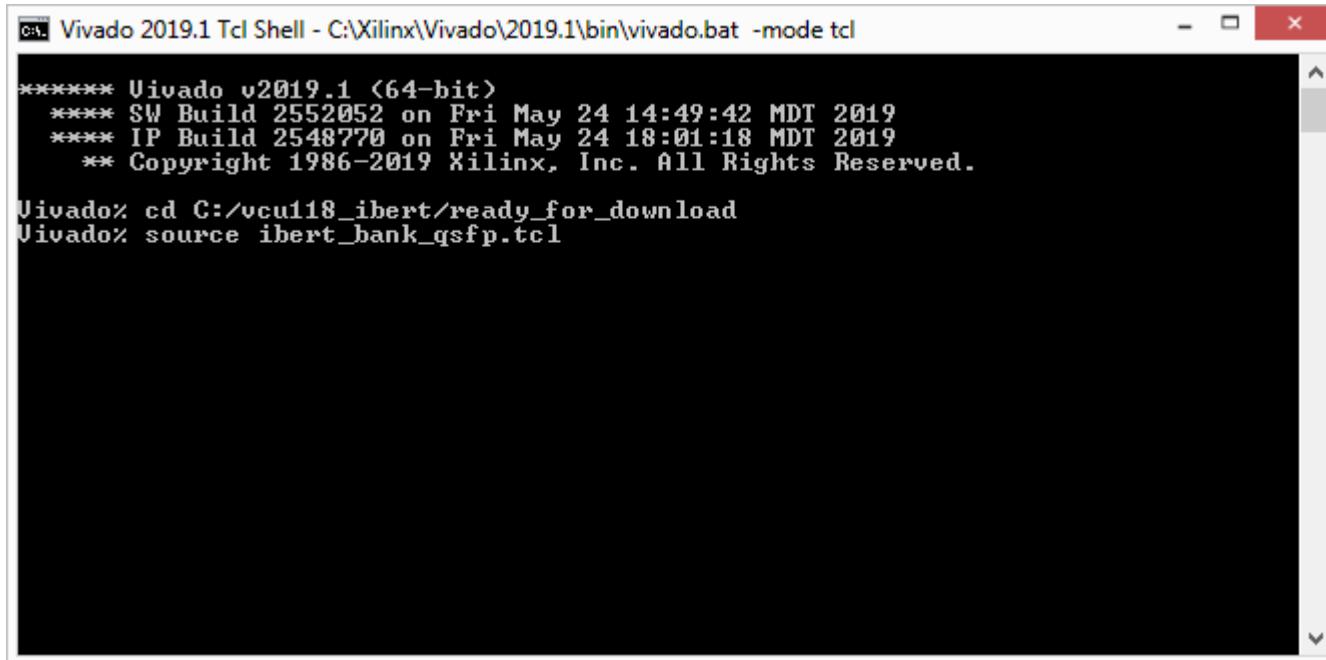
# Testing IBERT QSFP



# Testing IBERT QSFP

- > In a Vivado Tcl Shell type:

```
cd C:/vcu118_ibert/ready_for_download  
source ibert_bank_qsfp.tcl
```



The screenshot shows a Windows command-line interface window titled "Vivado 2019.1 Tcl Shell - C:\Xilinx\Vivado\2019.1\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2019.1 (64-bit)  
***** SW Build 2552052 on Fri May 24 14:49:42 MDT 2019  
***** IP Build 2548770 on Fri May 24 18:01:18 MDT 2019  
** Copyright 1986-2019 Xilinx, Inc. All Rights Reserved.  
  
Vivado> cd C:/vcu118_ibert/ready_for_download  
Vivado> source ibert_bank_qsfp.tcl
```

**Note:** This test requires a second user-supplied QSFP Loopback module

# Testing IBERT QSFP

- > 28 Gbps for QSFP
- > Close Vivado GUI and Tcl Shell when finished viewing

The screenshot shows the Vivado 2019.1 Hardware Manager interface. The title bar reads "Vivado 2019.1". The menu bar includes File, Edit, Tools, Reports, Window, Layout, View, Help, and Quick Access. The toolbar contains icons for file operations like Open, Save, and Close, along with a gear icon for settings. A "Dashboard" button is also present. On the right, a tab labeled "Serial I/O Analyzer" is visible. The main window is titled "HARDWARE MANAGER - localhost/xilinx\_tcf/Digilent/210308A629D9". Below the title, there are tabs for "Tcl Console", "Messages", "Serial I/O Links" (which is selected), and "Serial I/O Scans". The "Serial I/O Links" table has the following columns: Name, TX, RX, Status, Bits, Errors, BER, BERT Reset, TX Pattern, and RX Pattern. The table lists 8 links under "Link Group 0":

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern
Ungrouped Links (0)									
Link Group 0 (8)							Reset	PRBS 31-bit	PRBS 31-bit
Link 0	MGT_X1Y48/TX	MGT_X1Y48/RX	28.125 Gbps	3.289E12	0E0	3.041E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 1	MGT_X1Y49/TX	MGT_X1Y49/RX	28.125 Gbps	3.289E12	0E0	3.041E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 2	MGT_X1Y50/TX	MGT_X1Y50/RX	28.125 Gbps	3.289E12	0E0	3.041E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 3	MGT_X1Y51/TX	MGT_X1Y51/RX	28.125 Gbps	3.289E12	0E0	3.041E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 4	MGT_X1Y52/TX	MGT_X1Y52/RX	28.125 Gbps	3.289E12	0E0	3.041E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 5	MGT_X1Y53/TX	MGT_X1Y53/RX	28.125 Gbps	3.289E12	0E0	3.041E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 6	MGT_X1Y54/TX	MGT_X1Y54/RX	28.125 Gbps	3.289E12	0E0	3.041E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 7	MGT_X1Y55/TX	MGT_X1Y55/RX	28.125 Gbps	3.289E12	0E0	3.041E-13	Reset	PRBS 31-bit	PRBS 31-bit

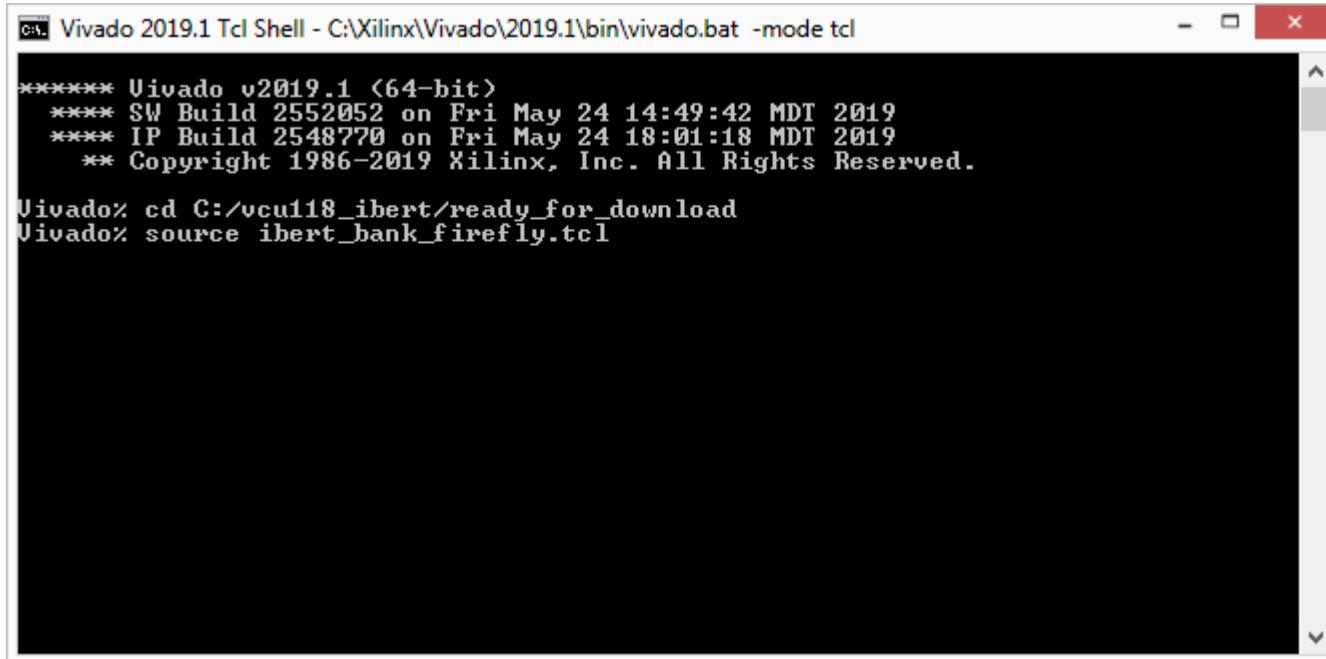
# Testing IBERT FireFly



# Testing IBERT FireFly

- > In a Vivado Tcl Shell type:

```
cd C:/vcu118_ibert/ready_for_download  
source ibert_bank_firefly.tcl
```



The screenshot shows a Windows command-line interface window titled "Vivado 2019.1 Tcl Shell - C:\Xilinx\Vivado\2019.1\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2019.1 (64-bit)  
***** SW Build 2552052 on Fri May 24 14:49:42 MDT 2019  
***** IP Build 2548770 on Fri May 24 18:01:18 MDT 2019  
** Copyright 1986-2019 Xilinx, Inc. All Rights Reserved.  
  
Vivado> cd C:/vcu118_ibert/ready_for_download  
Vivado> source ibert_bank_firefly.tcl
```

# Testing IBERT FireFly

- > 28 Gbps for FireFly
- > Close Vivado GUI and Tcl Shell when finished viewing

The screenshot shows the Vivado 2019.1 Hardware Manager interface. The title bar reads "Vivado 2019.1". The menu bar includes File, Edit, Tools, Reports, Window, Layout, View, Help, and Quick Access. The toolbar contains icons for New, Open, Save, Import, Export, and Dashboard. The main window is titled "HARDWARE MANAGER - localhost/xilinx\_tcf/Digilent/210308A629D9". The "Serial I/O Links" tab is selected, showing a table with the following data:

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern
Ungrouped Links (0)									
Link Group 0 (4)							Reset	PRBS 31-bit	PRBS 31-bit
Link 0	MGT_X1Y56/TX	MGT_X1Y56/RX	28.125 Gbps	4.858E12	0E0	2.058E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 1	MGT_X1Y57/TX	MGT_X1Y57/RX	28.125 Gbps	4.858E12	0E0	2.058E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 2	MGT_X1Y58/TX	MGT_X1Y58/RX	28.128 Gbps	4.858E12	0E0	2.058E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 3	MGT_X1Y59/TX	MGT_X1Y59/RX	28.125 Gbps	4.858E12	0E0	2.058E-13	Reset	PRBS 31-bit	PRBS 31-bit

# Create IBERT Design

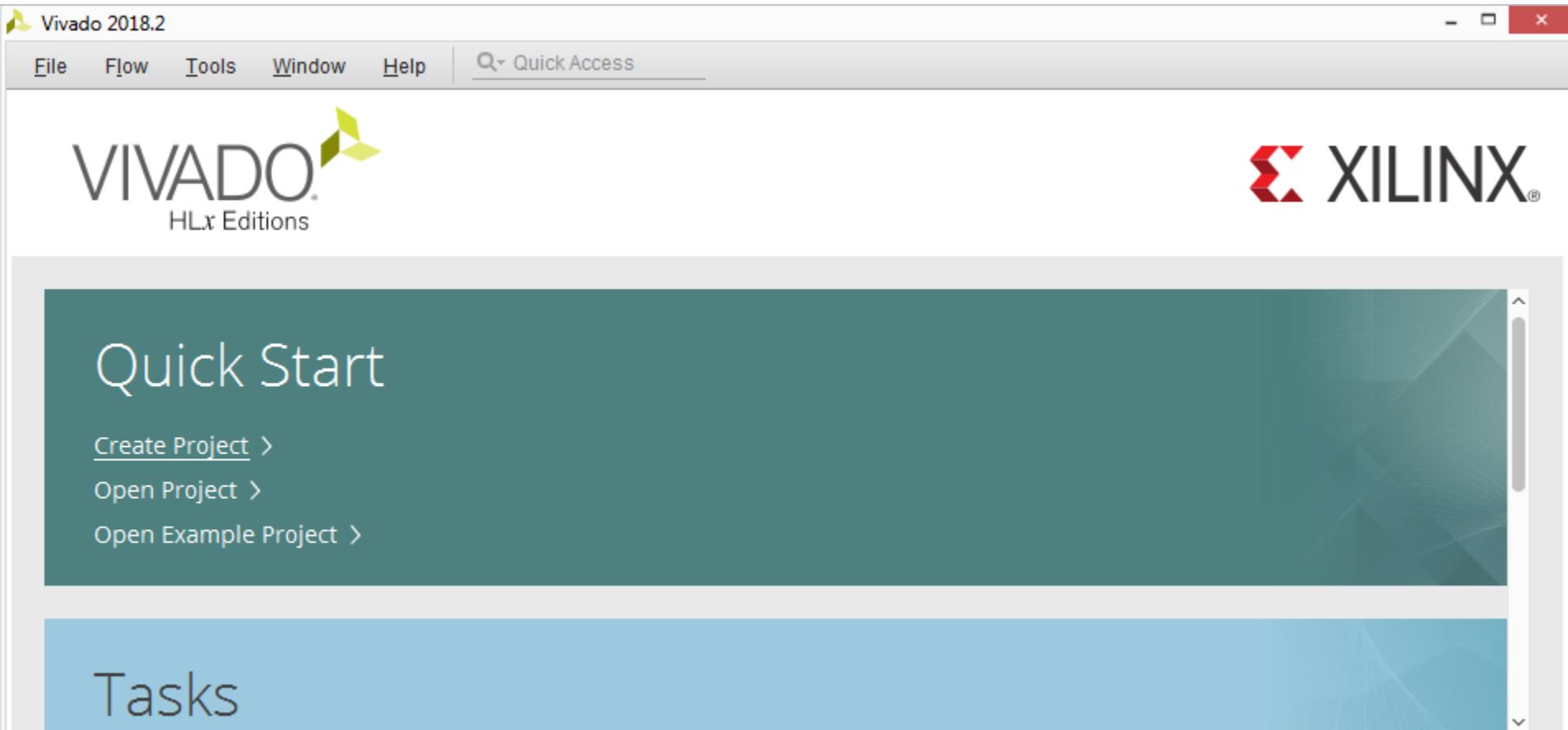


# Create IBERT Design

## > Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2019.1 → Vivado

## > Select Create Project



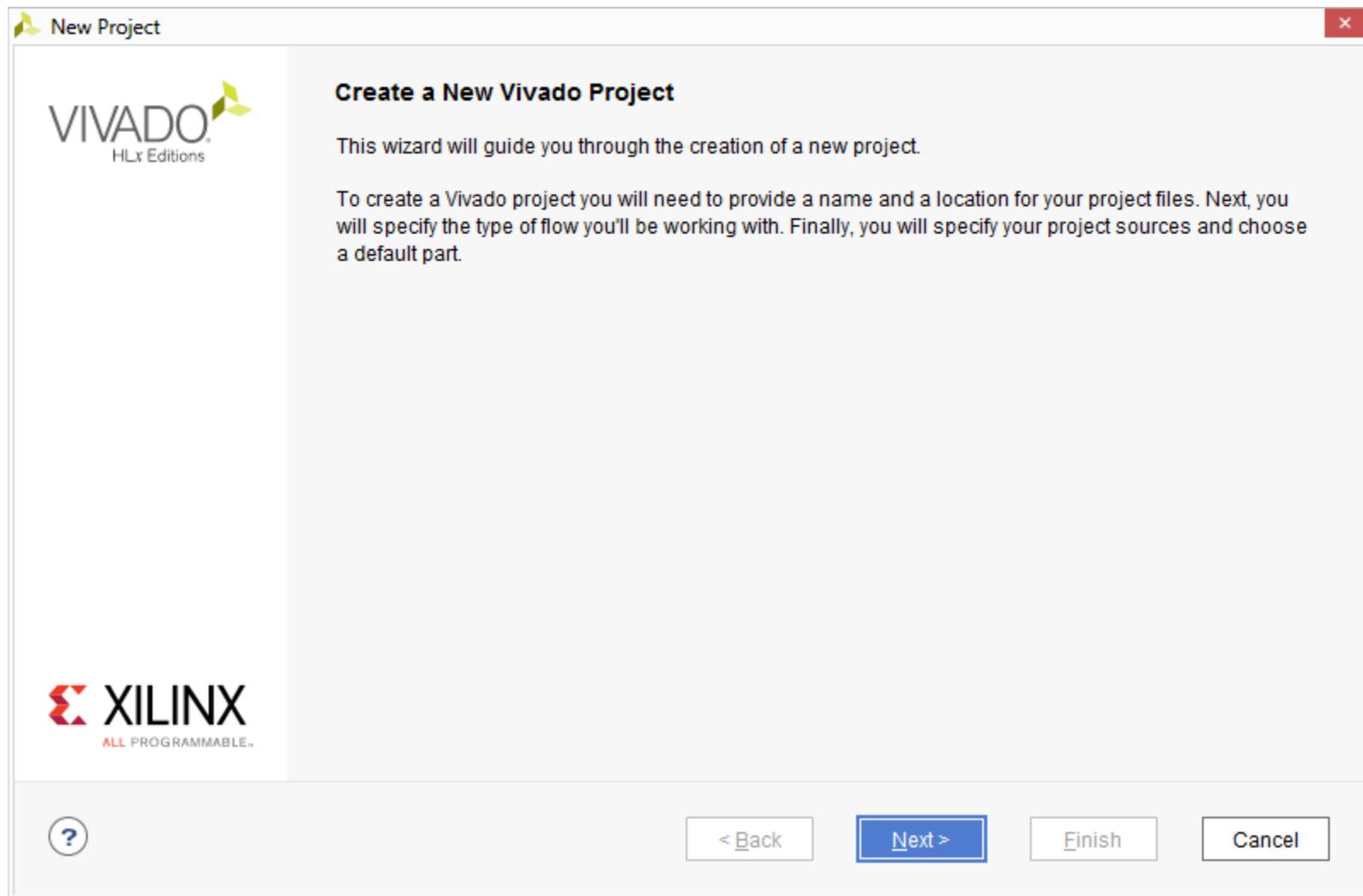
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Note: Presentation applies to the VCU118

**XILINX**

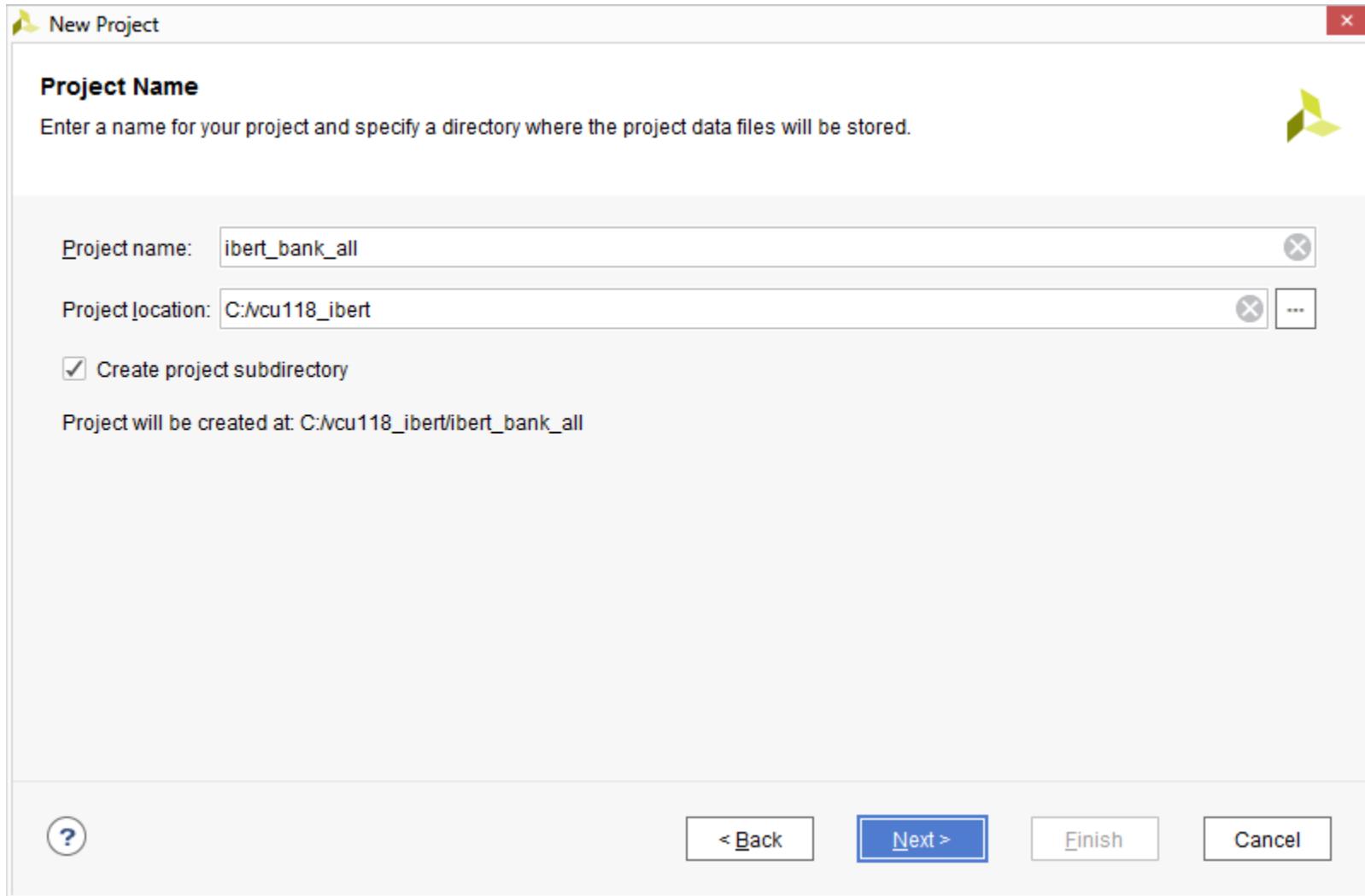
# Create IBERT Design

> Click Next



# Create IBERT Design

- > Set the Project name and location to `ibert_bank_all` and `C:/vcu118_ibert`; check Create project subdirectory



Note: Vivado generally requires forward slashes in paths

# Create IBERT Design

## > Select RTL Project

» Select Do not specify sources at this time

New Project

**Project Type**  
Specify the type of project to create.

RTL Project  
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.  
 Do not specify sources at this time

Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.  
 Do not specify sources at this time

I/O Planning Project  
Do not specify design sources. You will be able to view part/package resources.

Imported Project  
Create a Vivado project from a Synplify, XST or ISE Project File.

Example Project  
Create a new Vivado project from a predefined template.

[?](#)   [< Back](#)   [Next >](#)   [Finish](#)   [Cancel](#)

# Create IBERT Design

- > Under Boards, select the VCU118 Rev 2.0

New Project

**Default Part**  
Choose a default Xilinx part or board for your project. This can be changed later.

Parts | Boards

Reset All Filters

Vendor: All Name: All

Search:

Display Name	Preview	Vendor	File V
Virtex UltraScale+ VCU118 Evaluation Platform		xilinx.com	2.0
Virtex UltraScale+ VCU1525 Acceleration Development Board		xilinx.com	1.1

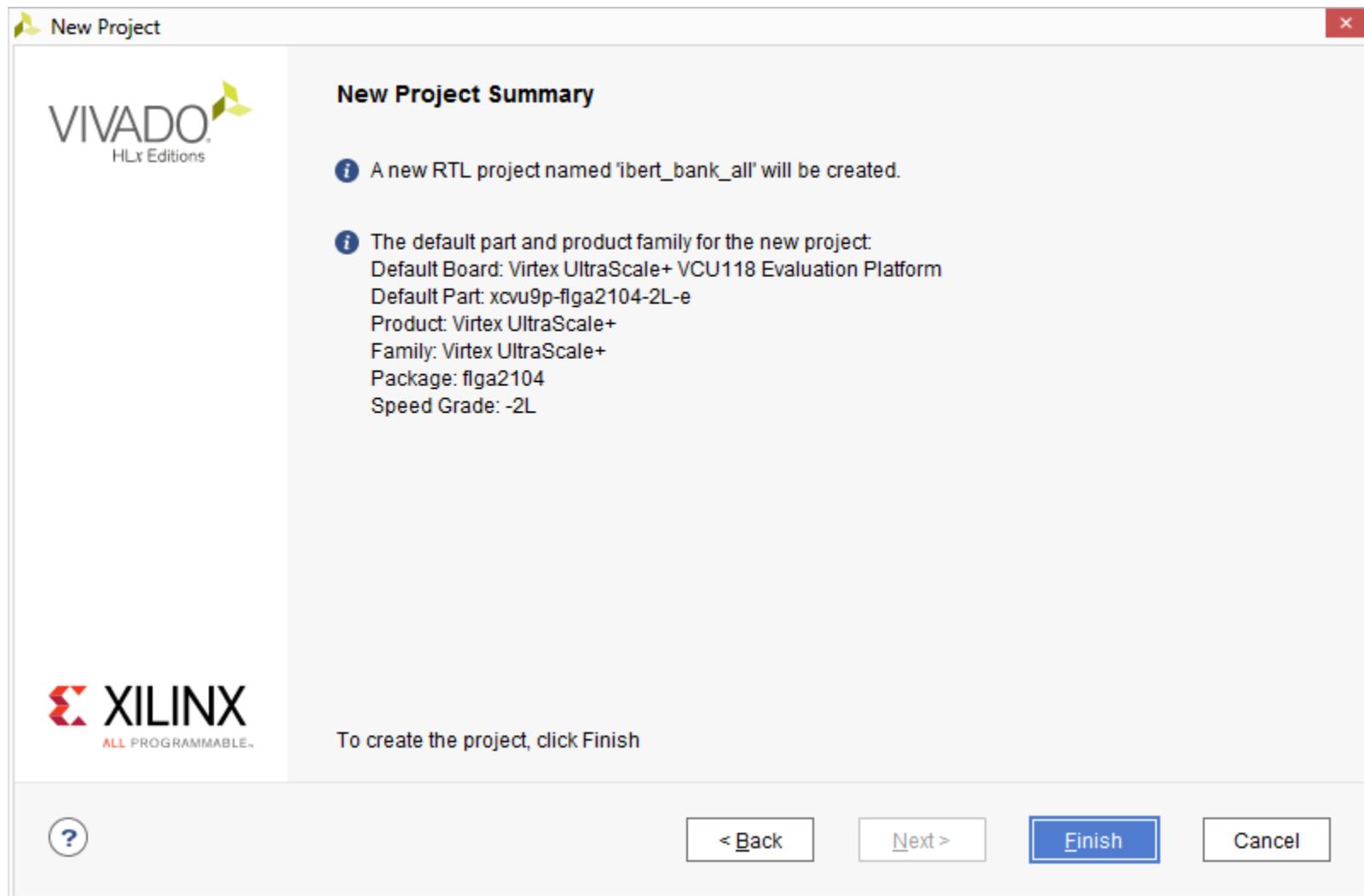
< >

?

< Back Next > Finish Cancel

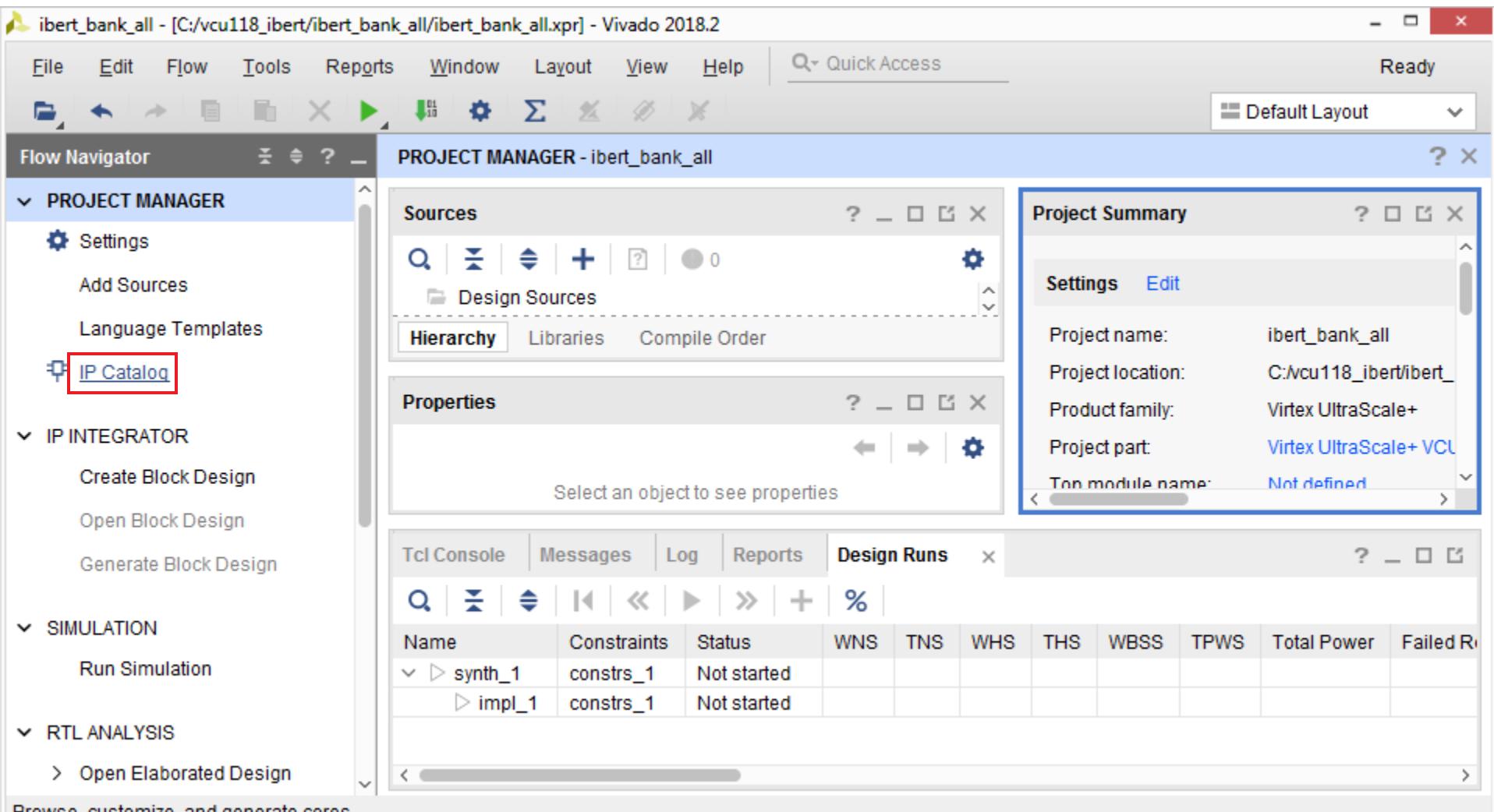
# Create IBERT Design

> Click Finish



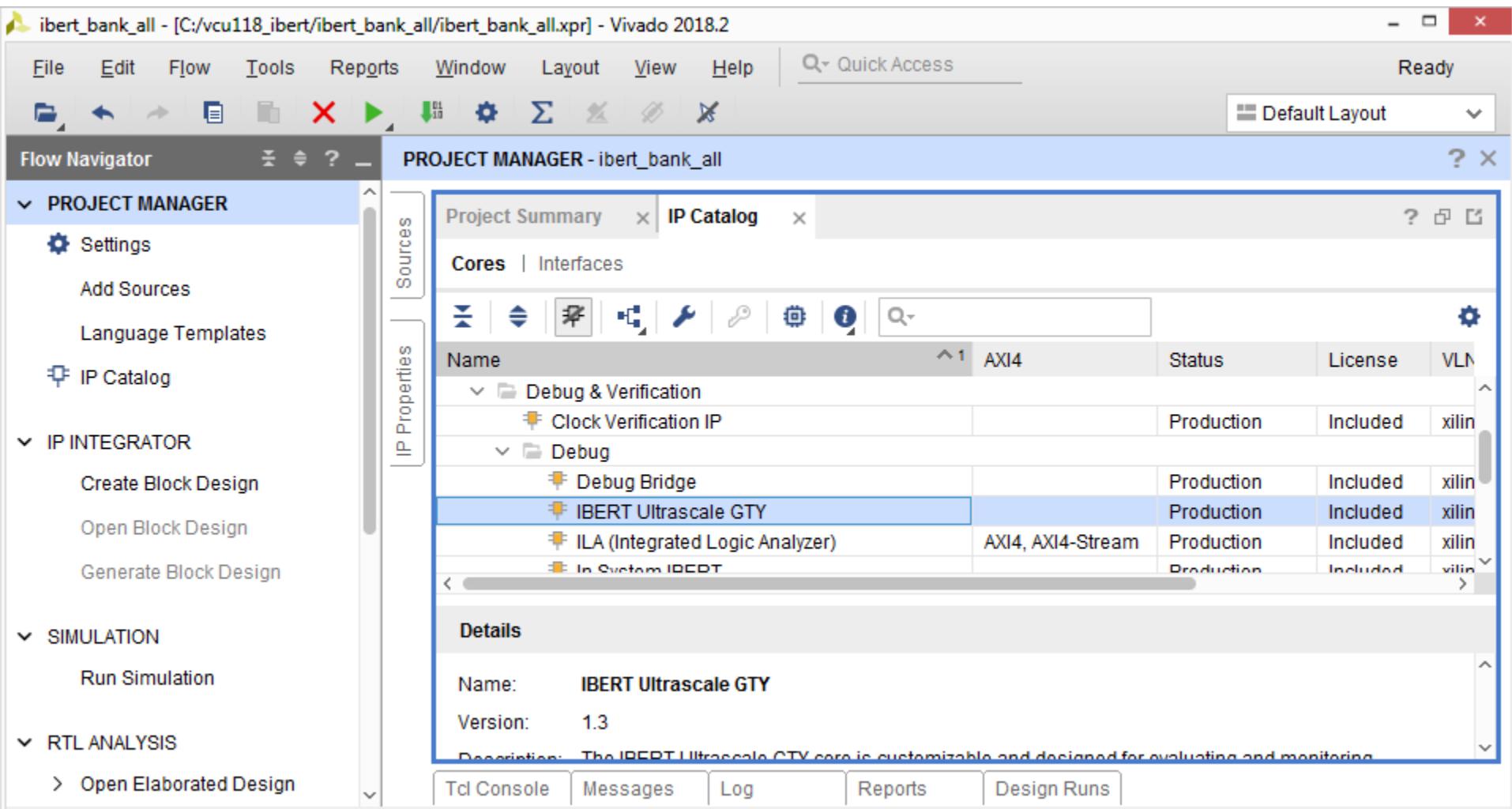
# Create IBERT Design

> Click on IP Catalog



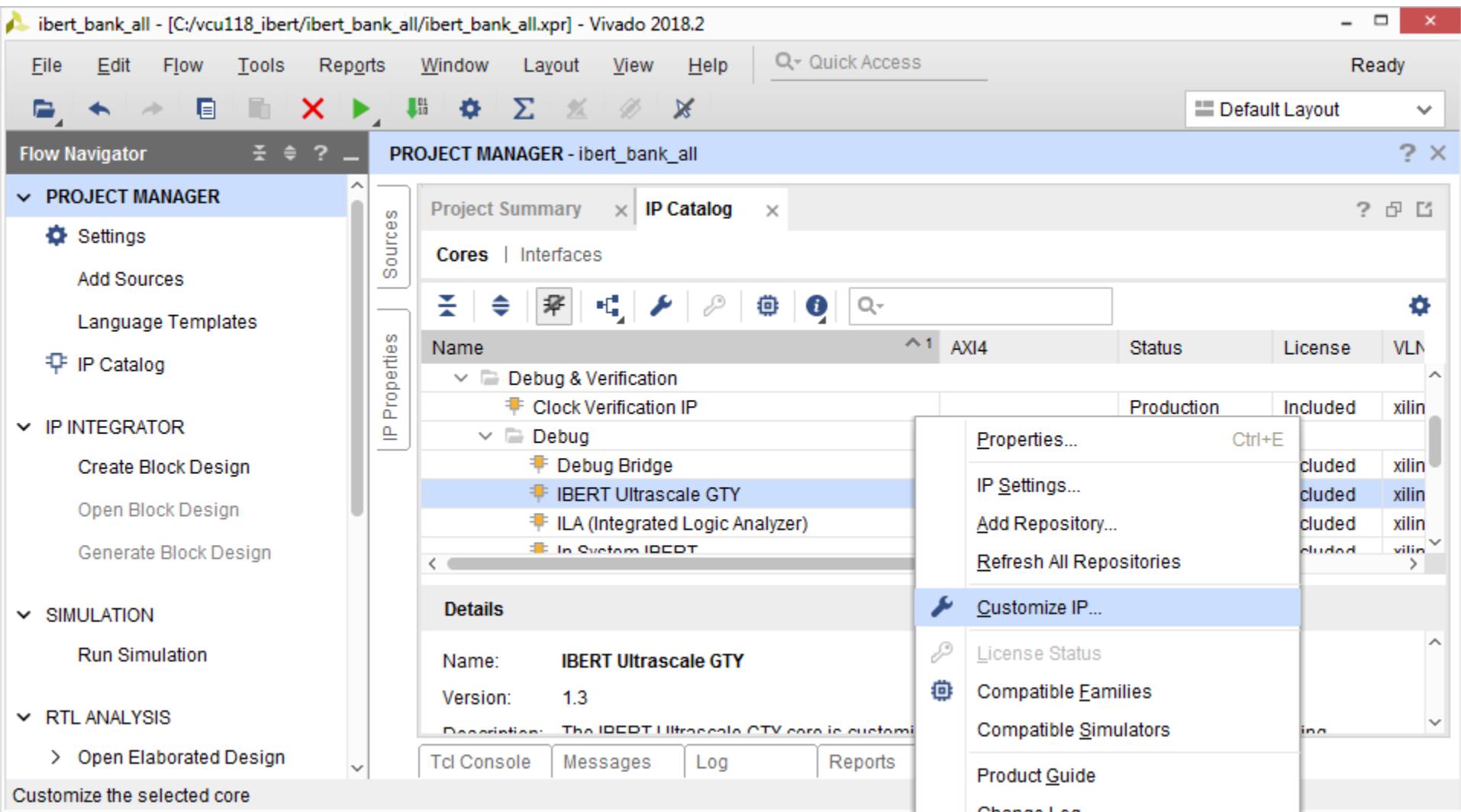
# Create IBERT Design

- > Select IBERT UltraScale GTY, v1.3 under Debug & Verification



# Create IBERT Design

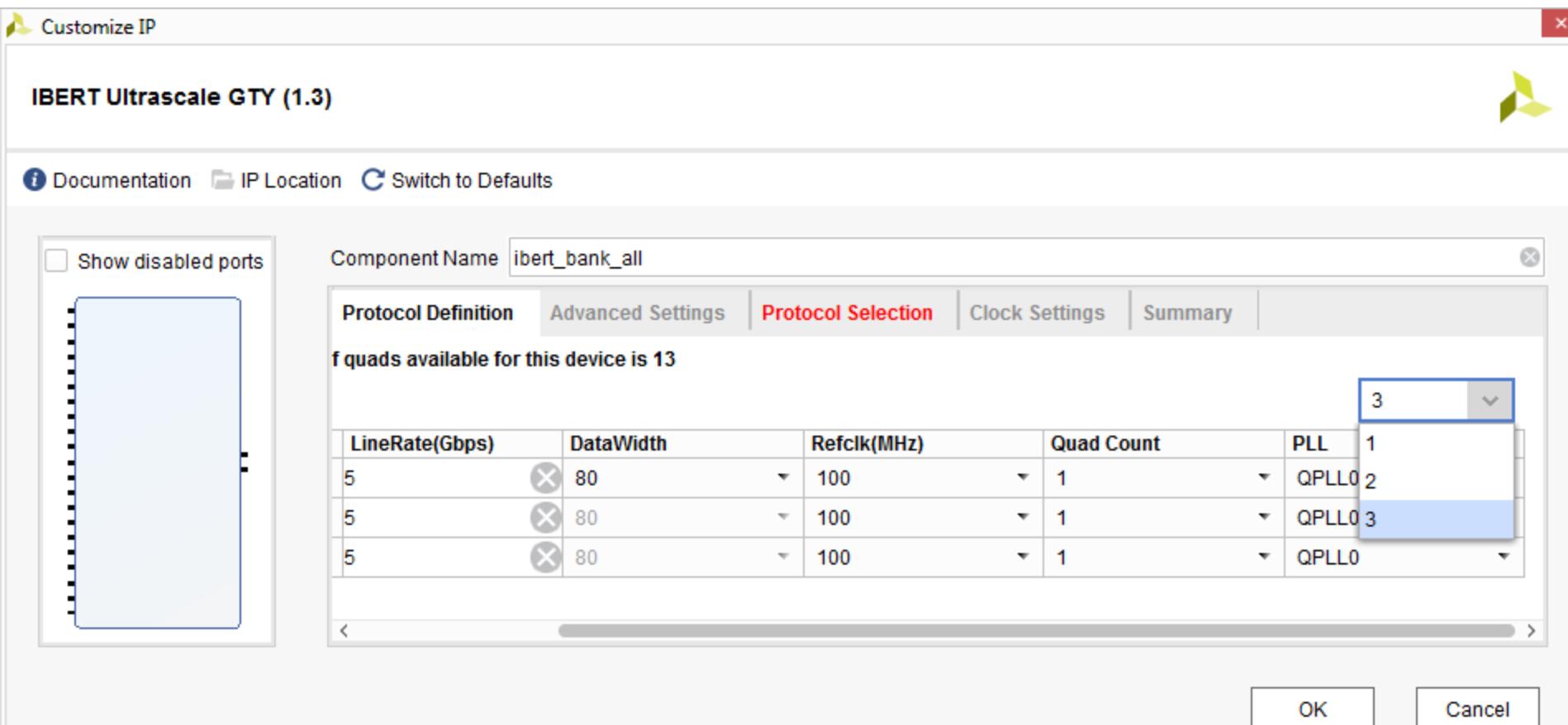
- > Right click on IBERT UltraScale GTY and select Customize IP...



Note: Presentation applies to the VCU118

# Create IBERT Design

- > Set the Component name: `ibert_bank_all`
- > Under the Protocol Definition tab
  - » Select 3 Protocols



# Create IBERT Design

## > Under the Protocol Definition tab

- » Protocol Custom 1: LineRate: **25.000**, Refclk: **156.25** Quad Count: **6**
- » Protocol Custom 2: LineRate: **8.000**, Refclk: **100** Quad Count: **4**
- » Protocol Custom 3: LineRate: **28.125**, Refclk: **156.25** Quad Count: **3**

Customize IP

IBERT Ultrascale GTY (1.3)

Documentation IP Location Switch to Defaults

Show disabled ports

Component Name: ibert\_bank\_all

Protocol Definition Advanced Settings Protocol Selection Clock Settings Summary

The maximum number of quads available for this device is 13

Number of Protocols

Protocol	LineRate(Gbps)	DataWidth	Refclk(MHz)	Quad Count
Custom 1	25.000	80	156.25	6
Custom 2	8.000	80	100	4
Custom 3	28.125	80	156.25	3

OK Cancel

# Create IBERT Design

## > Under the Protocol Selection tab

» Set QUAD\_120 to QUAD\_127 to Custom 1 / 25.000 Gbps

The screenshot shows the 'Customize IP' window for an 'IBERT Ultrascale GTY (1.3)' component. The 'Protocol Selection' tab is active. The table lists seven GTY locations (QUAD\_120 to QUAD\_127, QUAD\_224) and their corresponding protocol settings. QUAD\_120, QUAD\_121, QUAD\_122, QUAD\_125, QUAD\_126, and QUAD\_127 are all set to 'Custom 1 / 25.000 Gbps'. QUAD\_127 is highlighted with a blue border. QUAD\_224 is set to 'None'. The 'Refclk Selection' column shows 'MGTREFCLK0 120' through 'MGTREFCLK0 127' respectively.

GTY Location	Protocol Selected	Refclk Selection
QUAD_120	Custom 1 / 25.000 Gbps	MGTREFCLK0 120
QUAD_121	Custom 1 / 25.000 Gbps	MGTREFCLK0 121
QUAD_122	Custom 1 / 25.000 Gbps	MGTREFCLK0 122
QUAD_125	Custom 1 / 25.000 Gbps	MGTREFCLK0 125
QUAD_126	Custom 1 / 25.000 Gbps	MGTREFCLK0 126
QUAD_127	Custom 1 / 25.000 Gbps	MGTREFCLK0 127
QUAD_224	None	None

# Create IBERT Design

## > Under the Protocol Selection tab

- » Set QUAD\_224 to QUAD\_227 to Custom 2 / 8.000 Gbps, and MGTREFCLK0 225
- » Set QUAD\_231 to QUAD\_233 to Custom 3 / 28.125 Gbps

Customize IP

IBERT Ultrascale GTY (1.3)

Documentation IP Location Switch to Defaults

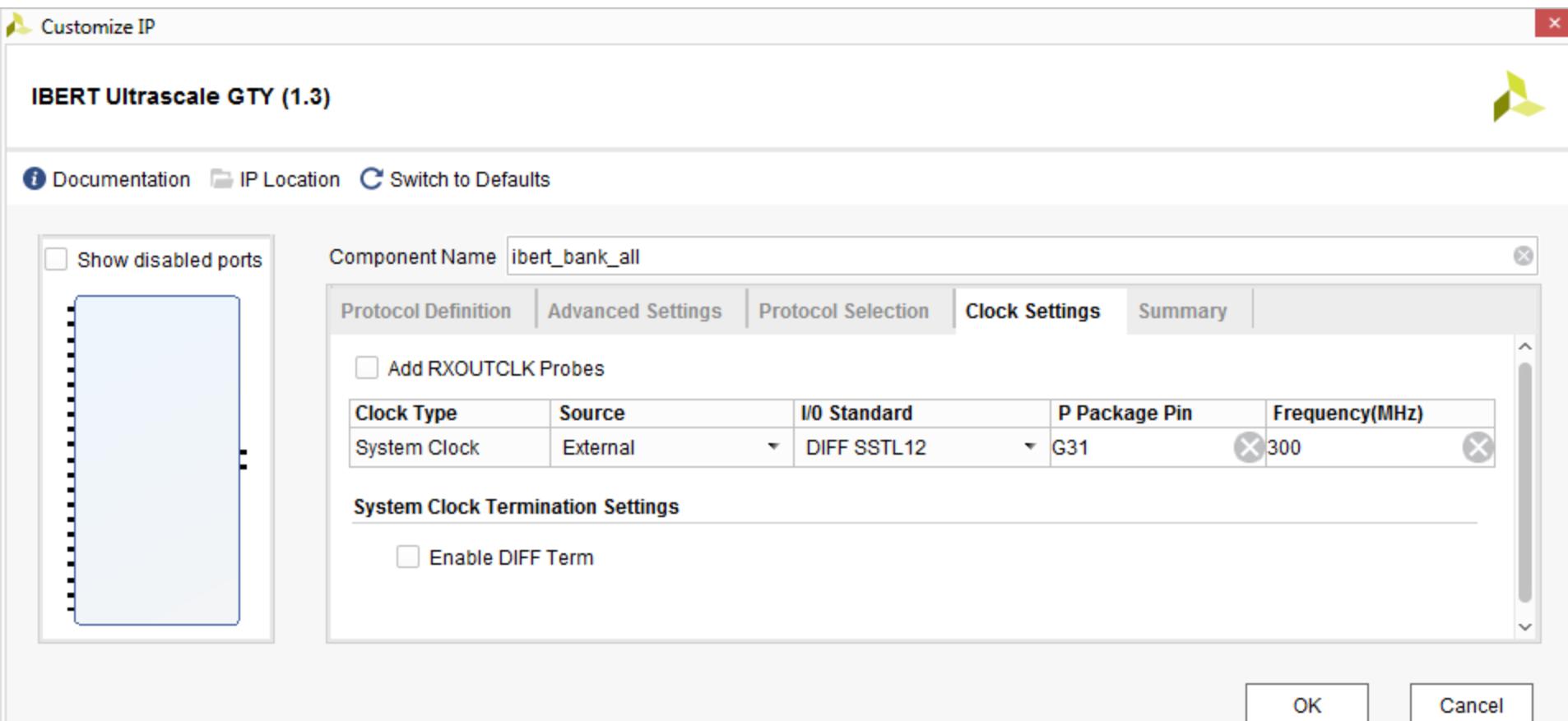
Show disabled ports Component Name: ibert\_bank\_all

Protocol Definition	Advanced Settings	Protocol Selection	Clock Settings	Summary
QUAD_224	Custom 2 / 8.000 Gbps	MGTREFCLK0 225		
QUAD_225	Custom 2 / 8.000 Gbps	MGTREFCLK0 225		
QUAD_226	Custom 2 / 8.000 Gbps	MGTREFCLK0 225		
QUAD_227	Custom 2 / 8.000 Gbps	MGTREFCLK0 225		
QUAD_231	Custom 3 / 28.125 Gbps	MGTREFCLK0 231		
QUAD_232	Custom 3 / 28.125 Gbps	MGTREFCLK0 232		
QUAD_233	Custom 3 / 28.125 Gbps	MGTREFCLK0 233		

OK Cancel

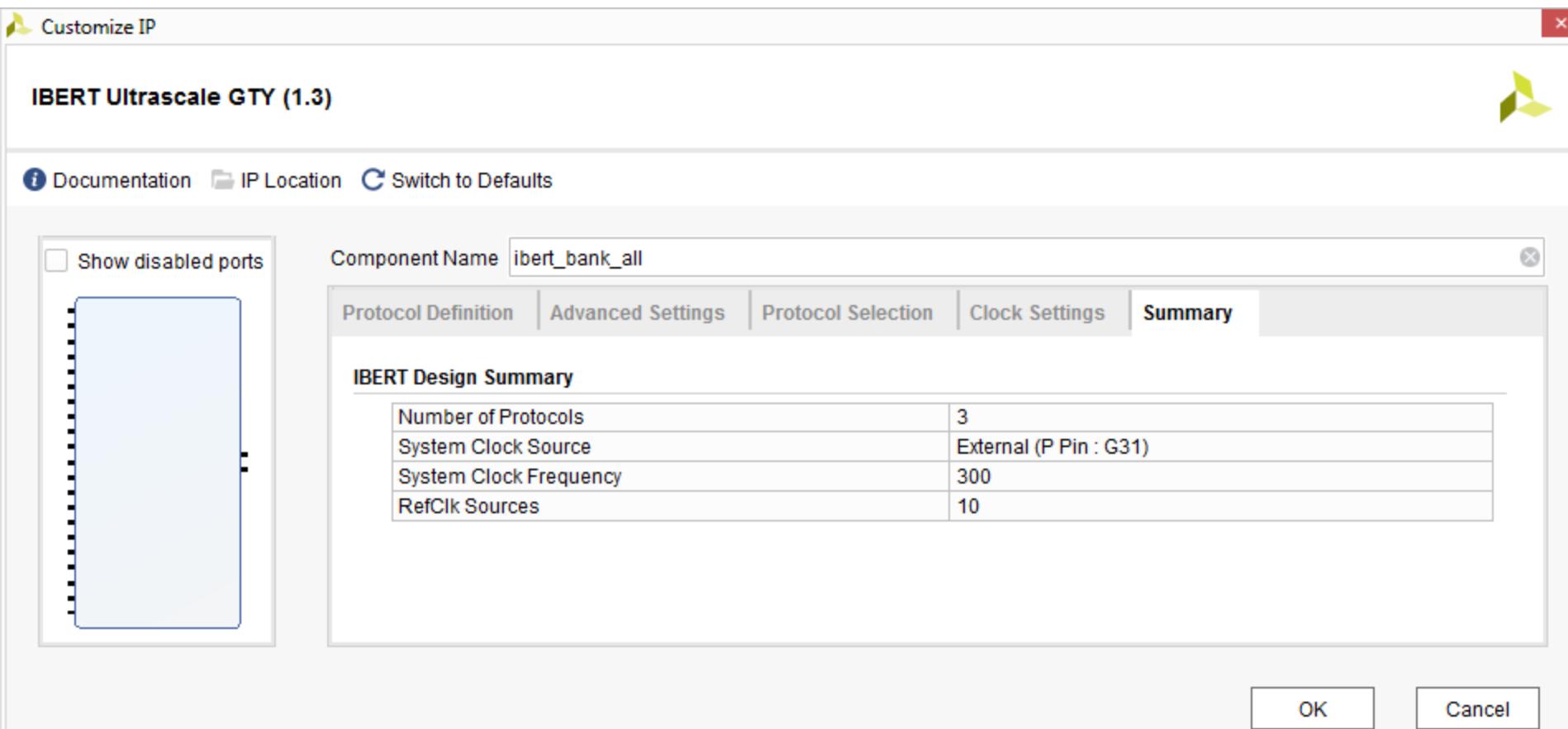
# Create IBERT Design

- > Under the Clock Settings tab, set the System Clock:
  - » DIFF SSTL12, P Package Pin: G31, Frequency: 300



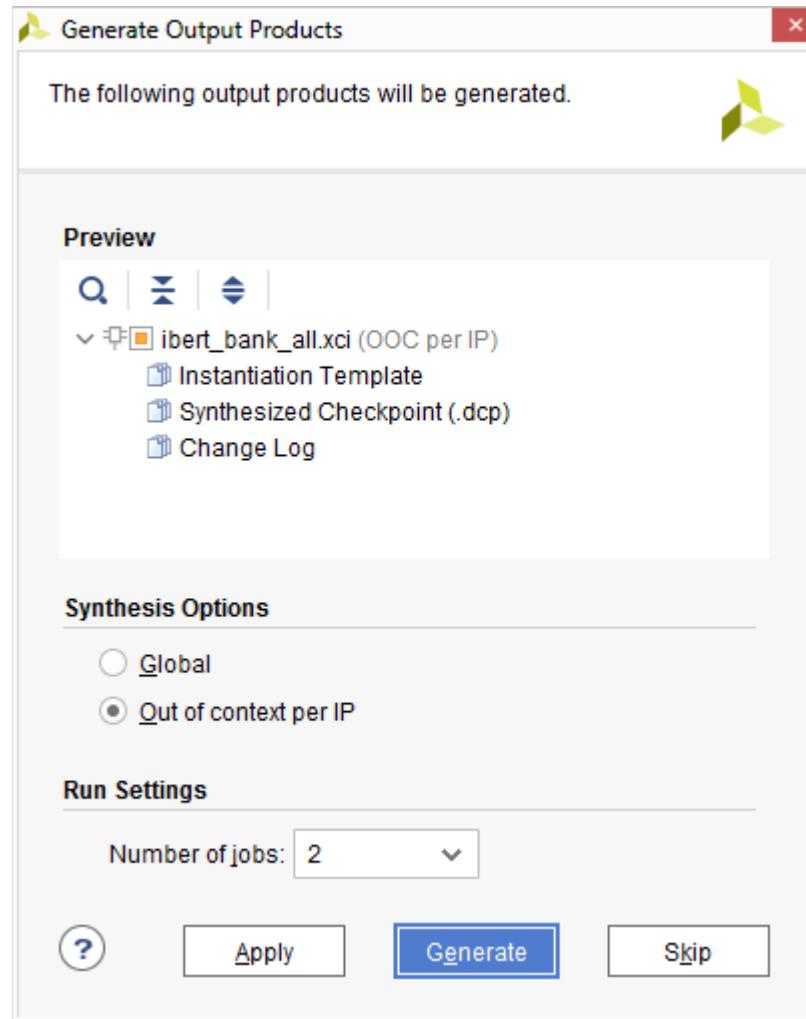
# Create IBERT Design

- > Review the summary and click OK



# Create IBERT Design

## > Click Generate

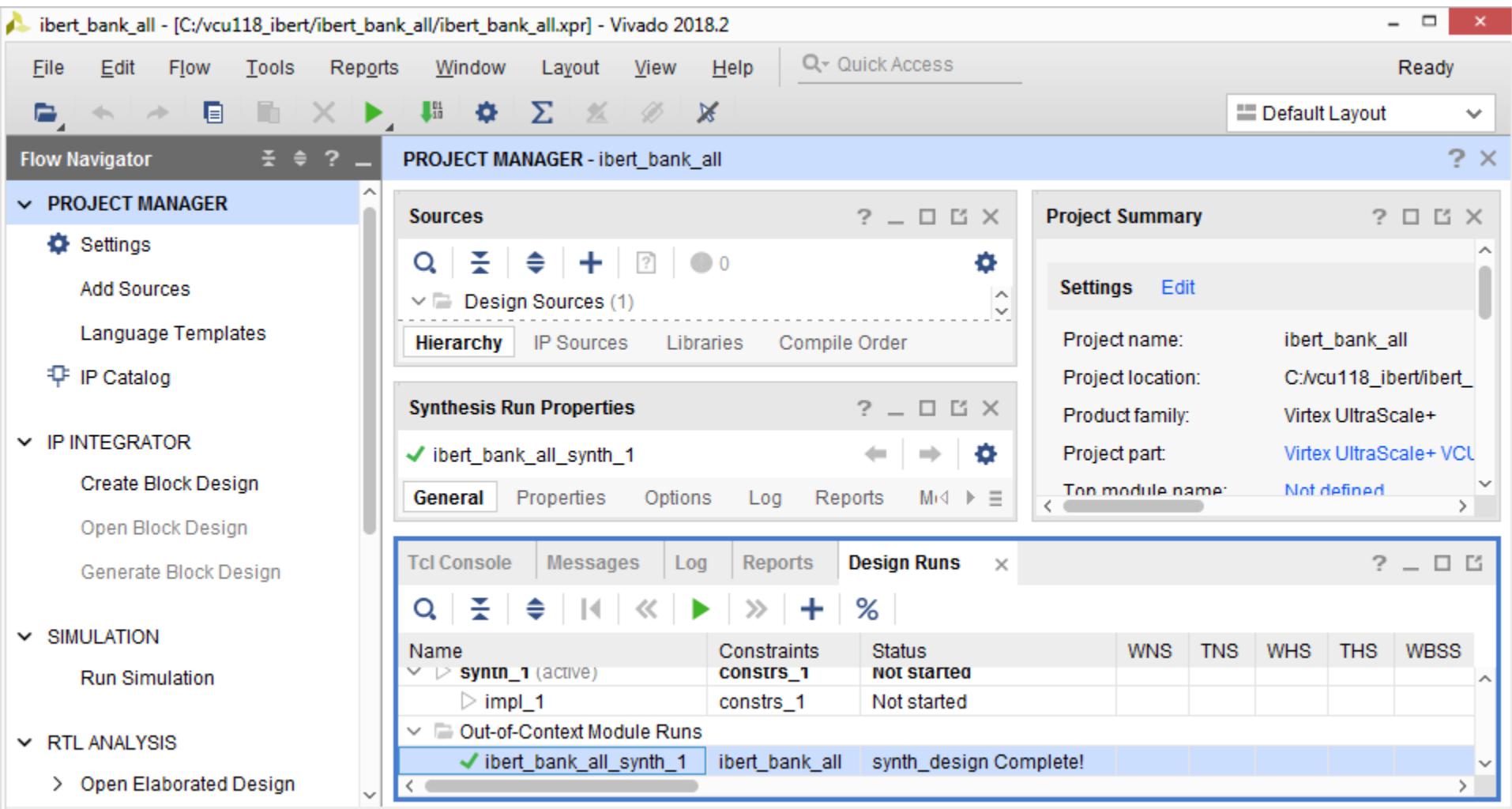


Note: This step will take about 30 minutes

# Create IBERT Design

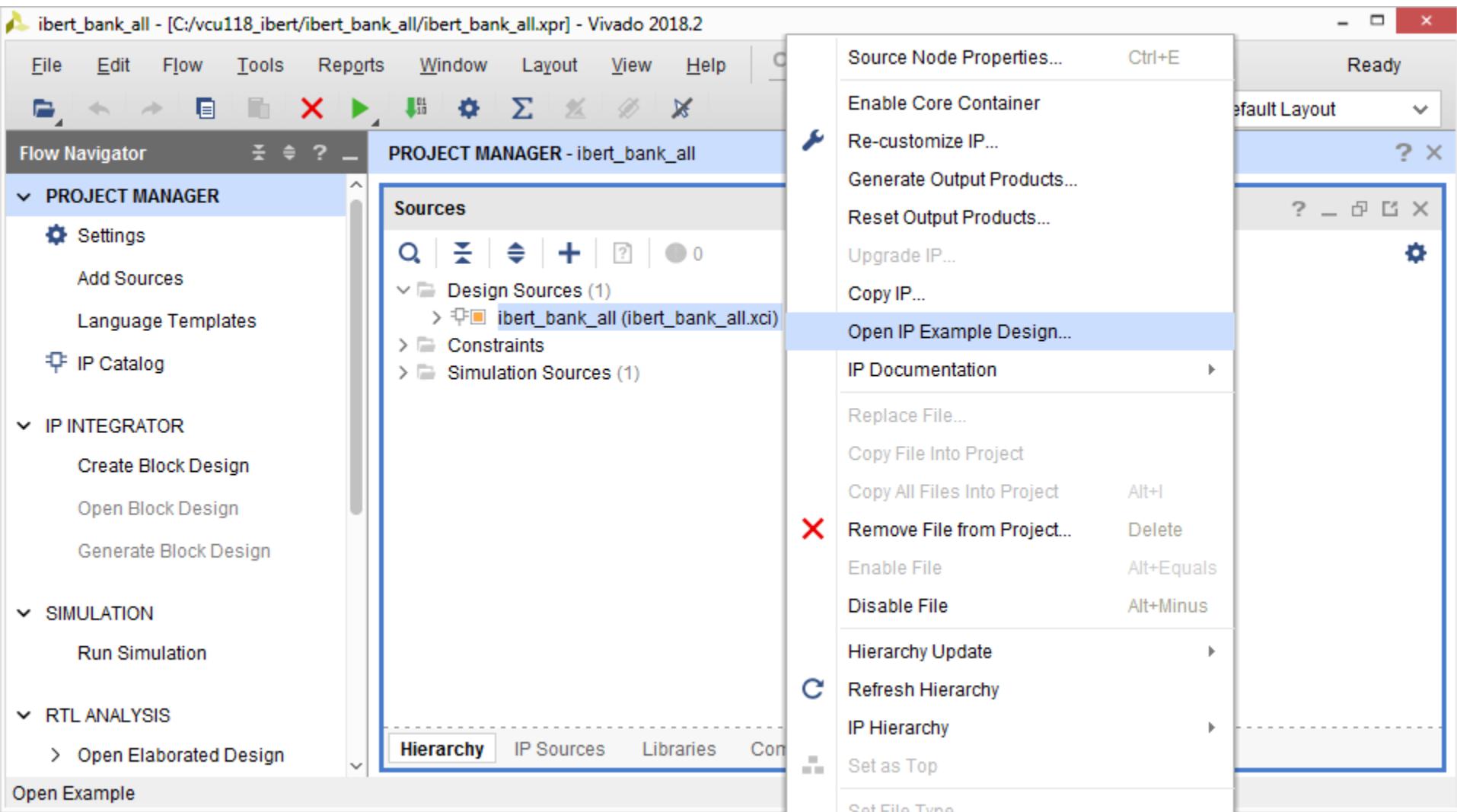
## > The Generated IBERT IP appears in Design Sources

» Wait until checkmark appears on ibert\_bank\_all\_synth\_1



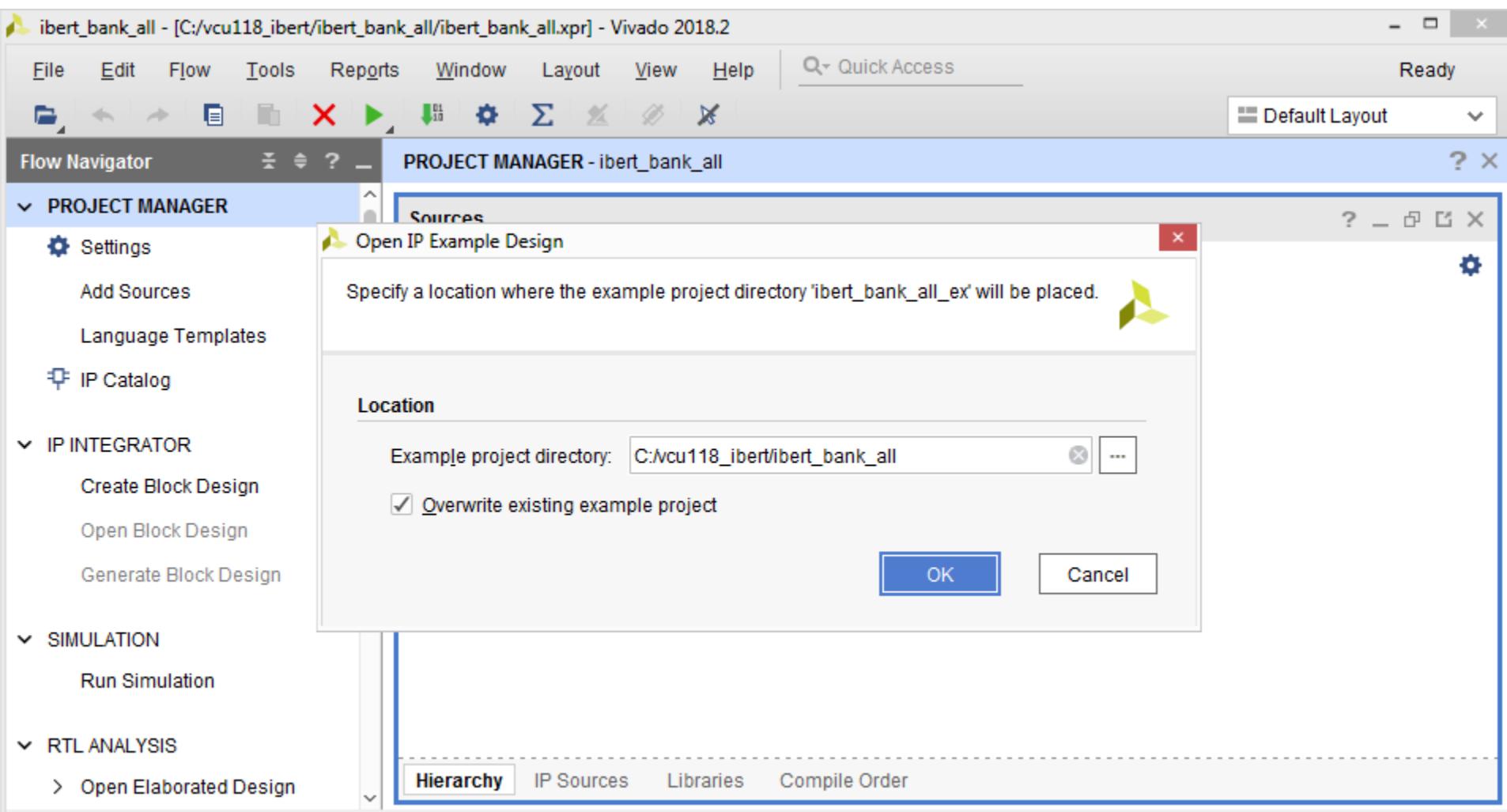
# Compile Example Design

- > Right click on ibert\_bank\_all and select Open IP Example Design...



# Compile Example Design

- > Set the location to C:/vcu118\_ibert/ibert\_bank\_all and click OK



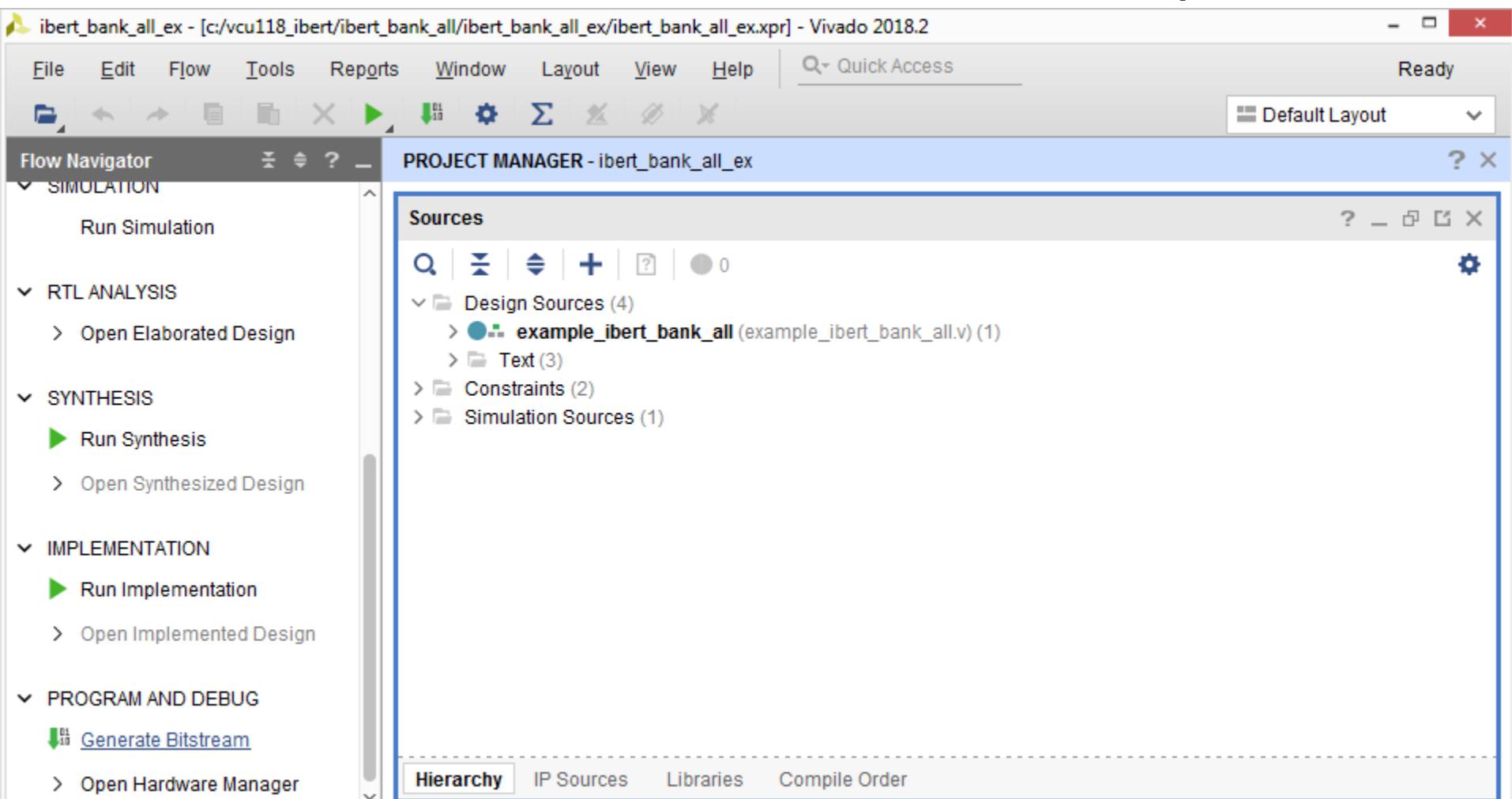
Open Example

Note: Presentation applies to the VCU118

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# Compile Example Design

- > A new project is created under <design path>/
- > Click Generate Bitstream; takes about 100 minutes to compile

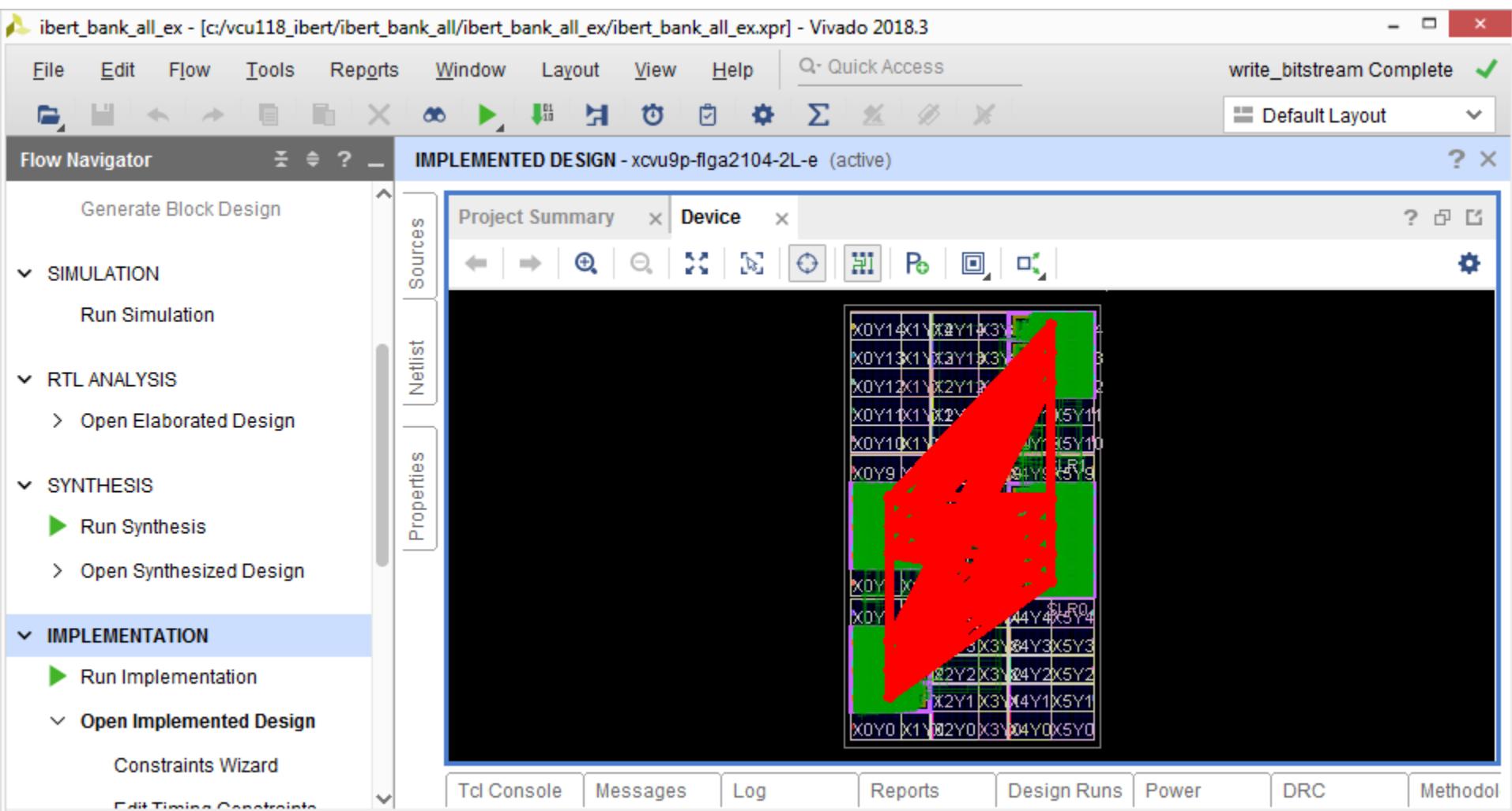


Generate a programming file after implementation

Note: The original project window can be closed

# Compile Example Design

- > Open and view the Implemented Design



# References



# References

## > IBERT IP

- » IBERT for UltraScale GTY Transceivers – PG196
  - [https://www.xilinx.com/support/documentation/ip\\_documentation/ibert\\_ultrascale\\_gty/v1\\_3/pg196-ibert-ultrascale-gty.pdf](https://www.xilinx.com/support/documentation/ip_documentation/ibert_ultrascale_gty/v1_3/pg196-ibert-ultrascale-gty.pdf)

## > Vivado Programming and Debugging

- » Vivado Design Suite Programming and Debugging User Guide – UG908
  - [https://www.xilinx.com/support/documentation/sw\\_manuals/xilinx2019\\_1/ug908-vivado-programming-debugging.pdf](https://www.xilinx.com/support/documentation/sw_manuals/xilinx2019_1/ug908-vivado-programming-debugging.pdf)

# Documentation



# Documentation

- > **Virtex UltraScale+**
  - » Virtex UltraScale+ FPGA Family
    - <https://www.xilinx.com/products/silicon-devices/fpga/virtex-ultrascale-plus.html>
- > **VCU118 Documentation**
  - » Virtex UltraScale+ FPGA VCU118 Evaluation Kit
    - <https://www.xilinx.com/products/boards-and-kits/vcu118.html>
  - » VCU118 Board User Guide – UG1224
    - [https://www.xilinx.com/support/documentation/boards\\_and\\_kits/vcu118/ug1224-vcu118-eval-bd.pdf](https://www.xilinx.com/support/documentation/boards_and_kits/vcu118/ug1224-vcu118-eval-bd.pdf)
  - » VCU118 Evaluation Kit Quick Start Guide User Guide – XTP453
    - [https://www.xilinx.com/support/documentation/boards\\_and\\_kits/vcu118/xtp453-vcu118-quickstart.pdf](https://www.xilinx.com/support/documentation/boards_and_kits/vcu118/xtp453-vcu118-quickstart.pdf)
  - » VCU118 - Known Issues and Release Notes Master Answer Record
    - <https://www.xilinx.com/support/answers/68268.html>