

VCU118 Restoring Flash Contents

May 2019



Revision History

Date	Version	Description
05/29/19	9.0	Updated for 2019.1. Some screenshots not updated.
12/10/18	8.0	Updated for 2018.3. Some screenshots not updated.
06/18/18	7.0	Updated for 2018.2.
04/09/18	6.0	Updated for 2018.1.
12/20/17	5.0	Updated for 2017.4.
10/26/17	4.0	Updated for 2017.3.1. For Rev 2.0, with Production Silicon, and QSPI Flash devices.
06/20/17	3.0	Updated for 2017.2.
04/19/17	2.0	Updated for 2017.1.
01/16/17	1.1	Updated SW16 settings.
12/19/16	1.0	Initial version for 2016.4.

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Overview

- > Xilinx VCU118 Board
- > Software Requirements
- > VCU118 Setup
- > Restoring VCU118 QSPI Flash
- > Run Flash Designs
- > References

VCU118 Restoring Flash Contents Description

> **Description**

- » Vivado is used to restore the onboard non-volatile memories with the contents used in the [VCU118 Quick Start Guide](#) (XTP453) for the QSPI Flash

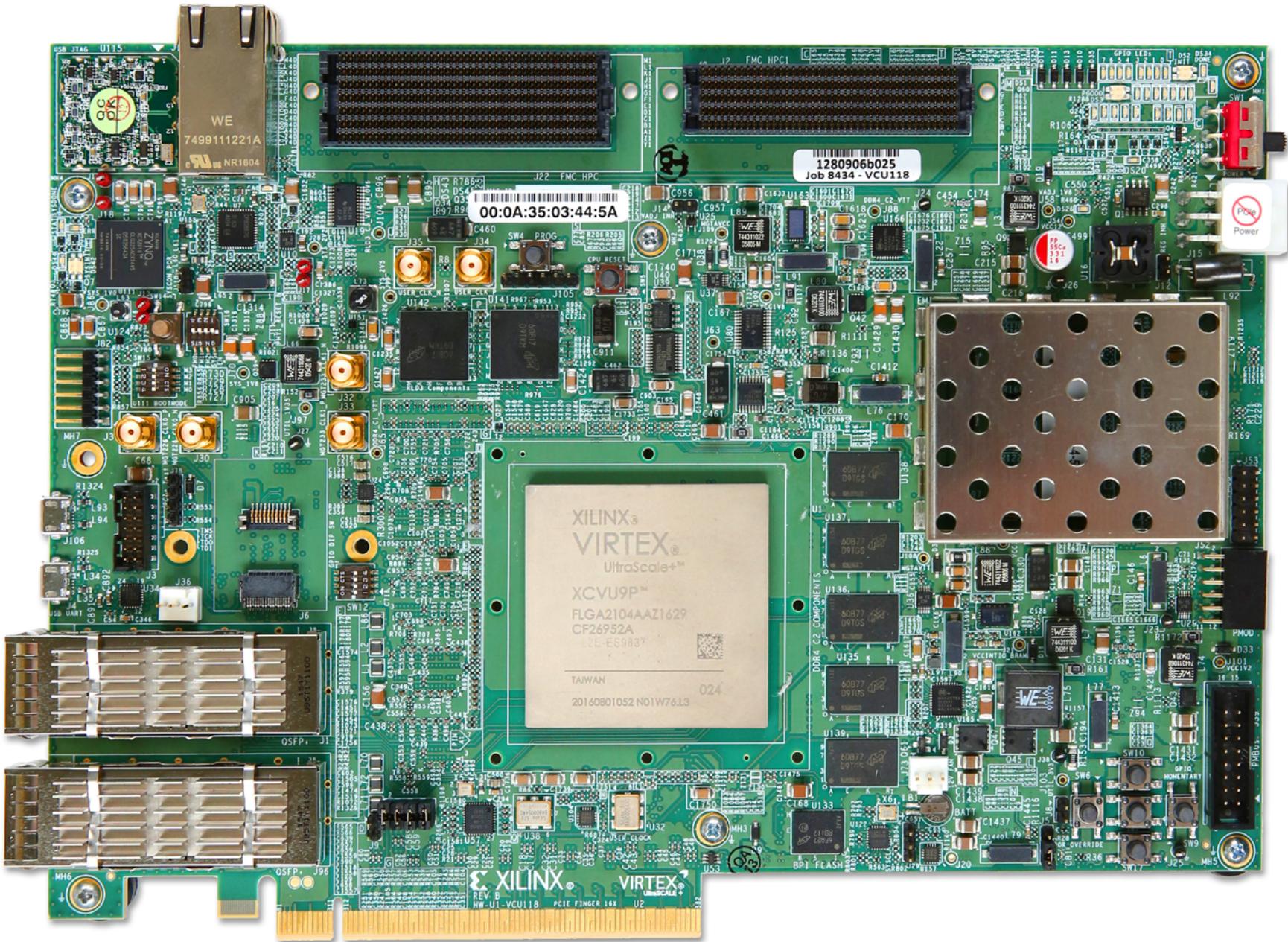
> **Reference Design Source and Applications**

- » BlinkBIST XTP441

> **Files for Flash Restoration**

- » RDF0393 - VCU118 Restoring Flash Design Files (2019.1 C) ZIP file

Xilinx VCU118 Board



VCU118 Software Install and Board Setup

- > Complete setup steps in XTP449 – VCU118 Software Install and Board Setup:
 - » Software Requirements
 - » VCU118 Board Setup

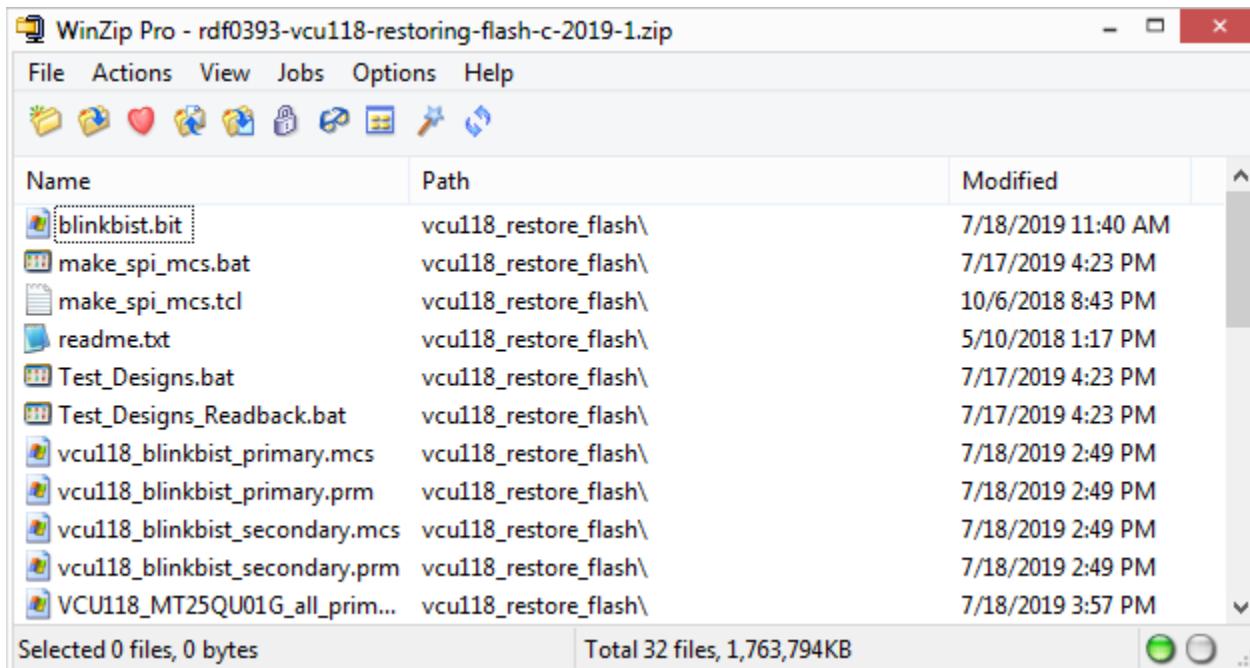


Restoring VCU118 QSPI Flash



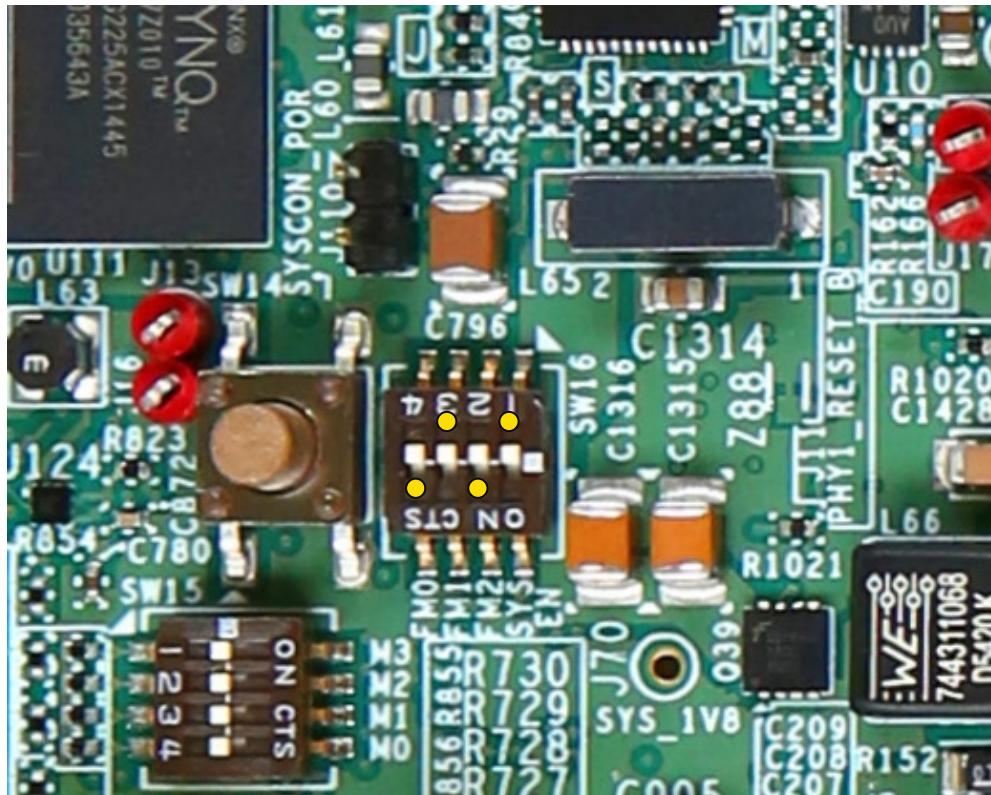
Restoring VCU118 QSPI Flash

- > Unzip the RDF0393 - VCU118 Restoring Flash Design Files (2019.1 C) ZIP file to your C:\ drive
 - » Available through <http://www.xilinx.com/vcu118>



Restoring VCU118 QSPI Flash

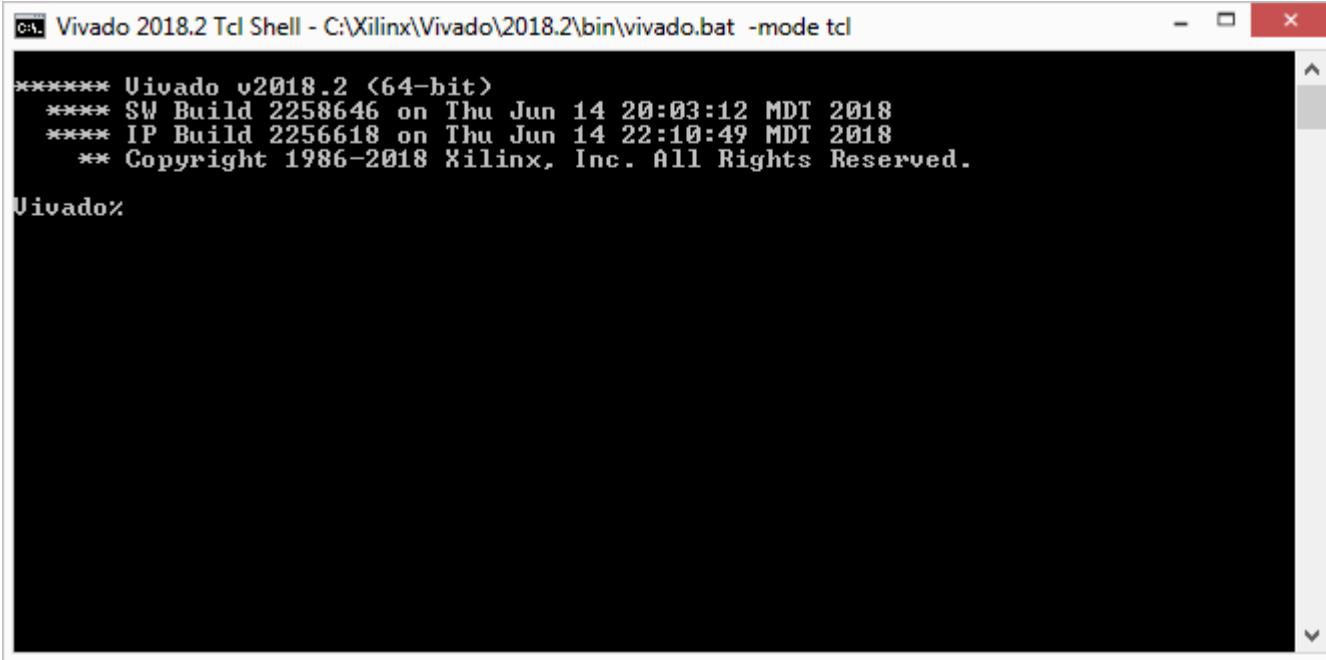
- > Set JTAG mode ($M[2:0] = 101$) to program QSPI Flash
- > Disable System Controller booting (Position 1 off)
- > Set SW16 to 0101 (1 = on, Position 1 \rightarrow Position 4)



Restoring VCU118 QSPI Flash

> Open a Vivado Tcl Shell:

Start → All Programs → Xilinx Design Tools → Vivado 2019.1 →
Vivado 2019.1 Tcl Shell



Vivado 2018.2 Tcl Shell - C:\Xilinx\Vivado\2018.2\bin\vivado.bat -mode tcl

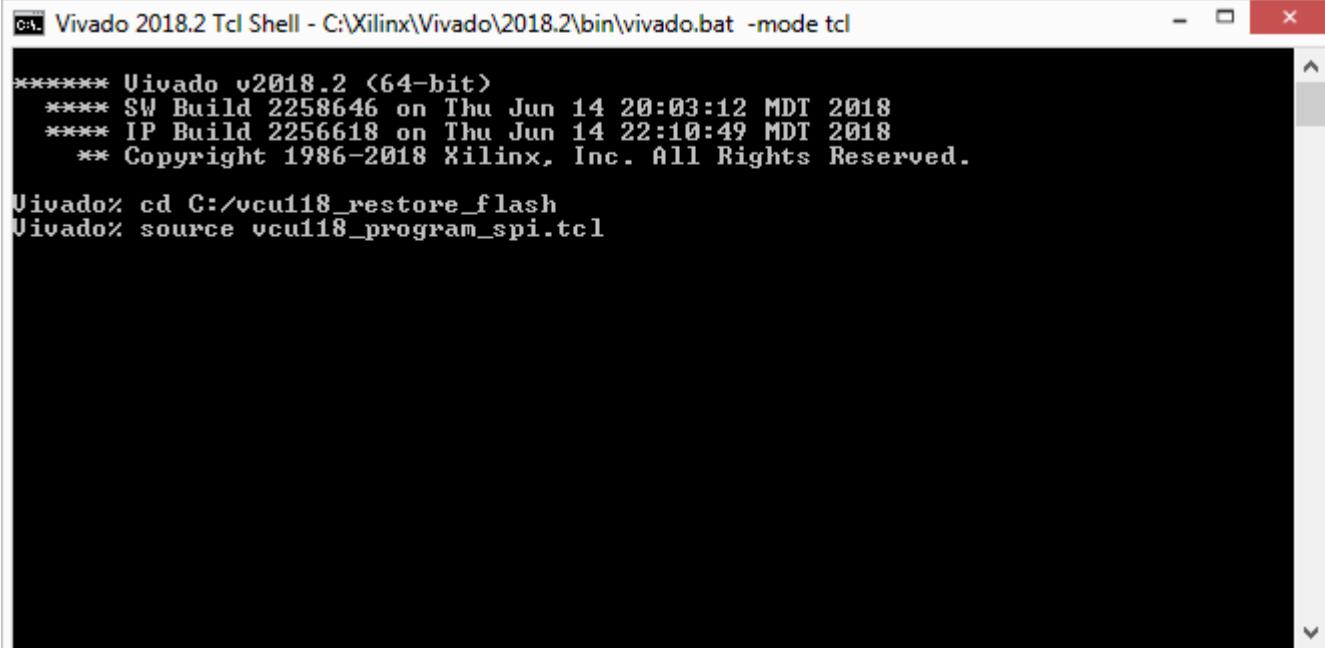
```
***** Vivado v2018.2 (64-bit)
***** SW Build 2258646 on Thu Jun 14 20:03:12 MDT 2018
***** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.
```

Vivado>

Restoring VCU118 QSPI Flash

- > In the Vivado Tcl Shell type:

```
cd C:/vcu118_restore_flash  
source vcu118_program_spi.tcl
```



```
C:\> Vivado 2018.2 Tcl Shell - C:\Xilinx\Vivado\2018.2\bin\vivado.bat -mode tcl  
***** Vivado v2018.2 (64-bit)  
**** SW Build 2258646 on Thu Jun 14 20:03:12 MDT 2018  
**** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018  
** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.  
  
Vivado> cd C:/vcu118_restore_flash  
Vivado> source vcu118_program_spi.tcl
```

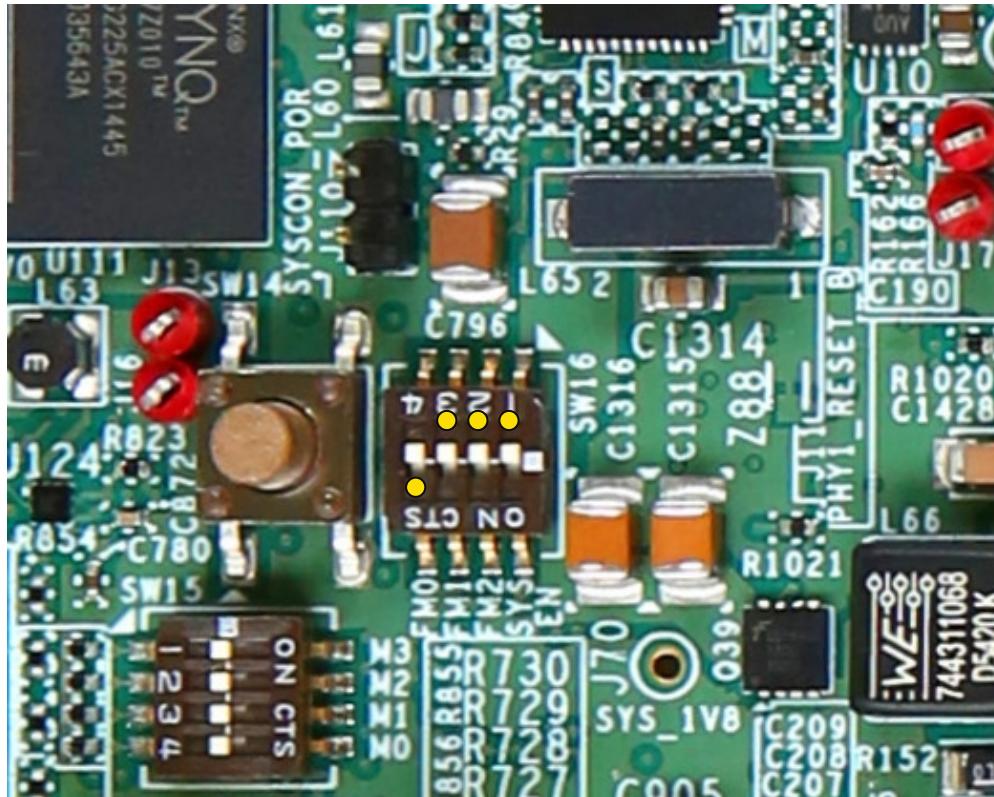
Restoring VCU118 QSPI Flash

- > Operation complete, QSPI Flash programmed

```
C:\ Vivado 2018.2 Tcl Shell - C:\Xilinx\Vivado\2018.2\bin\vivado.bat -mode tcl
# program_hw_cfgmem -hw_cfgmem [get_property PROGRAM.HW_CFGMEM [lindex [get_hw_devices] 0 ]]
Performing operation on qspi device 0
Mfg ID : 20  Memory Type : bb  Memory Capacity : 21  Device ID 1 : 0  Device ID 2 : 0
Performing Erase Operation...
Erase Operation successful.
Performing Program and Verify Operations...
Program/Verify Operation successful.
Performing operation on qspi device 1
Mfg ID : 20  Memory Type : bb  Memory Capacity : 21  Device ID 1 : 0  Device ID 2 : 0
Performing Erase Operation...
Erase Operation successful.
Performing Program and Verify Operations...
Program/Verify Operation successful.
INFO: [Labtoolstcl 44-377] Flash programming completed successfully
program_hw_cfgmem: Time <s>: cpu = 00:00:11 ; elapsed = 00:16:07 . Memory <MB>:
peak = 1043.230 ; gain = 65.563
# close_hw_target [current_hw_target [get_hw_targets */xilinx_tcf/Digilent/*]]
INFO: [Labtoolstcl 44-464] Closing hw_target localhost:3121/xilinx_tcf/Digilent/
210308A5F09C
# disconnect_hw_server localhost:3121
# close_hw
Vivado%
```

Run Flash designs

- > Set QSPI mode ($M[2:0] = 001$) to load FPGA from Flash
- > Disable System Controller booting (Position 1 off)
- > Set SW16 to 0001 (1 = on, Position 1 → Position 4)



Run Flash designs – BIST

- > Cycle board power
- > As per [XTP453](#):



STEP 3: Run the Built-In Self-Test

The BIST consists of a set of pass/fail tests. On power-up, the Clock, DDR, BRAM, flash memory, and I2C tests are run without user input.

A passing test is indicated when the corresponding GPIO LED for each test is ON. See the following table for the LED that corresponds to each test.

The DIP and pushbutton (PB) tests require user interaction as described in the following section. The blinking LED indicates which test is waiting for user input.

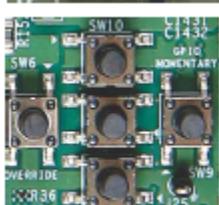
Board Self-Test Assignments for GPIO LEDs

GPIO LEDs							
7	6	5	4	3	2	1	0
Clock	DDR	BRAM	Flash	I2C	DIP	PB	NA



SW12 is the GPIO DIP switch. To complete the test, push all four switches to the ON position.

A passing test is indicated when GPIO LED 2 is ON.



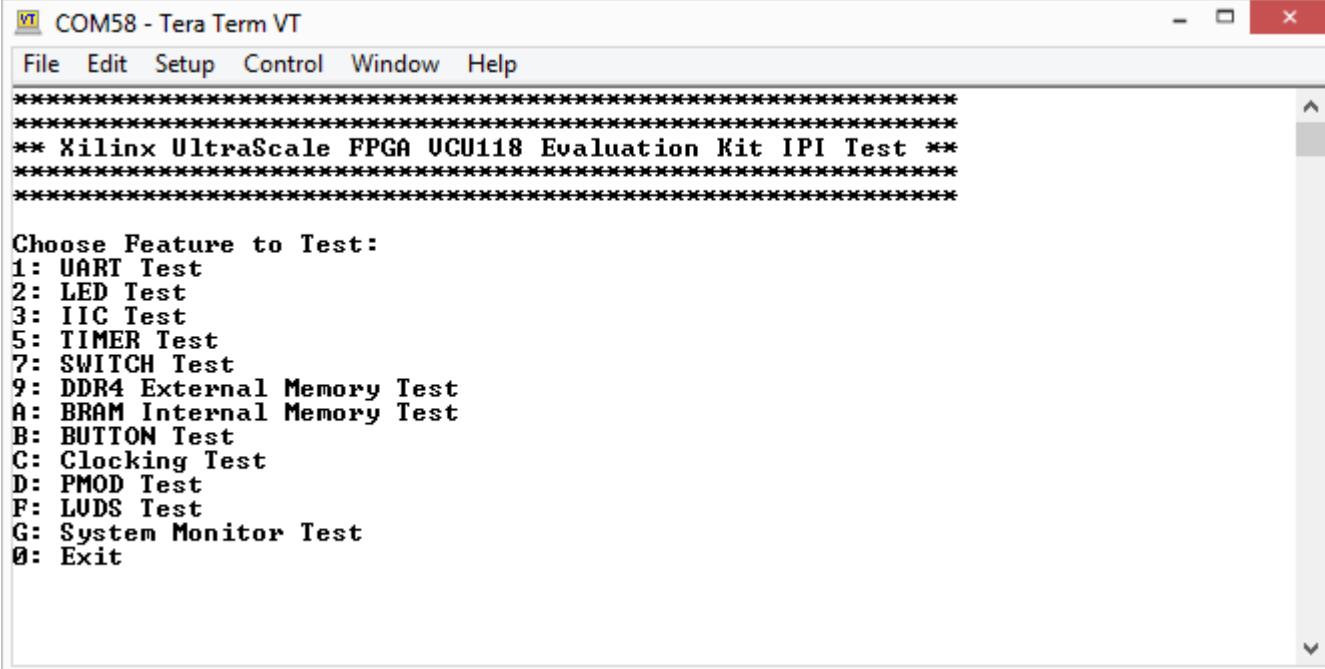
The PB test checks pushbutton operation.

To complete the test, push the N, W, S, and E pushbuttons in any order. Then push the center pushbutton.

A passing test is indicated when GPIO LED 1 is ON.

Run Flash designs – BIST

- > After BIST completes, the IPI Application runs in the terminal window



COM58 - Tera Term VT

File Edit Setup Control Window Help

```
*****
** Xilinx UltraScale FPGA VCU118 Evaluation Kit IPI Test **
*****
```

Choose Feature to Test:

- 1: UART Test
- 2: LED Test
- 3: IIC Test
- 5: TIMER Test
- 7: SWITCH Test
- 9: DDR4 External Memory Test
- A: BRAM Internal Memory Test
- B: BUTTON Test
- C: Clocking Test
- D: PMOD Test
- F: LVDS Test
- G: System Monitor Test
- 0: Exit

References



References

- > **UltraScale Configuration**
 - » UltraScale Architecture Configuration User Guide – UG570
 - https://www.xilinx.com/support/documentation/user_guides/ug570-ultrascale-configuration.pdf

Documentation



Documentation

> Virtex UltraScale+

- » Virtex UltraScale+ FPGA Family
 - <https://www.xilinx.com/products/silicon-devices/fpga/virtex-ultrascale-plus.html>

> VCU118 Documentation

- » Virtex UltraScale+ FPGA VCU118 Evaluation Kit
 - <https://www.xilinx.com/products/boards-and-kits/vcu118.html>
- » VCU118 Board User Guide – UG1224
 - https://www.xilinx.com/support/documentation/boards_and_kits/vcu118/ug1224-vcu118-eval-bd.pdf
- » VCU118 Evaluation Kit Quick Start Guide User Guide – XTP453
 - https://www.xilinx.com/support/documentation/boards_and_kits/vcu118/xtp453-vcu118-quickstart.pdf
- » VCU118 - Known Issues and Release Notes Master Answer Record
 - <https://www.xilinx.com/support/answers/68268.html>