

VCU118 IP Integrator Application

May 2019



Revision History

Date	Version	Description
05/29/19	9.0	Updated for 2019.1. Some screenshots not updated.
12/10/18	8.0	Updated for 2018.3. Some screenshots not updated.
06/18/18	7.0	Updated for 2018.2.
04/09/18	6.0	Updated for 2018.1.
12/20/17	5.0	Updated for 2017.4.
10/26/17	4.0	Updated for 2017.3.1. For Rev 2.0, with Production Silicon, and QSPI Flash devices.
06/20/17	3.0	Updated for 2017.2.
04/19/17	2.0	Updated for 2017.1.
12/19/16	1.0	Initial version for 2016.4.

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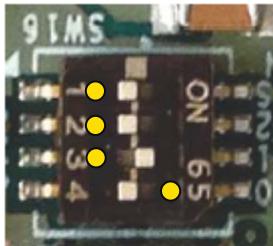
Overview

- > Xilinx VCU118 Board
- > Software Requirements
- > VCU118 Setup
- > VCU118 IPI Design
- > Compile VCU118 IPI Design
- > Program VCU118 with IPI Design
- > References

VCU118 Board Self Test Demo

> Follow the instructions in the VCU118 Quick Start Guide, XTP453

- » http://www.xilinx.com/support/documentation/boards_and_kits/vcu118/xtp453-vcu118-quickstart.pdf
- » For the Rev 2.0 VCU118, due to QSPI, set SW16 to 0001

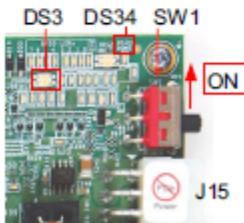


STEP 1: Set Configuration Switches

Set the configuration mode DIP switch (SW16) so that the BIST file is loaded at power-up from the BPI flash memory as shown below:

Switch	Setting*	Purpose
SW16-1	0	SYSCTRL_ENABLE
SW16-2	0	FPGA configuration mode: 010=Load from BPI flash
SW16-3	1	101=JTAG configuration
SW16-4	0	

* 1=ON, 0=OFF



STEP 2: Connect Power to the Board

Connect the 6-pin power supply plug to J15, and power up the board using the SW1 switch.

When LED DS3 glows green, the power system is good.

When DONE LED DS34 glows blue, the Virtex UltraScale+ FPGA is configured successfully.

VCU118 Board Self Test Demo

- > Follow the instructions in the VCU118 Quick Start Guide, XTP453

» http://www.xilinx.com/support/documentation/boards_and_kits/vcu118/xtp453-vcu118-quickstart.pdf



STEP 3: Run the Built-In Self-Test

The BIST consists of a set of pass/fail tests. On power-up, the Clock, DDR, BRAM, flash memory, and I2C tests are run without user input.

A passing test is indicated when the corresponding GPIO LED for each test is ON. See the following table for the LED that corresponds to each test.

The DIP and pushbutton (PB) tests require user interaction as described in the following section. The blinking LED indicates which test is waiting for user input.

Board Self-Test Assignments for GPIO LEDs

GPIO LEDs							
7	6	5	4	3	2	1	0
Clock	DDR	BRAM	Flash	I2C	DIP	PB	NA

VCU118 Board Self Test Demo

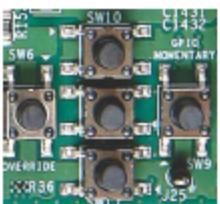
- > Follow the instructions in the VCU118 Quick Start Guide, XTP453

» http://www.xilinx.com/support/documentation/boards_and_kits/vcu118/xtp453-vcu118-quickstart.pdf



SW12 is the GPIO DIP switch. To complete the test, push all four switches to the ON position.

A passing test is indicated when GPIO LED 2 is ON.



The PB test checks pushbutton operation.

To complete the test, push the N, W, S, and E pushbuttons in any order. Then push the center pushbutton.

A passing test is indicated when GPIO LED 1 is ON.

VCU118 IPI Design Description

> **Description**

- » The IP Integrator (IPI) application uses an MicroBlaze system to verify board functionality. A UART based terminal program interface offers users a menu of tests to run.

> **Block Design Source**

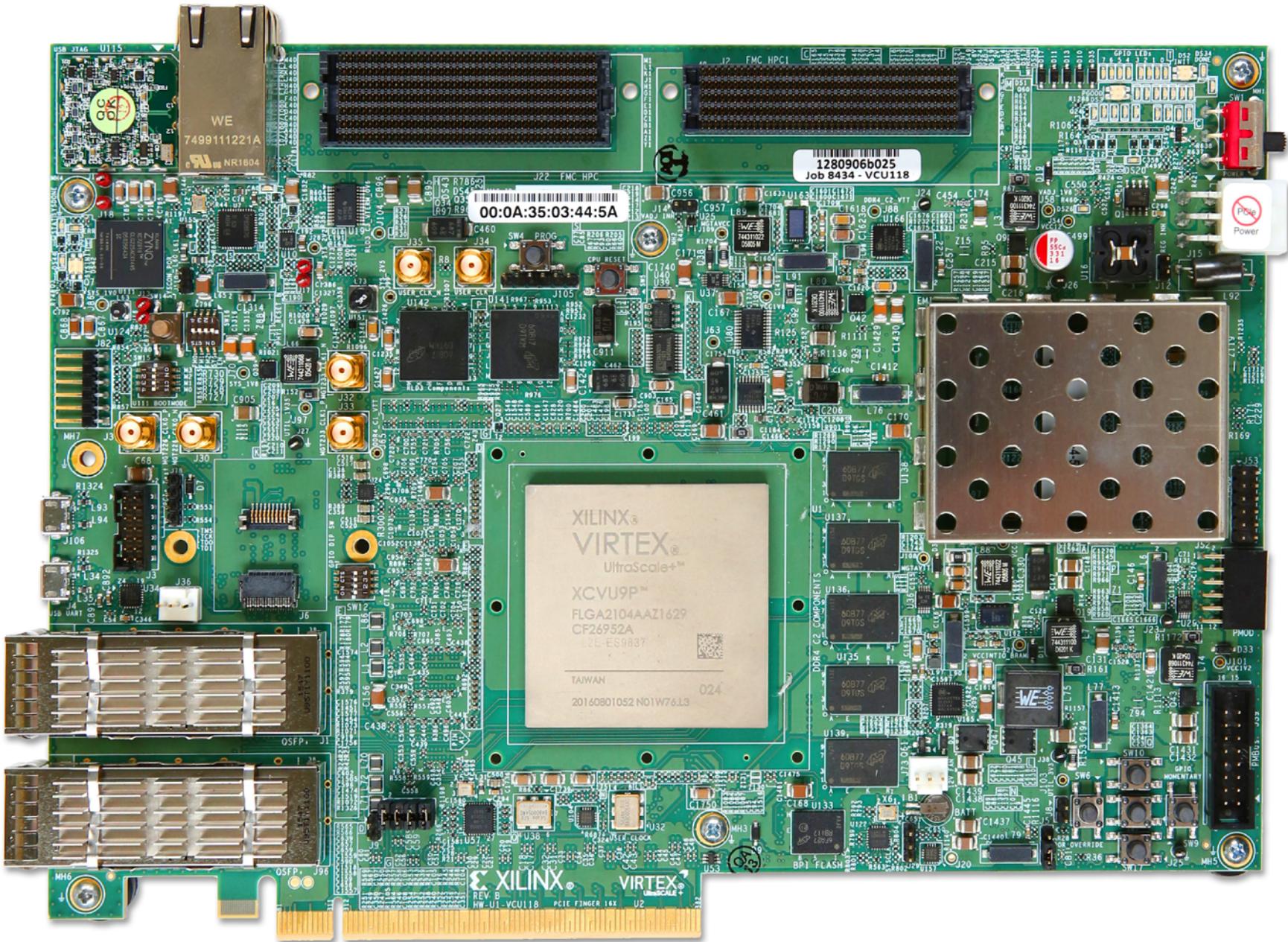
- » RDF0389 - VCU118 IPI Design Files (2019.1 C) ZIP file

VCU118 IPI Design Description

> Block Design IP

- » Processor and Subsystems: MicroBlaze, MicroBlaze Debug Module (MDM), Proc Sys Reset, AXI Interrupt Controller
- » AXI Bus: AXI Interconnect, AXI Timer
- » Memory: Dual DDR4 SDRAM (MIG), AXI BRAM Controller, Block Memory Generator, MicroBlaze Memory
- » Ethernet: AXI Ethernet, AXI DMA
- » Video: AXI4-Stream to Video Out, Video Timing Controller, Test Pattern Generator
- » Peripherals: AXI IIC, AXI GPIO, AXI UART16550, System Management Wizard
- » Other IP: Clocking Wizard, Constant, Concat, Util Diff IO, top_addr, freq_counter
 - [Vivado Design Suite Tcl Command Reference Guide](#) (UG835)
 - [Designing IP Subsystems Using IP Integrator](#) (UG994)

Xilinx VCU118 Board



VCU118 Software Install and Board Setup

- > Complete setup steps in XTP449 – VCU118 Software Install and Board Setup:

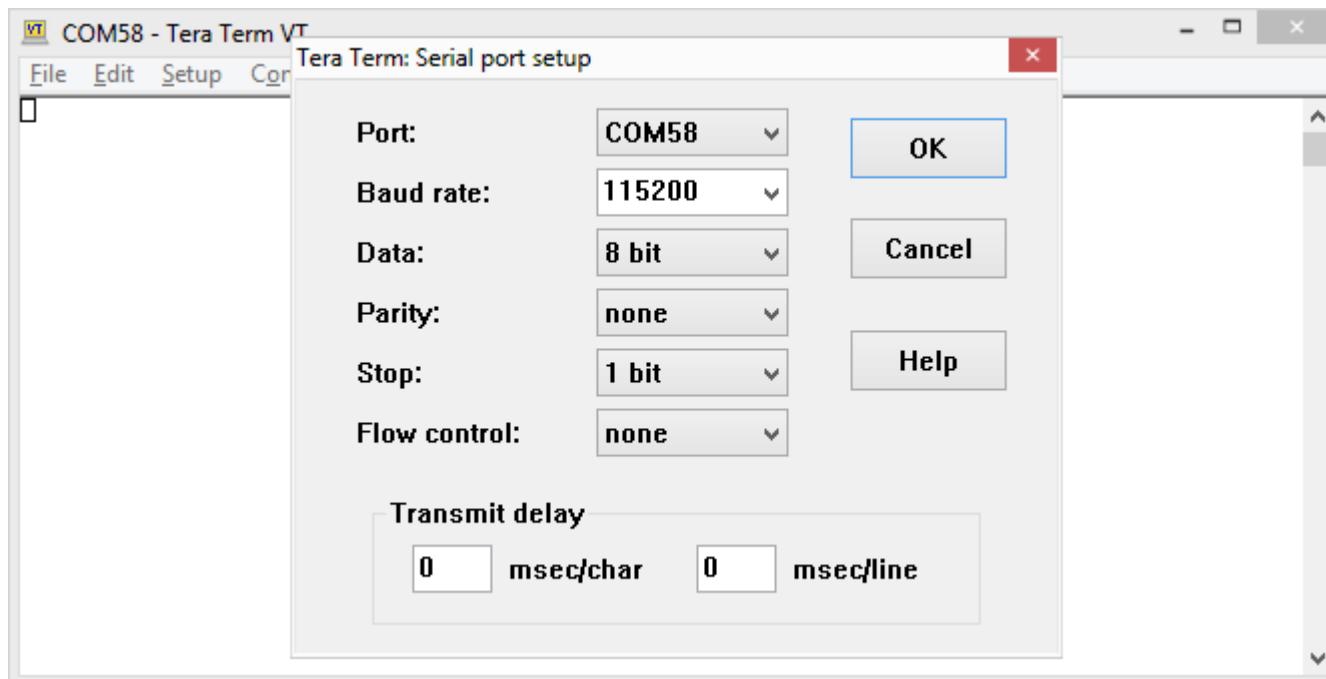
- » Software Requirements
- » VCU118 Board Setup
- » UART Driver Install
- » Clock Setup
- » Optional Hardware Setup



VCU118 Setup

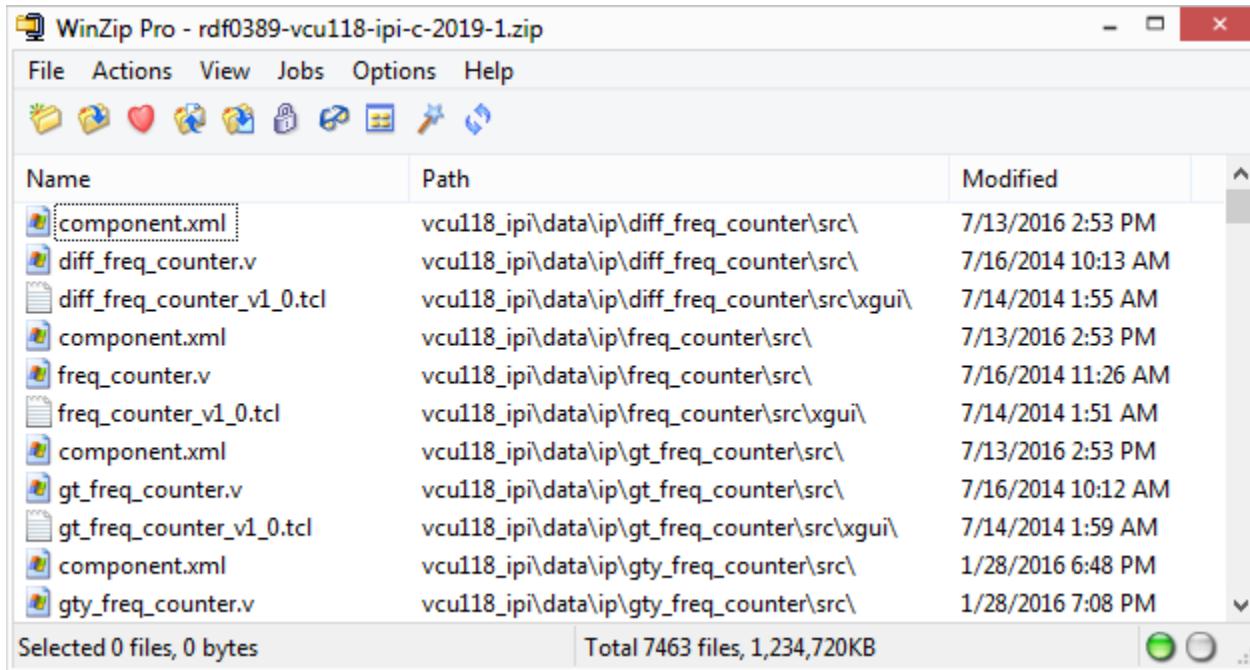
> Start the Terminal Program

- » Select the USB Standard Com Port as noted in the XTP449 Setup Guide
- » Set the baud to 115200



VCU118 Setup

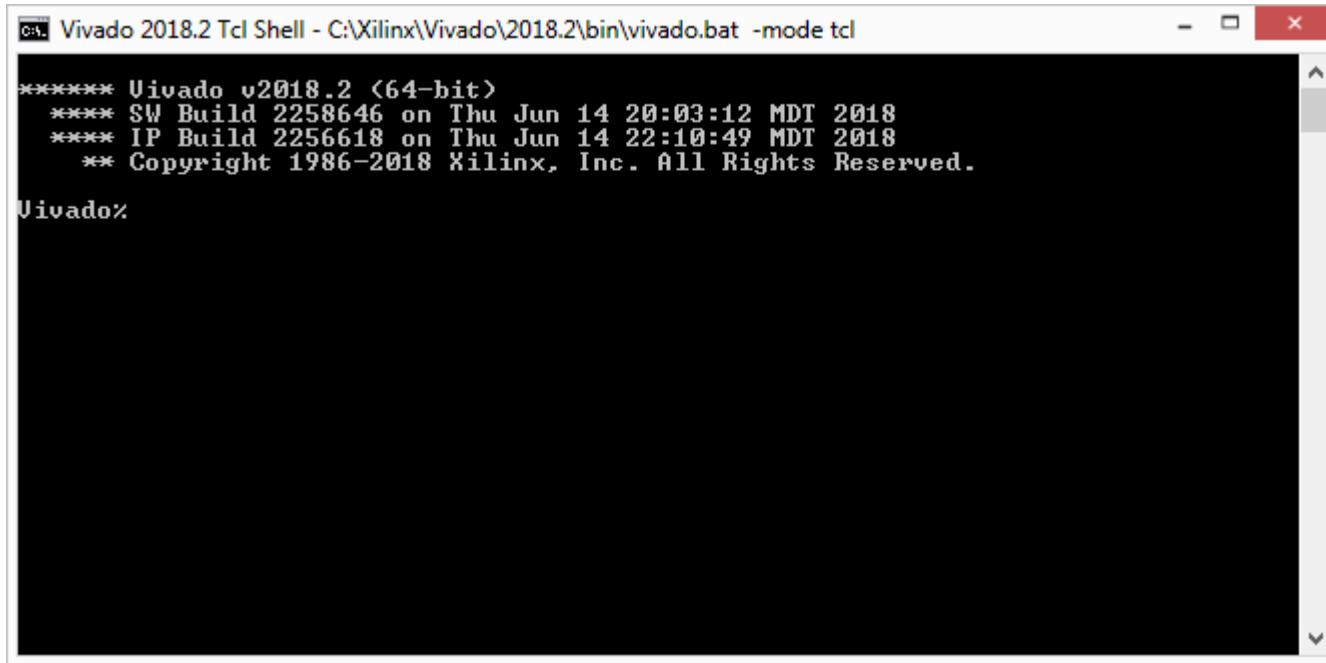
- > Unzip the RDF0389 - VCU118 IPI Design Files (2019.1 C) ZIP file



VCU118 IPI Design

> Open a Vivado Tcl Shell:

Start → All Programs → Xilinx Design Tools → Vivado 2019.1 →
Vivado 2019.1 Tcl Shell



The screenshot shows a Windows command-line interface window titled "Vivado 2018.2 Tcl Shell - C:\Xilinx\Vivado\2018.2\bin\vivado.bat -mode tcl". The window displays the following startup information:

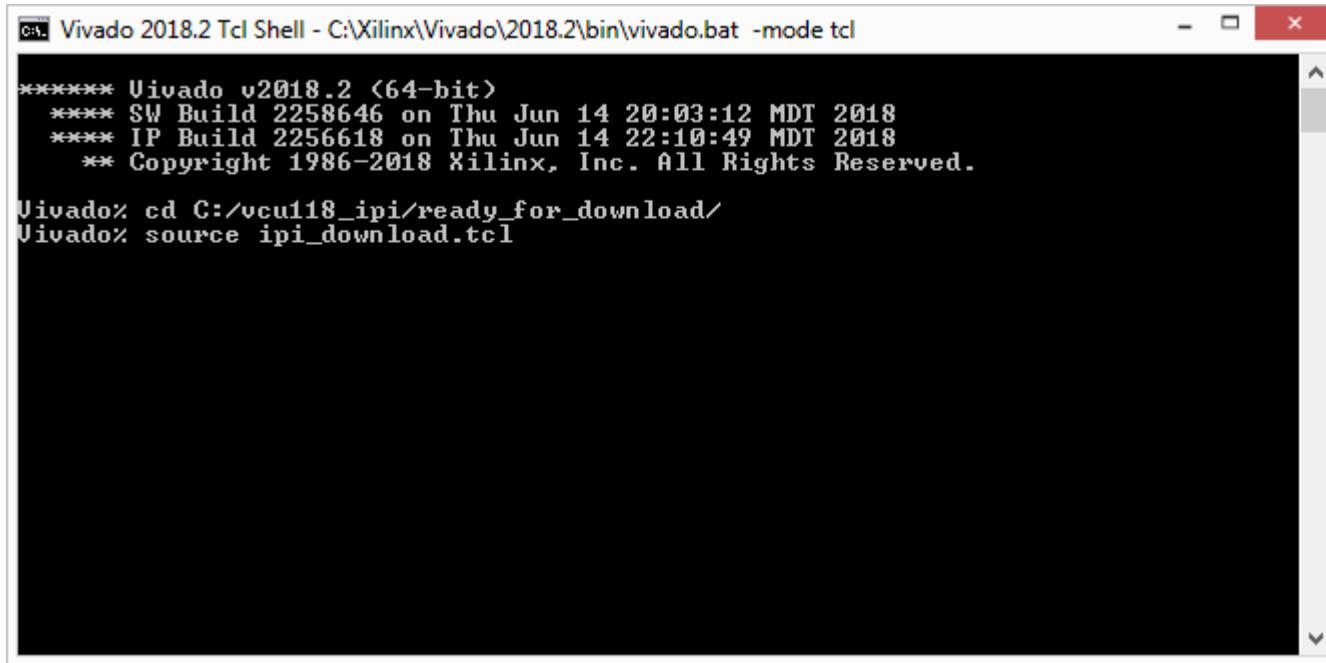
```
***** Vivado v2018.2 (64-bit)
***** SW Build 2258646 on Thu Jun 14 20:03:12 MDT 2018
***** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.
```

At the bottom of the window, the text "Vivado>" is visible, indicating the prompt for further commands.

VCU118 IPI Design

- > Download the IPI bitstream
- > In the Vivado Tcl Shell type:

```
cd C:/vcu118_ipi/ready_for_download/  
source ipi_download.tcl
```

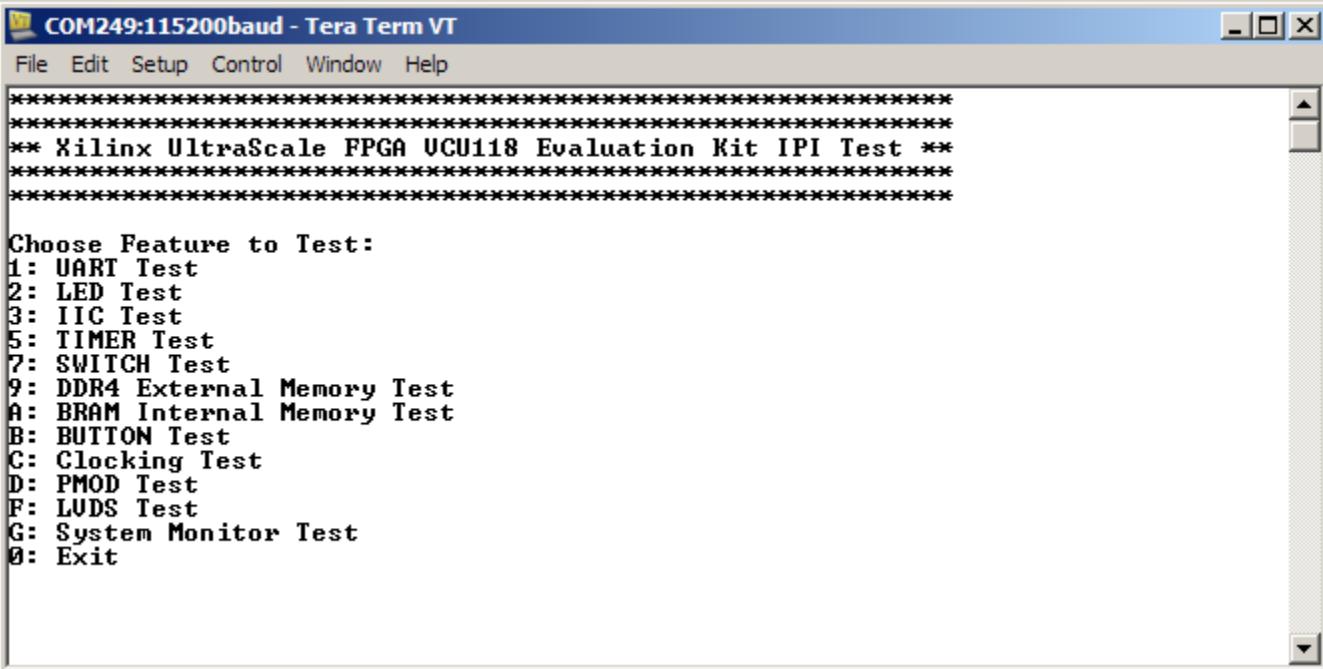


The screenshot shows a Windows command-line interface window titled "Vivado 2018.2 Tcl Shell - C:\Xilinx\Vivado\2018.2\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2018.2 (64-bit)  
***** SW Build 2258646 on Thu Jun 14 20:03:12 MDT 2018  
***** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018  
** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.  
  
Vivado> cd C:/vcu118_ipi/ready_for_download/  
Vivado> source ipi_download.tcl
```

VCU118 IPI Design

> View initial IPI screen



The screenshot shows a terminal window titled "COM249:115200baud - Tera Term VT". The window has a blue header bar with the title and standard menu options: File, Edit, Setup, Control, Window, Help. Below the header is a scrollable text area. The text area displays the following content:

```
*****
** Xilinx UltraScale FPGA VCU118 Evaluation Kit IPI Test **
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: IIC Test
5: TIMER Test
7: SWITCH Test
9: DDR4 External Memory Test
A: BRAM Internal Memory Test
B: BUTTON Test
C: Clocking Test
D: PMOD Test
F: LVDS Test
G: System Monitor Test
0: Exit
```

VCU118 IPI Design

> UART Test

- » Type “1” to start the UART Test
- » After each test, press any key to return to the main menu

The screenshot shows a terminal window titled "COM249:115200baud - Tera Term VT". The menu options listed are:

- 5: TIMER Test
- 7: SWITCH Test
- 9: DDR4 External Memory Test
- A: BRAM Internal Memory Test
- B: BUTTON Test
- C: Clocking Test
- D: PMOD Test
- F: LVDS Test
- G: System Monitor Test
- 0: Exit

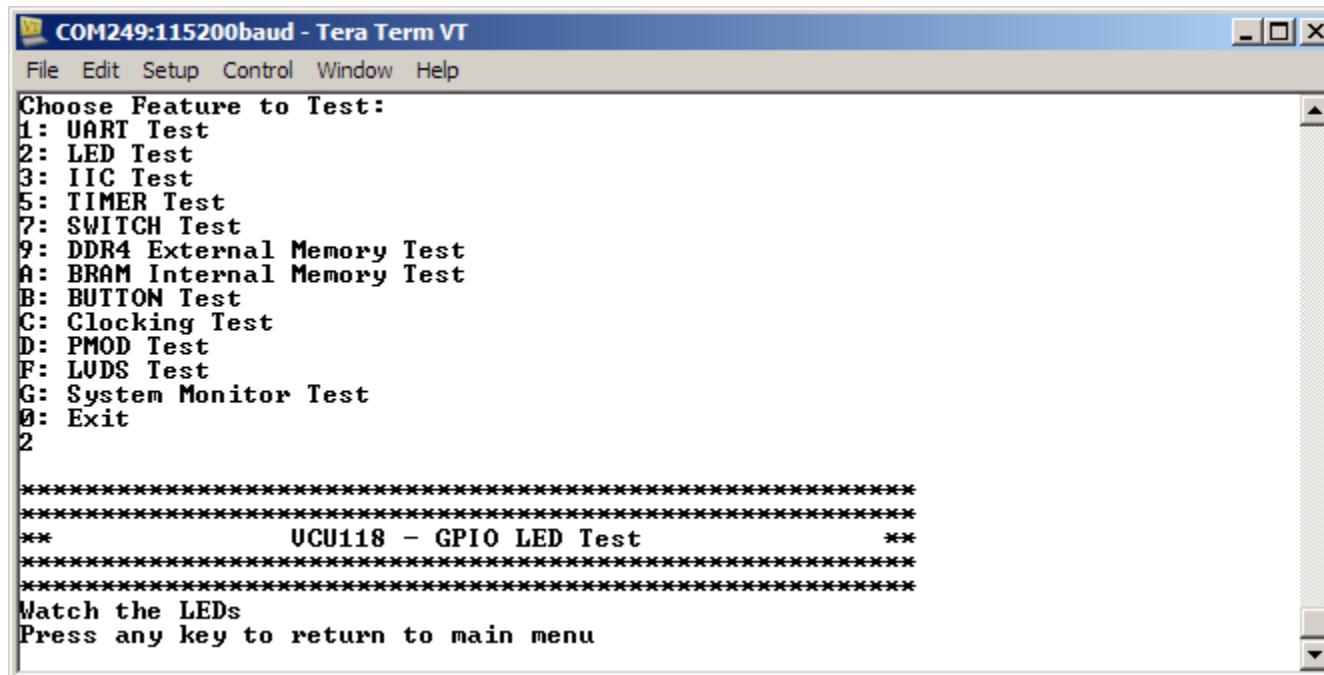
The user has typed "1" to start the UART Test. The output shows:

```
*****
**          UCU118 - UART Test          **
*****
Testing UART
115200,8,N,1
Hello world!
UART Test Passed

Press any key to return to main menu
```

VCU118 IPI Design

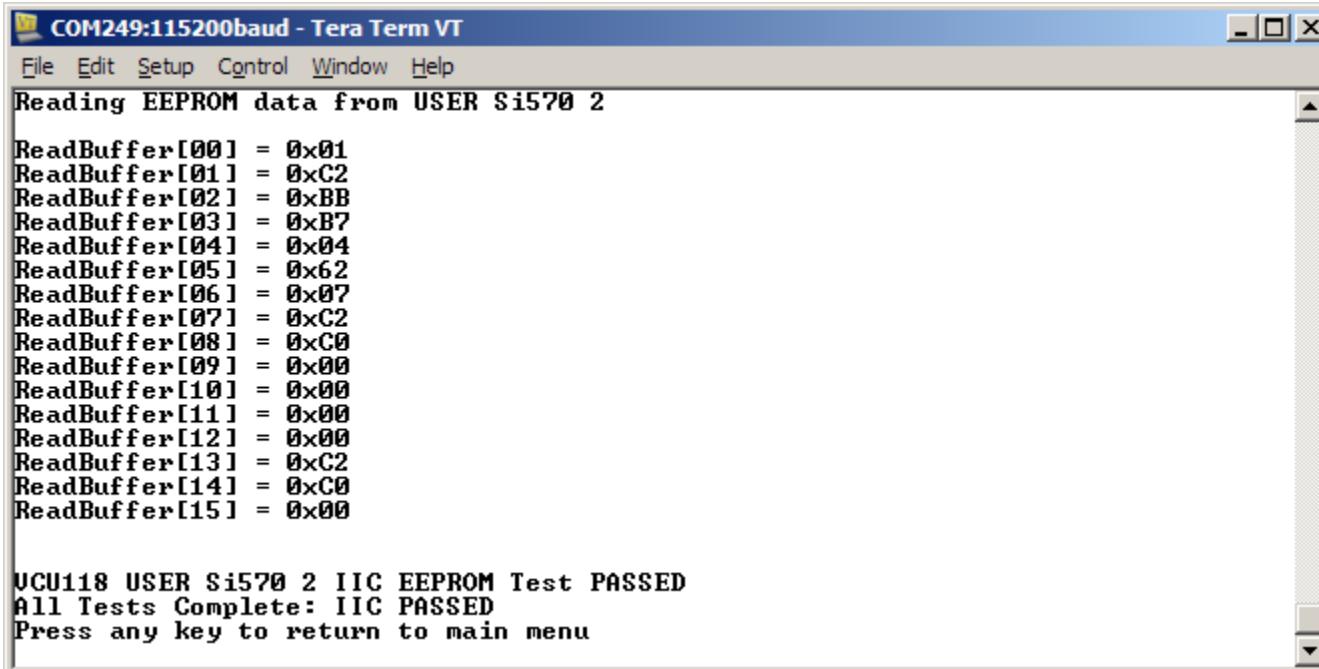
- > LED Test
 - » Type 2 to begin LED Test
- > View Walking 1's pattern on GPIO LEDs
 - » Sequence repeats twice



VCU118 IPI Design

> IIC Test

» Type 3 to begin IIC Test



The screenshot shows a terminal window titled "COM249:115200baud - Tera Term VT". The window has a menu bar with File, Edit, Setup, Control, Window, and Help. The main text area displays the following output:

```
Reading EEPROM data from USER Si570 2
ReadBuffer[00] = 0x01
ReadBuffer[01] = 0xC2
ReadBuffer[02] = 0xBB
ReadBuffer[03] = 0xB7
ReadBuffer[04] = 0x04
ReadBuffer[05] = 0x62
ReadBuffer[06] = 0x07
ReadBuffer[07] = 0xC2
ReadBuffer[08] = 0xC0
ReadBuffer[09] = 0x00
ReadBuffer[10] = 0x00
ReadBuffer[11] = 0x00
ReadBuffer[12] = 0x00
ReadBuffer[13] = 0xC2
ReadBuffer[14] = 0xC0
ReadBuffer[15] = 0x00

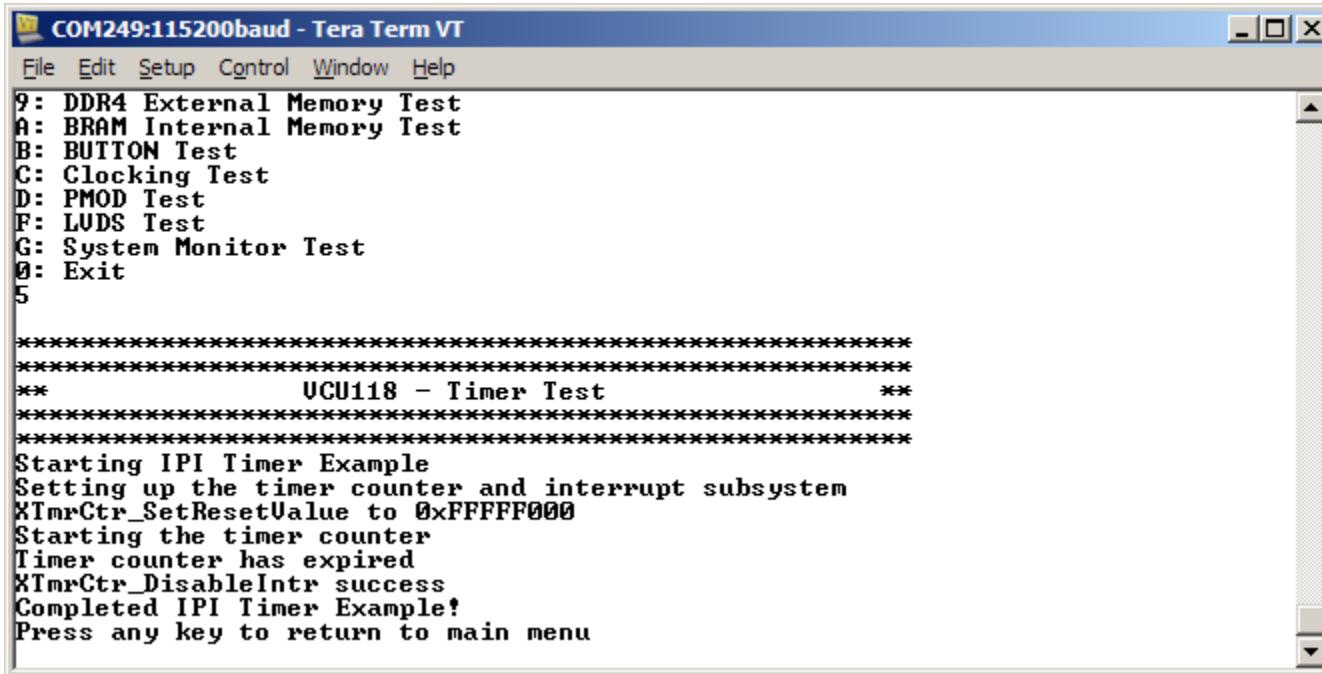
VCU118 USER Si570 2 IIC EEPROM Test PASSED
All Tests Complete: IIC PASSED
Press any key to return to main menu
```

Note: Requires second QSPI Loopback module

VCU118 IPI Design

> Timer Test

» Type 5 to begin Timer Test



The screenshot shows a terminal window titled "COM249:115200baud - Tera Term VT". The window has a menu bar with File, Edit, Setup, Control, Window, and Help. Below the menu is a list of test options:

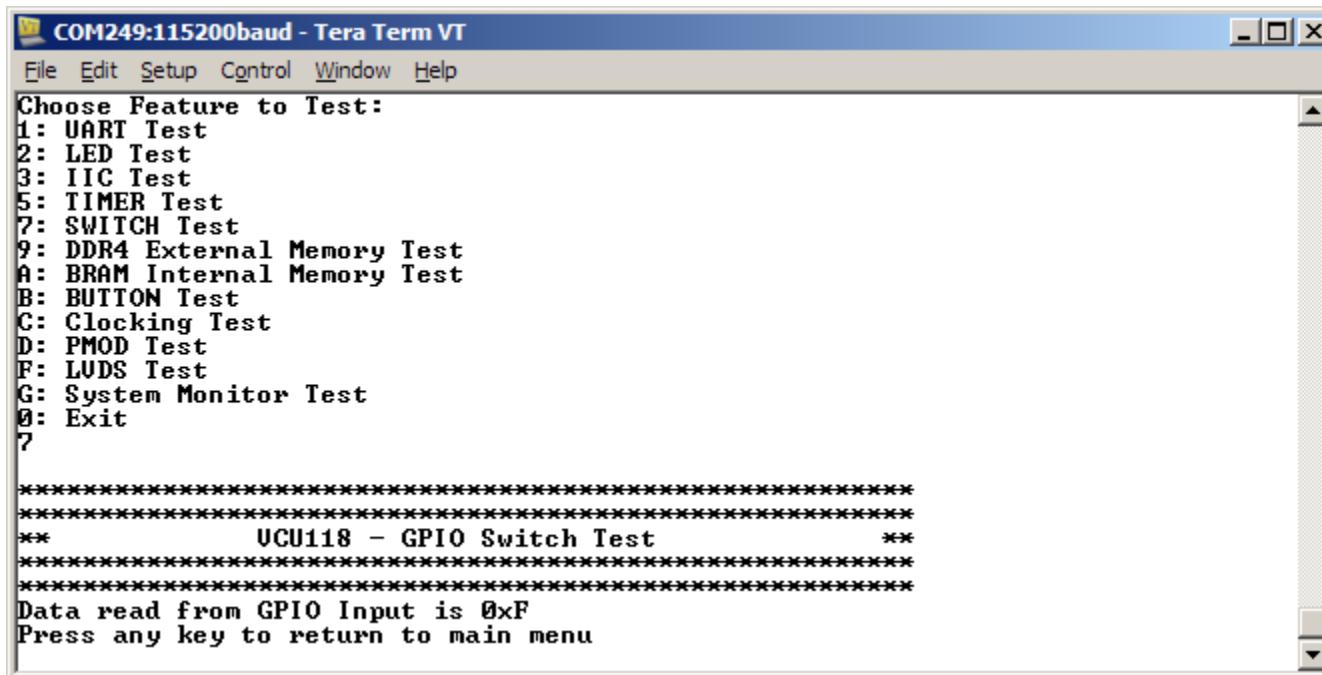
```
File Edit Setup Control Window Help
9: DDR4 External Memory Test
A: BRAM Internal Memory Test
B: BUTTON Test
C: Clocking Test
D: PMOD Test
F: LVDS Test
G: System Monitor Test
0: Exit
5

*****
**          UCU118 - Timer Test          **
*****
Starting IPI Timer Example
Setting up the timer counter and interrupt subsystem
XTmrCtr_SetResetValue to 0xFFFFF000
Starting the timer counter
Timer counter has expired
XTmrCtr_DisableIntr success
Completed IPI Timer Example!
Press any key to return to main menu
```

VCU118 IPI Design

> GPIO Switch Test

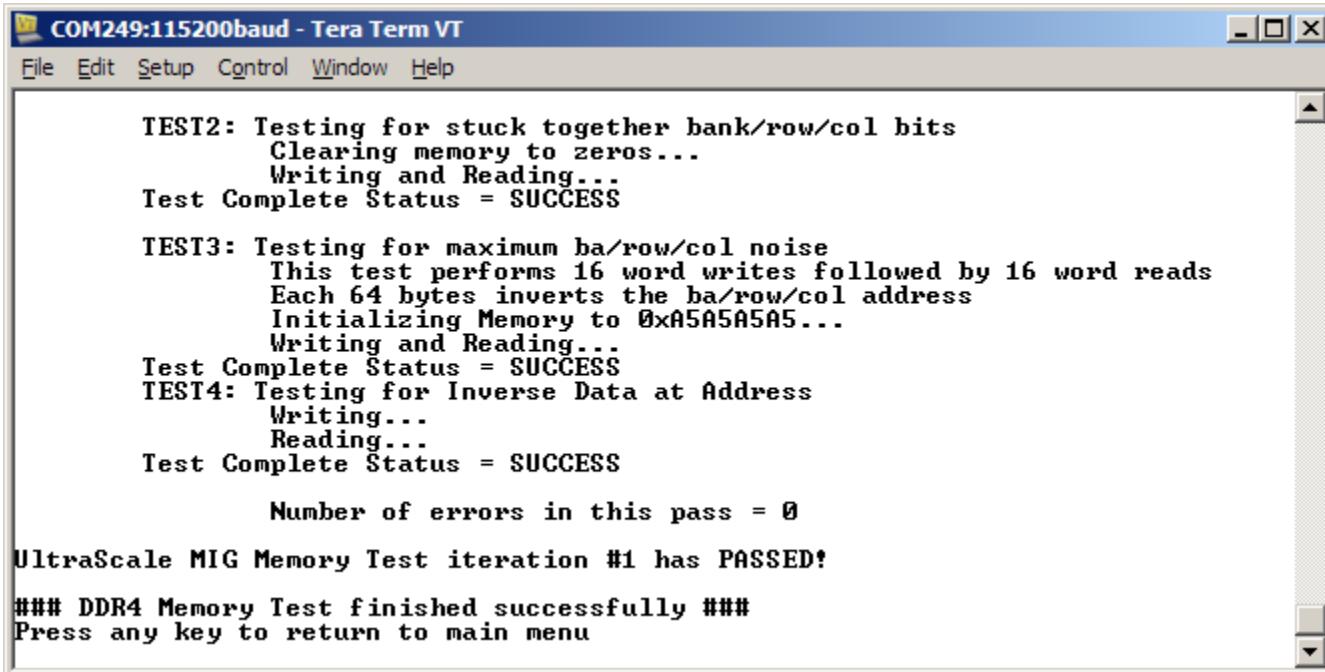
- » Set 4-position GPIO DIP Switch (SW12)
- » Type 7 to begin GPIO Switch Test
 - Reads switch settings



VCU118 IPI Design

> DDR4 Memory Test

- » Type 9 to begin DDR4 Memory Test
- » Tests both VCU118 DDR4 banks



The screenshot shows a terminal window titled "COM249:115200baud - Tera Term VT". The window contains the following text output from a DDR4 memory test:

```
TEST2: Testing for stuck together bank/row/col bits
Clearing memory to zeros...
Writing and Reading...
Test Complete Status = SUCCESS

TEST3: Testing for maximum ba/row/col noise
This test performs 16 word writes followed by 16 word reads
Each 64 bytes inverts the ba/row/col address
Initializing Memory to 0xA5A5A5A5...
Writing and Reading...
Test Complete Status = SUCCESS
TEST4: Testing for Inverse Data at Address
Writing...
Reading...
Test Complete Status = SUCCESS

Number of errors in this pass = 0

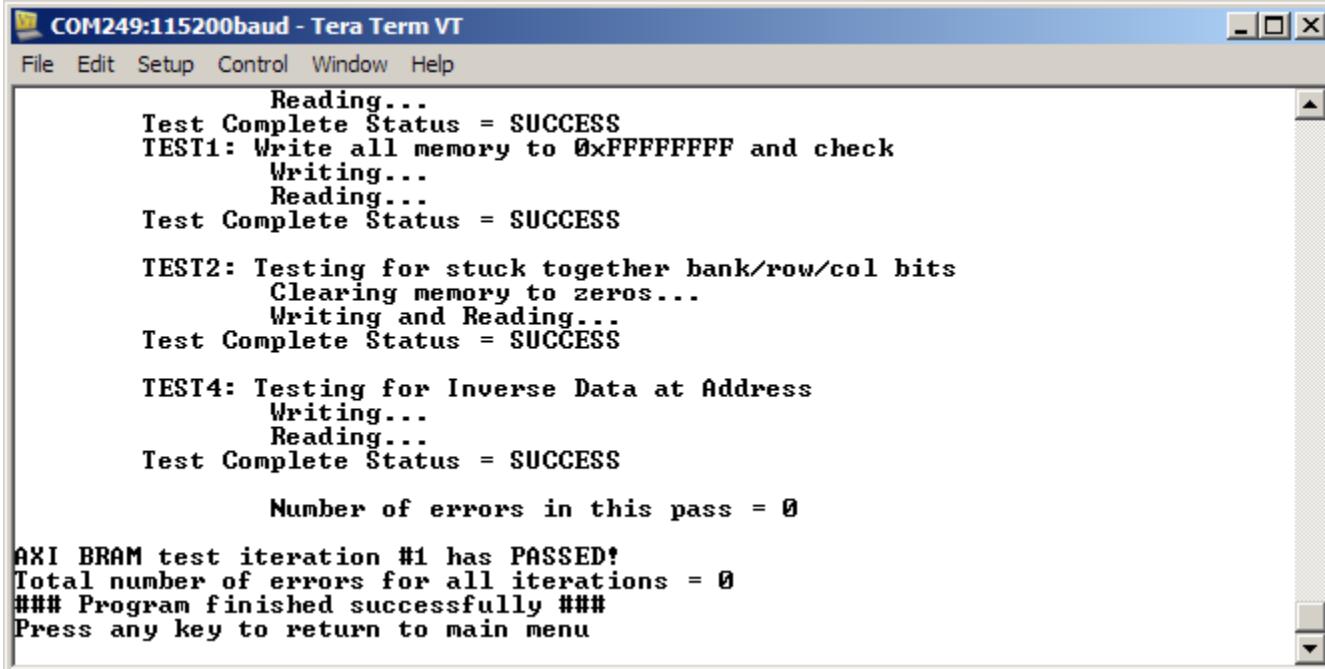
UltraScale MIG Memory Test iteration #1 has PASSED!

### DDR4 Memory Test finished successfully ###
Press any key to return to main menu
```

VCU118 IPI Design

> Internal Memory Test

» Type A to begin BRAM Memory Test



The screenshot shows a terminal window titled "COM249:115200baud - Tera Term VT". The window contains the following text output from a BRAM memory test:

```
Reading...
Test Complete Status = SUCCESS
TEST1: Write all memory to 0xFFFFFFFF and check
Writing...
Reading...
Test Complete Status = SUCCESS

TEST2: Testing for stuck together bank/row/col bits
Clearing memory to zeros...
Writing and Reading...
Test Complete Status = SUCCESS

TEST4: Testing for Inverse Data at Address
Writing...
Reading...
Test Complete Status = SUCCESS

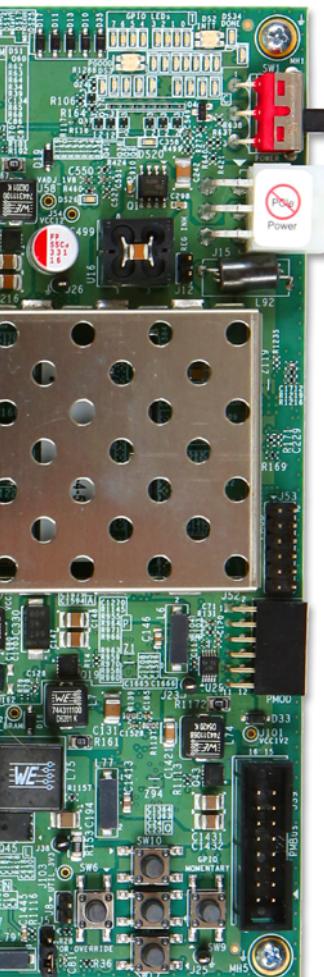
Number of errors in this pass = 0

AXI BRAM test iteration #1 has PASSED!
Total number of errors for all iterations = 0
### Program finished successfully ####
Press any key to return to main menu
```

VCU118 IPI Design

> Button Test

» Type B to begin Button Test



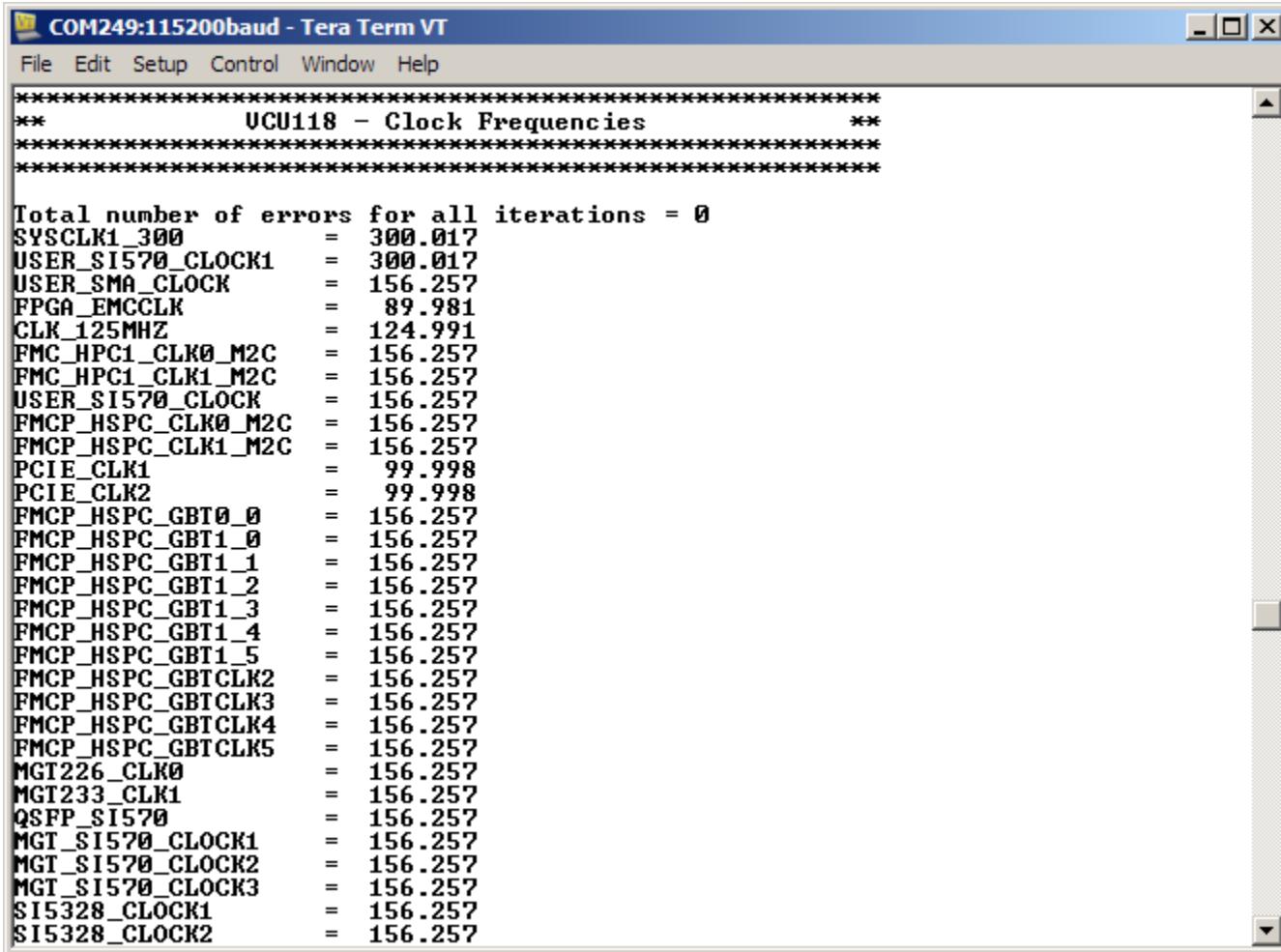
```
COM249:115200baud - Tera Term VT
File Edit Setup Control Window Help
F: LVDS Test
G: System Monitor Test
Q: Exit
B

*****
**          UCU118 - Button Test          **
*****
Press west button
Press south button
Press east button
Press north button
Press center button
Press any button
Press any key to return to main menu
```

VCU118 IPI Design

> Clock Test

- » The clocks must be set up as detailed in XTP449
- » Type C to begin Clock Test



The screenshot shows a terminal window titled "COM249:115200baud - Tera Term VT". The window displays the output of a clock frequency test for the VCU118. The title bar reads "UCU118 - Clock Frequencies". The main text area shows a table of clock names and their measured frequencies. The table includes columns for clock name and frequency value.

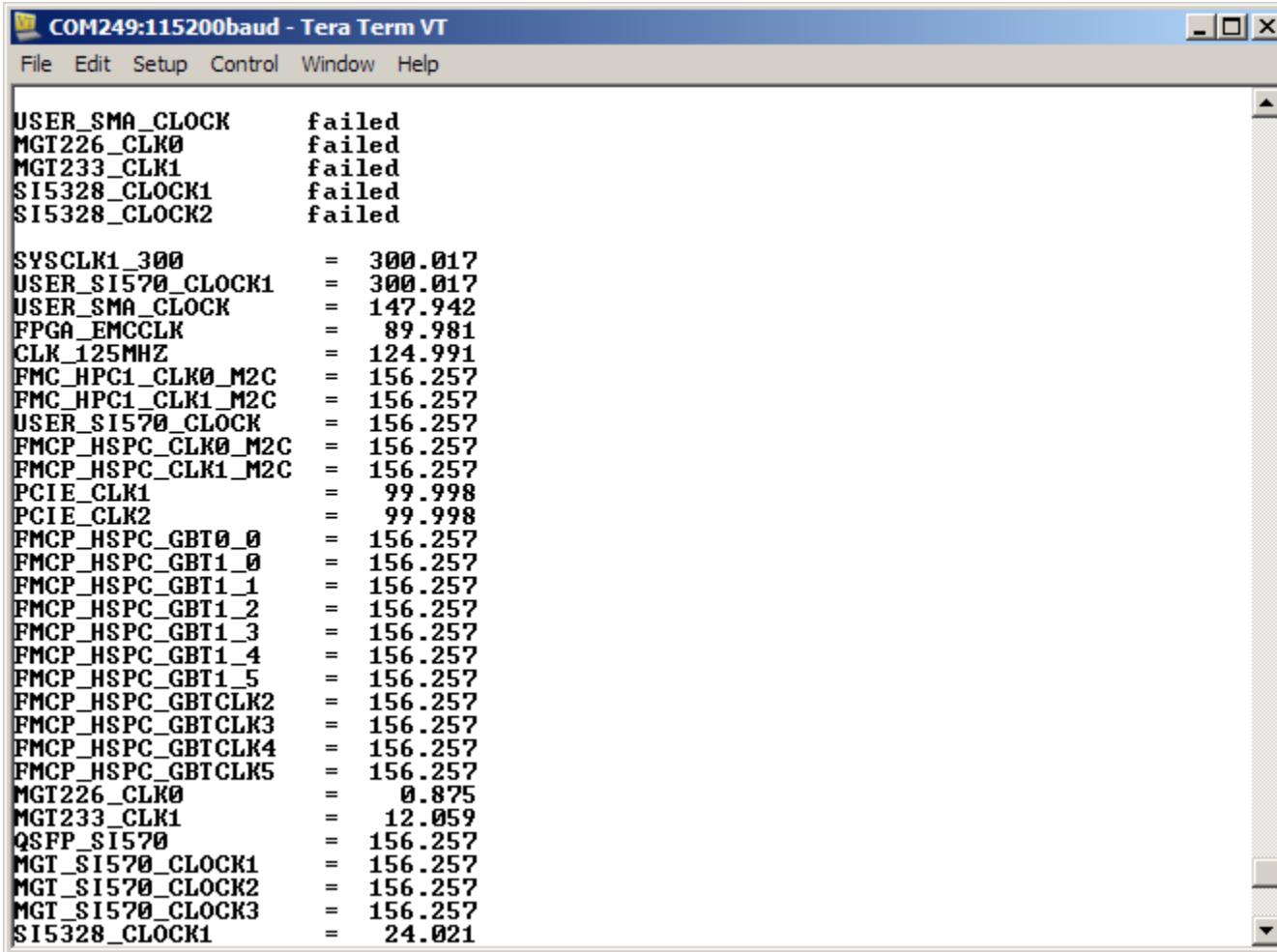
Clock Name	Frequency
SYSCLK1_300	= 300.017
USER_SI570_CLOCK1	= 300.017
USER_SMA_CLOCK	= 156.257
FPGA_EMCCCLK	= 89.981
CLK_125MHZ	= 124.991
FMC_HPC1_CLK0_M2C	= 156.257
FMC_HPC1_CLK1_M2C	= 156.257
USER_SI570_CLOCK	= 156.257
FMCP_HSPC_CLK0_M2C	= 156.257
FMCP_HSPC_CLK1_M2C	= 156.257
PCIE_CLK1	= 99.998
PCIE_CLK2	= 99.998
FMCP_HSPC_GBT0_0	= 156.257
FMCP_HSPC_GBT1_0	= 156.257
FMCP_HSPC_GBT1_1	= 156.257
FMCP_HSPC_GBT1_2	= 156.257
FMCP_HSPC_GBT1_3	= 156.257
FMCP_HSPC_GBT1_4	= 156.257
FMCP_HSPC_GBT1_5	= 156.257
FMCP_HSPC_GBTCLK2	= 156.257
FMCP_HSPC_GBTCLK3	= 156.257
FMCP_HSPC_GBTCLK4	= 156.257
FMCP_HSPC_GBTCLK5	= 156.257
MGT226_CLK0	= 156.257
MGT233_CLK1	= 156.257
QSFP_SI570	= 156.257
MGT_SI570_CLOCK1	= 156.257
MGT_SI570_CLOCK2	= 156.257
MGT_SI570_CLOCK3	= 156.257
SI5328_CLOCK1	= 156.257
SI5328_CLOCK2	= 156.257

Note: Requires optional clock sources

VCU118 IPI Design

> Clock Test

- » Without the proper setup, some clocks will show a failure
- » The clock setup must be repeated after a power cycle



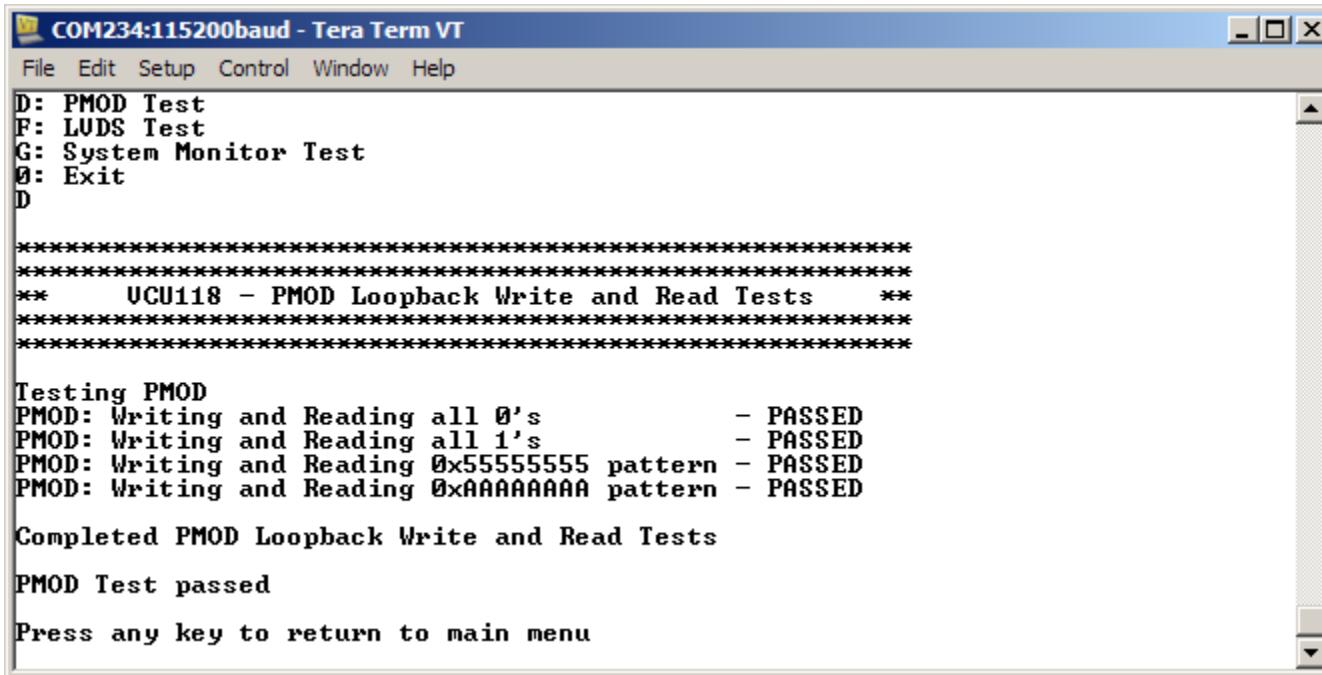
The screenshot shows a terminal window titled "COM249:115200baud - Tera Term VT". The window contains a list of clock configurations and their values. Some entries are marked as failed, while others have specific values assigned.

Clock Name	Status	Value
USER_SMA_CLOCK	failed	
MGT226_CLK0	failed	
MGT233_CLK1	failed	
S15328_CLOCK1	failed	
S15328_CLOCK2	failed	
SYSCLK1_300	=	300.017
USER_SI570_CLOCK1	=	300.017
USER_SMA_CLOCK	=	147.942
FPGA_EMCCCLK	=	89.981
CLK_125MHZ	=	124.991
FMC_HPC1_CLK0_M2C	=	156.257
FMC_HPC1_CLK1_M2C	=	156.257
USER_SI570_CLOCK	=	156.257
FMCP_HSPC_CLK0_M2C	=	156.257
FMCP_HSPC_CLK1_M2C	=	156.257
PCIE_CLK1	=	99.998
PCIE_CLK2	=	99.998
FMCP_HSPC_GBT0_0	=	156.257
FMCP_HSPC_GBT1_0	=	156.257
FMCP_HSPC_GBT1_1	=	156.257
FMCP_HSPC_GBT1_2	=	156.257
FMCP_HSPC_GBT1_3	=	156.257
FMCP_HSPC_GBT1_4	=	156.257
FMCP_HSPC_GBT1_5	=	156.257
FMCP_HSPC_GBTCLK2	=	156.257
FMCP_HSPC_GBTCLK3	=	156.257
FMCP_HSPC_GBTCLK4	=	156.257
FMCP_HSPC_GBTCLK5	=	156.257
MGT226_CLK0	=	0.875
MGT233_CLK1	=	12.059
QSFP_SI570	=	156.257
MGT_SI570_CLOCK1	=	156.257
MGT_SI570_CLOCK2	=	156.257
MGT_SI570_CLOCK3	=	156.257
S15328_CLOCK1	=	24.021

VCU118 IPI Design

> PMOD Loopback Test

- » This test requires the optional PMOD jumpers
- » Type D to begin PMOD Loopback Test



COM234:115200baud - Tera Term VT

File Edit Setup Control Window Help

```
D: PMOD Test
F: LUDS Test
G: System Monitor Test
Ø: Exit
D

*****
** UCU118 - PMOD Loopback Write and Read Tests **
*****

Testing PMOD
PMOD: Writing and Reading all 0's      - PASSED
PMOD: Writing and Reading all 1's      - PASSED
PMOD: Writing and Reading 0x55555555 pattern - PASSED
PMOD: Writing and Reading 0xAAAAAAA pattern - PASSED

Completed PMOD Loopback Write and Read Tests

PMOD Test passed

Press any key to return to main menu
```

VCU118 IPI Design

> LVDS Loopback Test

- » This test requires a second XM107 board
- » Type F to begin LVDS Loopback Test

The screenshot shows a terminal window titled "COM234:115200baud - Tera Term VT". The window contains a list of 16 test entries, each showing a write operation followed by a read operation at the same address, with the word "pattern" and a status of "PASSED". Below this list, a message indicates the completion of FMC LVDS loopback tests and states that the test passed. A final instruction at the bottom prompts the user to press any key to return to the main menu.

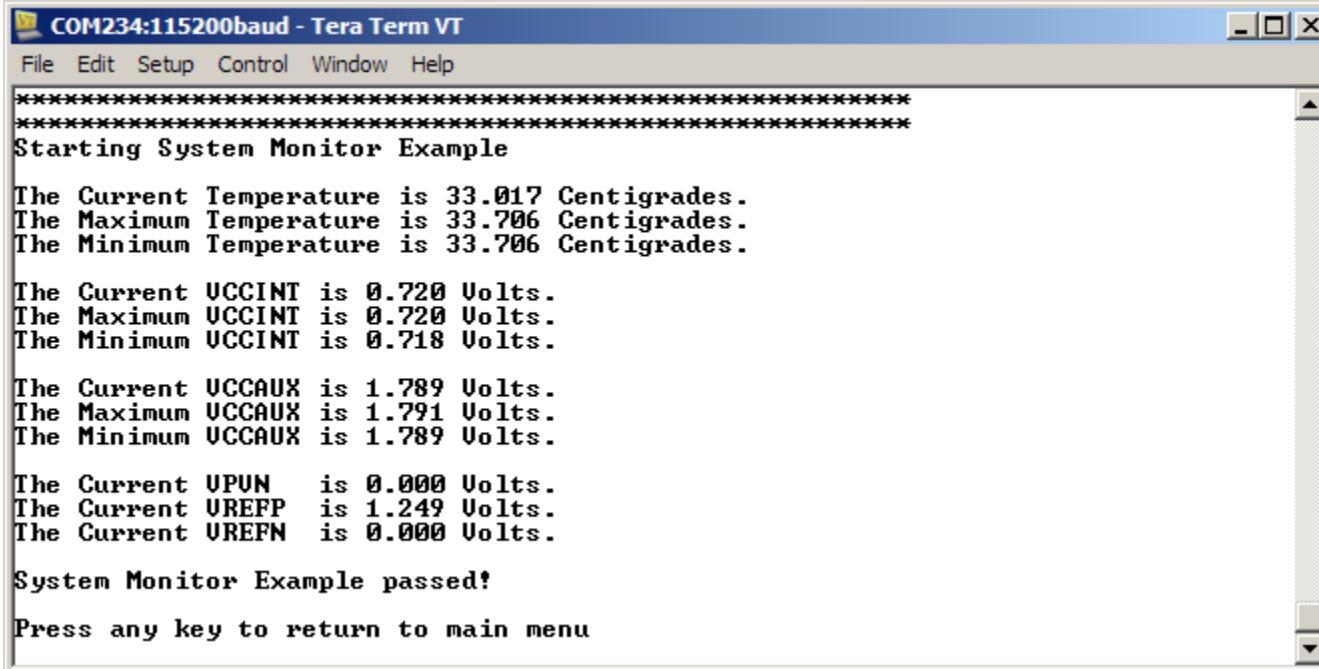
```
HPC1_LA: Writing and Reading 0x00000002 pattern - PASSED
HPC1_LA: Writing and Reading 0x00000004 pattern - PASSED
HPC1_LA: Writing and Reading 0x00000008 pattern - PASSED
HPC1_LA: Writing and Reading 0x00000010 pattern - PASSED
HPC1_LA: Writing and Reading 0x00000020 pattern - PASSED
HPC1_LA: Writing and Reading 0x00000040 pattern - PASSED
HPC1_LA: Writing and Reading 0x00000080 pattern - PASSED
HPC1_LA: Writing and Reading 0x00000100 pattern - PASSED
HPC1_LA: Writing and Reading 0x00000200 pattern - PASSED
HPC1_LA: Writing and Reading 0x00000400 pattern - PASSED
HPC1_LA: Writing and Reading 0x00000800 pattern - PASSED
HPC1_LA: Writing and Reading 0x00001000 pattern - PASSED
HPC1_LA: Writing and Reading 0x00002000 pattern - PASSED
HPC1_LA: Writing and Reading 0x00004000 pattern - PASSED
HPC1_LA: Writing and Reading 0x00008000 pattern - PASSED
HPC1_LA: Writing and Reading 0x00010000 pattern - PASSED

Completed FMC LVDS Loopback Write and Read Tests
FMC LVDS Test passed
Press any key to return to main menu
```

VCU118 IPI Design

> System Monitor Test

» Type G to begin System Monitor Test



The screenshot shows a terminal window titled "COM234:115200baud - Tera Term VT". The window has a menu bar with File, Edit, Setup, Control, Window, and Help. The main text area displays the following output:

```
*****
*****
Starting System Monitor Example
The Current Temperature is 33.017 Centigrades.
The Maximum Temperature is 33.706 Centigrades.
The Minimum Temperature is 33.706 Centigrades.

The Current UCCINT is 0.720 Volts.
The Maximum UCCINT is 0.720 Volts.
The Minimum UCCINT is 0.718 Volts.

The Current UCCAUX is 1.789 Volts.
The Maximum UCCAUX is 1.791 Volts.
The Minimum UCCAUX is 1.789 Volts.

The Current UPUN is 0.000 Volts.
The Current UREFP is 1.249 Volts.
The Current UREFN is 0.000 Volts.

System Monitor Example passed!
Press any key to return to main menu
```

Compile VCU118 IPI Design

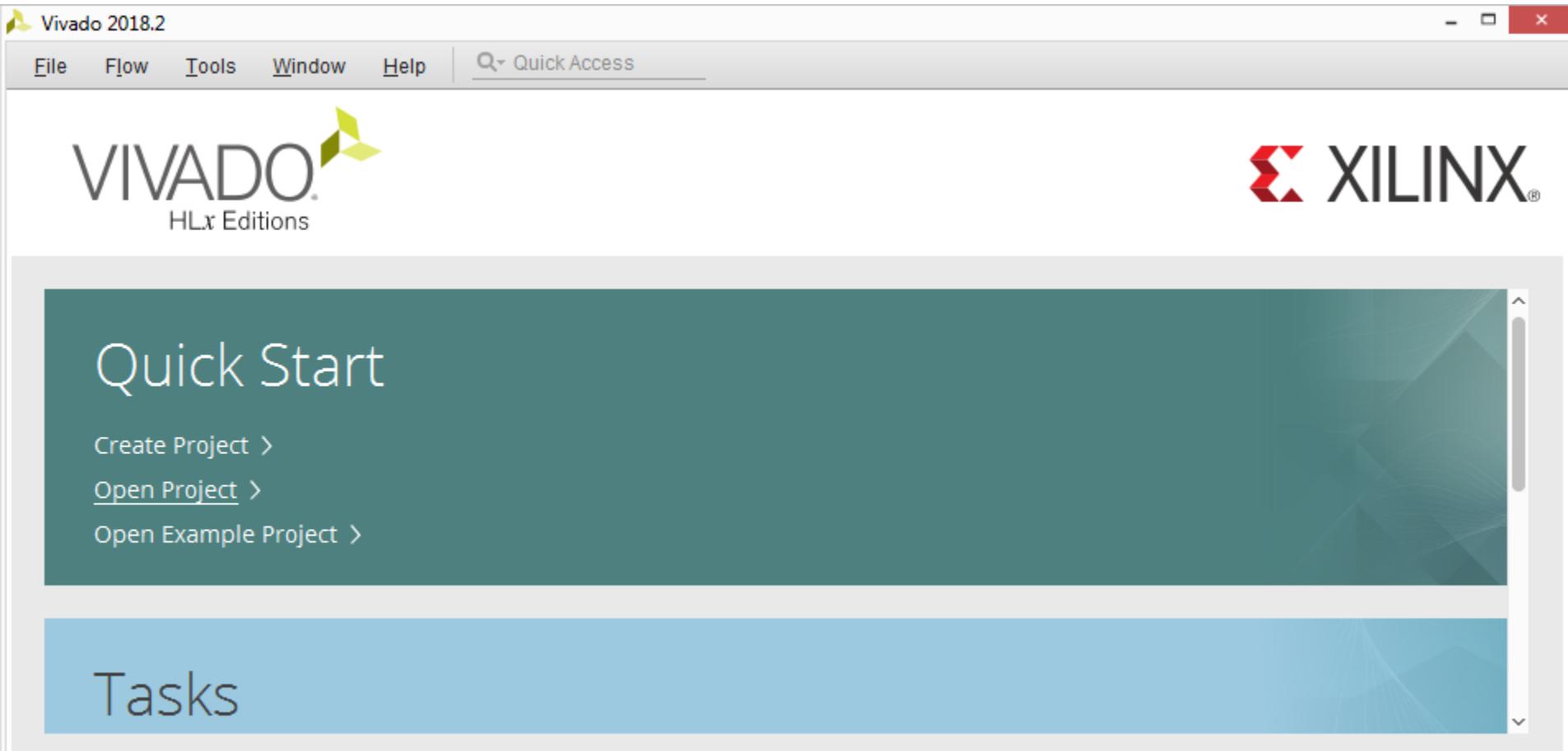


Compile VCU118 IPI Design

> Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2019.1 → Vivado

> Select Open Project



Open Project

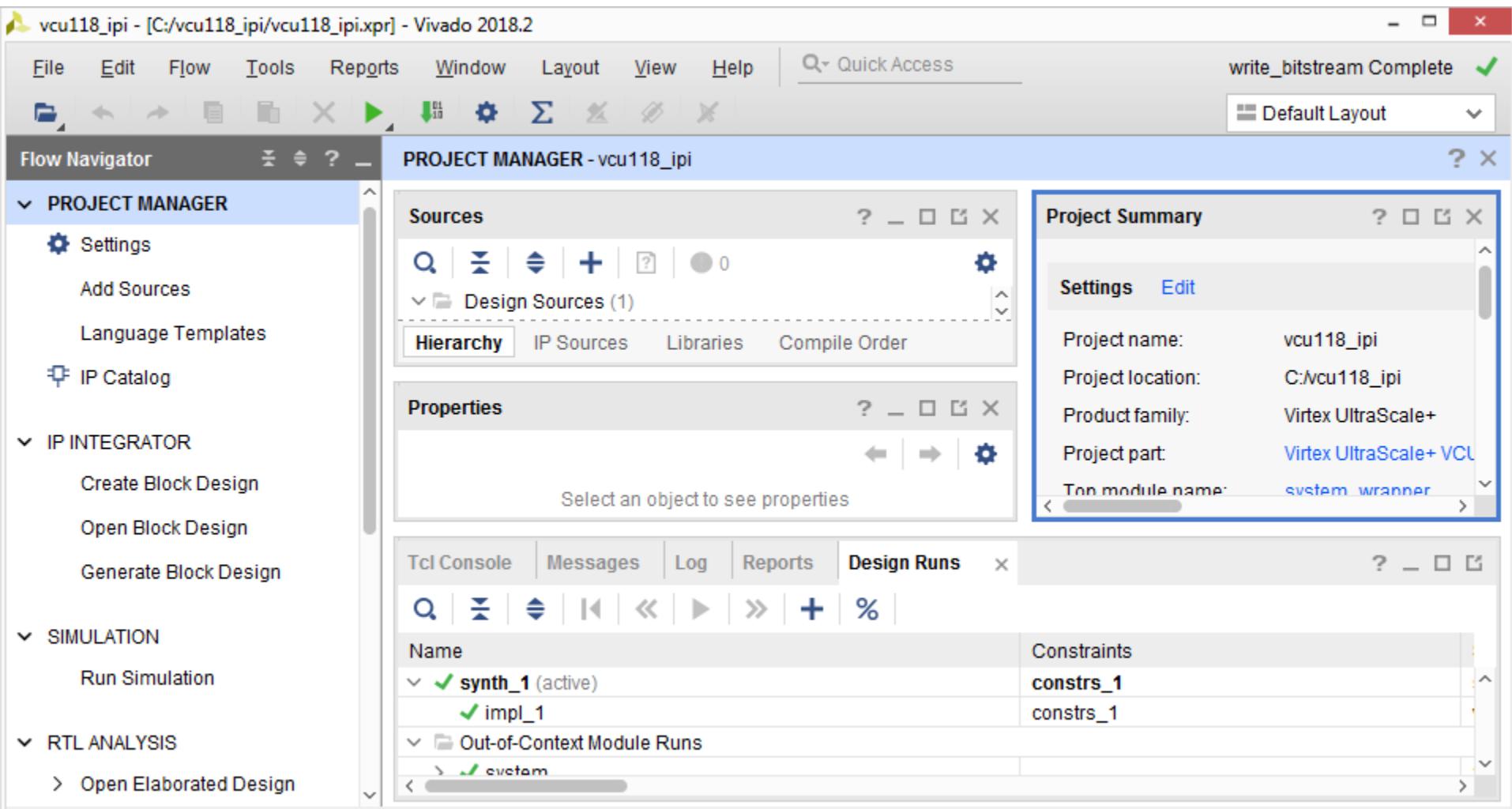
Note: Presentation applies to the VCU118

XILINX

Compile VCU118 IPI Design

> Open the VCU118 Design:

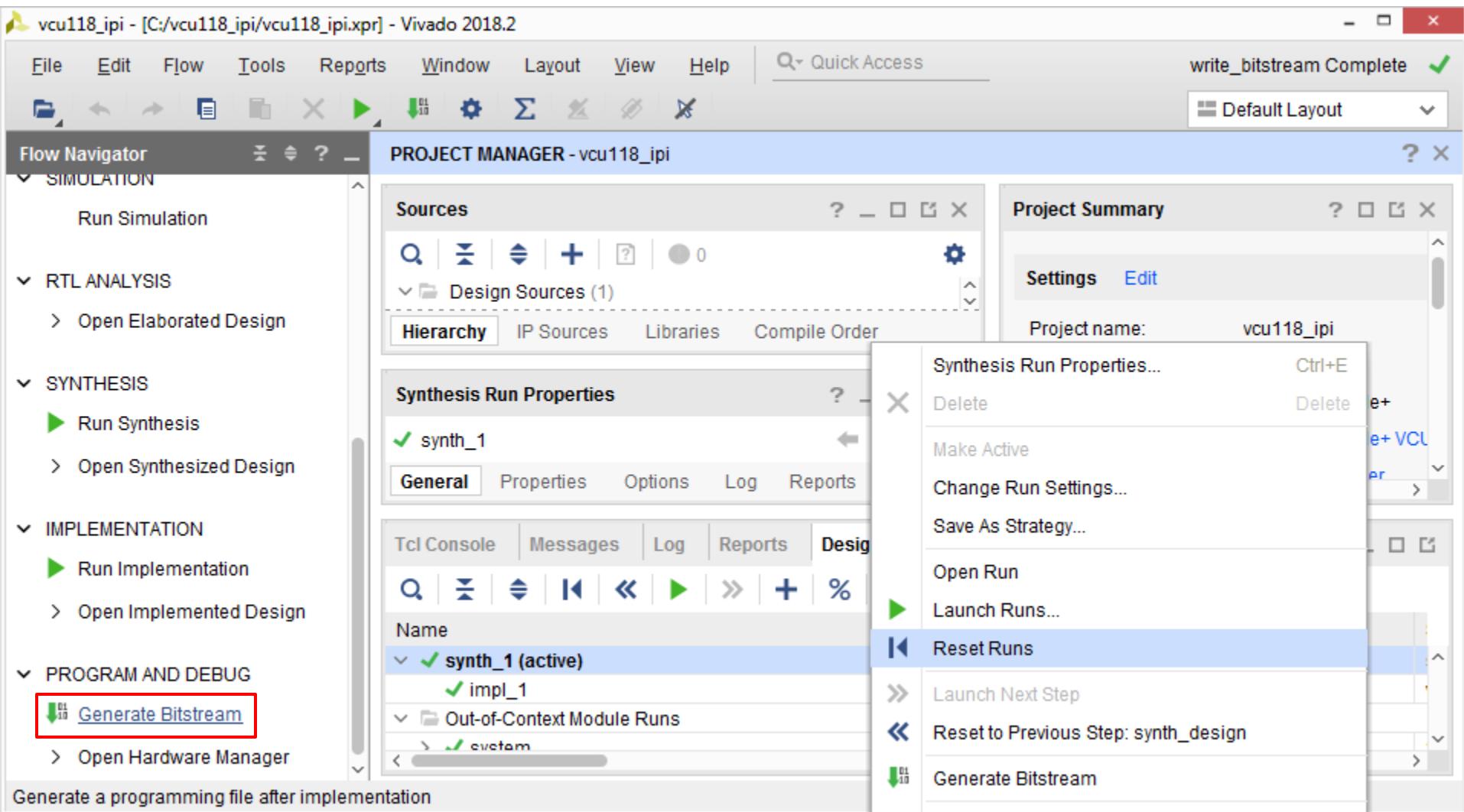
» C:\vcu118_ipi\vcu118_ipi.xpr



Compile VCU118 IPI Design

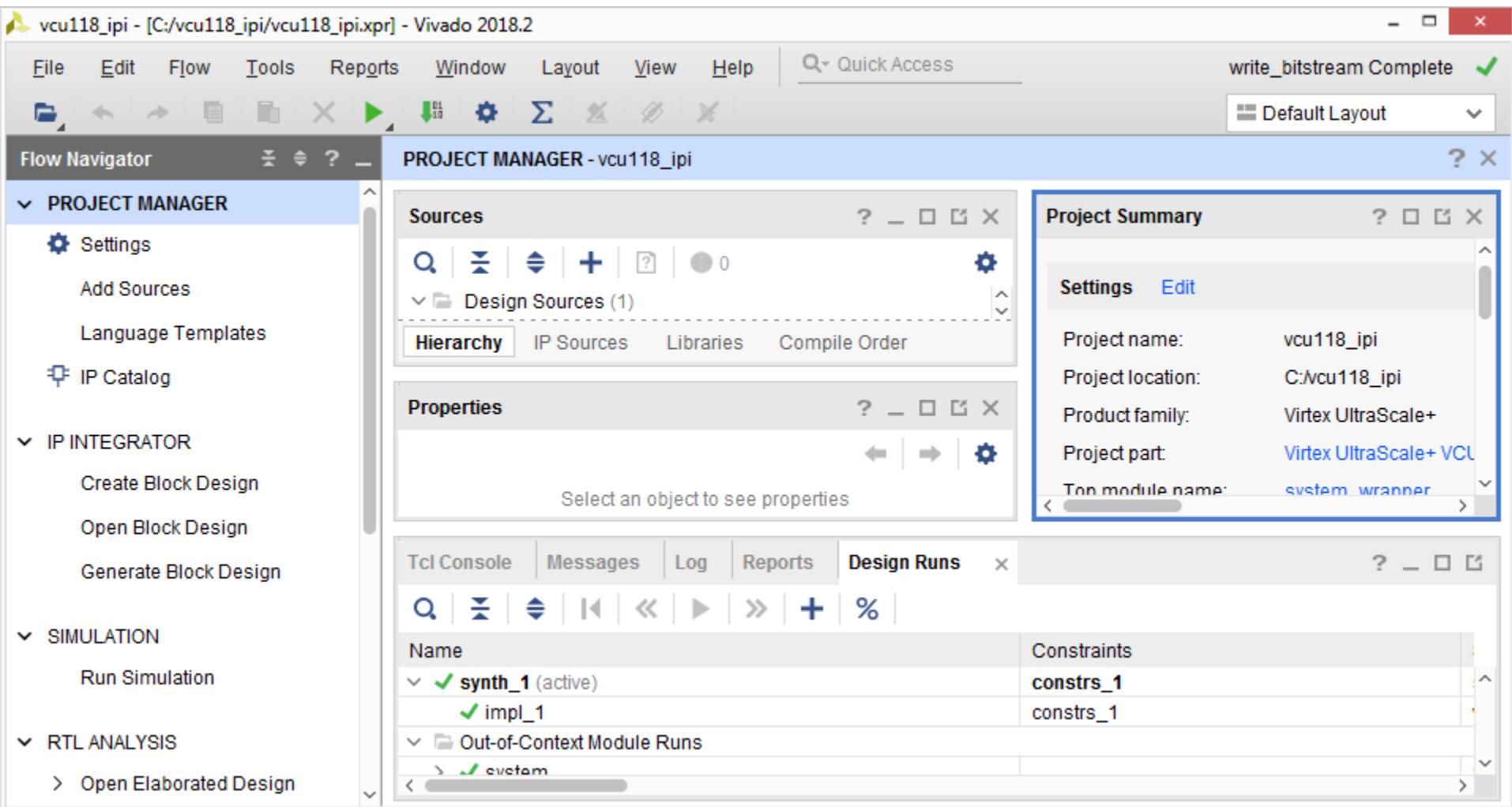
> The design is fully implemented; you can recompile, or export to SDK

» To recompile, right-click synth_1, select Reset Runs then Generate Bitstream



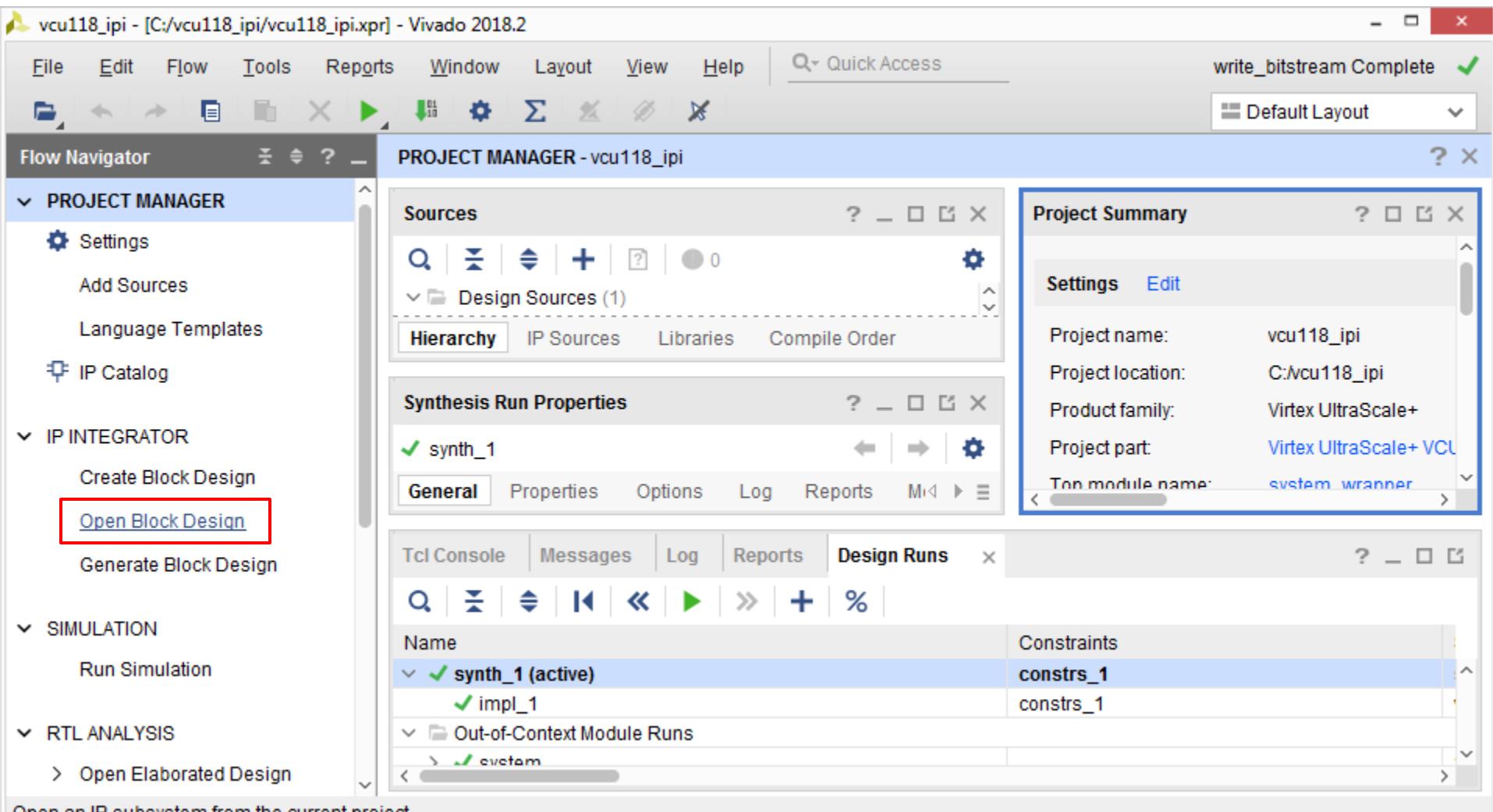
Compile VCU118 IPI Design

- Once done, both the Synthesis and Implementation will have green check marks



Compile VCU118 IPI Design

- > The IPI Design has been implemented with IP Integrator (IPI)
- > Click Open Block Design

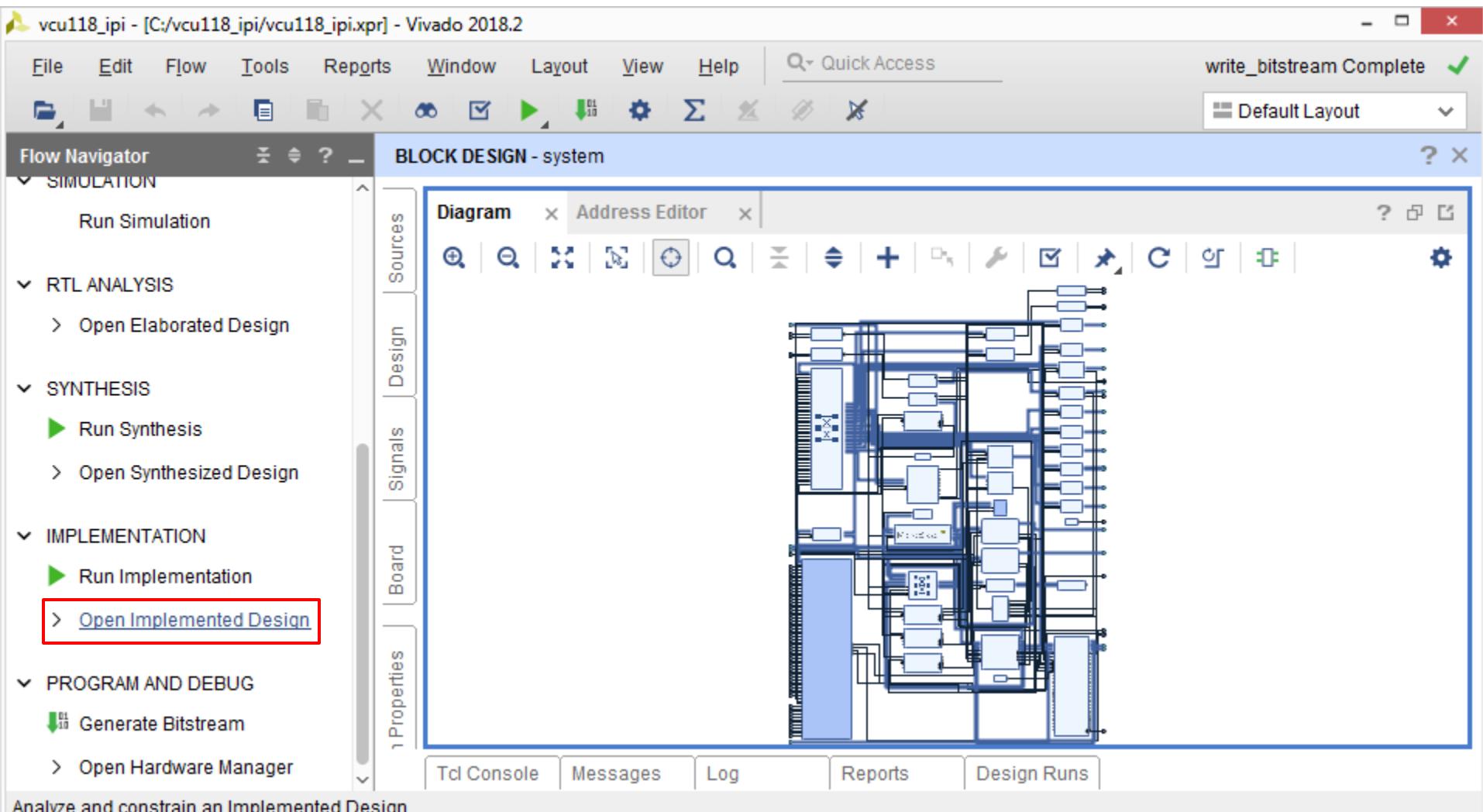


Note: Presentation applies to the VCU118

 XILINX

Compile VCU118 IPI Design

- > The DDR4 IP blocks have been highlighted
- > Click Open Implemented Design

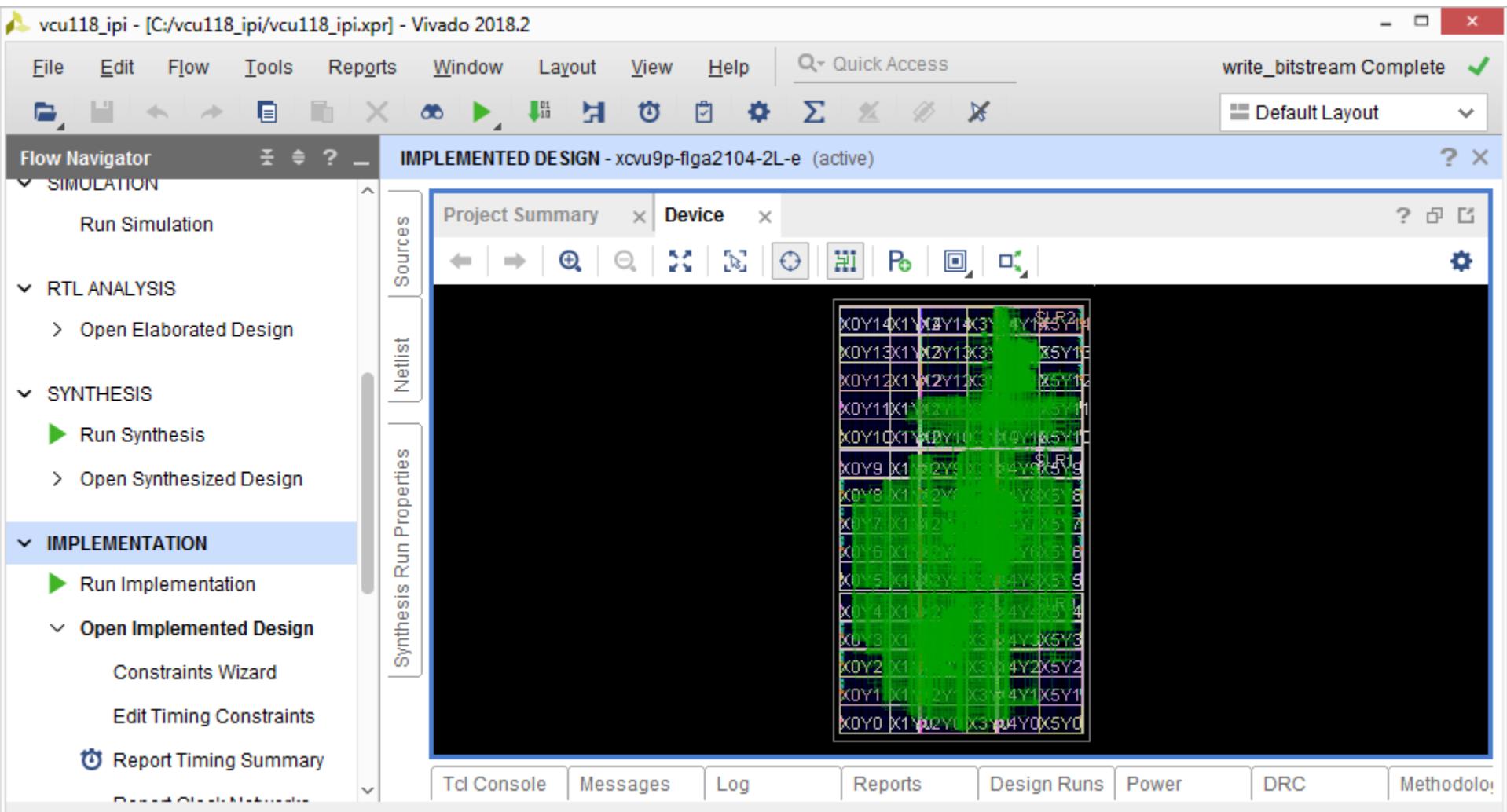


Note: Presentation applies to the VCU118

 XILINX

Compile VCU118 IPI Design

> View Implemented Design

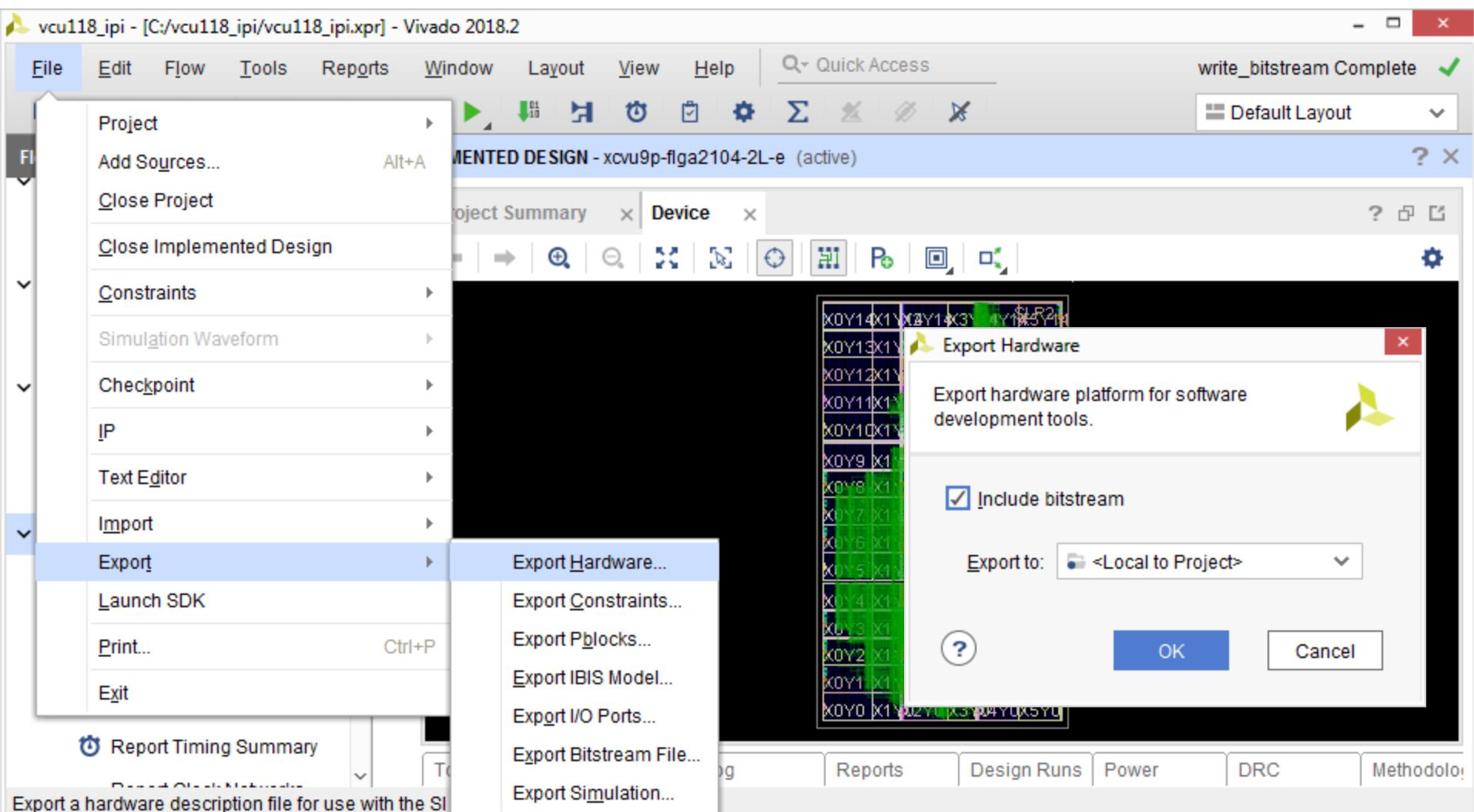


Note: Presentation applies to the VCU118

 XILINX

Compile VCU118 IPI Design

- > Select File → Export → Export Hardware
- > Select Include Bitstream and click OK

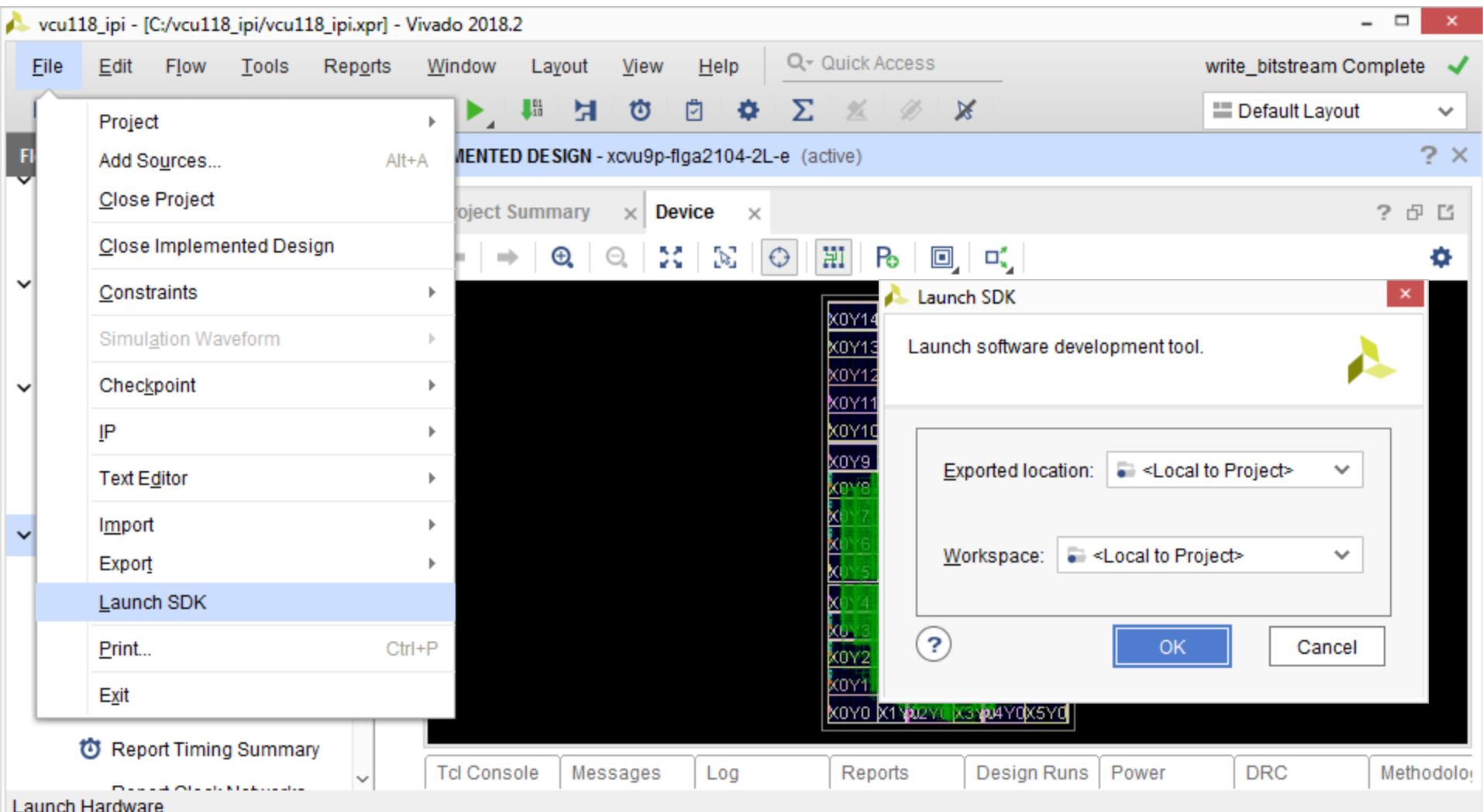


Note: Presentation applies to the VCU118

 XILINX

Compile VCU118 IPI Design

- > Select File → Launch SDK
- > Click OK



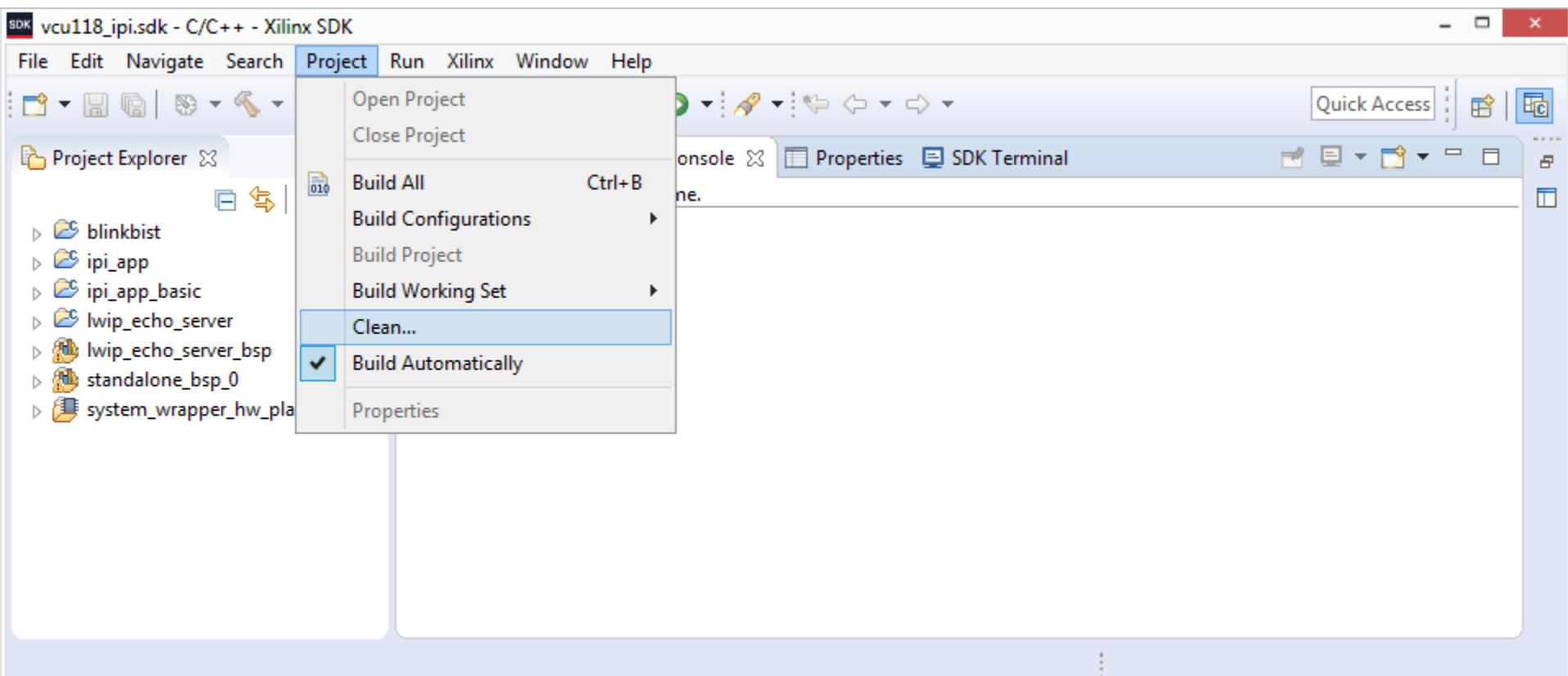
Note: Presentation applies to the VCU118

 XILINX

Compile VCU118 Software in SDK

> SDK Software Compile - Build ELF files in SDK

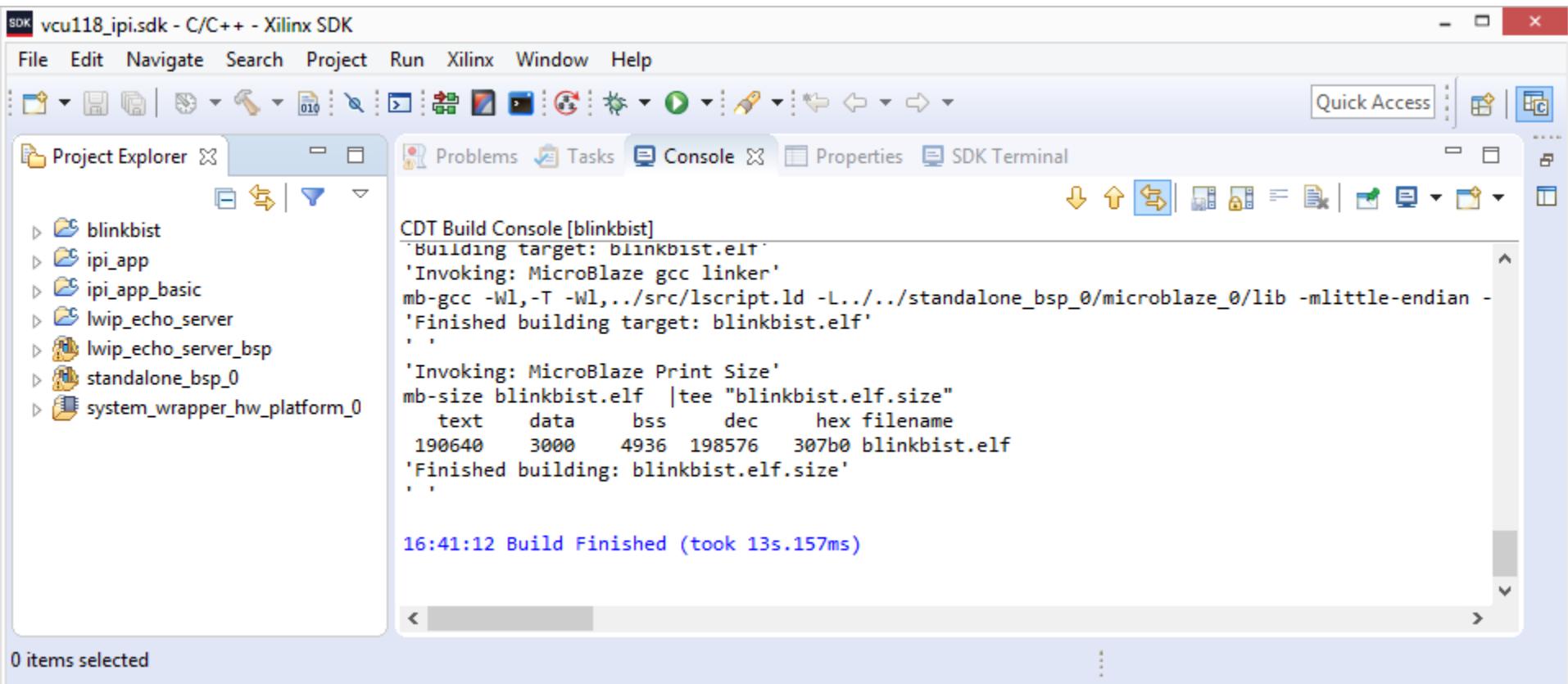
» Select Project → Clean...



Compile VCU118 Software in SDK

> SDK Software Compile - Build ELF files in SDK

» When done, close SDK and return to Vivado



The screenshot shows the Xilinx SDK interface with the title bar "SDK vcu118_ipi.sdk - C/C++ - Xilinx SDK". The menu bar includes File, Edit, Navigate, Search, Project, Run, Xilinx, Window, and Help. The toolbar has various icons for file operations. The left pane is the "Project Explorer" showing projects: blinkbist, ipi_app, ipi_app_basic, lwip_echo_server, lwip_echo_server_bsp, standalone_bsp_0, and system_wrapper_hw_platform_0. The right pane is the "Console" tab, which displays the build logs:

```
CDT Build Console [blinkbist]
'Building target: blinkbist.elf'
'Invoking: MicroBlaze gcc linker'
mb-gcc -Wl,-T -Wl,../src/lscript.ld -L../../standalone_bsp_0/microblaze_0/lib -mlittle-endian -
'Finished building target: blinkbist.elf'
'

'Invoking: MicroBlaze Print Size'
mb-size blinkbist.elf |tee "blinkbist.elf.size"
    text      data      bss      dec      hex filename
 190640      3000     4936   198576   307b0 blinkbist.elf
'Finished building: blinkbist.elf.size'
'

16:41:12 Build Finished (took 13s.157ms)
```

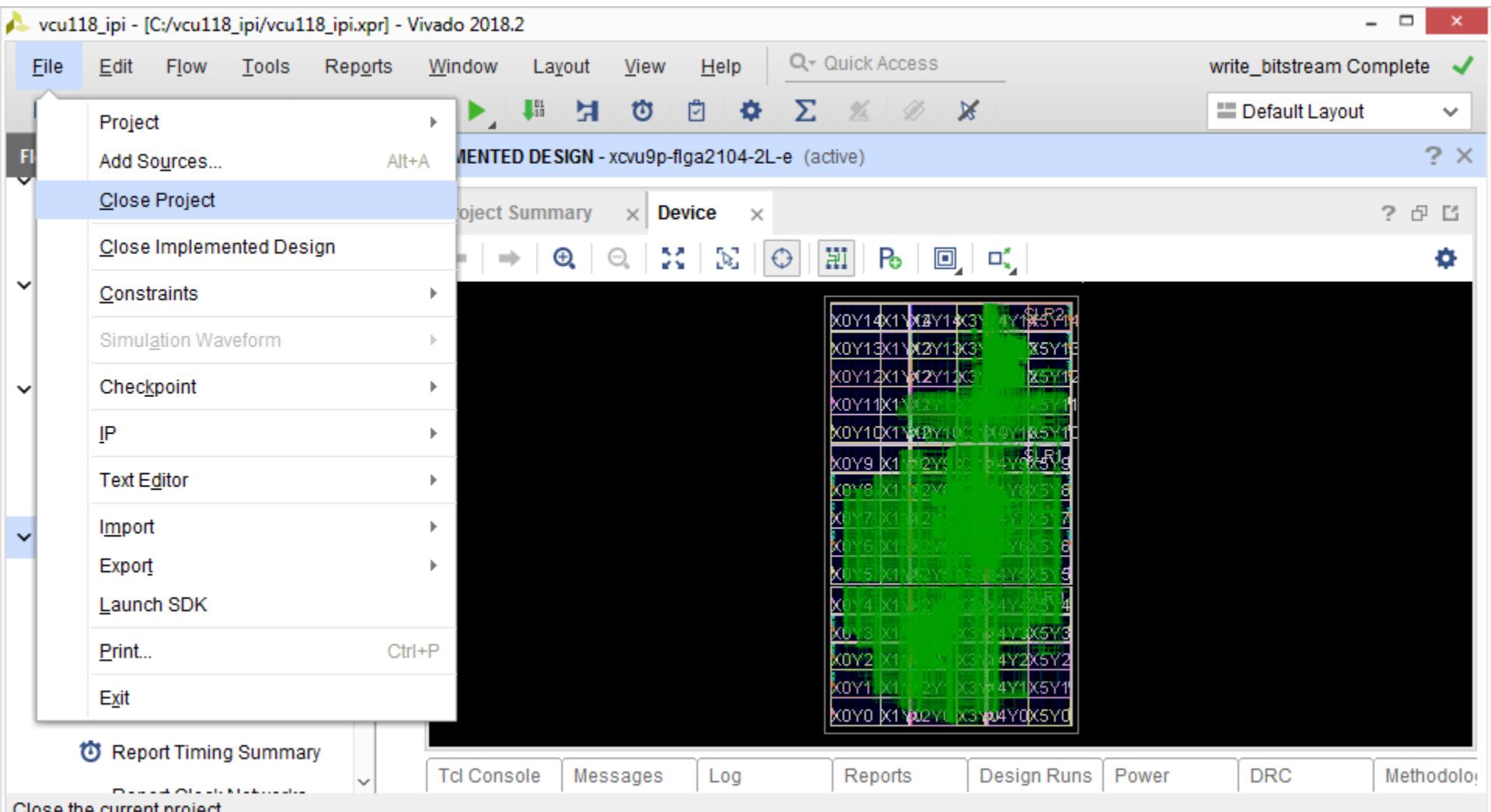
At the bottom left, it says "0 items selected".

Program VCU118 with IPI Design



Program VCU118 with IPI Design

> Close the Project



Note: Presentation applies to the VCU118

 XILINX

Program VCU118 with IPI Design

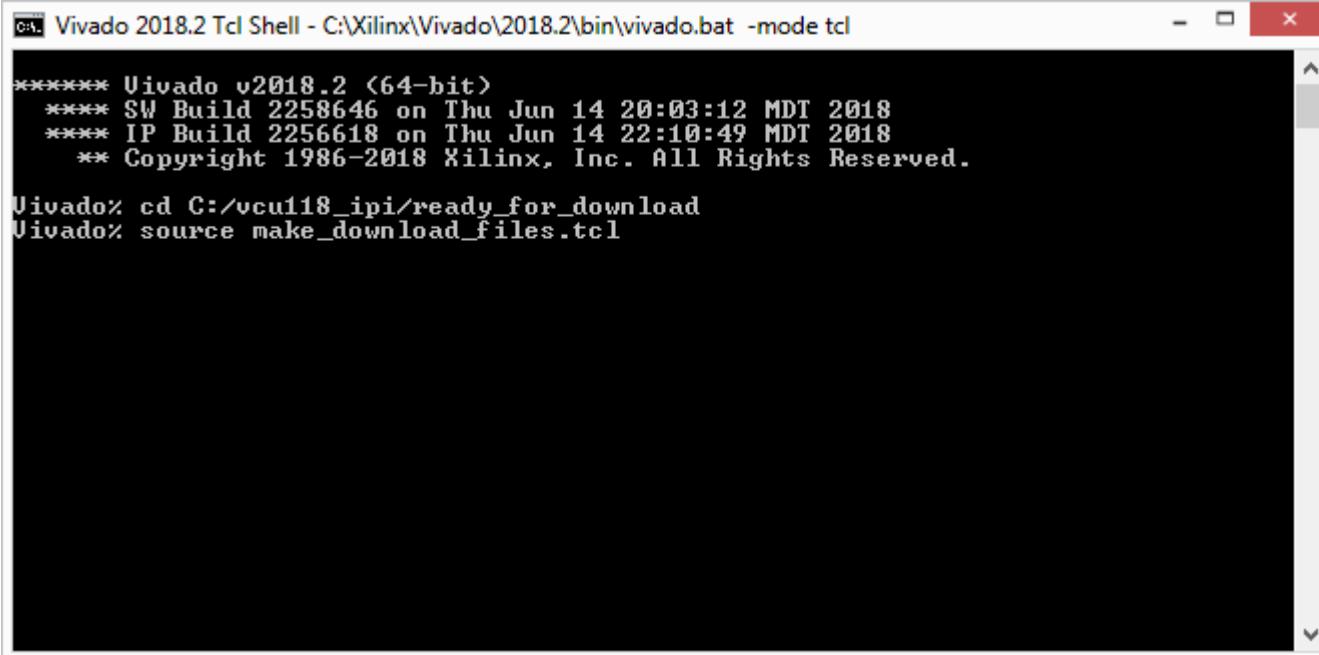
> Program the bitstreams with ELF files

> Open a Vivado Tcl shell and type:

```
cd C:/vcu118_ipi/ready_for_download
```

```
source make_download_files.tcl
```

> This script uses Tcl commands to add the ELF files to the IPI project , then generates the IPI bitstream



The screenshot shows a terminal window titled "Vivado 2018.2 Tcl Shell - C:\Xilinx\Vivado\2018.2\bin\vivado.bat -mode tcl". The window displays the following text:

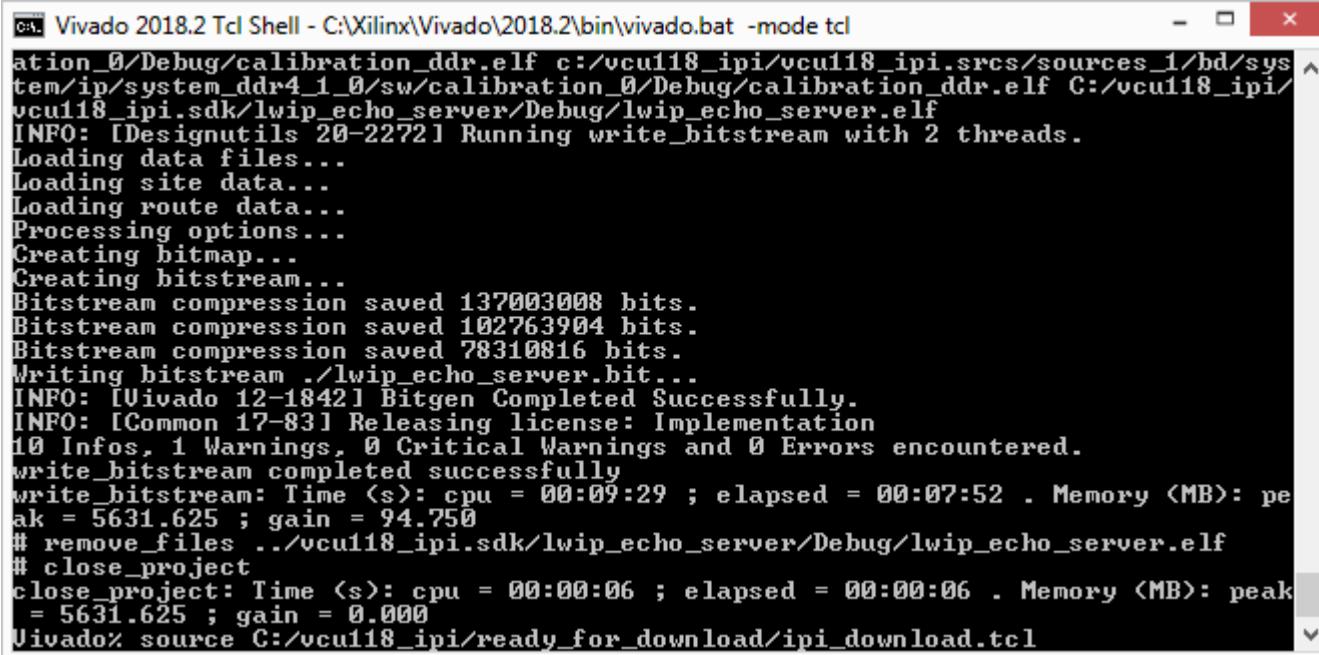
```
***** Vivado v2018.2 (64-bit)
***** SW Build 2258646 on Thu Jun 14 20:03:12 MDT 2018
***** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

Vivado> cd C:/vcu118_ipi/ready_for_download
Vivado> source make_download_files.tcl
```

Program VCU118 with IPI Design

- > Download the IPI bitstream
- > In the Vivado Tcl Shell type:

```
source C:/vcu118_ipi/ready_for_download/ipi_download.tcl
```

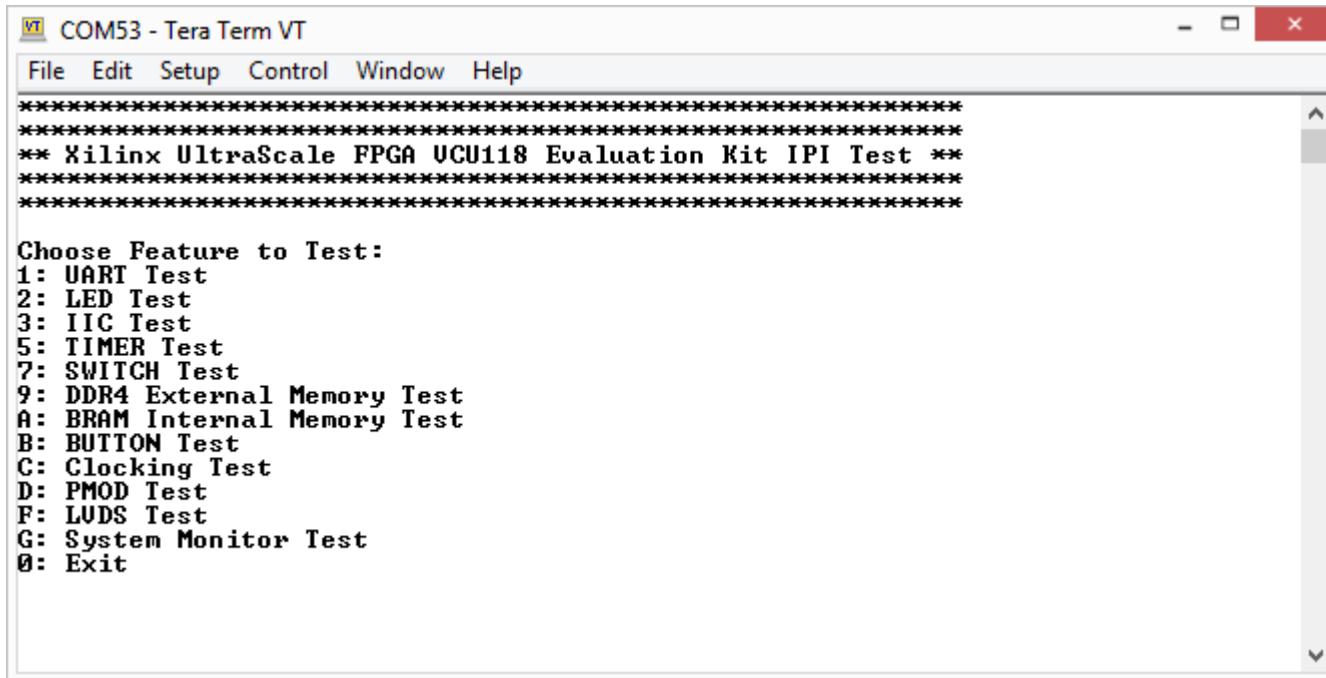


The screenshot shows a terminal window titled "Vivado 2018.2 Tcl Shell - C:\Xilinx\Vivado\2018.2\bin\vivado.bat -mode tcl". The window displays the output of a Tcl script named "ipi_download.tcl". The script performs several tasks: it sources a configuration file, loads data files, processes options, creates a bitmap, and generates a bitstream. It then compresses the bitstream and writes it to a file named "lwip_echo_server.bit". The process is completed successfully, with no errors or critical warnings. Finally, the script removes the temporary file and closes the project.

```
action_0/Debug/calibration_ddr.elf c:/vcu118_ipi/vcu118_ipi.srcs/sources_1/bd/system/ip/system_ddr4_1_0/sw/calibration_0/Debug/calibration_ddr.elf C:/vcu118_ipi/vcu118_ipi.sdk/lwip_echo_server/Debug/lwip_echo_server.elf
INFO: [Designutils 20-2272] Running write_bitstream with 2 threads.
Loading data files...
Loading site data...
Loading route data...
Processing options...
Creating bitmap...
Creating bitstream...
Bitstream compression saved 137003008 bits.
Bitstream compression saved 102763904 bits.
Bitstream compression saved 78310816 bits.
Writing bitstream ./lwip_echo_server.bit...
INFO: [Vivado 12-1842] Bitgen Completed Successfully.
INFO: [Common 17-831] Releasing license: Implementation
10 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
write_bitstream completed successfully
write_bitstream: Time <s>: cpu = 00:09:29 ; elapsed = 00:07:52 . Memory <MB>: peak = 5631.625 ; gain = 94.750
# remove_files ..../vcu118_ipi.sdk/lwip_echo_server/Debug/lwip_echo_server.elf
# close_project
close_project: Time <s>: cpu = 00:00:06 ; elapsed = 00:00:06 . Memory <MB>: peak = 5631.625 ; gain = 0.000
Vivado% source C:/vcu118_ipi/ready_for_download/ipi_download.tcl
```

Program VCU118 with IPI Design

- > IPI Application runs in the terminal window



The screenshot shows a terminal window titled "COM53 - Tera Term VT". The window has a menu bar with "File", "Edit", "Setup", "Control", "Window", and "Help". The main content area displays the following text:

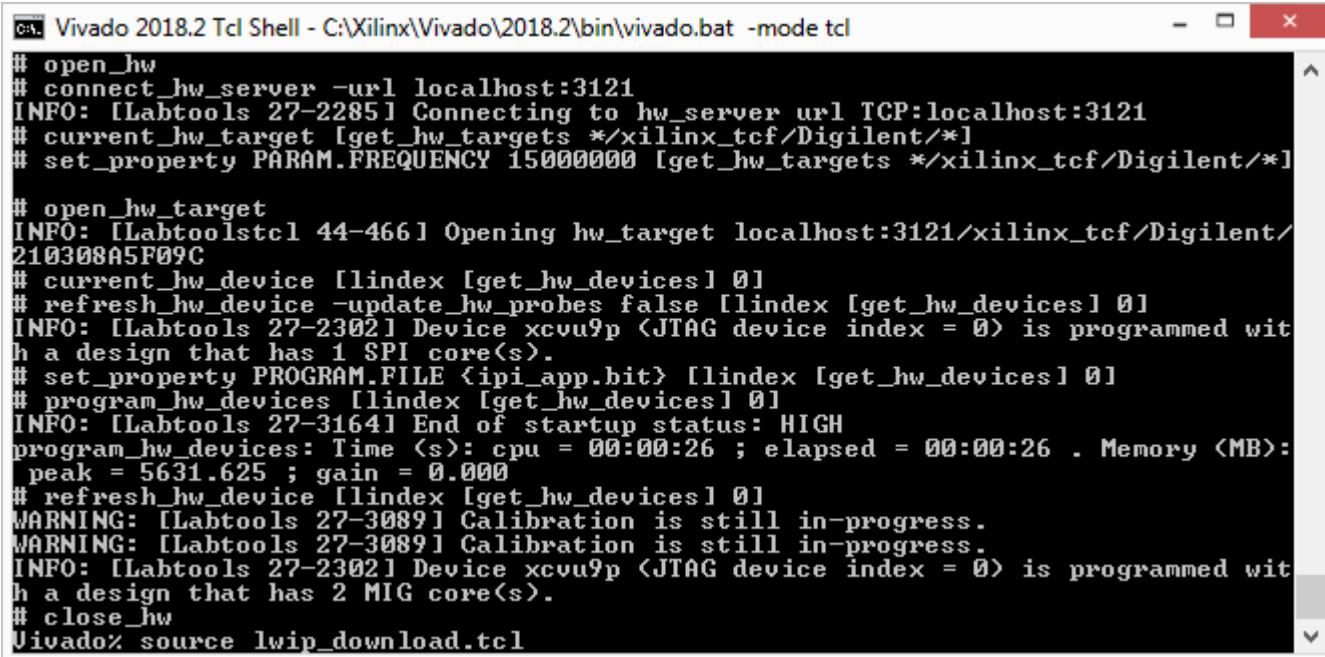
```
*****
** Xilinx UltraScale FPGA VCU118 Evaluation Kit IPI Test **
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: IIC Test
5: TIMER Test
7: SWITCH Test
9: DDR4 External Memory Test
A: BRAM Internal Memory Test
B: BUTTON Test
C: Clocking Test
D: PMOD Test
F: LVDS Test
G: System Monitor Test
0: Exit
```

Run the LwIP Ethernet Design



Run the LwIP Ethernet Design

- > Download the LwIP bitstream
- > In the Vivado Tcl Shell type:
`source lwip_download.tcl`

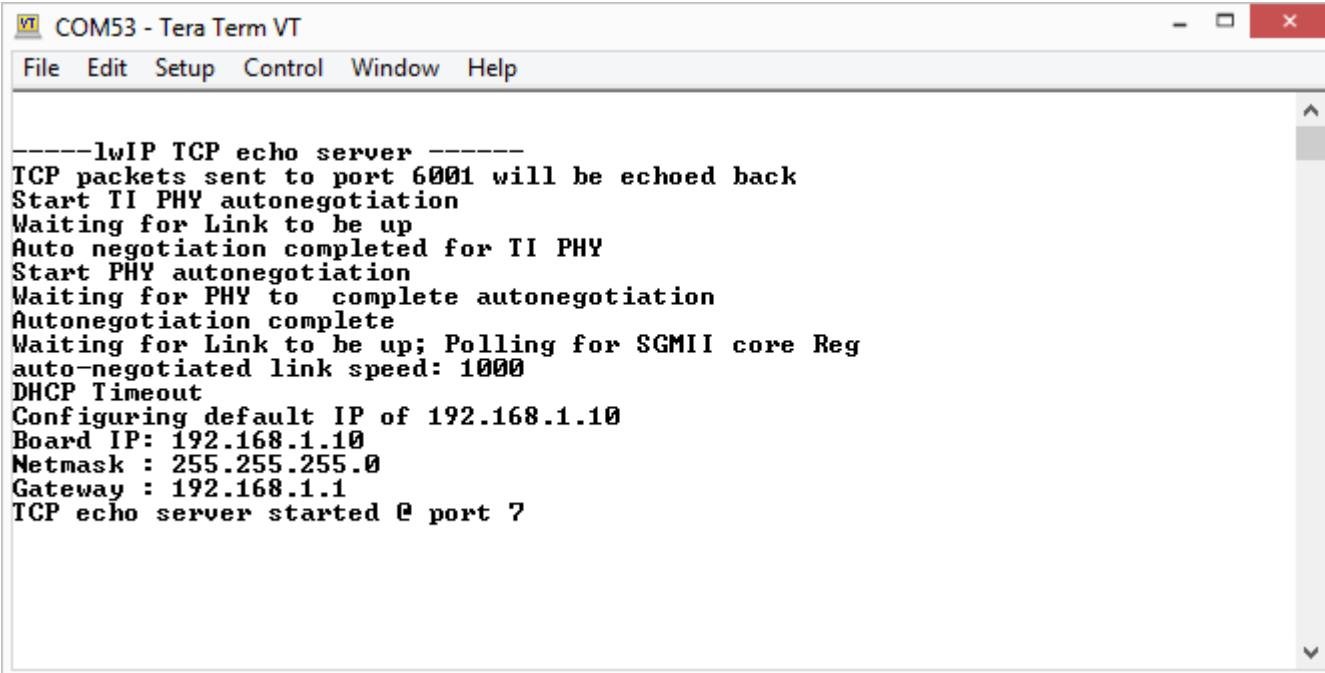


```
# open_hw
# connect_hw_server -url localhost:3121
INFO: [Labtools 27-2285] Connecting to hw_server url TCP:localhost:3121
# current_hw_target [get_hw_targets */xilinx_tcf/Digilent/*]
# set_property PARAM.FREQUENCY 15000000 [get_hw_targets */xilinx_tcf/Digilent/*]

# open_hw_target
INFO: [Labtools 44-466] Opening hw_target localhost:3121/xilinx_tcf/Digilent/
210308A5F09C
# current_hw_device [lindex [get_hw_devices] 0]
# refresh_hw_device -update_hw_probes false [lindex [get_hw_devices] 0]
INFO: [Labtools 27-2302] Device xcvu9p (JTAG device index = 0) is programmed with
a design that has 1 SPI core(s).
# set_property PROGRAM.FILE {ipi_app.bit} [lindex [get_hw_devices] 0]
# program_hw_devices [lindex [get_hw_devices] 0]
INFO: [Labtools 27-3164] End of startup status: HIGH
program_hw_devices: Time <s>: cpu = 00:00:26 ; elapsed = 00:00:26 . Memory <MB>:
peak = 5631.625 ; gain = 0.000
# refresh_hw_device [lindex [get_hw_devices] 0]
WARNING: [Labtools 27-3089] Calibration is still in-progress.
WARNING: [Labtools 27-3089] Calibration is still in-progress.
INFO: [Labtools 27-2302] Device xcvu9p (JTAG device index = 0) is programmed with
a design that has 2 MIG core(s).
# close_hw
Vivado% source lwip_download.tcl
```

Run the LwIP Ethernet Design

- > View LwIP echo server screen



The screenshot shows a terminal window titled "COM53 - Tera Term VT". The window has a menu bar with File, Edit, Setup, Control, Window, and Help. The main pane displays the following text:

```
----lwIP TCP echo server ----
TCP packets sent to port 6001 will be echoed back
Start TI PHY autonegotiation
Waiting for Link to be up
Auto negotiation completed for TI PHY
Start PHY autonegotiation
Waiting for PHY to complete autonegotiation
Autonegotiation complete
Waiting for Link to be up; Polling for SGMII core Reg
auto-negotiated link speed: 1000
DHCP Timeout
Configuring default IP of 192.168.1.10
Board IP: 192.168.1.10
Netmask : 255.255.255.0
Gateway : 192.168.1.1
TCP echo server started @ port 7
```

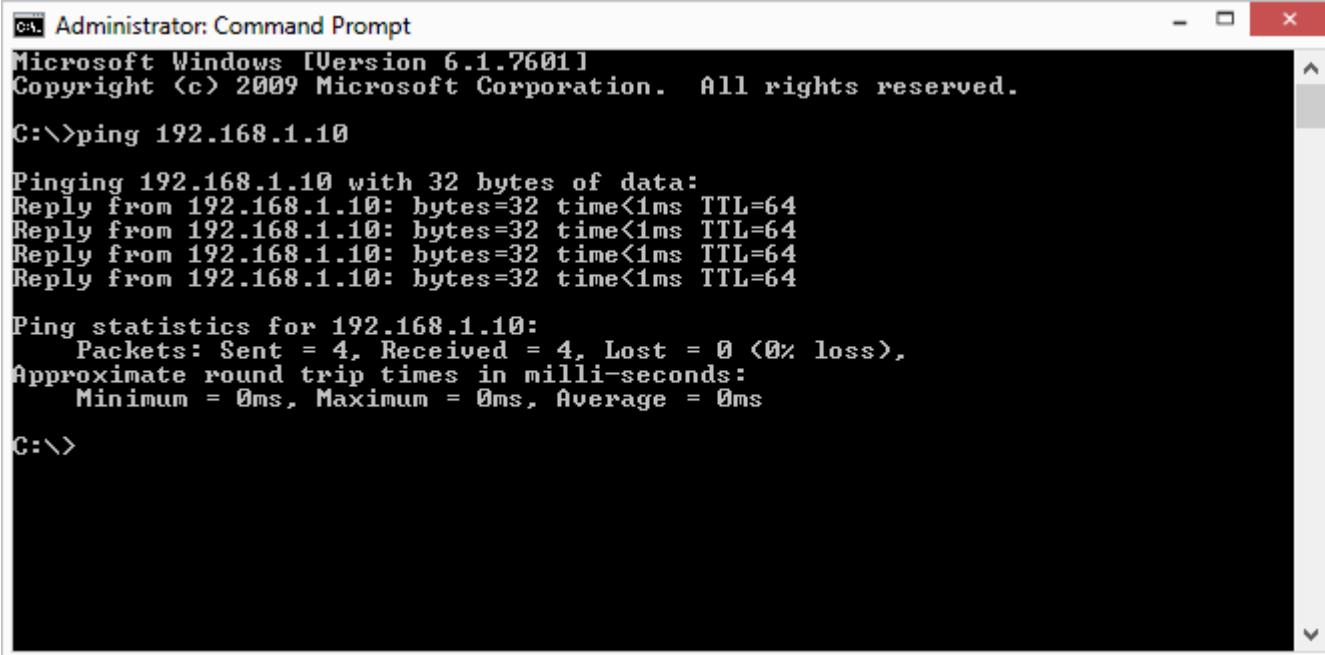
Note: Kit includes Crossover Ethernet cable; must use non-Crossover Ethernet cable for 1000 Mbps operation

Run the LwIP Ethernet Design

- > From a DOS window on the PC Host, enter the command:

ping 192.168.1.10

- » Ping from PC host 192.168.1.2 to KCU105 target 192.168.1.10



```
C:\>Administrator: Command Prompt
Microsoft Windows [Version 6.1.7601]
Copyright <c> 2009 Microsoft Corporation. All rights reserved.

C:>ping 192.168.1.10

Pinging 192.168.1.10 with 32 bytes of data:
Reply from 192.168.1.10: bytes=32 time<1ms TTL=64

Ping statistics for 192.168.1.10:
    Packets: Sent = 4, Received = 4, Lost = 0 (0% loss),
    Approximate round trip times in milli-seconds:
        Minimum = 0ms, Maximum = 0ms, Average = 0ms

C:>
```

Note: Don't ping LwIP while it is initializing

References



References

> Vivado Release Notes

- » Vivado Design Suite User Guide - Release Notes – UG973
 - https://www.xilinx.com/support/documentation/sw_manuals/xilinx2019_1/ug973-vivado-release-notes-install-license.pdf
- » Vivado Design Suite 2019 - Vivado Known Issues
 - <https://www.xilinx.com/support/answers/72162.html>

> IP Integrator Documentation

- » Vivado Design Suite Tcl Command Reference Guide – UG835
 - https://www.xilinx.com/support/documentation/sw_manuals/xilinx2019_1/ug835-vivado-tcl-commands.pdf
- » Designing IP Subsystems Using IP Integrator – UG994
 - https://www.xilinx.com/support/documentation/sw_manuals/xilinx2019_1/ug994-vivado-ip-subsystems.pdf

> UltraScale Configuration

- » UltraScale Architecture Configuration User Guide – UG570
 - https://www.xilinx.com/support/documentation/user_guides/ug570-ultrascale-configuration.pdf

Documentation



Documentation

- > **Virtex UltraScale+**
 - » Virtex UltraScale+ FPGA Family
 - <https://www.xilinx.com/products/silicon-devices/fpga/virtex-ultrascale-plus.html>
- > **VCU118 Documentation**
 - » Virtex UltraScale+ FPGA VCU118 Evaluation Kit
 - <https://www.xilinx.com/products/boards-and-kits/vcu118.html>
 - » VCU118 Board User Guide – UG1224
 - https://www.xilinx.com/support/documentation/boards_and_kits/vcu118/ug1224-vcu118-eval-bd.pdf
 - » VCU118 Evaluation Kit Quick Start Guide User Guide – XTP453
 - https://www.xilinx.com/support/documentation/boards_and_kits/vcu118/xtp453-vcu118-quickstart.pdf
 - » VCU118 - Known Issues and Release Notes Master Answer Record
 - <https://www.xilinx.com/support/answers/68268.html>