Small-Chip Report

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We constructed a small superconducting quantum chip with four transmon qubits and conducted simulations and analysis. Here, we present the work we have done regarding the chip.

Device design: The superconducting chip consists of several Transmon qubits, coplanar waveguides, charge lines, and a few launchpads for the input and output of RF signals. The Transmon qubits are arranged in a symmetric, rhombus-like pattern on the chip. Each qubit is interconnected via coplanar waveguides (CPW), and each Transmon is connected to two other Transmons through these waveguides. We have custom-made charge lines that are capacitively coupled to each Transmon, allowing for the control and manipulation of the qubit states. These charge lines typically use capacitive coupling, and their electrical signals influence the energy levels of the qubits. This enables qubit control, frequency tuning, and initialization, and helps to reduce charge sensitivity. Each Transmon is connected to a readout system, which in turn is linked to a V-launchpad. This launchpad facilitates the connection of the chip to external measurement equipment.

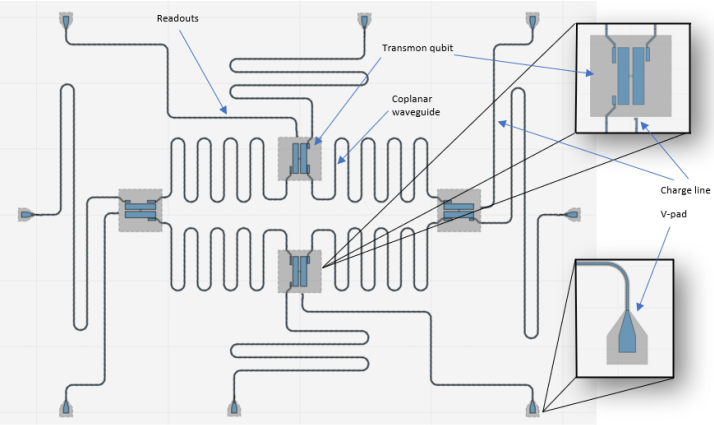

Figure 1: Labeled diagram of superconducting chip

Certain analyses have been done on Ansys HFSS which shows how the superconducting chip interacts with the microwave signals or electromagnetic waves.

Simulations

- EPR Analysis
- Capacitance Analysis
- S-Parameter Analysis

EPR Analysis: It is a method based on Energy participation ratio (EPR) used for quantizing multiple dissipative or non-linear elements (e.g. Josephson junction) in a superconducting circuit device. The EPRs obey universal constraints and are calculated from one electromagnetic eigenmode simulation. We performed an eigenmode simulation of the above 'Small-Chip' using Ansys HFSS and extracted the EPR-related data using the **pyEPR module** and **Qiskit-Metal**. For the eigenmode simulation, we have taken 12 modes, based on the number of CPW resonators

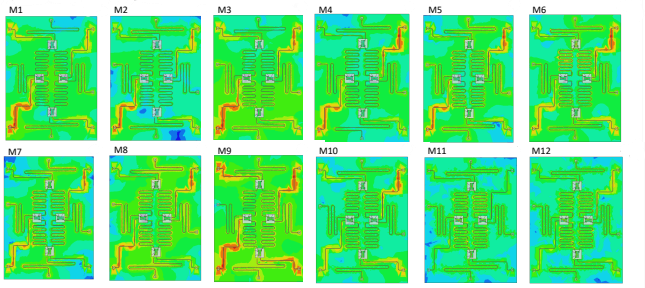

Figure 2: Eigenmode simulations of Small-Chip

used in the chip. The V-pads are designed as lumped ports with 50Ω resistance with an integration line, connected to charge lines via CPW. We also conducted an H-field simulation to recognize which mode corresponds to each element of the chip and to identify the optimal mode frequency for efficient chip operation. Figure 2 represents all 12 modes of H-field profiles and their interaction with CPW resonators on the chip. Mode 9 (M9) interacts more with charge lines among others, indicating the optimized mode or frequency (5.7826GHz) at which we can efficiently take control of the chip or we can say easily manipulate the qubit's states to have the desirable output. Although other modes resonate with other resonators, describing their resonance frequencies, we are not mentioning the description of each mode here. The EPR-related data is shown in Table 1. From the data we can say that all the modes with any of the junctions have a higher value of EPR, either a hybrid mode or a resonator mode, and modes with lesser values of EPR might be a qubit mode. From the data, I could say Modes: M3, M4, M5, M6 may be resonator or hybrid ones and M0, M1, M2, and M3 may be qubit modes. The above picture represents all 12 modes of H-field profiles and their interaction with coplanar waveguide resonators on the chip. Mode 9 (M9) interacts more with charge lines among others, indicating the optimized mode or frequency (5.7826GHz) at which we can efficiently take control over the chip or we can say easily manipulate the qubit's states to have the desirable output. Although other modes resonate with other resonators, describing their resonance frequencies, we are not mentioning the description of each mode here. The EPR-related data is shown in **Table 1**. From the data we can say that all the modes with any of the junctions have a higher value of EPR, either a hybrid mode or a resonator mode, and modes with lesser values of EPR might be qubit modes. From the data, I could say Modes: M3, M4, M5, M6 may be resonator or hybrid ones and M0, M1, M2, and M3 may be qubit modes.

Mesh analysis: The software employs the finite element method to solve Maxwell's equations, which govern the electromagnetic field. This approach involves meshing, where the software divides the design into several geometries known as mesh cells. Each cell has an E-field strength, and the software solves the Maxwell equations for these cells

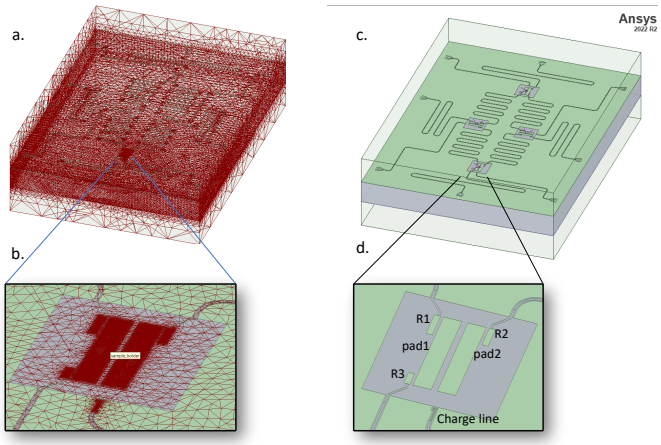

Figure 3: (a)The mesh cell generated after the simulation. (b) The Mesh for Transmon Qubit-1. (c) The chip rendered in Ansys on silicon base (c) Transmon Qubit-1

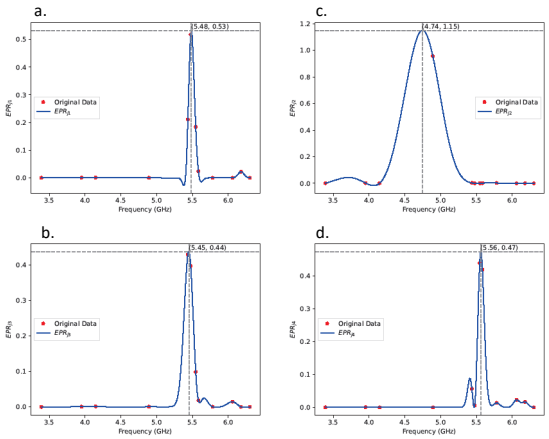

Figure 4: Plots of EPR of JJs vs Frequency

to predict the electric field as measured in real life. After each simulation pass, the software reduces the sizes of the cells, resulting in distinct outcomes derived from different mesh cells. To compute the change in frequency, each result is compared with the preceding one to determine the Max Delta Frequency (%). The simulation continues until this change converges to the target value of Max Delta Frequency per pass. The process concludes when the Delta function meets the target, unless the Minimum Number of Passes and Minimum Converged Pass in the setup are assigned values other than 1.
Here we have mentioned certain mesh parameters e.g **Maximum Number of Passes**:10, **Minimum Number of Passes**:1, **Target**:0.02, **Completed Mesh number of passes**:6.

We have also plotted the EPR vs modal frequency graph for each transmon qubit in Figure 4.

Capacitance Analysis: Capacitance analysis was conducted using Q3D Extractor in Ansys, focusing on Transmon Qubit-1 as shown in Figure 3. For analysis, all the Josephson Junction or all inductive elements were removed, and **Boundaries** were assigned to pads, connecting pads, and charge lines (Material: Copper with a thickness:1mm). **Nets** were assigned to all components mentioned.. pads: pad1, pad2—connecting pads: R1, R2, R3— charge line: chargeline. The labeled diagram is shown in Figure 3(c)

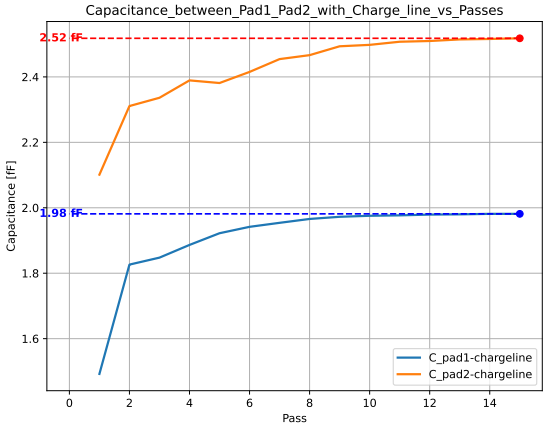

Figure 5: Plot of capacitance in between pad1 with charge line and pad2 with charge line

The capacitance analysis revealed that the results were frequency-independent, with consistent plots for solution frequencies of 1 GHz and 5.7826 GHz. Some Q3D extractor parameters are mentioned here: **Adaptive passes** in Setup: Percentage Error:0.5 – Minimum Converged Passes:2 – Maximum Number of Passes:10 – and Minimum Number of Passes:2.
Upon further analysis, we generated the capacitance matrix **Table 2** and plots that depict the variation in capacitance between the pads and the pads & charge line as the number of simulation passes increases (Figure 4). These graphs demonstrate that the capacitance converges to a specific value after a certain number of passes. This converged value will be used for the calculation of additional parameters.

We also analyzed the capacitance plots between R_i (where i=1,2,3) and the pads, as shown in Figure 5. The saturation values indicated in the graph align closely with the capacitance matrix presented in Table 2

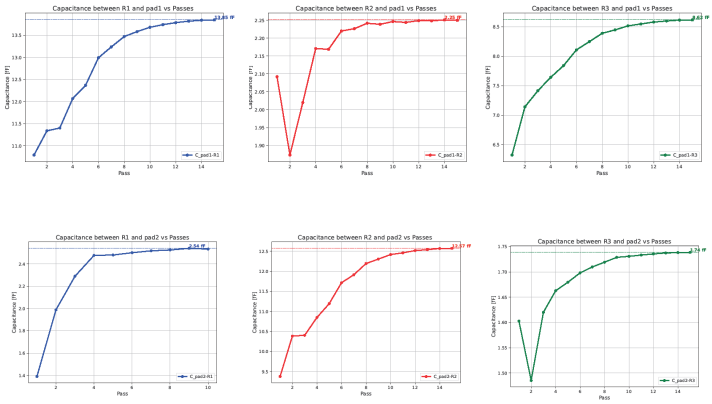

Figure 6: Plots of Capacitance in between R_i, i=1,2,3 and Pad1 and pad2

By performing Capacitance analysis, we can determine the value of E_c for the Josephson junction and track its change with the number of simulation passes. The formula for E_c is given by

$$E_C = \frac{e^2}{2C_\Sigma} \tag{1}$$

Here C_Σ represents the capacitance in between the pad1

and pad2, which can be evaluated as

$$C_{\sum} = C_{\sum_{pad1}} + C_{\sum_{pad2}} \tag{2}$$

$$C_{\sum_{pad1}} = C_{pad1,pad1} + \sum_{i \neq j} C_{ij} \tag{3}$$

$$C_{\sum_{pad2}} = C_{pad2,pad2} + \sum_{i \neq j} C_{ij} \tag{4}$$

Here i, j refer to R1, R2, R3, pad1, pad2, chargeline. We plotted the Josephson junction capacitance energy, E_c, against the number of passes. This variation in the number of passes corresponds to changes in the capacitance between the components of Qubit-1. To create a continuous curve for E_c versus passes, we performed cubic-spline interpolation. The approximate value of E_c, as indicated in the graph, is around 0.0015 meV, showing slight oscillations as it converges.

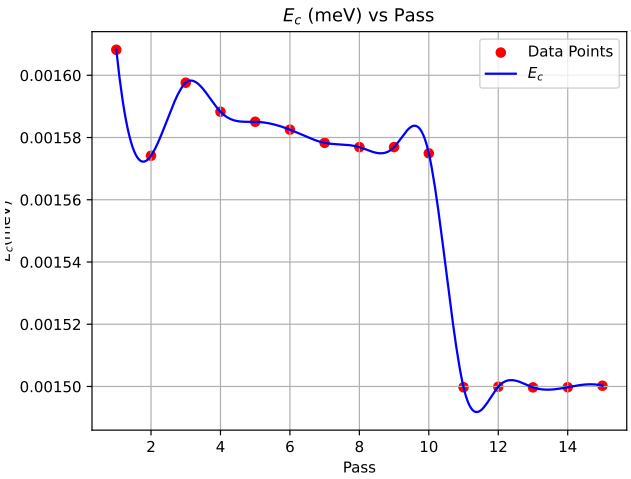

Figure 7: Plot of E_c (meV) vs passes

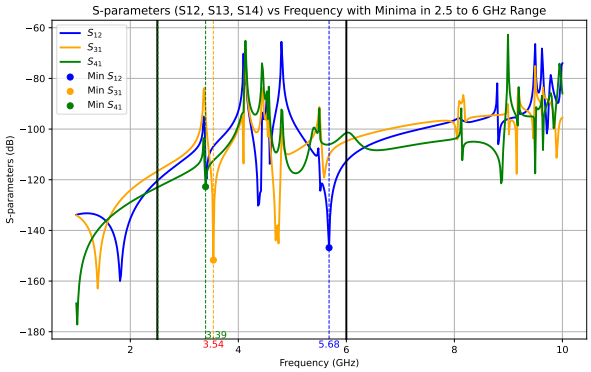

Figure 8: Plot of S-parameters (S12, S13, S14) vs Frequency

S-Parameter analysis: We have performed S-Parameter analysis using **Modal Network** simulation type in Ansys HFSS for the whole chip. We have implemented 50Ω ports at the end of each charge line with an integration line defined on the ports from the ground to the ends of the transmission line to show the signal's path. Then we have plotted S_{ij}-Parameter curves, where i, j=1,2,3, describing the RF signal behavior with circuit components when the signal is given as input from j-th port terminal to have output at i-th port terminal. As modal frequencies are approximately in the range of 3GHz to 7GHz, that's why in the S-parameter graph we have restricted our frequency domain from 2.5GHz to 6GHz. Let's take the curve S_{12} in Figure 7, the peak is a little bit deeper, which means the involvement of qubit-2 with qubit-1 is quite sufficient to affect each other state, however in a multi-qubit chip, we want to control each qubit individually so far as to control and measure each qubit separately. In my opinion, although there will always be some interaction between qubit-qubit systems, still, we can change certain parameters such that the dip can be made smaller. So similar analyses can be done for S_{12}, S_{13}, S_{14} curves, and as mentioned above it should be feasible with small dips.
Further, we can also find coupling strength from the curves which shows how much an element of a chip can interact with another element. Also, the Active S-parameter can be plotted using HFSS (Modal Network simulation) which describes the interaction of the microwave signals with the qubit which would be the qubit's state-specific, which means we can show different peaks corresponding to different states of the qubit ($|g>$ or $|e>$). For this analysis, lumped ports have been defined on the end-edge of the charge line, and the readout with 50Ω impedance with an integration line serves the direction of microwave signals.

Currently, I am conducting further analysis of this chip, focusing on how geometrical parameters affect the maximum coupling strength, increase qubit coherence times, reduce dielectric losses, and influence the dependence of E_c and E_J. My goal is to integrate a Purcell filter into the chip to reduce qubit-qubit coupling, enabling better control over each individual qubit.

Data extracted from simulations

Table 1: EPRrelated data of Small-Chip

Index	freq_GHz	j1	j2	j3	j4
0	3.3893	2.37×10^{-5}	8.88×10^{-4}	8.23×10^{-6}	1.36×10^{-4}
1	3.9495	6.23×10^{-4}	1.62×10^{-3}	4.29×10^{-4}	7.85×10^{-4}
2	4.1457	1.00×10^{-3}	3.07×10^{-4}	1.32×10^{-3}	4.51×10^{-6}
3	4.8906	1.46×10^{-4}	0.956	3.51×10^{-4}	1.10×10^{-6}
4	5.4356	0.211	2.46×10^{-3}	0.429	5.62×10^{-2}
5	5.4751	0.518	4.92×10^{-7}	0.396	6.42×10^{-3}
6	5.5450	0.184	3.37×10^{-5}	9.84×10^{-2}	0.440
7	5.5828	2.39×10^{-2}	1.18×10^{-3}	1.83×10^{-2}	0.420
8	5.7826	9.82×10^{-5}	2.31×10^{-3}	2.33×10^{-4}	1.38×10^{-2}
9	6.0600	5.41×10^{-5}	4.80×10^{-6}	1.44×10^{-2}	2.31×10^{-2}
10	6.1780	2.22×10^{-2}	4.08×10^{-6}	2.01×10^{-5}	1.68×10^{-2}
11	6.3018	3.18×10^{-4}	4.11×10^{-5}	6.85×10^{-5}	3.23×10^{-5}

Table 2: Capacitance matrix of one qubit of Small-Chip

	chargeline	*pad1*	*pad2*	*R1*	*R2*	*R3*
chargeline	9.89	-1.98	-2.50	-0.23	-0.22	-0.37
pad1	-1.98	91.77	-40.72	-13.68	-2.25	-8.51
pad2	-2.50	-40.72	86.15	-2.53	-12.42	-1.73
R1	-0.23	-13.68	-2.53	22.68	-0.41	-0.31
R2	-0.22	-2.25	-12.42	-0.41	20.57	-0.18
R3	-0.37	-8.51	-1.73	-0.31	-0.18	14.84