PROJECT REPORT

PROBLEM STATEMENT

A standard master combination lock has a dial with the numbers 0 to 39 on it. It works as follows. You reset it by spinning it

clockwise past 0 a few times. Then you turn it ant-iclockwise to the first number in the combination, positioning the dial so that the

number is directly under the arrow. Then you spin the dial clockwise again, past 0 once, to the second number of the combination.

Finally you spin the dial anti-clockwise a second time directly to the last number of the combination. At this point the lock will open. Design the logic for this system.

Top Level Block Diagram

Anticlockwise Clockwise Clockwise Converter (ADC) Clock Master Combination Lock Lock Status Two 7 segment LED displays LED displays

Inputs and Outputs.

There are three button inputs in the circuit. Anti-Clockwise, Clockwise and Lock. The outputs in the circuit are two 7-Bit LED displays to display the numbers being entered and one LED which shows if the lock is locked or unlocked.

- 1. The clockwise button is used to rotate the dial in a clockwise direction.
- 2. The anti-clockwise button is used to rotate the dial in an anticlockwise direction.

3. The lock button is used to lock and reset the circuit provided it is unlocked.

Assumptions:

- 1. We are considering a seven bit binary number (say $A_6A_5A_4A_3A_2A_1A_0$) for our lock combination.
- 2. Here, the MSB, i.e. A_6 denotes the sense of rotation (0 for clockwise, 1 for anti-clockwise)
- 3. The next two bits, i.e. A_5A_4 denotes the first digit of the number entered on the Master Combination Lock. (00 for 0, 01 for 1, 10 for 2, 11 for 3).
- 4. The next 4 bits, i.e. $A_3A_2A_1A_0$ denote the second digit of the number entered on the Master Combination Lock. (0000 for 0,0001 for 1,0010 for 2,0011 for 3,0100 for 4,0101 for 5,0110 for 6,0111 for 7,1000 for 8,1001 for 9). The rest are essentially don't- care conditions since our circuit doesn't use them.
- 5. The Preset password is 18 11 20.

Logic For Reset:

The password the user is trying to enter can be reset by rotating past 0 in clockwise direction for 3 times. To implement this we have used 17-bit comparator, 1-2 bit comparator and one 2-bit counter.

One input to the 7 bit comparator is fixed to 0000000 and the other input is the number entered to the lock by the user. If the user crosses 0 clockwise, the o/p to the comparator becomes 1 and is fed to the counter. The output of the counter are the two bits which are connected to a two input and gate which detects when the value of counter goes to 3. When the value of the counter goes to 3,the o/p of the AND gate becomes 1 which is used as the reset signal and is given to various components in the circuit as asynchronous reset.

Functionality:

There is one 4 bit counter for the digit in units place and one 2 bit counter for the digit in tens' place. The first counter is a mod 10 up down counter that counts from 0 to 9, for the digit in ones' place. The second counter is a mod 4 up down counter

that counts from 0 to 3 for the digit in tens' place. The second counter (tens' place) counts up when we go clockwise and the digit in the previous counter is 9 i.e. 1001 and counts down when we go anticlockwise and the digit in the previous counter is 0 i.e. 0000. To check that the digit is 9 and 0 in the previous counter we used 1 4bit NOR gate (for 0) and 1 2bit AND gate (for 9). The outputs of the counters are connected to 2 hex digit displays to display the current location in the lock wheel.

There is a D flip flop which stores the sense of rotation, i.e. if the movement is anticlockwise it stores a 1 and for clockwise it stores a 0. This is given to the MSB of the combination entered by the user as explained in the assumptions section.

There is a 3-bit MOD 5 counter which keeps track of the number of digits matched with the preset password. Initially the value of the counter is set to 0. The output of this counter is given as select lines to a 4:1 MUX which contains the preset password. The output of this MUX is given to a 7 bit comparator. The input combination of the lock entered by the user is also sent as an input to this comparator. When the output of the above mentioned counter is 0, the 0th input in MUX gets selected and is compared with the input. When the output of the counter is 1, the 1st input of the MUX gets selected and so on. When the 3rd input gets matched, the counter goes to 4 which is also the condition of the lock being unlocked.

In order to check if the inputs are being given from the correct directions, 2 D-FFs are used, one that activates on a rising edge, and the other on a falling edge and are fed the output of the comparator as the clock. Through this, the values of the direction of rotation at the time of the match and the next direction are saved, and are checked if they move in the opposite direction for the first and the second number through a 4:1 MUX. After the first number is matched, it checks if there was a direction change when reaching 0 in clockwise direction and then checks the second number, and then matches the last number to unlock the lock.

The first and third inputs to the MUX compare the present and previous directions and check if they move in the opposite direction when the number matches the respective key. And the last input to the MUX is the output of the comparator as the lock opens automatically when the last number is reached.

If the password entered has gone beyond the current password while going the clockwise or anticlockwise direction i.e. if password is 34 and we moved beyond it to 33 or less or if the password is 4 and user goes beyond 4, the lock will not open even if the user goes back and tries to enter the correct password and as a result they have to reset the circuit and start again.

For ensuring this condition we connected the output of the comparator and the counter which counts the current correct passwords we have entered to AND, OR and NOT gates and a D flipflop.

For example

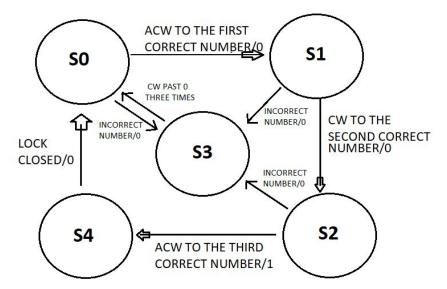
Let the passwords be 18 (anticlockwise) , 11 (clockwise) and 20 (anticlockwise). The counter is at 0 initially and the D flip flip gives output Q=0 AND Q'=1 Once we move anticlockwise to 18 and we move beyond 18 the counter becomes 1 but the comparator shows that current input is less than the password and this then changes the D flip flop output Q=1 and Q'=0 .If we change direction about 18 to clockwise the D flip flop output is not changed . Same logic is used for the second password 11 .

When we go to 11 the counter is at 2 (0 to 1 from going 18 and 1 to 2 from going beyond 0 in clockwise direction). At 11 the same conditions as above are checked i.e if we go beyond 11 and D flip flop gives output Q=1 AND Q'=0.

The Q' output and the comparator output (if the comparator gives 4) outputs are entered into an AND gate to make sure that if the user enters the wrong password initially and tries to enter the correct password right after, the circuit does not unlock and they have to reset by the reset condition mentioned. This ensure that the person cannot unlock the lock by guess work.

To reset the circuit asynchronously the user has to rotate the clock 3 times past 0 in clockwise direction. We used a 7 bit comparator (to compare that the user goes beyond 0 three times in the clockwise direction) and a counter (to count that 0 has been crossed three times) once the counter has counted till 3 (AND gate used as 3 is 11) the whole circuit resets asynchronously.

State Diagram



Here, the output 0/1 shows the lock status with 0 being locked and 1 being unlocked.

Sample Input/Output

The sample input and outputs have been screen recorded.

The google drive link for the folder is

https://drive.google.com/drive/folders/12ktRWohPYid92UyitxHJURboY7Y2oUx9?usp=sharing

Video 1: Unlocking the lock

https://drive.google.com/file/d/ISJKjaArGzTUkY9UTIoDa6Pyd0fVZvoBA/view?usp=sharing

Video 2: Incorrect Password and Resetting the lock:

https://drive.google.com/file/d/187UciwvBau2O4VONYTk4YDt-2N5F-3s1/view?usp=sharing

Video 3: Additional Features

https://drive.google.com/file/d/IGTZ0OXSRXti-TXYTO-Q5hqhU1RGAOcqm/view?usp=sharing

Additional Features

In the updated version of this master combination lock we have added the function to change the current password by the user after they have entered the correct password set by the manufacturer. Initially the manufacturer will set the password by using the clock display. After the password has been set the password is added

to the circuit for use. Once the user enters the password set by the manufacturer ,he/she can change the password of their desire.

They have to enter the password they wish to set and press the SET button for the first code to be entered and so on for the second and third password. The direction they have to move to unlock the lock still remains the same. After the passwords have been changed the user has to press the LOCK button to lock the master combination lock.

To store the password we have used 3 6bit registers for the passcodes and 3 bit extenders to ensure the direction to unlock remains the same.

Note - the password set would still have the same sense as before i.e. the first password has to be entered by going anti clockwise, the second password after crossing zero set clockwise and the final password by going anticlockwise.

Bill of Materials

S.No.	Item	Description	Qty	Unit Price	Amount
1	IC 7474	Dual D Flip Flop	2	20.00	40.00
2	IC 7432	Quad OR (2 IP)	2	18.00	36.00
3	IC 7404	Hex NOT (2 IP)	1	35.00	35.00
4	IC 7490	4 bit-Binary Counter	1	25.00	25.00
5	IC 7402	NOR (4 IP)	1	16.00	16.00
6	IC 7408	Quad AND (2 IP)	2	16.00	32.00
7	IC 7411	Triple AND (3 IP)	2	15.00	30.00
8	IC 7486	Quad XOR (2 IP)	1	14.00	14.00
9	IC 7476	Dual JK Flip Flop	1	190.00	190.00
10	IC 7449	BCD-TO-SEVEN-SEGME NT DECODERS	2	34.00	68.00
11	IC 7493	4 bit- Decade Counter	2	50.00	100.00
12	IC 74688	8 Bit Comparator	1	54.00	54.00
13	IC 74153	Dual 4:1 MUX	3	15.00	30.00
14	IC 7485	4 Bit Comparator	2	19.00	38.00

Submitted By

A SOHAN REDDY	2019A7PS0168G	
UDAY DHAL	2019A8PS0406G	
ADITYA JAIN	2019A3PS1102G	
VARNIT JAIN	2019A3PS0468G	
ANOUSHKA PARWANI	2019A8PS0273G	
KUSHAGRA GOYAL	2019A3PS0515G	