CBCS SCHEME

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17CS32

Third Semester B.E. Degree Examination, Dec.2018/Jan.2019
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain construction and working principle of operations of n-channel D-MOSFET along with its drain and trans-conductance characteristics. **(10 Marks)**

b. Write the difference between JEFT's and MOSFET's. **(05 Marks)**

c. For a given self-bias configuration in Fig.Q.1(c), determine i) I_{d_Q} and $V_{gs_{eq}}$ ii) V_{ds} and V_D. **(05 Marks)**

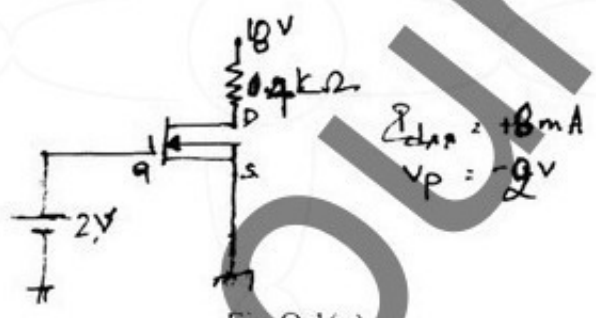

Fig.Q.1(c)

OR

2 a. List of differences between ideal and practical op-amp amplifier. **(06 Marks)**

b. With a neat diagram and waveform explain astable multivibrator using 555 timers. **(07 Marks)**

c. With neat diagram and waveform explain the working of relaxation oscillation oscillator. **(07 Marks)**

Module-2

3 a. Explain positive and negative logic. List the equivalence between them. **(08 Marks)**

b. Find the minimal SOP form for the given min-terns using K-map.
$F(A, B, C, D) = \sum m(4, 5, 6) + d(10, 12, 13, 14, 15)$. **(06 Marks)**

c. Find the minimal POS form for the given MAX-TERM using K-map.
$f(a, b, c, d) = \pi M(5, 7, 8, 9, 12) + d(0, 6, 10, 15)$. **(06 Marks)**

OR

4 a. Using Quine-Mc-Clusky method simplify the following Boolean equation.
$f(a, b, c, d) = \sum m(0, 1, 10, 11, 13, 15) + d(2, 3, 12, 14)$. **(10 Marks)**

b. Define Hazard. Explain different types of Hazards. **(06 Marks)**

c. Write the VHDL code for the circuit shown in Fig.Q.4(c): **(04 Marks)**

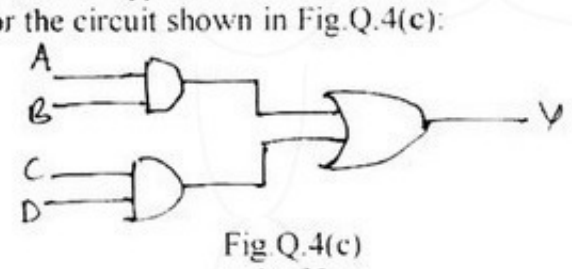

Fig.Q.4(c)

Module-3

5 a. What is multiplexers? Design 8:1 multiplexer using 2:1 multiplexers. **(08 Marks)**

b. Explain the purpose of using parity generators and checkers using suitable illustrations. **(06 Marks)**

c. What is magnitude comparator? Explain 1 bit magnitude comparator. **(06 Marks)**

OR

6 a. Design 7-segment decoder using PLA. **(06 Marks)**

b. With neat logic diagram and truth table, explain negative edge triggered J-K flip-flop. **(06 Marks)**

c. What is an Adder? Explain with truth table the half Adder, full Adder, half subtractor and full subtractor. **(08 Marks)**

Module-4

7 a. With a neat logic diagram and truth table explain the working of J-K master slave flip-flop using NAND gates. **(08 Marks)**

b. Give characteristic table, characteristic equation and excitation table for S-R, D and J-K flip-flop. **(08 Marks)**

c. Write a VHDL code for D-flip-flop. **(04 Marks)**

OR

8 a. What is a register? With neat diagram explain 4-bit parallel-in-serial out shift register. **(08 Marks)**

b. Explain with a neat diagram how a shift register can be applied for serial-addition. **(06 Marks)**

c. Differentiate between synchronous and asynchronous counters. **(06 Marks)**

Module-5

9 a. Define counter. Design a synchronous counter for the sequence, $0 \rightarrow 3 \rightarrow 1 \rightarrow 2 \rightarrow 6 \rightarrow 7 \rightarrow 0 \rightarrow 3$ using J-K flip flop. **(12 Marks)**

b. Explain with neat diagram the working principle of Digital Clock. **(08 Marks)**

OR

10 a. Explain the binary ladder with digital input of 1000. **(06 Marks)**

b. Explain 2-bit simultaneous A/D converter. **(08 Marks)**

c. Explain the terms accuracy and resolution for D/A converters. **(06 Marks)**

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