EEDG/CE 6303: Testing and Testable Design (Spring'2024)

Department of Electrical & Computer Engineering

The University of Texas at Dallas

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Cover Page for All Submissions

(Assignment, Project, Codes/Simulations/CAD, Examinations, etc.)

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Submission Materials for (e.g. Homework #, Project #): Homework 1

Statement of Academic Honesty

I certify that:

i. the attached report (for assignment, project, codes/simulations/CAD, examinations, etc.) is my own work, based on my personal study and/or research,
ii. I have acknowledged/cited all material and sources used in its preparation, whether they be books, articles, reports, lecture notes, and any other kind of document, electronic or personal communication,
iii. I have not used **generative AI (e.g. ChatGPT or similar tools)** in preparing this report,
iv. this report has not previously been submitted for assessment in EEDG/CE 6303 or any other course at UT Dallas or elsewhere,
v. I have not copied in part or whole or otherwise plagiarized the work of other students and/or persons, and
vi. I have read and understood the Department and University policies on scholastic dishonesty as outlined in: http://www.utdallas.edu/deanofstudents/dishonesty/.

Name: Uday Teja Bandaru Date: 01/30/2024

Signature: 

1. Read the article titled: Toyota Case: Single Bit Flip That Killed (available in https://www.eetimes.com/toyota□case-single-bit-flip-that-killed/). In at most one page, comment on how circuit/system testing may prevent such scenarios.

Ans:

As per the information in the article that suggests the failure in a system, even that could be a single bit flip. It is clearly stated that, if a failure occurs in the critical part of the system, that could lead to a disaster like the unfortunate incident that occurred. This failure/ errors could cost a lot in terms of losses.

Checking the reliability/safety of the product is of utmost importance. This verification should be followed from the early part of the design if the product is being built as per the specifications and as per the constraints in that product depending on the use cases.

Building the product right and building the right product is the short version to determine importance of the validating throughout the process. Functional verification, formal verifications are being performed as part of the process of product development.

By detecting the faults in the system, maybe in software or hardware by evaluating the behavior and responses, engineers can take corrective action to mitigate the failures and thereby improving the performance of the system.

2. The design and analysis (test, assessment) of electrostatic discharge (ESD) protection circuits are critical for integrated chips (IC) reliability. For IC device testing using traditional methods, various ESD pulses are applied and the analysis of their behavior (e.g., current-voltage (IV) curves) is observed to ensure reliability. Search the Internet to find an article on ESD stress assessment/testing in integrated chips. One source is the electronic databases in the UTD McDermott library (http://www.utdallas.edu/library). In your search, relevant keywords/phrases include: pre- and post- ESD stress analysis, IV curve tracing/shift, human body model (HBM) versus charged device model (CDM),

testing high-speed interfaces Transmit (TX) and Receive (RX) pins, device characterization with transmission line pulse (TLP). In at most three pages, (i) summarize the key part of the paper (e.g. model, methodology, results), (ii) explain your own opinion on using statistical analysis (that is the foundation of machine-learning approaches) for ESD stress assessment. Attach the article that you found to your report.

Ans:

1. Summary

   Usually, the ESD protection designs in ICs are time consuming and require manual interpretation of the IV curves with pre and post data. As a IC has huge quantity of hardware elements embedded in it and numerous inputs are implemented, checking the IV curves at each and every IO pins is really require huge amount of work, so this kind of tedious testing may be one of the reason for missing the market window.

   There could be many reasons why this manual testing procedure could not be certainly reliable, such as missing a critical design failure, lack of Automation test environment (ATE), not covering entire range of extreme stress parameters which in turn leads to missing PTF etc. when we have good amount of data at each and every IO(lets say) regards the all the IV characteristics and their deviation with normal behavior at extreme stresses on ICs, there are more likely to have anomalies, so usage of Machine learning algorithm clearly reduces the time that is being spent to detect the recurring patterns when it is properly trained

   Machine Learning technique require the list of classes that have deviated behavior or IV shift at the pins and when all the data is collected, we can train the model which has certain neural configurations, this generates weights and biases for each neuron in the neural network and they are ready to detect any analogies.

   For an IC pin, HBM or CDM might give a curve in IV a certain shift under a stress environment, and the behavior is documented in the paper for different outcomes such as PASS/FAIL/ICP/PTF. These data could be different for each IO pin, as their logical implementations are different, and this is the data to be collected that is required to be fed for the machine learning model. The software flow is, that the ESD tester outputs IV data and gives it to the ML environment, which is previously trained, on which under ATE product functional tests are run

where anomalies are detected and reported and again this reverts to the design phase of ESD and debug.

ML method of analysis to detect the impact of ESD stress, especially CDM, on high-speed interface pins like Tx and Rx, as well as this paper talks about analyzing data from numerous devices and correlating variations to design parameters can help establish predictive designs for on chip components.

As per the paper, the results of ML algorithm have returned a confusion matrix which has data for deducing key performance metrics and are run for both HBM and CDM pulses and PTFs are detected as expected, here the focus is put on the scope of ML in the field of Testing/ validation.

2. Opinion

Implementation of ML algorithms in analysis of ESD protection designs has huge potential to become normalized ways for circuit analysis, detecting potential failure through anomalies in the future. The scope of this can be explored as well in addition to the potential use cases which are mentioned in the paper such as post-ESD stress analysis, device characterization with TLP. As the precision of ML depends on the provided data for training and data comes from the test engineers in the manual way, this helps to mitigate the errors in the procedure and reduce the manual labor but not eliminate them and manual verification will always be needed.

Reference paper/article:

C. Middaugh, M. Nourani, C. Duvvury and J. Schichl, "ESD Stress Data Analysis with Machine Learning: A Case Study," 2023 45th Annual EOS/ESD Symposium (EOS/ESD), Riverside, CA, USA, 2023, pp. 1-9, doi: 10.23919/EOS/ESD58195.2023.10287736. keywords: {Measurement;Analytical models;Data analysis;Time to market;Machine learning;Electrostatic discharges;Data models},