The University of Texas at Dallas
Dept. of Electrical and Computer Engineering

EEDG/CE 6303: Testing and Testable Design
HW # 1: *Due on Tuesday, September 7, 2021 - 11:59 pm (US CST)*

When you submit your homeworks, to help us grade and identify your work, you need to comply with the following guidelines carefully:

- *Have* **a cover page** *for each document (e.g. homework, project, report, etc.) that you submit. A sample of cover page is provided in the course webpage. This page must include: (1) your name as it appears in your* **student ID card***, (2) course name/number, (3) homework/project number, and (4) the* **Statement of Academic Honesty** *that you sign.*

1. Chapter 1: 3, 4
2. Read this article titled: Toyota Case: Single Bit Flip That Killed (available in https://www.eetimes.com/toyota-case-single-bit-flip-that-killed/). In at most two pages, comment how testing circuits using **single-event upset (SEU) fault model** may prevent such scenarios.
3. **Reliability of circuits** has received a great deal of attention in recent years. There are many angles to reliability of integrated chips such as definition of reliability metric, impact of fabrication process, design for reliability (DFR) and long term effect. Search the Internet to find a paper on broad area of circuit's reliability. In at most two pages, summarize the key part of the paper (e.g. model, methodology, results) and your own view toward reliability of integrated chips. One rich source is the electronic databases in the UTD McDermott library (http://www.utdallas.edu/library).