The University of Texas at Dallas
Dept. of Electrical and Computer Engineering

EEDG/CE 6303: Testing and Testable Design
HW # 4: *Due on Tuesday, Nov. 2, 2021 - 11:59 pm (US CST)*

When you submit your homework, to help us grade and identify your work, you need to comply with the following guidelines carefully:

- *Have* **a cover page** *for each document (e.g. homework, project, report, etc.) that you submit. A sample of cover page is provided in the course webpage. This page must include: (1) your name as it appears in your* **student ID card***, (2) course name/number, (3) homework/project number, and (4) the* **Statement of Academic Honesty** *that you sign.*

1. Find the robust and non-robust test patterns for the following **path delay** faults in Figure 8.13: (i) $\uparrow x_3c_2c_3z$, (ii) $\downarrow x_3c_2c_3z$, (iii) $\uparrow x_1c_1c_3z$, (iv) $\downarrow x_1c_1c_3z$.

2. Find the robust and non-robust test patterns for the following **path delay** faults in Figure 8.20: (i) $\uparrow x_3c_2c_3c_4c_6z$, (ii) $\downarrow x_3c_2c_3c_4c_6z$, (iii) $\uparrow x_2c_1c_3c_5z$, (iv) $\downarrow x_2c_1c_3c_5z$.

3. Consider the above two circuits (Figures 8.13 and 8.20 and path delay faults). Use Synopsys toolset to implement the circuits and find robust and non-robust test patterns. A short guide for path delay fault testing is at the end of Test Tutorial in the course webpage. Report and discuss the results.

4. From your text, solve the following problems:
   – Chapter 14: 4, 5, 6, 7 and 8.

5. Determine if: (i) AFs, (ii) SAFs, (iii) TFs, (iv) unlinked CFs (CFin, CFid, CSst), and (v) linked CFids faults can be detected by MARCH C– test shown below.

$$\{M0 :\Updownarrow (w0); M1 :\Uparrow (r0, w1); M2 :\Uparrow (r1, w0); M3 :\Downarrow (r0, w1); M4 :\Downarrow (r1, w0); M5 :\Updownarrow (r0)\}$$

   As you know, in some categories (e.g. coupling faults), there may be multiple faults. You need to justify/prove your answer for each fault. To do this for each case, carefully tabulate which March element(s) (M_i) stimulates it and which element(s) detects it. If there are multiple scenarios to detect a particular fault, list them all.

6. Determine if: (i) AFs, (ii) SAFs, (iii) TFs, (iv) unlinked CFs (CFin, CFid, CSst), and (v) linked CFids faults can be detected by IFA-13 march test shown below.

$$\{M0 :\Uparrow (w0); M1 :\Uparrow (r0, w1, r1); M2 :\Uparrow (r1, w0, r0); M3 :\Downarrow (r0, w1, r1);$$
$$M4 :\Downarrow (r1, w0, r0); Delay; M5 :\Uparrow (r0, w1); Delay; M6 :\Uparrow (r1)\}$$

   As you know, in some categories (e.g. coupling faults), there may be multiple faults. You need to justify/prove your answer for each fault. To do this for each case, carefully tabulate which March element(s) (M_i) stimulates it and which element(s) detects it. If there are multiple scenarios to detect a particular fault, list them all.

7. Read the following paper available in *http://www.utdallas.edu/library/*. Summarize and comment on your understanding of the paper in at most 2 pages.

   S. Hamdioui, A. J. van de Goor and M. Rodgers "March SS: A Test for All Static Simple RAM Faults," in *Proceedings of the IEEE International Workshop on Memory Technology, Design and Testing (MTDT 2002)*, pp. 1-6, July 2002.