EEDG/CE 6303: Testing and Testable Design (Spring'2024)

Department of Electrical & Computer Engineering

The University of Texas at Dallas

Instructor: Mehrdad Nourani (nourani@utdallas.edu)

Cover Page for All Submissions

(Assignment, Project, Codes/Simulations/CAD, Examinations, etc.)

Last Name (as shown in the official UT Dallas Student ID Card): Bandaru

First Name: Uday Teja

Submission Materials for (e.g. Homework #, Project #): Homework 2

Statement of Academic Honesty

I certify that:

i. the attached report (for assignment, project, codes/simulations/CAD, examinations, etc.) is my own work, based on my personal study and/or research,
ii. I have acknowledged/cited all material and sources used in its preparation, whether they be books, articles, reports, lecture notes, and any other kind of document, electronic or personal communication,
iii. I have not used **generative AI (e.g. ChatGPT or similar tools)** in preparing this report,
iv. this report has not previously been submitted for assessment in EEDG/CE 6303 or any other course at UT Dallas or elsewhere,
v. I have not copied in part or whole or otherwise plagiarized the work of other students and/or persons, and
vi. I have read and understood the Department and University policies on scholastic dishonesty as outlined in: http://www.utdallas.edu/deanofstudents/dishonesty/.

Name: Uday Teja Bandaru Date: 02/15/2024

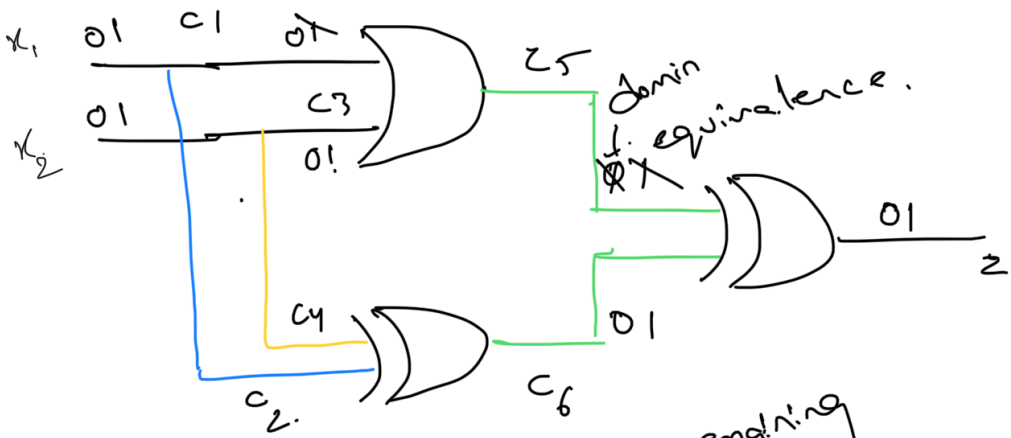
Signature: Uday Teja Bandaru

TTD Assignment 2

Udayteja Bandaru
UTB220000.

---

(1) a) circuit 3.23

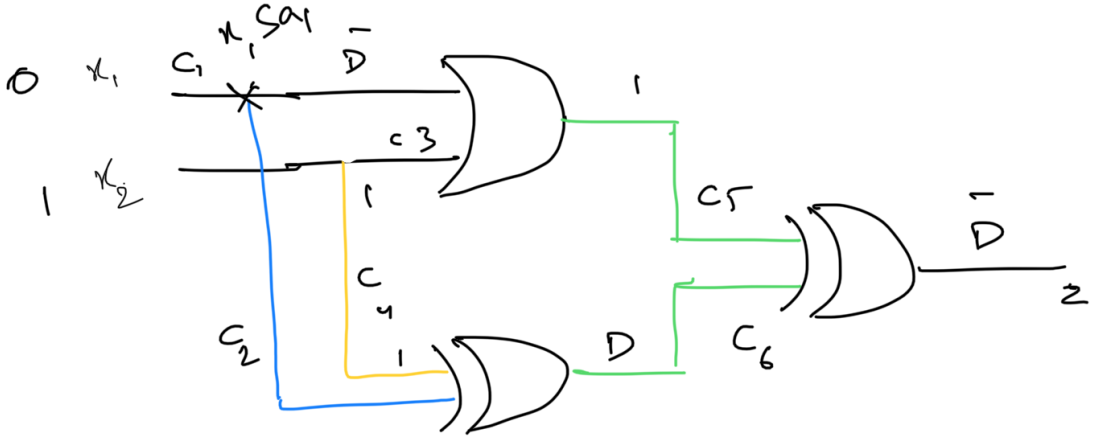


Collapse Ratio = $\frac{15}{18}$ = 83% (15 → remaining, 18 → total)

Collapsed faults →

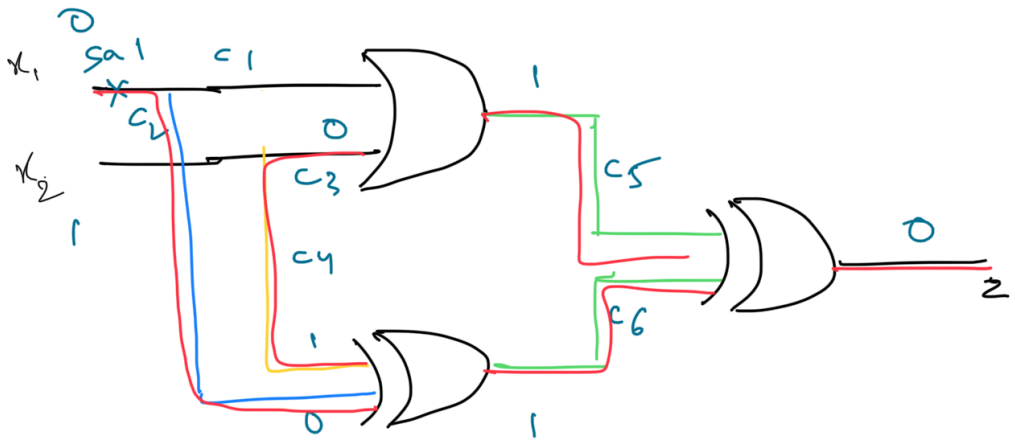
x_1 Sa0	c_2 Sa0	c_4 Sa1
x_1 Sa1	c_2 Sa1	c_6 Sa0
x_2 Sa0	c_3 Sa0	c_6 Sa1
x_2 Sa1	c_3 Sa1	z Sa0
c_1 Sa0	c_4 Sa0	z Sa1

Iteration 1 :- x_1 sa1



Pattern (0 1)

critical path

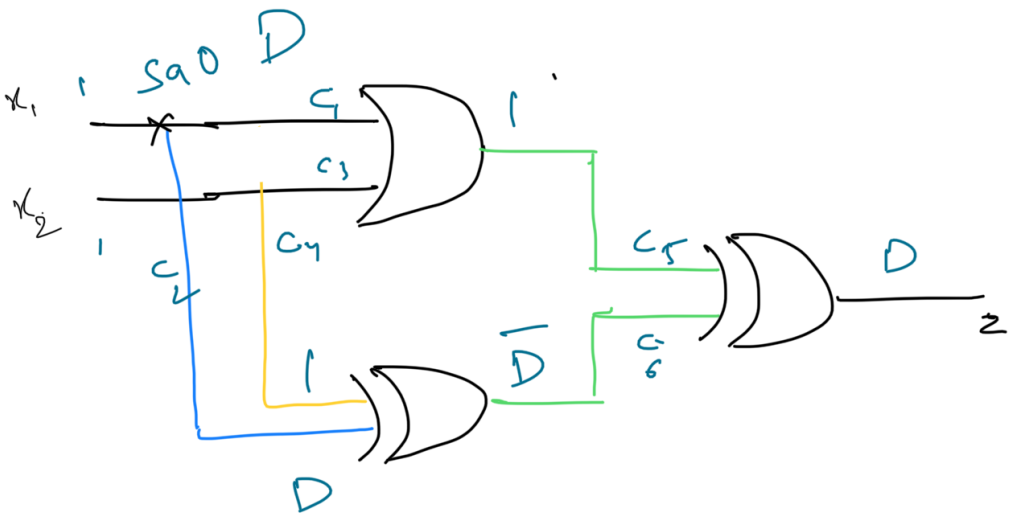


Faults = $\begin{bmatrix} x_1 sa_1 & \neq sa_1 & c_3 sa_0 \\ c_2 sa_1 & c_6 sa_0, & c_5 sa_0 \quad c_4 sa_0 \end{bmatrix}$

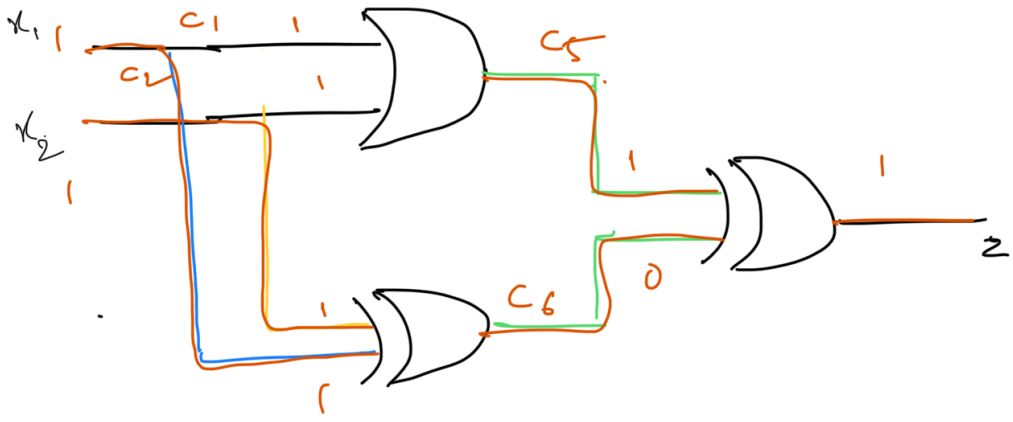
for pattern {0,1}

Rest = $x_2 sa_1$, $c_1 sa0, c_4 sa_1, c_4 sa_1$

Iteration 2 → x_1 sa0.



Test pattern (1, 1) → critical path is

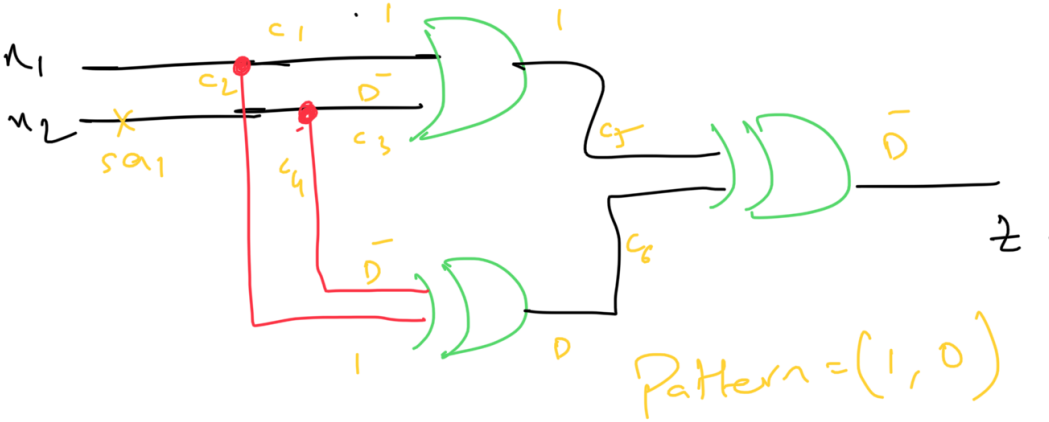


Faults for pattern 1,1

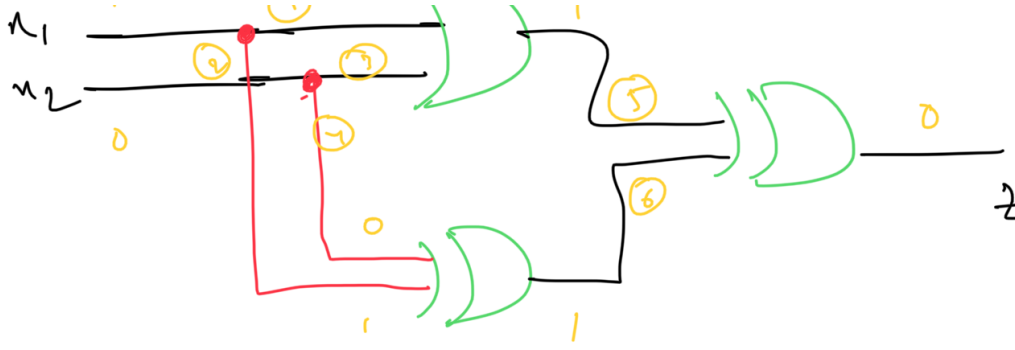
= x_1 sa0, x_2 sa0, c_2 sa0, c_4 sa0, c_5 sa0, c_6 sa1, z sa0

Remaining = x_1 sa1, x_2 sa1, c_1 sa0, c_2 sa1, c_3 sa0, c_3 sa1, c_4 sa1, c_6 sa0, z sa1

iteration -3 x_2 sa1



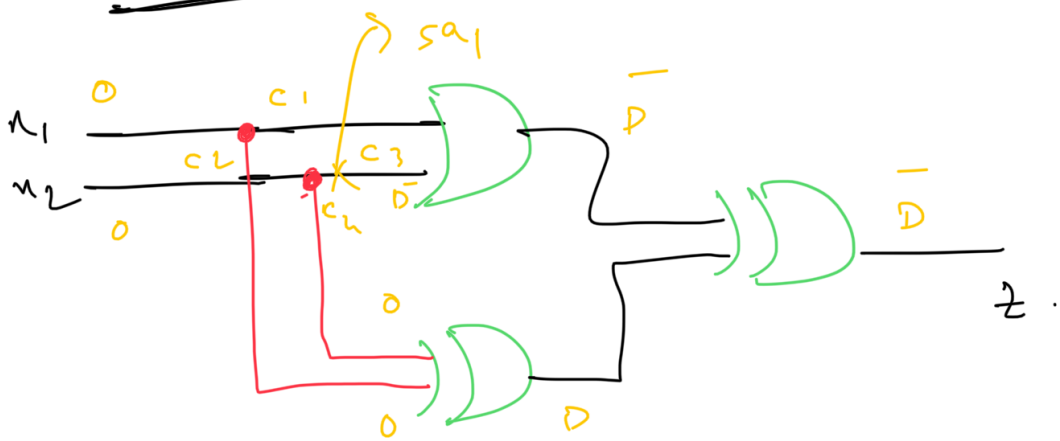
Pattern = (1, 0)



Faults = x_1 sa0 x_2 sa1 c_1 sa0 c_2 sa0 z sa1
c_4 sa1 c_6 sa0 c_5 sa0

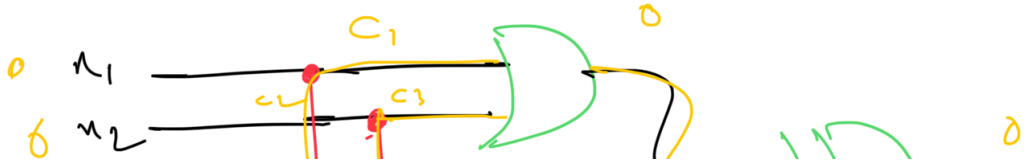
Rest = c_3 sa1

Iteration - 4 c_3 sa1



Pattern = 0, 0

Critical path



Detected

= z sa1 c_6 sa1 c_5 sa1

c_4 sa1 c_3 sa1 c_1 sa1

Rest = NULL

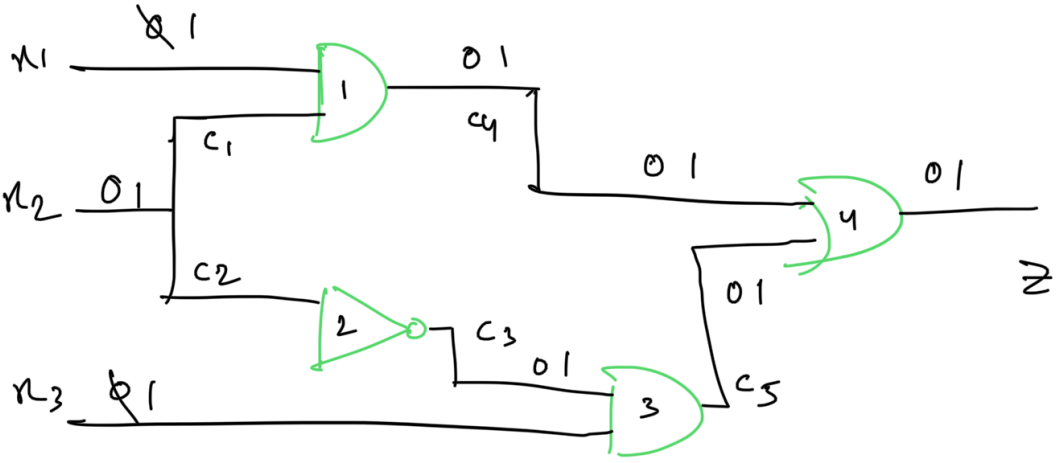
fault Coverage = 100%

---

circuit 3.34.

1 b

Apply checkpoint



Faults = 18

Detected faults = 8

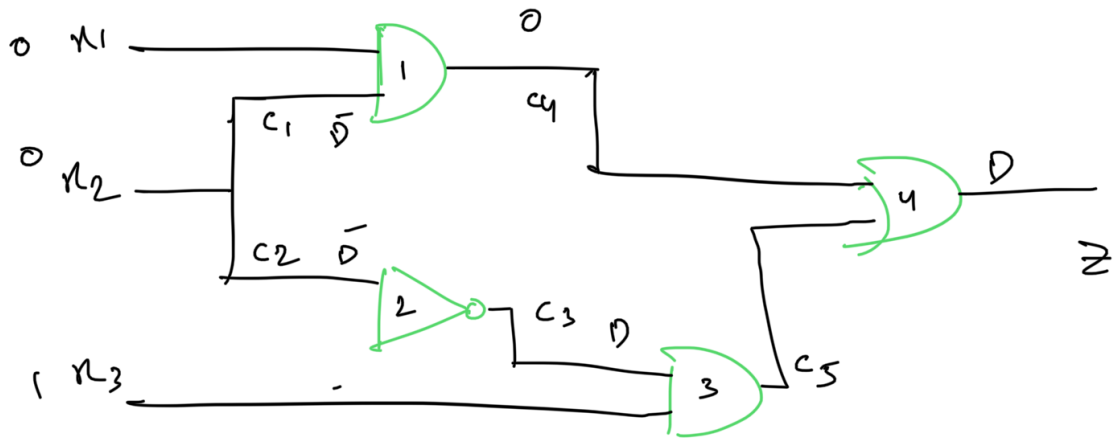
Collapse Ratio = 8/18 = 45%.

Rest of the faults =>

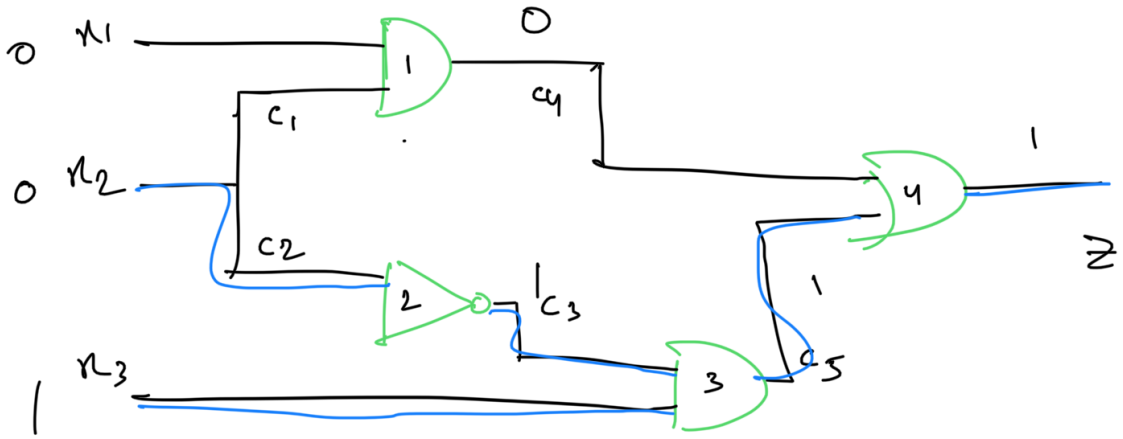
x_1 sa 1 $\quad c_1$ s0 $\quad c_1$ sa 1 $\quad x_2$ sa 0 $\quad x_2$ sa 1

c_2 sa 0 $\quad c_2$ sa 1 $\quad x_3$ sa 1

Iteration - 1 for x_2 sa 1



critical path tracing

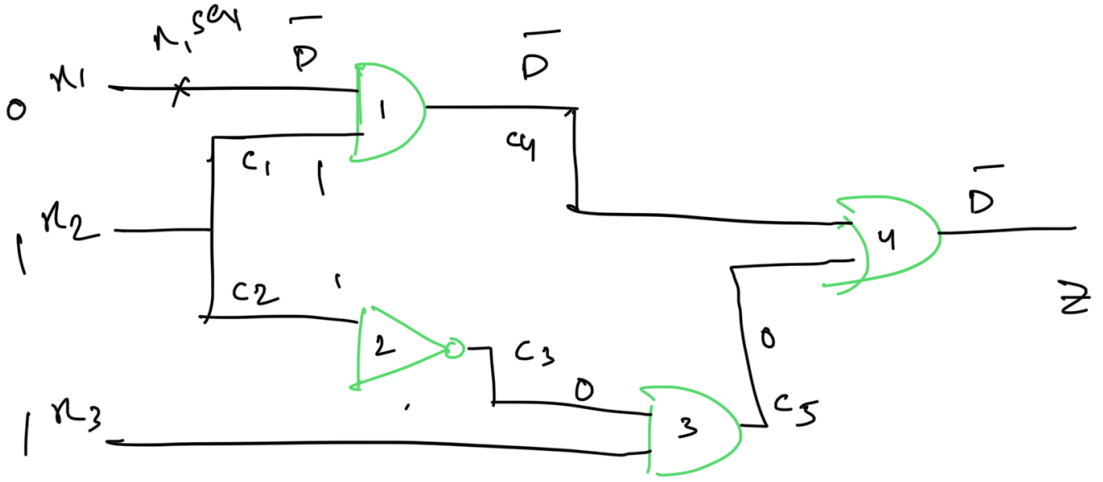


faults: Z sa 0, c_5 sa 0 $\quad x_3$ sa 0

c_0 sa 0 $\quad c_2$ sa 1 $\quad x_2$ sa 1

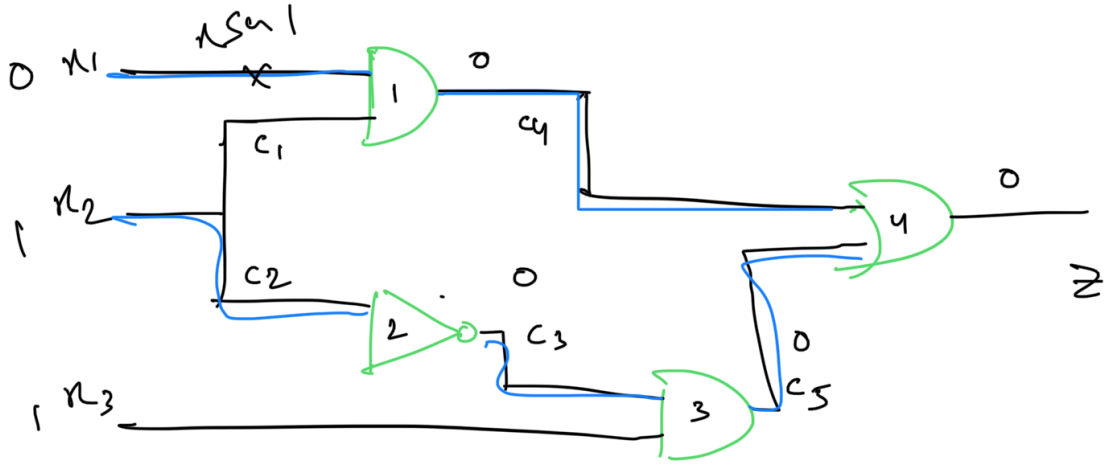
Rest = c_1 sa0 c_1 sa1 x_3 sa1

Iteration-2 x_1 sa1



Pattern (0, 1, 1)

critical path tracing.



faults - 2 sa1 c_5 sa1 c_3 sa1 x_2 sa0

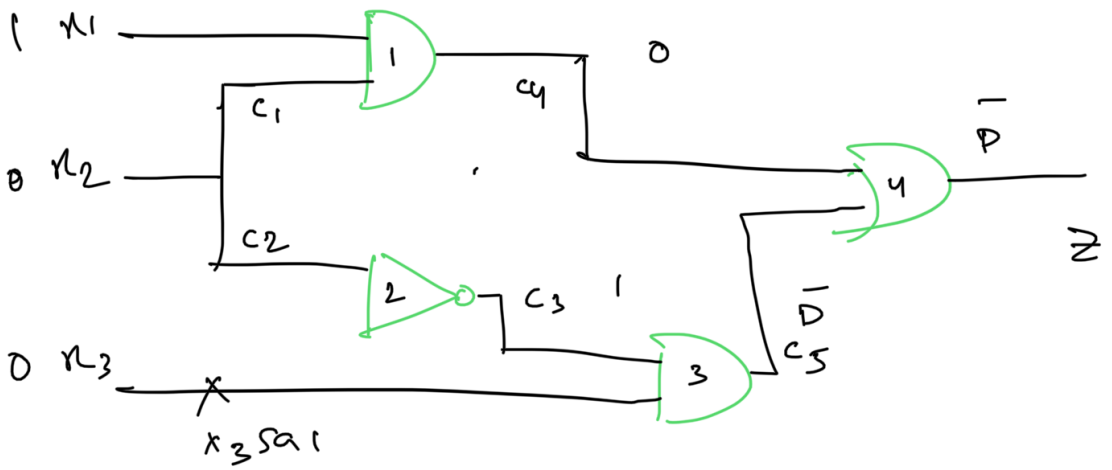
c_2 sa0 c_4 sa1 x_1 sa1

c_1 sa1 x_1 sa1

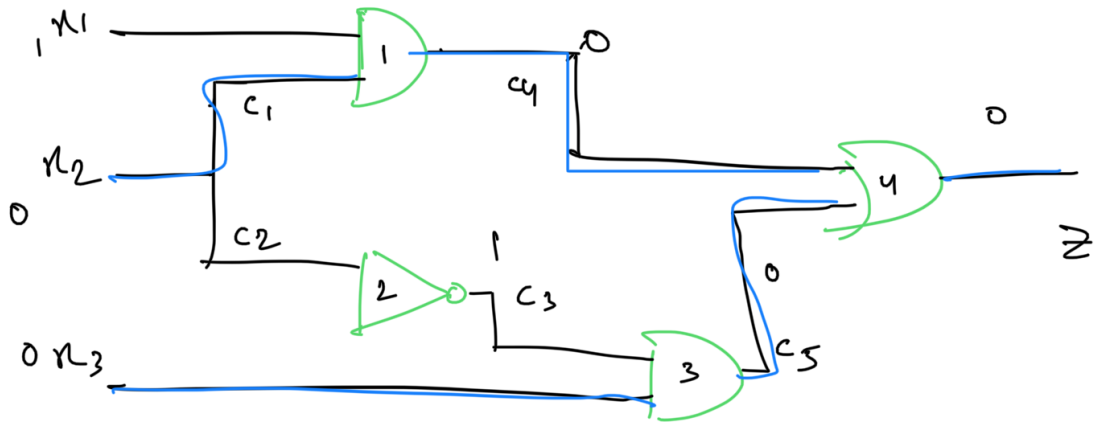
Rest = $c_1 sa0$ $x_3 sa1$

$c_2 sa1$

Iteration - 3 $x_3 sa1$



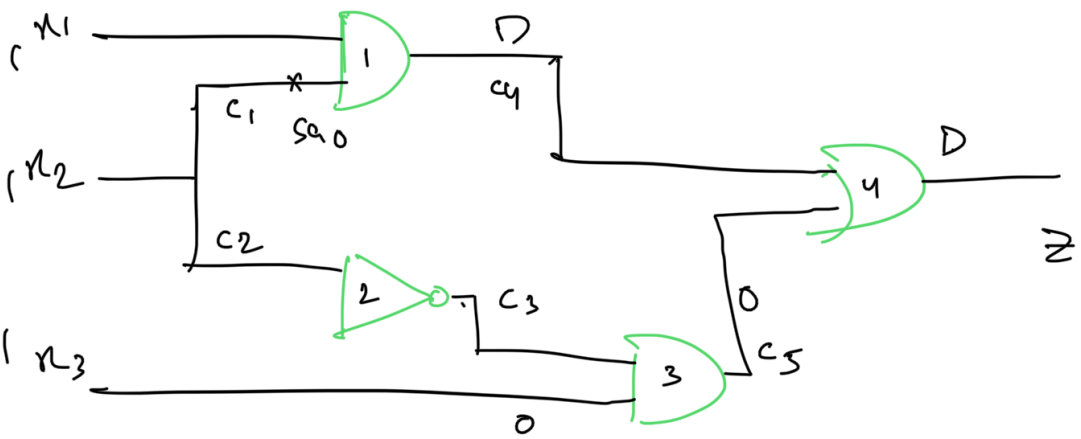
critical path tracing



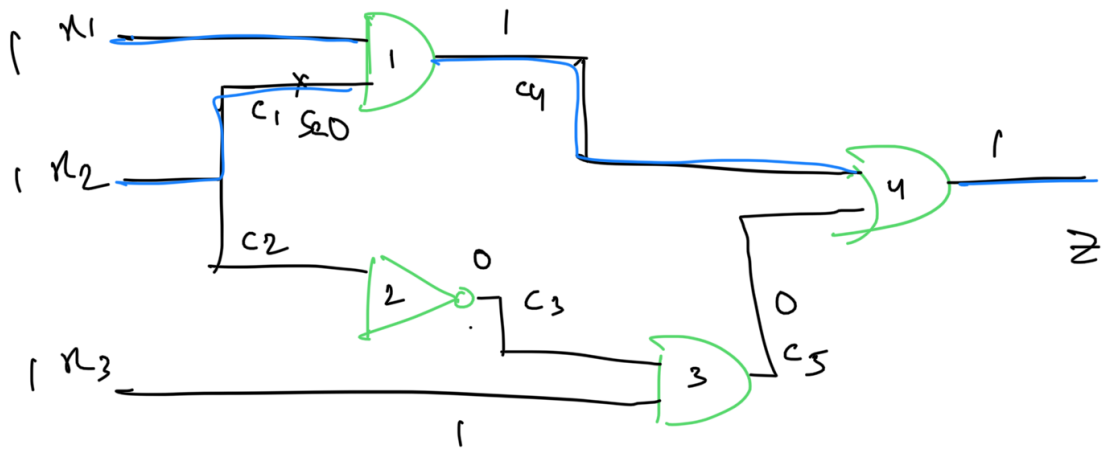
faults = $\begin{pmatrix} Z\ sa1 & c_5 sa1 & x_3 sa1 \\ c_4 sa1 & c_1 sa1 & x_2 sa1 \end{pmatrix}$

Rest = $c_1 sa0$

Iteration-4 c_1 SA0



critical path



Pattern = Z SA0 c_4 SA0 x_1 SA0 c_1 SA0

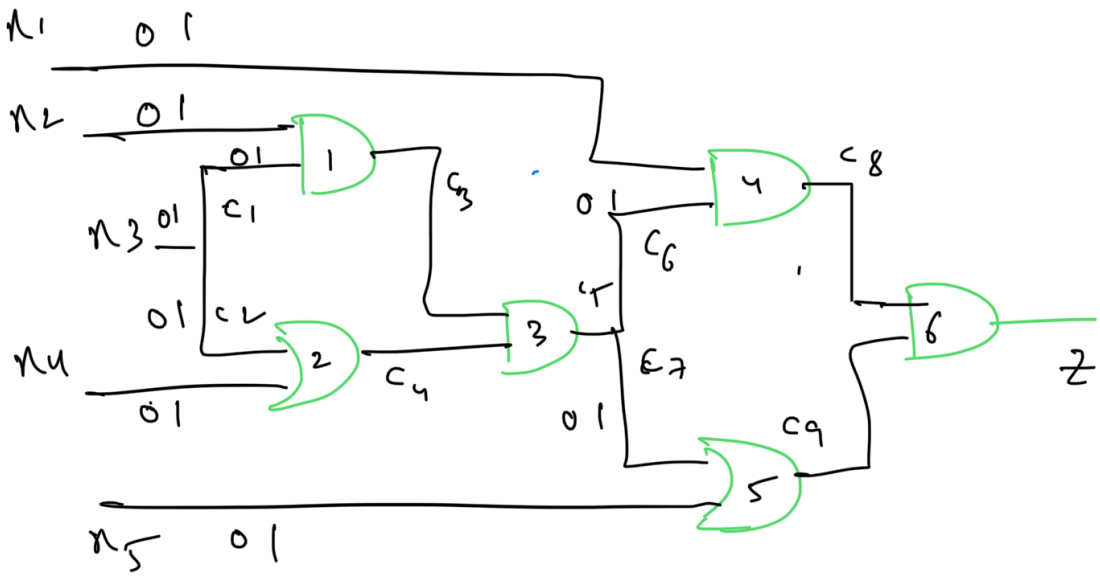
x_2 SA0

Rest Patterns = NULL.

Coverage = 100%

fault Cover)

Circuit 3.37.



Faults = 30

undetected = 4 ⇒ Ratio = 14/30 = 46.6

(faults = x_1 sa1 x_2 sa1 x_3 sa0 x_3 sa1

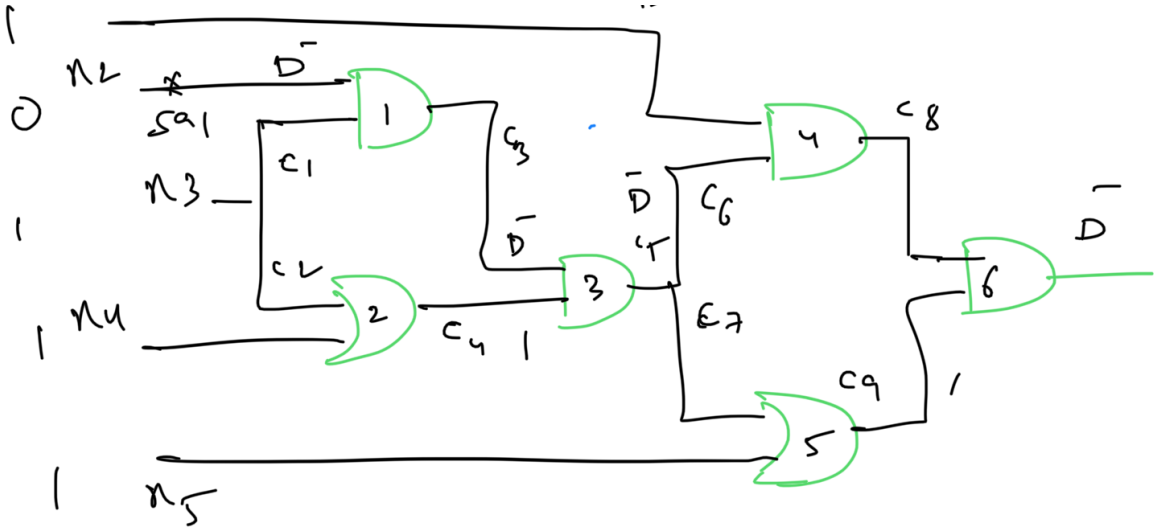
c_1 sa0 c_1 sa1 c_2 sa0 c_2 sa1 x_4 sa0

x_3 sa0 c_6 sa0 c_6 sa1 c_7 sa0 c_7 sa1)

Iteration 1 x_2 sa1

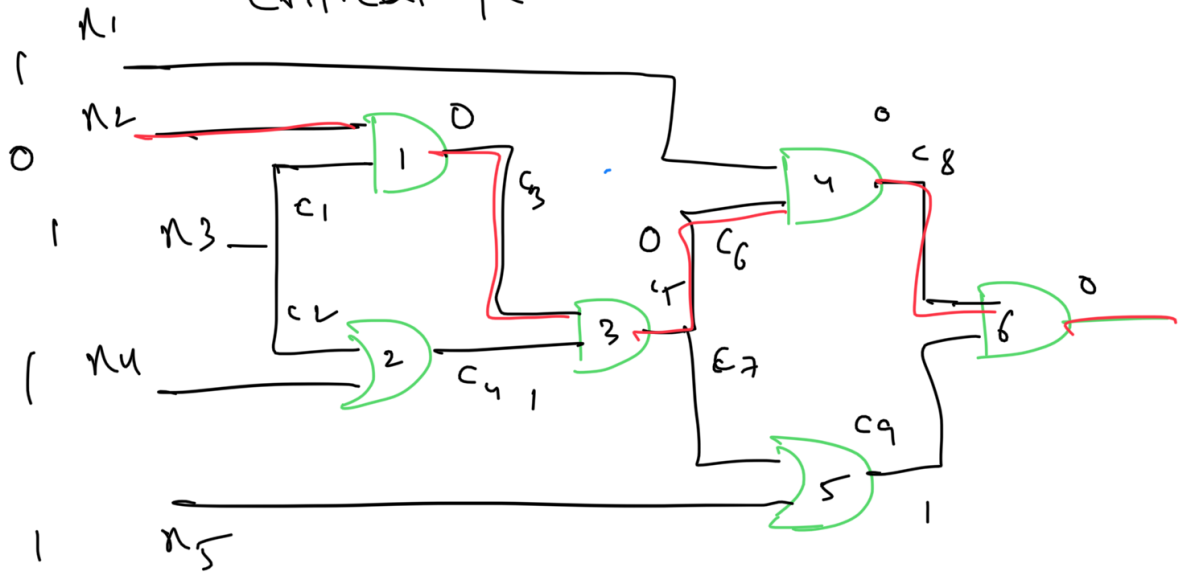
x_1

D



Pattern (1, 0 1 1 1)

critical path



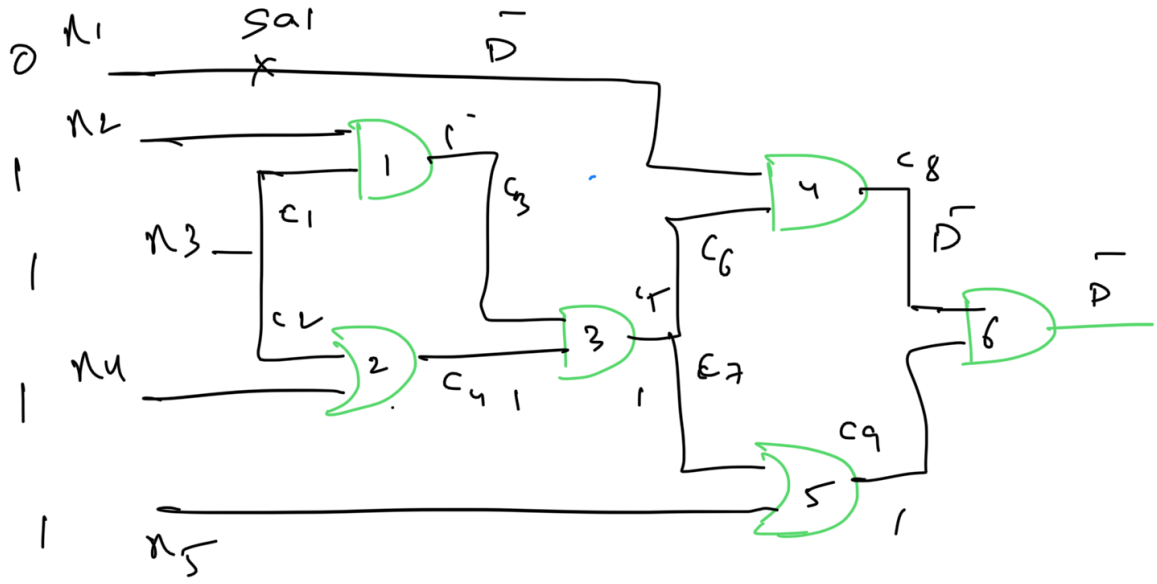
faults = $z\,sa1$ $c_8 sa1$ $c_6 sa1$ $c_5 sa1$ $c_3 sa1$ $x_2 sa1$

Rest = $x_3 sa0$ $x_3 sa1$ $c_1 sa0$ $c_1 sa1$ $c_2 sa0$ $c_2 sa1$

$c_6 sa0$ $c_7 sa0$ $c_7 sa1$

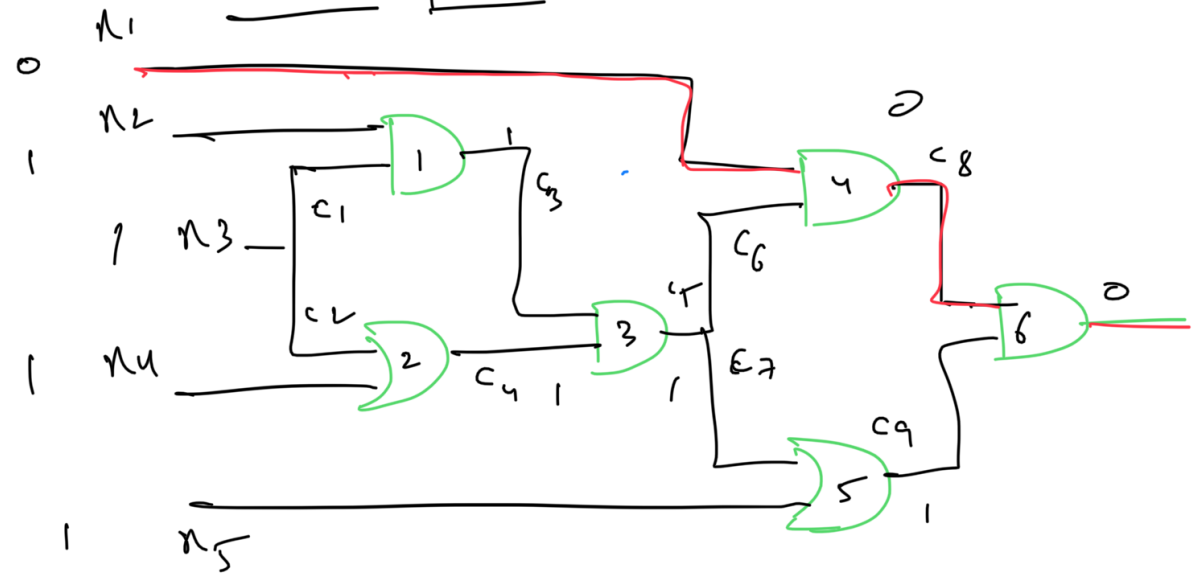
$x_4 sa0$ $x_3 sa0$

Iteration 2 $x_1 sa1$



Pattern = 0 1 1 1 1

critical path



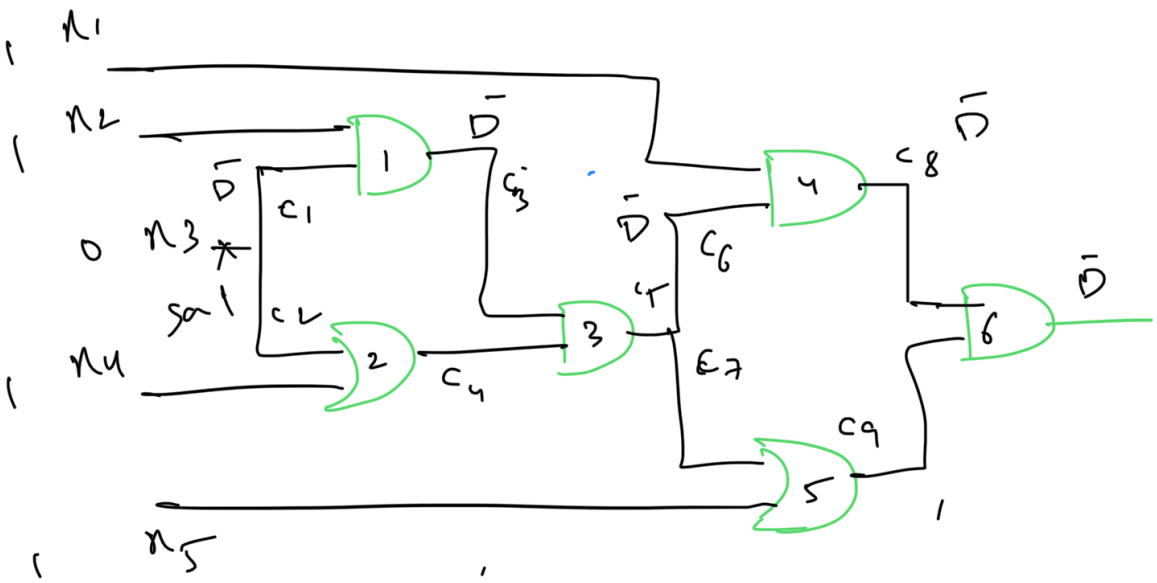
faults : $z\,sa1$, $c_8 sa1$, $x_1 sa1$

Rest = $x_2 sa1$ $x_3 sa0$ $x_3 sa1$ $c_1 sa0$ $c_1 sa1$,

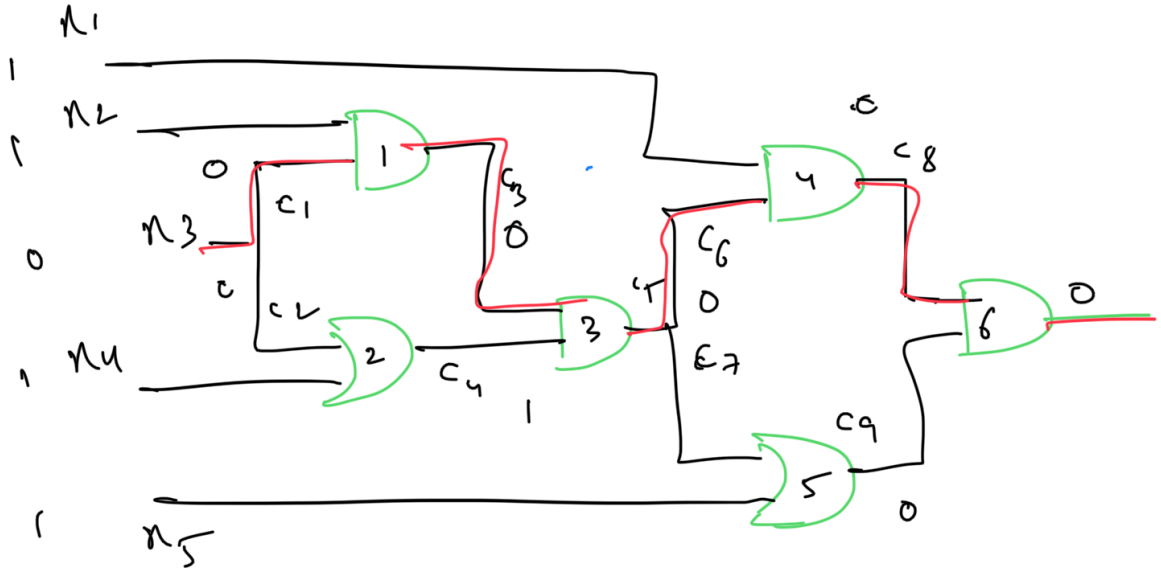
$c_2 sa0$ $c_2 sa1$ $x_4 sa0$ $x_3 sa0$

$c_6 sa0$ $c_6 sa1$ $c_7 sa0$ $c_7 sa1$

Iteration - 3 x_3 Sa1



Pattern : 1101 1



faults = x_3Sa1 c_1Sa1 c_3Sa1 c_5Sa1

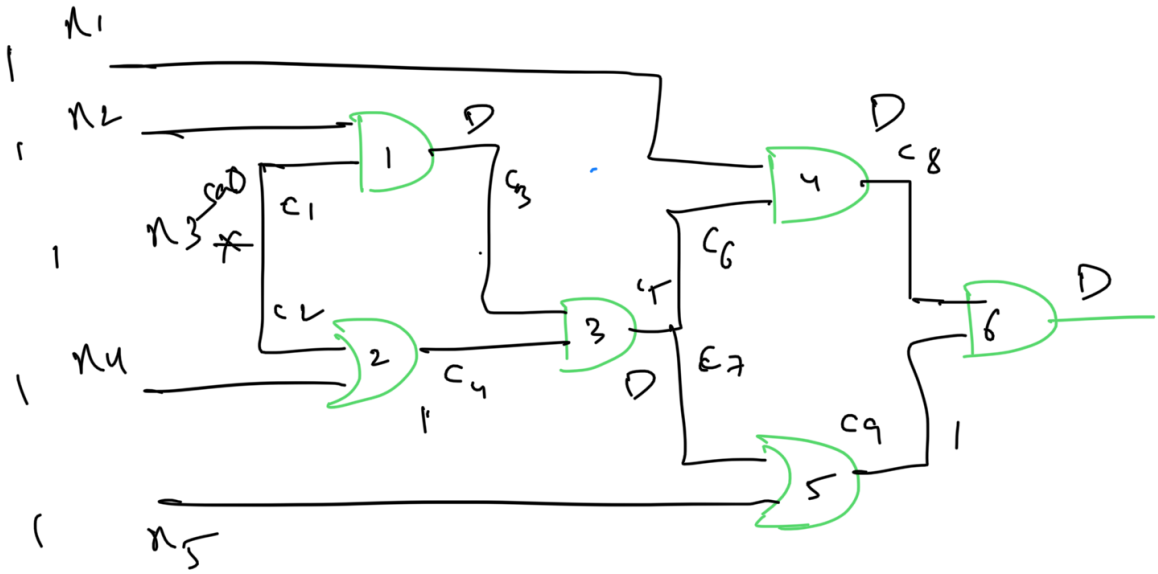
c_6Sa1 Z Sa1

c_6 sa 1

Rest = c_2 sa0 c_2 sa 1 x_4 sa0 x_5 sa0

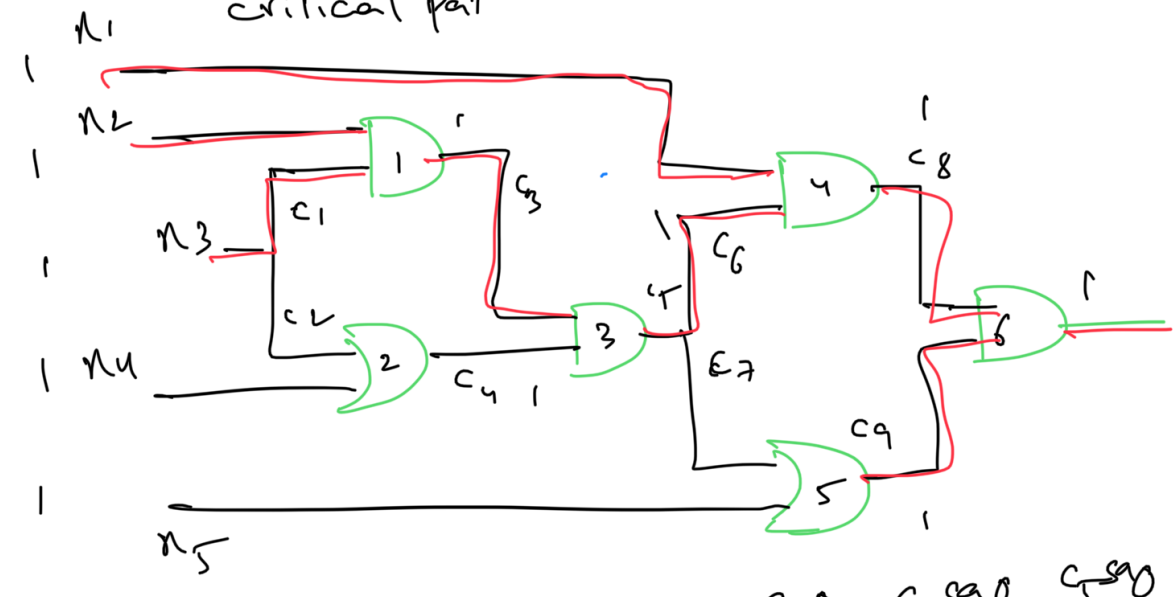
c_7 sa0 c_7 sa 1

Iteration - 4 x_3 sa0



Pattern = 1 1 1 1 1

critical part



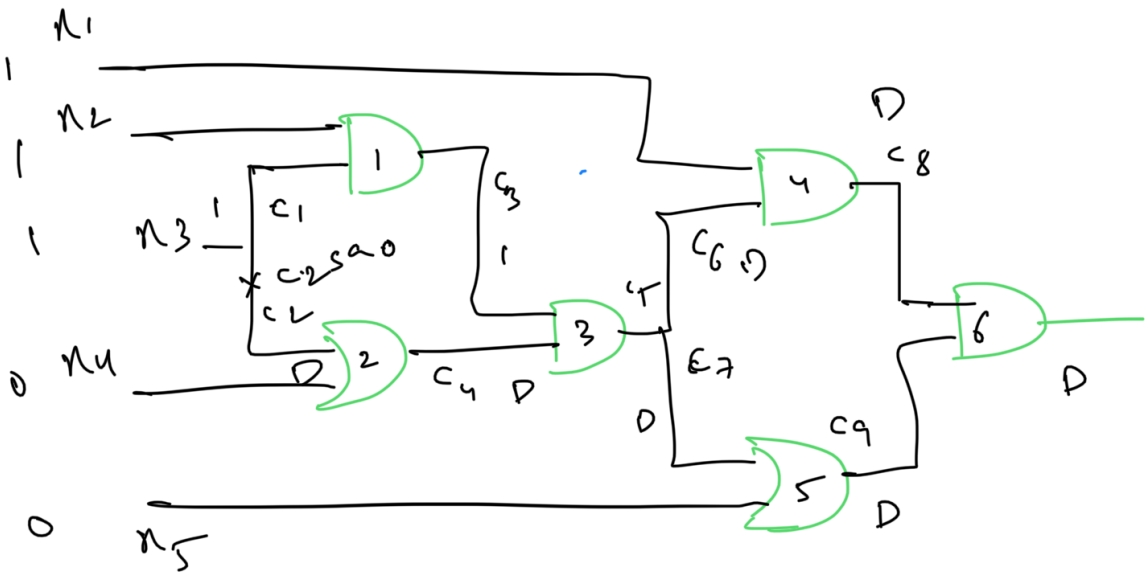
faults = 7sa0 C_9sa0 C_8 sa0 ...

C_3sa0 C_1sa0 n_1 sa0 $n_3$sa0 $n_2$sa0

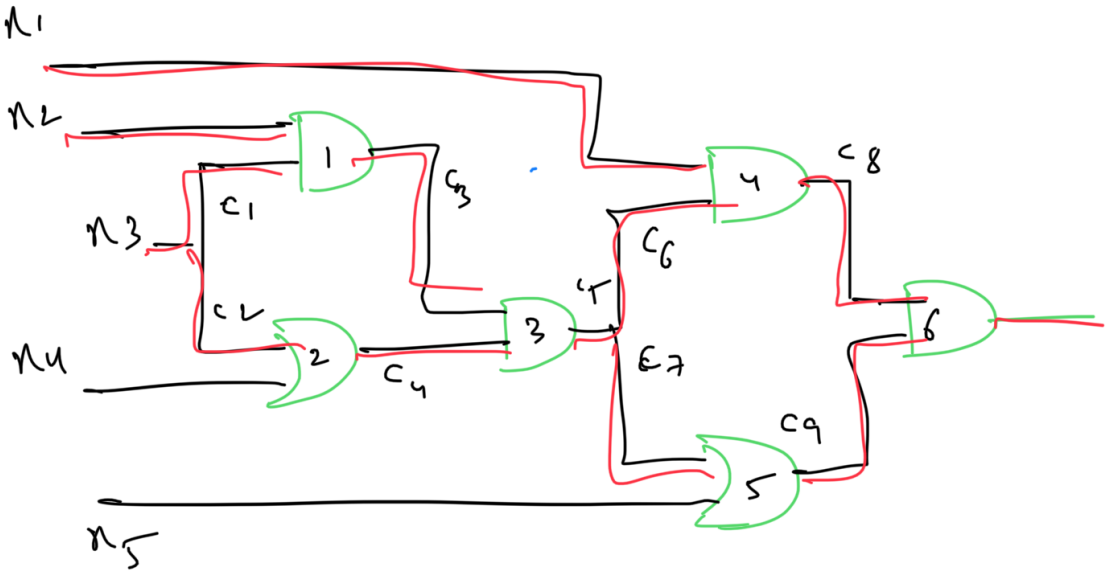
Rest = $n_3$sa1 C_1sa1 C_2sa0 C_2sa1

$n_4$sa0 C_7 sa0 , C_7sa1

Iteration-5 C_2sa0



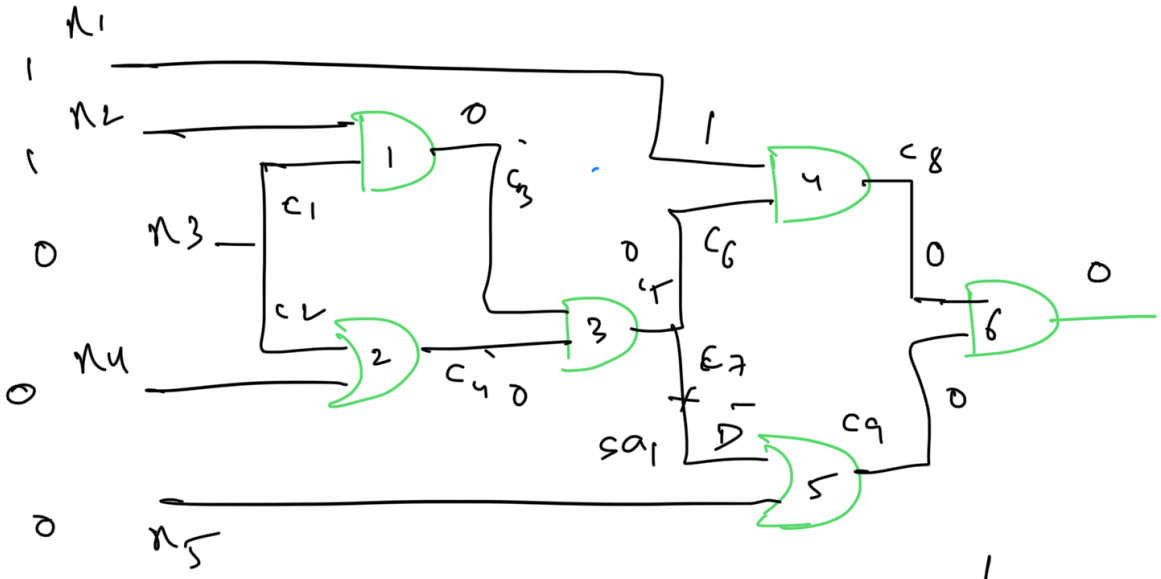
Pattern 11100



faults = $\overline{z}$ sa0 c_8 sa0 c_9 sa0 c_6 sa0 c_4 sa0 c_7 sa0 c_5 sa0 x_1 sa0 c_3 sa0 x_2 sa0 c_1 sa0 c_2 0 x_3 sa 0

Rest = c_2 sa 1 x_4 sa0 x_5 sa0 c_7 sa1

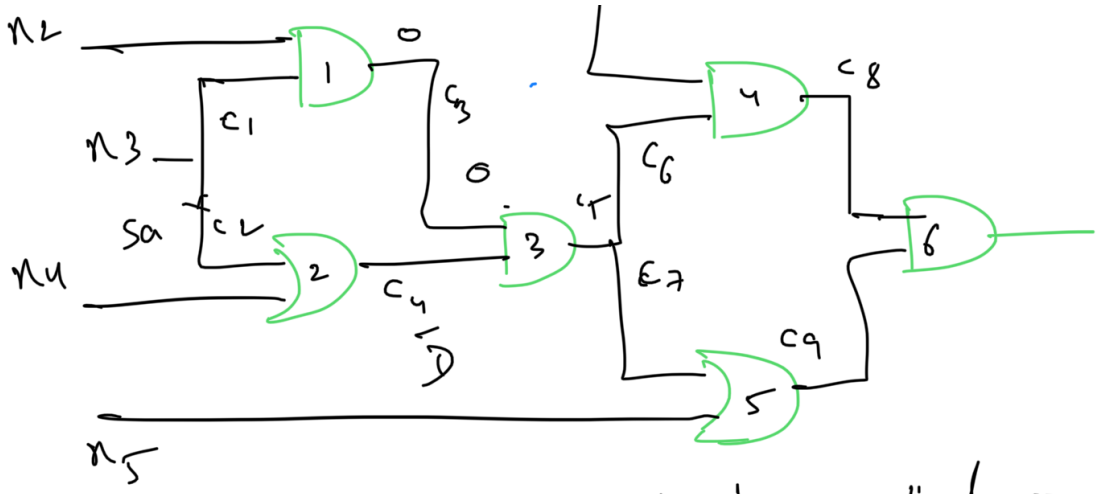
Iteration-6 c_7 sa 1



* D-algorithm cannot be applied, no Patterns

Iteration-7 = c_2 sa 1

x_1



* D algorithm cannot be applied, no patterns.

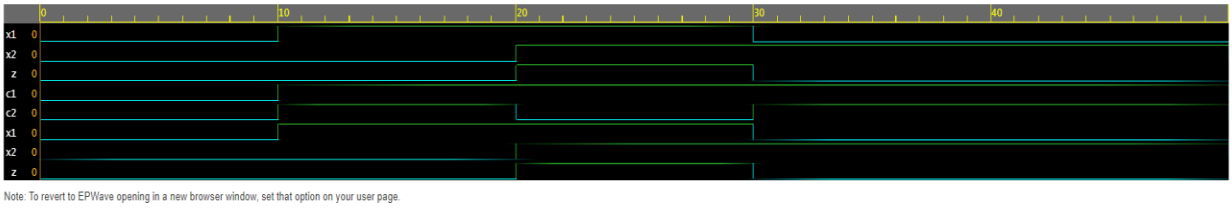
* for rest of the faults D-algo, not applicable,

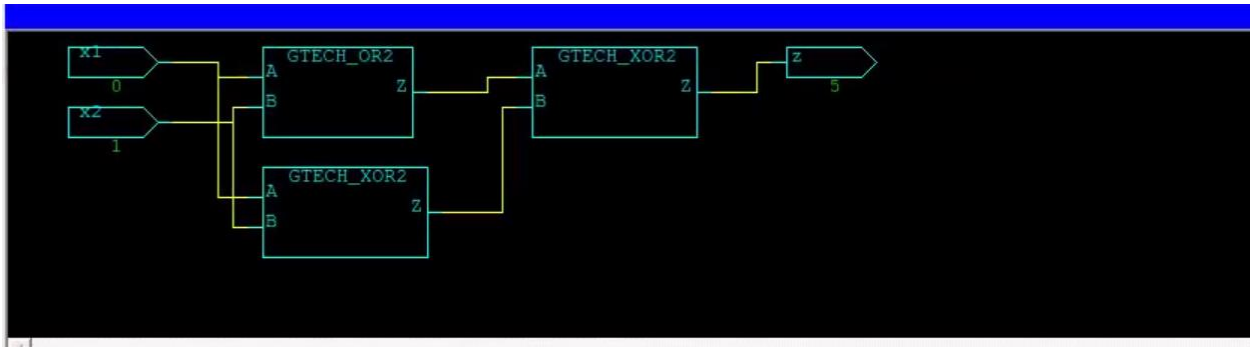
→ All faults are covered, so fault coverage is 100 %.

Question 2

Circuit 3.23- block, waveform, build, drc, atpg, faults and patterns

```
module circuit3_23(x1,x2,z);

input x1, x2;

output z;

wire c1,c2;


or g1(c1,x1,x2);

xor g2(c2,x1,x2);

xor g3(z,c1,c2);


endmodule
```



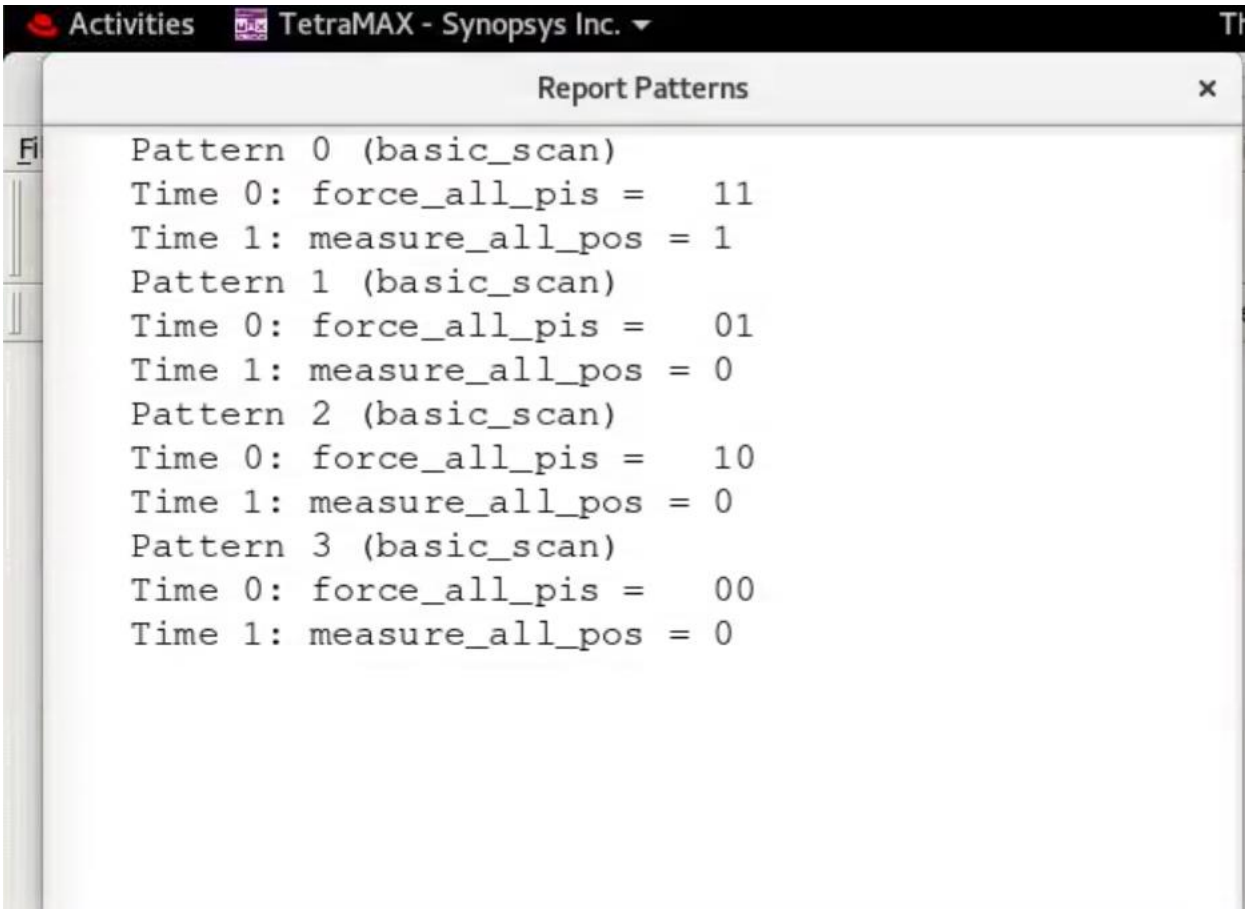


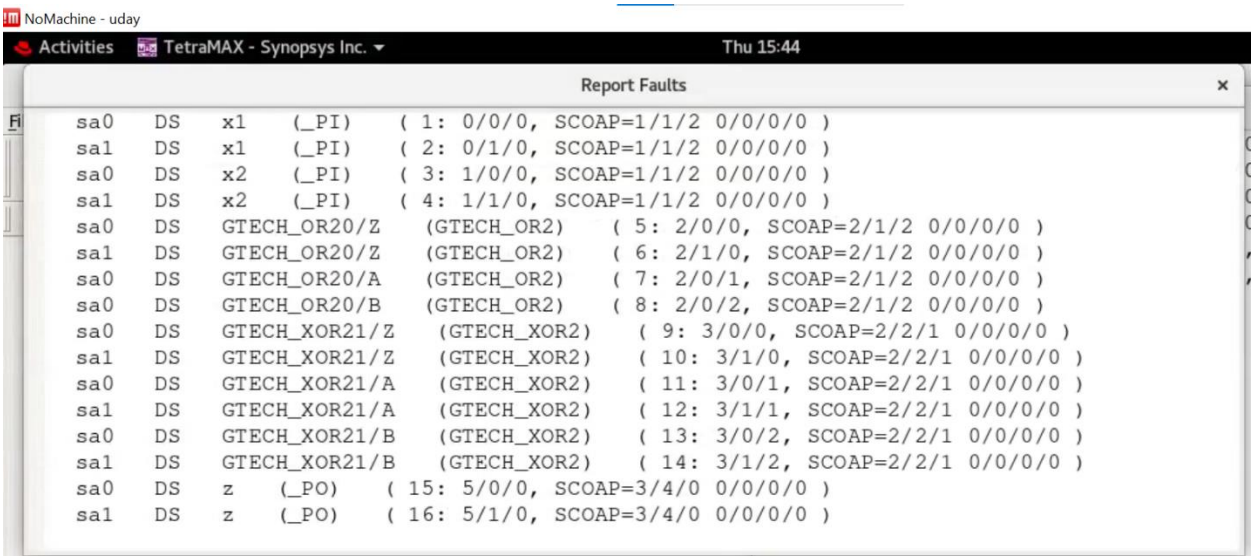
```
BUILD-T> run_build_model circuit3_23
  ---------------------------------------------------------------------------
  Begin build model for topcut = circuit3_23 ...
  ---------------------------------------------------------------------------
  There were 0 primitives and 0 faultable pins removed during model optimizations
  End build model: #primitives=6, CPU_time=0.00 sec, Memory=0MB
  ---------------------------------------------------------------------------
  Begin learning analyses...
  End learning analyses, total learning CPU time=0.00 sec.
  ---------------------------------------------------------------------------
```

```
DRC-T> run_drc
  ---------------------------------------------------------------------------
  Begin scan design rules checking...
  ---------------------------------------------------------------------------
  Begin simulating test protocol procedures...
  Test protocol simulation completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  Begin scan chain operation checking...
  Scan chain operation checking completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  Begin nonscan rules checking...
  Nonscan cell summary: #DFF=0  #DLAT=0  #RAM_outs=0  tla_usage_type=none
  Nonscan rules checking completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  Begin DRC dependent learning...
  Fast-sequential depth results: control=0(0), observe=0(0), detect=0(0), CPU time=0.00 sec
  DRC dependent learning completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  DRC Summary Report
  ---------------------------------------------------------------------------
  No violations occurred during DRC process.
  Design rules checking was successful, total CPU time=0.00 sec.
  ---------------------------------------------------------------------------
```

```
  ------------------------------------------------
  fault class                     code   #faults
  ------------------------------  ----  ---------
  Detected                         DT          16
  Possibly detected                PT           0
  Undetectable                     UD           0
  ATPG untestable                  AU           0
  Not detected                     ND           0
  ------------------------------------------------
  total faults                                 16
  test coverage                            100.00%
  ------------------------------------------------
            Pattern Summary Report
  ------------------------------------------------
  #internal patterns                            4
      #basic_scan patterns                      4
  ------------------------------------------------
TEST-T> report_faults -all -verbose
TEST-T> report_patterns -all -internal
TEST-T>
```

```
  ------------------------------------------------------------------------------
TEST-T> remove_faults -all
  0 faults were removed from the fault list.
TEST-T> add_faults -all
  16 faults were added to fault list.
TEST-T> run_atpg -ndetects 1
  ATPG performed for stuck fault model using internal pattern source.
  ----------------------------------------------------------
  #patterns     #faults     #ATPG faults  test      process
  stored     detect/active  red/au/abort  coverage  CPU time
  --------  -------------  ------------  --------  --------
  Begin deterministic ATPG: #collapsed_faults=16, abort_limit=10...
  4              16      0         0/0/0   100.00%      0.00

       Collapsed Stuck Fault Summary Report
  -----------------------------------------------
  fault class                     code   #faults
  ------------------------------  ----  ---------
  Detected                         DT          16
  Possibly detected                PT           0
  Undetectable                     UD           0
  ATPG untestable                  AU           0
  Not detected                     ND           0
  -----------------------------------------------
```

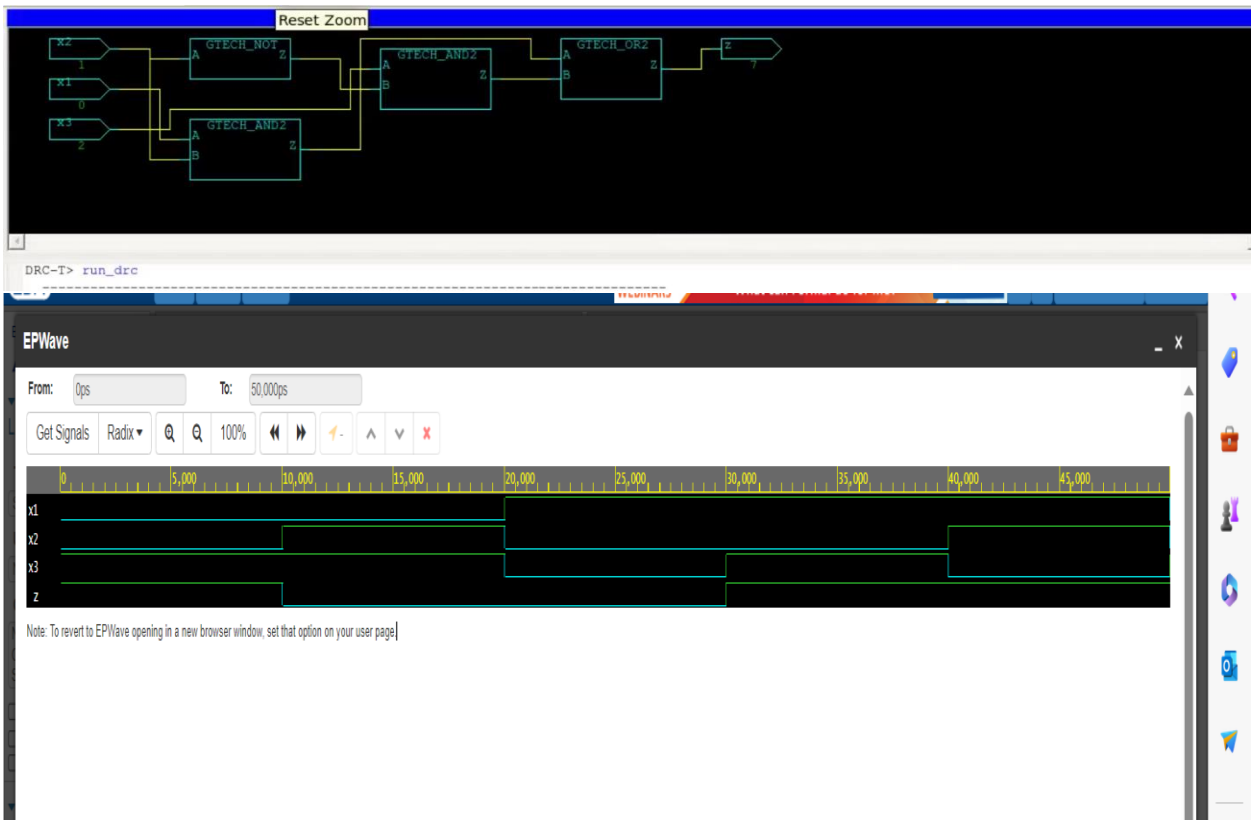

Activities
TetraMAX - Synopsys Inc.
Report Patterns
Pattern 0 (basic_scan)
Time 0: force_all_pis = 11
Time 1: measure_all_pos = 1
Pattern 1 (basic_scan)
Time 0: force_all_pis = 01
Time 1: measure_all_pos = 0
Pattern 2 (basic_scan)
Time 0: force_all_pis = 10
Time 1: measure_all_pos = 0
Pattern 3 (basic_scan)
Time 0: force_all_pis = 00
Time 1: measure_all_pos = 0


NoMachine - uday
Activities
TetraMAX - Synopsys Inc.
Thu 15:44
Report Faults
sa0 DS x1 (_PI) (1: 0/0/0, SCOAP=1/1/2 0/0/0/0)
sa1 DS x1 (_PI) (2: 0/1/0, SCOAP=1/1/2 0/0/0/0)
sa0 DS x2 (_PI) (3: 1/0/0, SCOAP=1/1/2 0/0/0/0)
sa1 DS x2 (_PI) (4: 1/1/0, SCOAP=1/1/2 0/0/0/0)
sa0 DS GTECH_OR20/Z (GTECH_OR2) (5: 2/0/0, SCOAP=2/1/2 0/0/0/0)
sa1 DS GTECH_OR20/Z (GTECH_OR2) (6: 2/1/0, SCOAP=2/1/2 0/0/0/0)
sa0 DS GTECH_OR20/A (GTECH_OR2) (7: 2/0/1, SCOAP=2/1/2 0/0/0/0)
sa0 DS GTECH_OR20/B (GTECH_OR2) (8: 2/0/2, SCOAP=2/1/2 0/0/0/0)
sa0 DS GTECH_XOR21/Z (GTECH_XOR2) (9: 3/0/0, SCOAP=2/2/1 0/0/0/0)
sa1 DS GTECH_XOR21/Z (GTECH_XOR2) (10: 3/1/0, SCOAP=2/2/1 0/0/0/0)
sa0 DS GTECH_XOR21/A (GTECH_XOR2) (11: 3/0/1, SCOAP=2/2/1 0/0/0/0)
sa1 DS GTECH_XOR21/A (GTECH_XOR2) (12: 3/1/1, SCOAP=2/2/1 0/0/0/0)
sa0 DS GTECH_XOR21/B (GTECH_XOR2) (13: 3/0/2, SCOAP=2/2/1 0/0/0/0)
sa1 DS GTECH_XOR21/B (GTECH_XOR2) (14: 3/1/2, SCOAP=2/2/1 0/0/0/0)
sa0 DS z (_PO) (15: 5/0/0, SCOAP=3/4/0 0/0/0/0)
sa1 DS z (_PO) (16: 5/1/0, SCOAP=3/4/0 0/0/0/0)

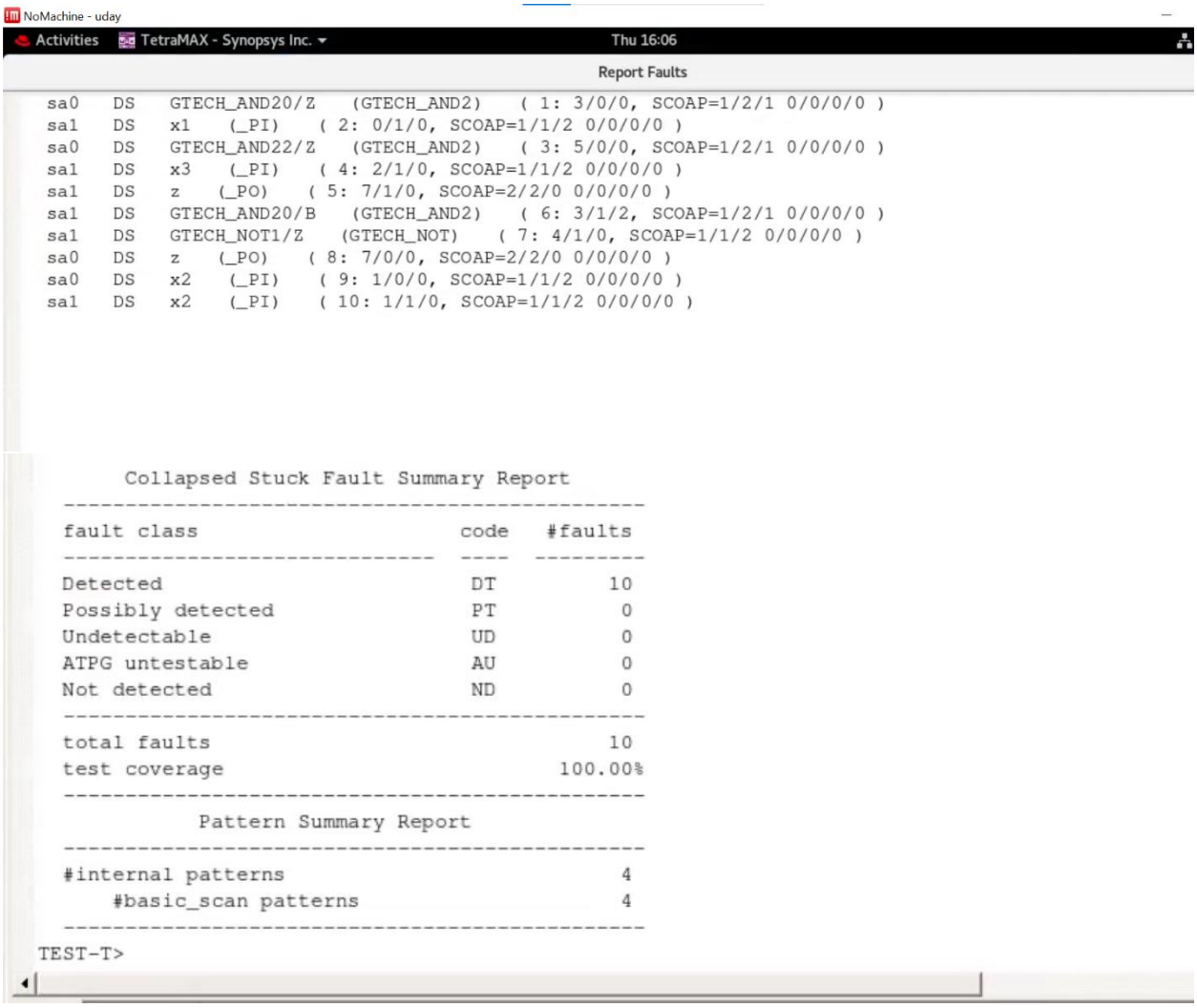
Circuit 3.34

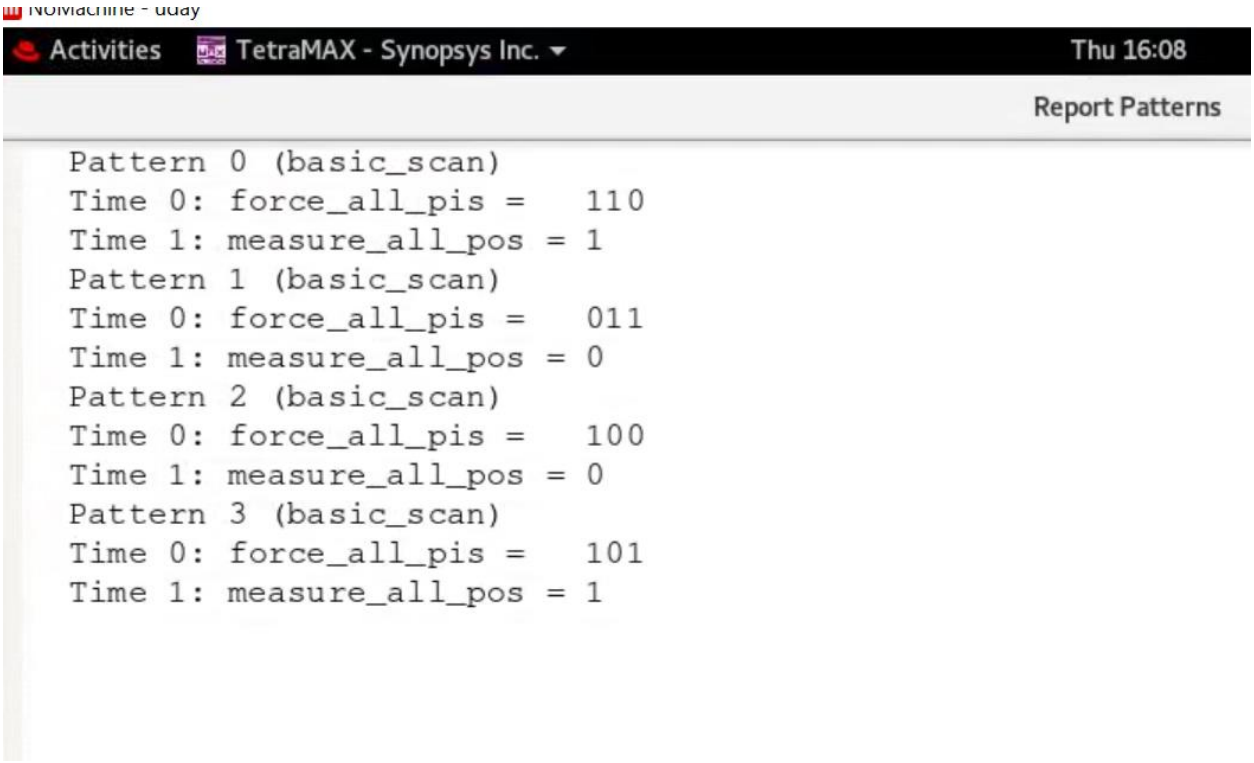
Circuit 3.23- block, waveform, build, drc, atpg, faults and patterns

```
module Q2_3_34(x1,x2,x3,z);
input x1, x2,x3;
output z;
wire c1,c2,c3;

 and g1(c1,x1,x2);
 not g2(c2,x2);
 and g3(c3,x3,c2);
 or g4(z,c1,c3);

endmodule
```



```
  ---------------------------------------------------------------------------
DRC-T> run_drc
  ---------------------------------------------------------------------------
  Begin scan design rules checking...
  ---------------------------------------------------------------------------
  Begin simulating test protocol procedures...
  Test protocol simulation completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  Begin scan chain operation checking...
  Scan chain operation checking completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  Begin nonscan rules checking...
  Nonscan cell summary: #DFF=0  #DLAT=0  #RAM_outs=0  tla_usage_type=none
  Nonscan rules checking completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  Begin DRC dependent learning...
  Fast-sequential depth results: control=0(0), observe=0(0), detect=0(0), CPU time=0.00 sec
  DRC dependent learning completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  DRC Summary Report
  ---------------------------------------------------------------------------
  No violations occurred during DRC process.
  Design rules checking was successful, total CPU time=0.00 sec.
  ---------------------------------------------------------------------------
BUILD-T> read_netlist /home/013/u/ut/utb220000/Spring24/TTD/WORK/c2_3.34.v
  Begin reading netlist ( /home/013/u/ut/utb220000/Spring24/TTD/WORK/c2_3.34.v )...
 Warning: Rule N5 (redefined module) was violated 1 times.

  End parsing Verilog file /home/013/u/ut/utb220000/Spring24/TTD/WORK/c2_3.34.v with 0 errors.
  End reading netlist: #modules=0, top=Q2_3_34, #lines=11, CPU_time=0.00 sec, Memory=0MB
BUILD-T> run_build_model Q2_3_34
  ---------------------------------------------------------------------------
  Begin build model for topcut = Q2_3_34 ...
  ---------------------------------------------------------------------------
  There were 0 primitives and 0 faultable pins removed during model optimizations
  End build model: #primitives=8, CPU_time=0.00 sec, Memory=0MB
  ---------------------------------------------------------------------------
  Begin learning analyses...
  End learning analyses, total learning CPU time=0.00 sec.
  ---------------------------------------------------------------------------
   10 faults were added to fault list.
 TEST-T> run_atpg -ndetects 1
  ATPG performed for stuck fault model using internal pattern source.
  ---------------------------------------------------------------
  #patterns     #faults     #ATPG faults  test      process
  stored     detect/active  red/au/abort  coverage  CPU time
  ---------  -------------  ------------  --------  --------
  Begin deterministic ATPG: #collapsed_faults=10, abort_limit=10...
  4              10      0         0/0/0   100.00%      0.00

       Collapsed Stuck Fault Summary Report
  -----------------------------------------------
  fault class                    code   #faults
  -----------------------------  ----  ---------
  Detected                        DT         10
  Possibly detected               PT          0
  Undetectable                    UD          0
  ATPG untestable                 AU          0
  Not detected                    ND          0
  -----------------------------------------------
  total faults                               10
  test coverage                          100.00%
  -----------------------------------------------
            Pattern Summary Report
```

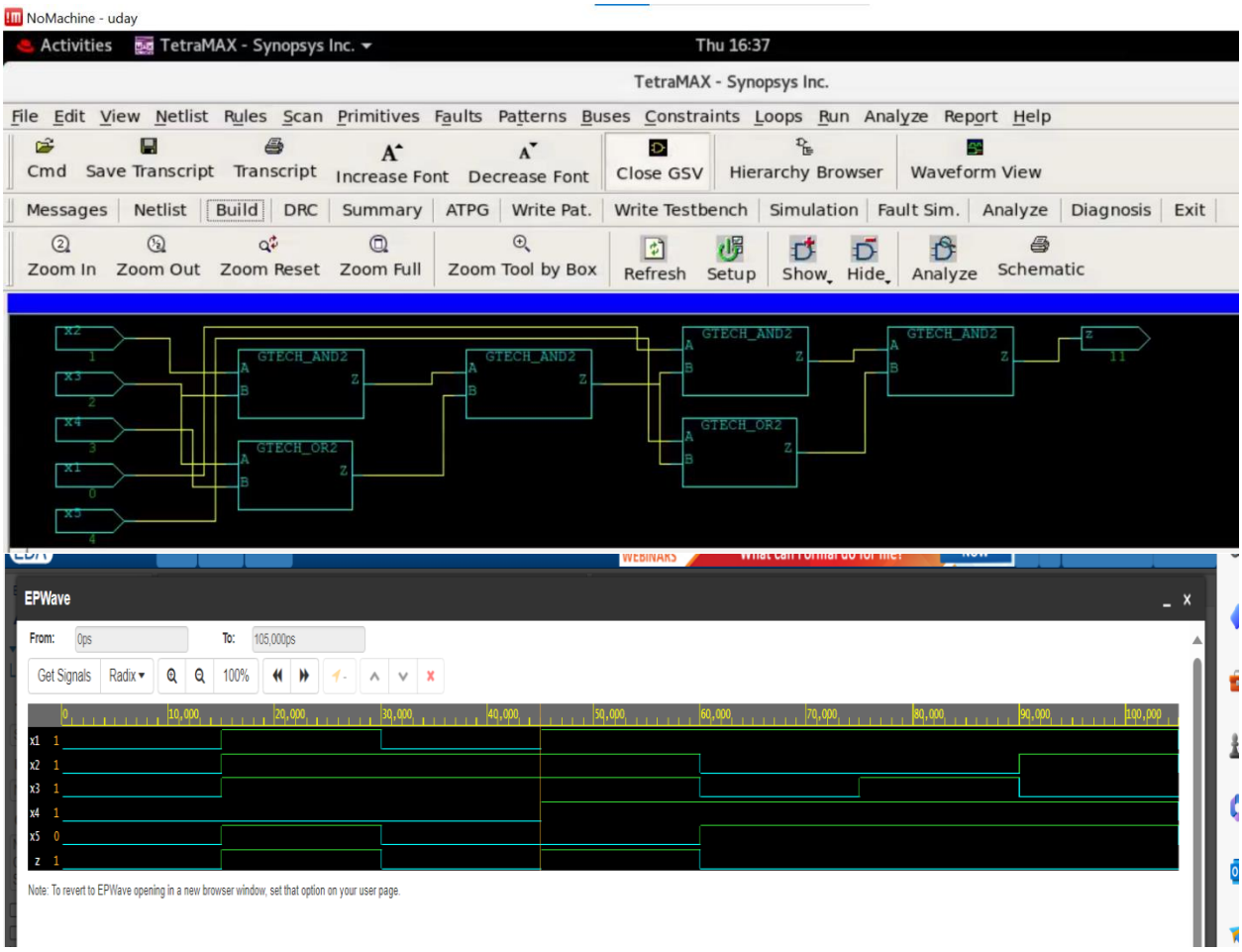

NoMachine - uday
Activities
TetraMAX - Synopsys Inc.
Thu 16:06
Report Faults
sa0 DS GTECH_AND20/Z (GTECH_AND2) (1: 3/0/0, SCOAP=1/2/1 0/0/0/0)
sa1 DS x1 (_PI) (2: 0/1/0, SCOAP=1/1/2 0/0/0/0)
sa0 DS GTECH_AND22/Z (GTECH_AND2) (3: 5/0/0, SCOAP=1/2/1 0/0/0/0)
sa1 DS x3 (_PI) (4: 2/1/0, SCOAP=1/1/2 0/0/0/0)
sa1 DS z (_PO) (5: 7/1/0, SCOAP=2/2/0 0/0/0/0)
sa1 DS GTECH_AND20/B (GTECH_AND2) (6: 3/1/2, SCOAP=1/2/1 0/0/0/0)
sa1 DS GTECH_NOT1/Z (GTECH_NOT) (7: 4/1/0, SCOAP=1/1/2 0/0/0/0)
sa0 DS z (_PO) (8: 7/0/0, SCOAP=2/2/0 0/0/0/0)
sa0 DS x2 (_PI) (9: 1/0/0, SCOAP=1/1/2 0/0/0/0)
sa1 DS x2 (_PI) (10: 1/1/0, SCOAP=1/1/2 0/0/0/0)
Collapsed Stuck Fault Summary Report
fault class code #faults
Detected DT 10
Possibly detected PT 0
Undetectable UD 0
ATPG untestable AU 0
Not detected ND 0
total faults 10
test coverage 100.00%
Pattern Summary Report
#internal patterns 4
#basic_scan patterns 4
TEST-T>



Circuit 3.37

Circuit 3.23- block, waveform, build, drc, atpg, faults and patterns

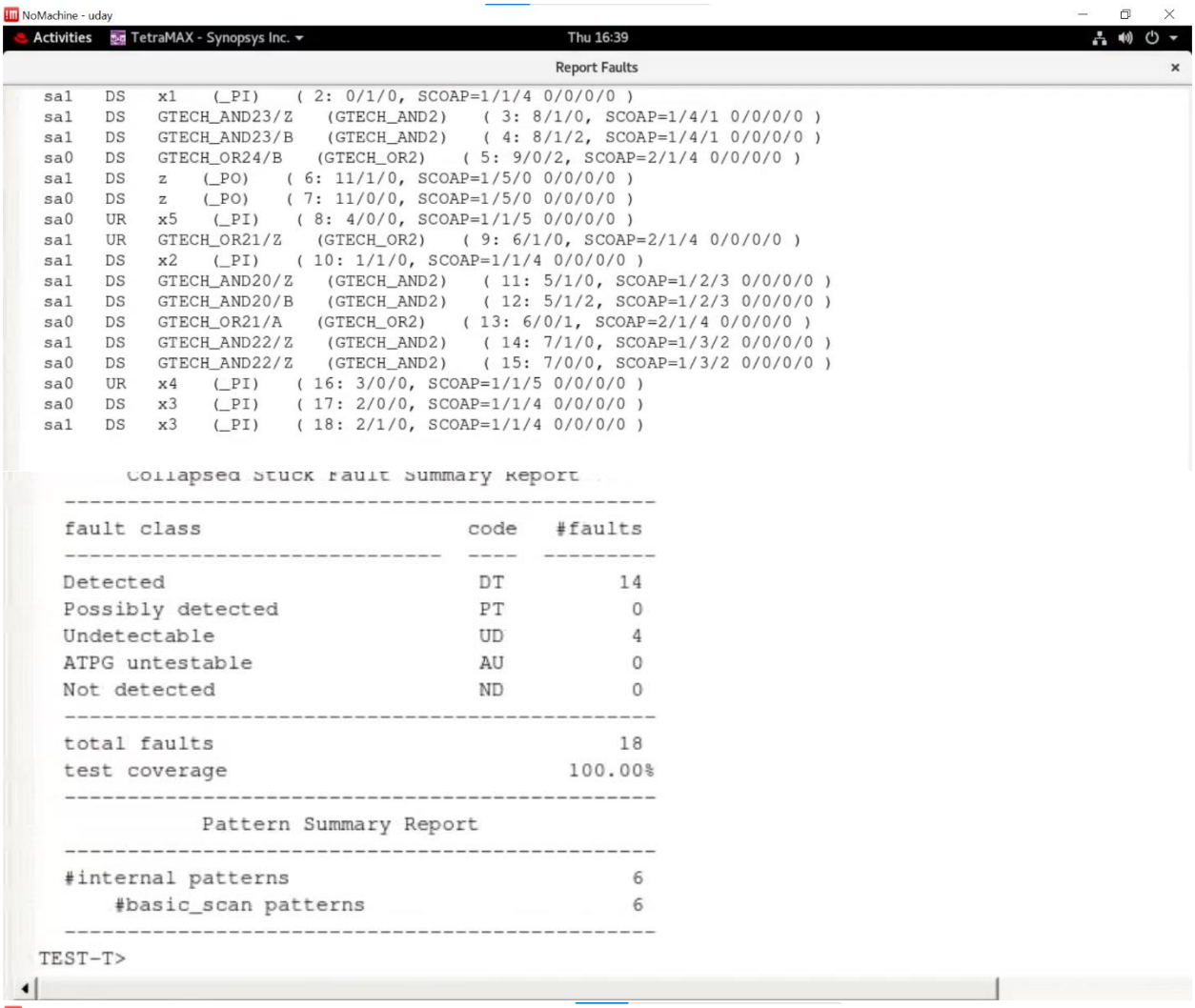
```
module Q3_3_37(x1,x2,x3,x4,x5,z);
input x1,x2,x3,x4,x5;
output z;
wire c1,c2,c3,c4,c5;

 and g1(c1,x2,x3);
 or g2(c2,x3,x4);
 and g3(c3,c1,c2);
 and g4(c4,x1,c3);
 or g5(c5,x5,c3);
 and g6(z,c4,c5);

endmodule
```

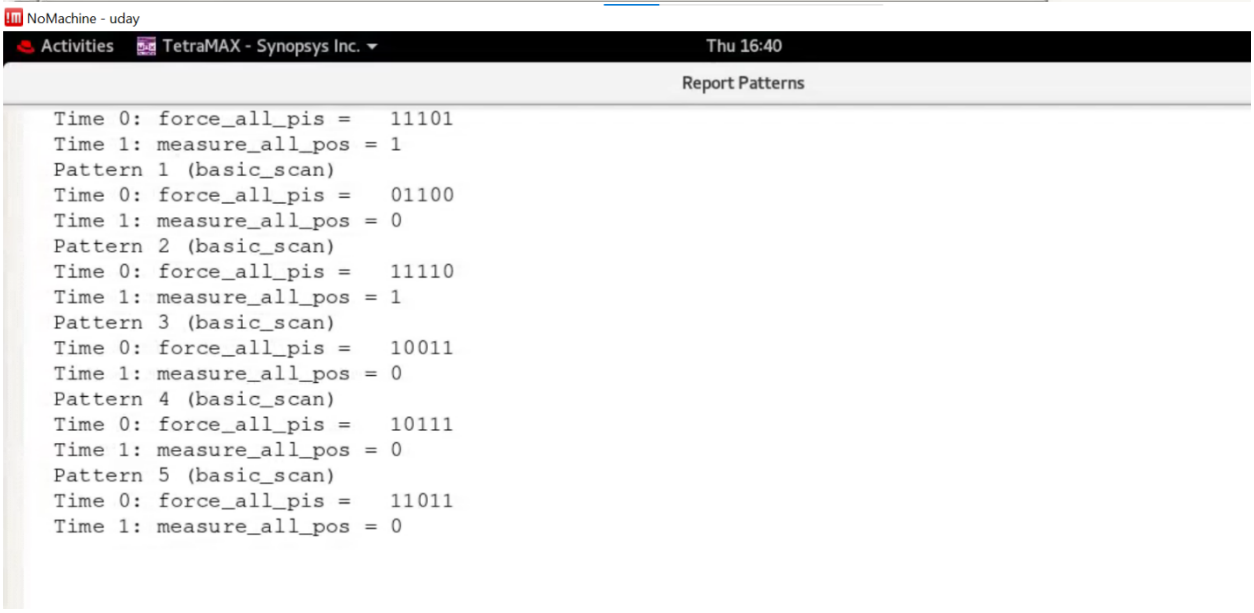

NoMachine - uday
Activities
TetraMAX - Synopsys Inc.
Thu 16:37
TetraMAX - Synopsys Inc.
File Edit View Netlist Rules Scan Primitives Faults Patterns Buses Constraints Loops Run Analyze Report Help
Cmd
Save Transcript
Transcript
Increase Font
Decrease Font
Close GSV
Hierarchy Browser
Waveform View
Messages Netlist Build DRC Summary ATPG Write Pat. Write Testbench Simulation Fault Sim. Analyze Diagnosis Exit
Zoom In
Zoom Out
Zoom Reset
Zoom Full
Zoom Tool by Box
Refresh
Setup
Show
Hide
Analyze
Schematic
GTECH_AND2
GTECH_OR2
EPWave
From:
0ps
To:
105,000ps
Get Signals
Radix
100%
x1
x2
x3
x4
x5
z
Note: To revert to EPWave opening in a new browser window, set that option on your user page.

```
DRC-T> run_drc
  ---------------------------------------------------------------------------
  Begin scan design rules checking...
  ---------------------------------------------------------------------------
  Begin simulating test protocol procedures...
  Test protocol simulation completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  Begin scan chain operation checking...
  Scan chain operation checking completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  Begin nonscan rules checking...
  Nonscan cell summary: #DFF=0  #DLAT=0  #RAM_outs=0  tla_usage_type=none
  Nonscan rules checking completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  Begin DRC dependent learning...
  Fast-sequential depth results: control=0(0), observe=0(0), detect=0(0), CPU time=0.00 sec
  DRC dependent learning completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  DRC Summary Report
  ---------------------------------------------------------------------------
  No violations occurred during DRC process.
  Design rules checking was successful, total CPU time=0.00 sec.
  ---------------------------------------------------------------------------
```

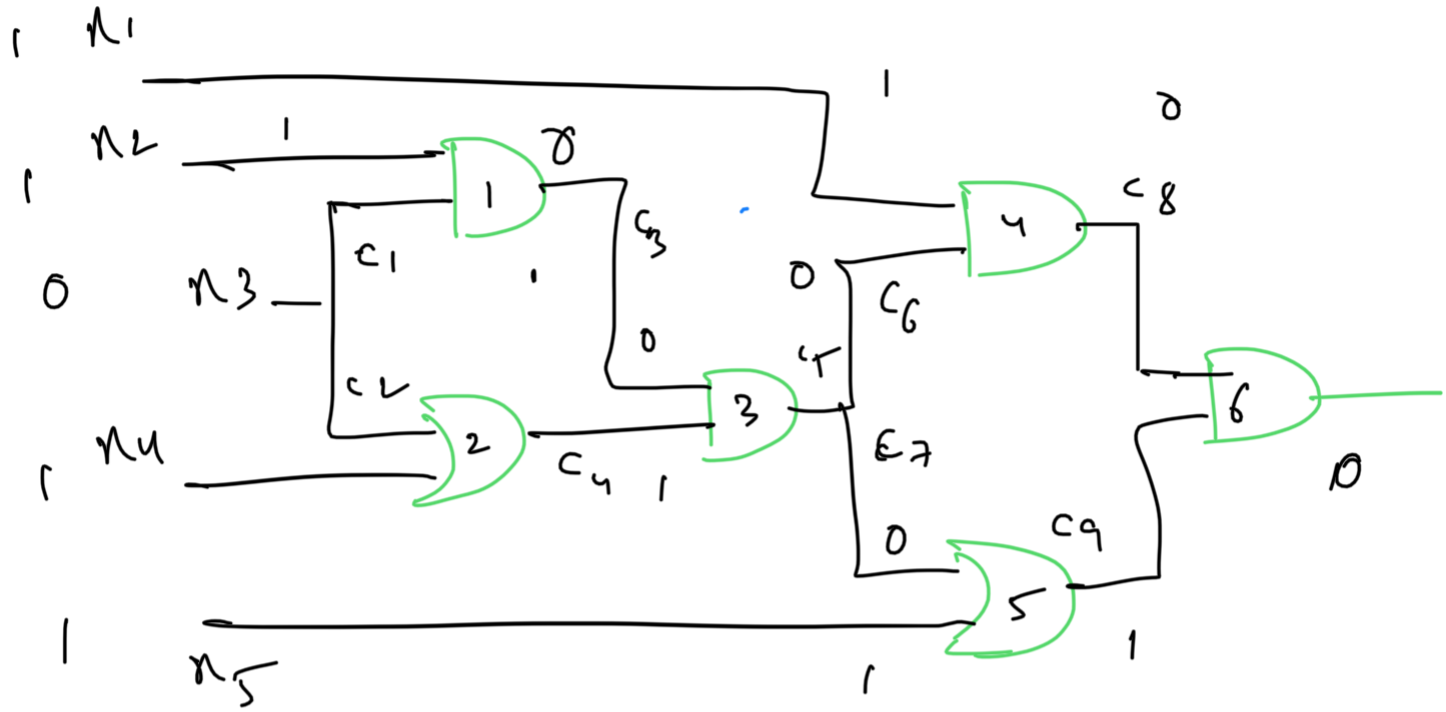
```
  End parsing Verilog file /home/013/u/ut/utb220000/Spring24/TTD/WORK/c3_3_37.v with 0 errors.
  End reading netlist: #modules=0, top=Q3_3_37, #lines=13, CPU_time=0.00 sec, Memory=0MB
BUILD-T> run_build_model Q3_3_37
  ---------------------------------------------------------------------------
  Begin build model for topcut = Q3_3_37 ...
  ---------------------------------------------------------------------------
  There were 0 primitives and 0 faultable pins removed during model optimizations
  End build model: #primitives=12, CPU_time=0.00 sec, Memory=0MB
  ---------------------------------------------------------------------------
  Begin learning analyses...
  End learning analyses, total learning CPU time=0.00 sec.
  ---------------------------------------------------------------------------
```

```
TEST-T> add_faults -all
  18 faults were added to fault list.
TEST-T> run_atpg -ndetects 1
  ATPG performed for stuck fault model using internal pattern source.
  ----------------------------------------------------------------
  #patterns     #faults     #ATPG faults  test      process
  stored     detect/active  red/au/abort  coverage  CPU time
  ---------  -------------  ------------  --------  --------
  Begin deterministic ATPG: #collapsed_faults=18, abort_limit=10...
  6              14       0         4/0/0   100.00%      0.00

       Collapsed Stuck Fault Summary Report
  -----------------------------------------------
  fault class                     code   #faults
  ------------------------------  ----  ---------
  Detected                         DT         14
  Possibly detected                PT          0
  Undetectable                     UD          4
  ATPG untestable                  AU          0
  Not detected                     ND          0
  -----------------------------------------------
  total faults                                18
  test coverage                           100.00%
  -----------------------------------------------
```


NoMachine - uday
Activities
TetraMAX - Synopsys Inc.
Thu 16:39
Report Faults
sa1 DS x1 (_PI) (2: 0/1/0, SCOAP=1/1/4 0/0/0/0)
sa1 DS GTECH_AND23/Z (GTECH_AND2) (3: 8/1/0, SCOAP=1/4/1 0/0/0/0)
sa1 DS GTECH_AND23/B (GTECH_AND2) (4: 8/1/2, SCOAP=1/4/1 0/0/0/0)
sa0 DS GTECH_OR24/B (GTECH_OR2) (5: 9/0/2, SCOAP=2/1/4 0/0/0/0)
sa1 DS z (_PO) (6: 11/1/0, SCOAP=1/5/0 0/0/0/0)
sa0 DS z (_PO) (7: 11/0/0, SCOAP=1/5/0 0/0/0/0)
sa0 UR x5 (_PI) (8: 4/0/0, SCOAP=1/1/5 0/0/0/0)
sa1 UR GTECH_OR21/Z (GTECH_OR2) (9: 6/1/0, SCOAP=2/1/4 0/0/0/0)
sa1 DS x2 (_PI) (10: 1/1/0, SCOAP=1/1/4 0/0/0/0)
sa1 DS GTECH_AND20/Z (GTECH_AND2) (11: 5/1/0, SCOAP=1/2/3 0/0/0/0)
sa1 DS GTECH_AND20/B (GTECH_AND2) (12: 5/1/2, SCOAP=1/2/3 0/0/0/0)
sa0 DS GTECH_OR21/A (GTECH_OR2) (13: 6/0/1, SCOAP=2/1/4 0/0/0/0)
sa1 DS GTECH_AND22/Z (GTECH_AND2) (14: 7/1/0, SCOAP=1/3/2 0/0/0/0)
sa0 DS GTECH_AND22/Z (GTECH_AND2) (15: 7/0/0, SCOAP=1/3/2 0/0/0/0)
sa0 UR x4 (_PI) (16: 3/0/0, SCOAP=1/1/5 0/0/0/0)
sa0 DS x3 (_PI) (17: 2/0/0, SCOAP=1/1/4 0/0/0/0)
sa1 DS x3 (_PI) (18: 2/1/0, SCOAP=1/1/4 0/0/0/0)
Collapsed Stuck Fault Summary Report
fault class code #faults
Detected DT 14
Possibly detected PT 0
Undetectable UD 4
ATPG untestable AU 0
Not detected ND 0
total faults 18
test coverage 100.00%
Pattern Summary Report
#internal patterns 6
#basic_scan patterns 6
TEST-T>


NoMachine - uday
Activities
TetraMAX - Synopsys Inc.
Thu 16:40
Report Patterns
Time 0: force_all_pis = 11101
Time 1: measure_all_pos = 1
Pattern 1 (basic_scan)
Time 0: force_all_pis = 01100
Time 1: measure_all_pos = 0
Pattern 2 (basic_scan)
Time 0: force_all_pis = 11110
Time 1: measure_all_pos = 1
Pattern 3 (basic_scan)
Time 0: force_all_pis = 10011
Time 1: measure_all_pos = 0
Pattern 4 (basic_scan)
Time 0: force_all_pis = 10111
Time 1: measure_all_pos = 0
Pattern 5 (basic_scan)
Time 0: force_all_pis = 11011
Time 1: measure_all_pos = 0

Question - 3.

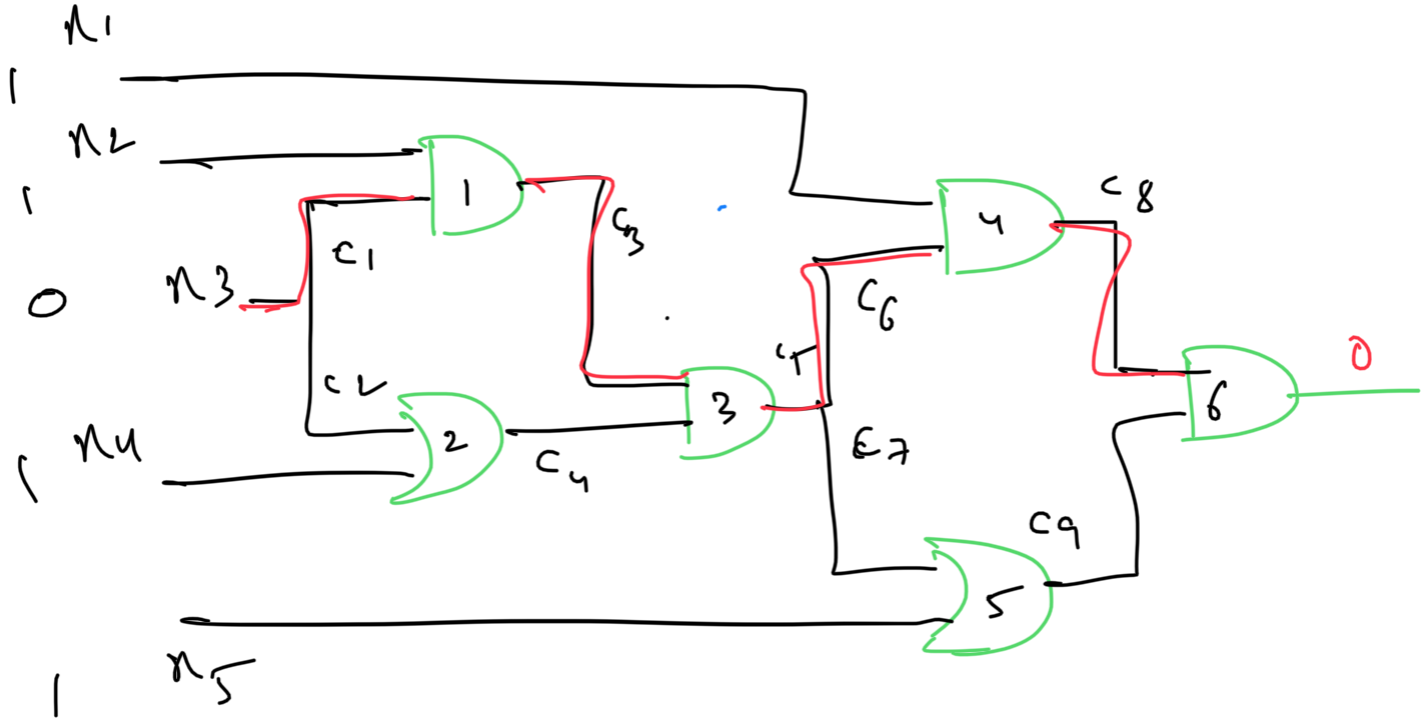


faults := x_1 sa1 x_2 sa0 x_2 sa1 x_3 sa0 x_3 sa1

x_4 sa0 x_4 sa1 x_3 sa1 c_1 sa1 c_2 sa0

c_6 sa0 c_6 sa1 c_7 sa0 c_7 sa1

critical path



$$\text{faults} = c_6\,sa1 \qquad c_1\,sa1 \quad x_3\,sa1$$