The University of Texas at Dallas
Dept. of Electrical and Computer Engineering

EEDG/CE 6303: Testing and Testable Design
HW # 3: *Due on Monday, Oct. 11, 2021 - 12:00 pm NOON (US CST)*

When you submit your homeworks, to help us grade and identify your work, you need to comply with the following guidelines carefully:

- *Have* **a cover page** *for each document (e.g. homework, project, report, etc.) that you submit. A sample of cover page is provided in the course webpage. This page must include: (1) your name as it appears in your* **student ID card***, (2) course name/number, (3) homework/project number, and (4) the* **Statement of Academic Honesty** *that you sign.*

1. For two circuits shown in Figures 3.23 and 3.34 of your text book (exactly as they are with no change to an equivalent topology) and for patterns $x_1x_2 = 00$ and $x_1x_2 = 11$ (for Figure 3.23) and patterns $x_1x_2x_3 = 001$ and $x_1x_2x_3 = 110$ (for Figure 3.34):

   (a) Demonstrate **parallel** fault simulation.

   (b) Demonstrate **deductive** fault simulation.

   (c) Demonstrate **concurrent** fault simulation.

   (d) Demonstrate **critical path tracing** fault simulation

2. For the two circuits shown in Figures 3.23 and 3.34 of your text book (exactly as shown),

   (a) Calculate all SCOAP measures.

   (b) Calculate the testability index for the circuit and comment on it.

3. Consider Figure 5.5 in your book. Assume FF is a D flip-flop without any set/reset line. Analyze this sequential circuit for 4 stuck-at faults: (i) x_1 s-a-0, (ii) x_1 s-a-1, (iii) x_2 s-a-0, (iv) x_2 s-a-1.

4. Consider Figure 5.27 in your book. Assume FF is a D flip-flop without any set/reset line. Analyze this sequential circuit for 4 stuck-at faults: (i) x_1 s-a-0, (ii) x_1 s-a-1, (iii) x_2 s-a-0, (iv) x_2 s-a-1.

5. Consider Figure 5.5 in your book. Use Synopsys toolset to implement two versions of it: (i) with D-FF without any set/reset, and (ii) with D-FF with set/reset. Run ATPG for sequential circuits in Tetramax on both versions and report and discuss the results.

   Note: Your report should include HDL (VHDL or Verilog) description, schematic of the circuit, some simulations to show the correct behavior, test analysis by Tetramax (e.g. faults, test patterns) and any other interesting observations.