

EEDG/CE 6303: Testing and Testable Design (Spring'2024)

Department of Electrical & Computer Engineering

The University of Texas at Dallas

Instructor: Mehrdad Nourani (nourani@utdallas.edu)

Cover Page for All Submissions

(Assignment, Project, Codes/Simulations/CAD, Examinations, etc.)

Last Name (as shown in the official UT Dallas Student ID Card): _____ Bandaru

First Name: _____ Uday Teja

Submission Materials for (e.g. Homework #, Project #): _____ Homework 3

Statement of Academic Honesty

I certify that:

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- ii. I have acknowledged/cited all material and sources used in its preparation, whether they be books, articles, reports, lecture notes, and any other kind of document, electronic or personal communication,
- iii. I have not used **generative AI (e.g. ChatGPT or similar tools)** in preparing this report,
- iv. this report has not previously been submitted for assessment in EEDG/CE 6303 or any other course at UT Dallas or elsewhere,
- v. I have not copied in part or whole or otherwise plagiarized the work of other students and/or persons, and
- vi. I have read and understood the Department and University policies on scholastic dishonesty as outlined in: <http://www.utdallas.edu/deanofstudents/dishonesty/>.

Name: _____ Uday Teja Bandaru

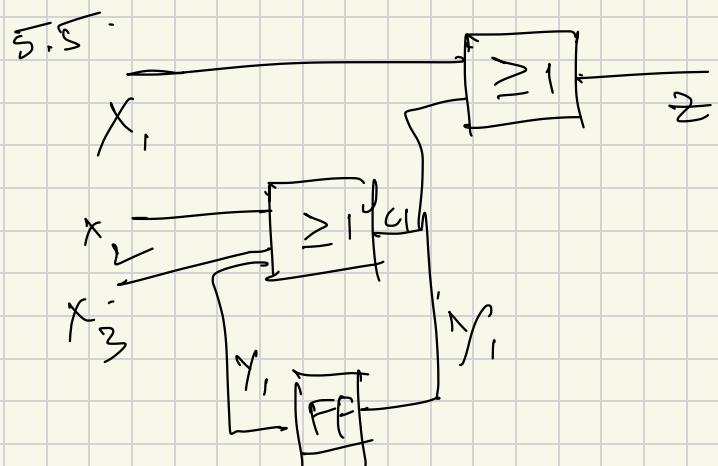
Date: _____ 03/7/2024

Uday Teja Bandaru

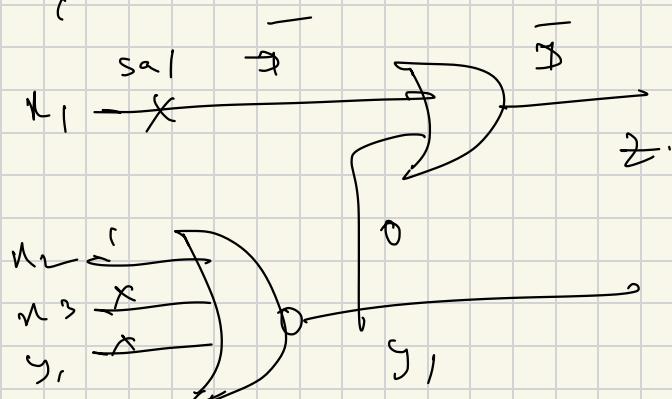
Signature: _____

T TD HW3

Uday Teja Bandaru
UTB220000.



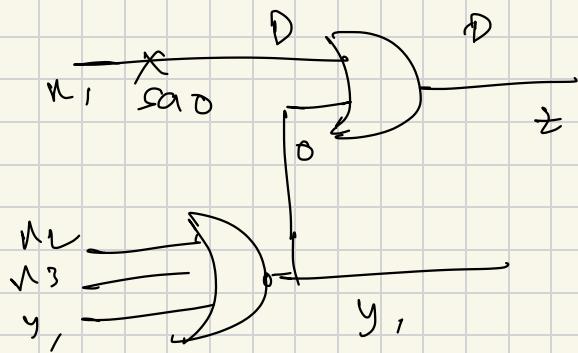
(i) n_c sa 1



Sequence = $(n_1, n_2, n_3) = (0, 1, x)$

$$\begin{array}{c} 0 \text{ or } 1 \\ \text{or } (0 \times 1) \rightarrow 001, 011 \end{array}$$

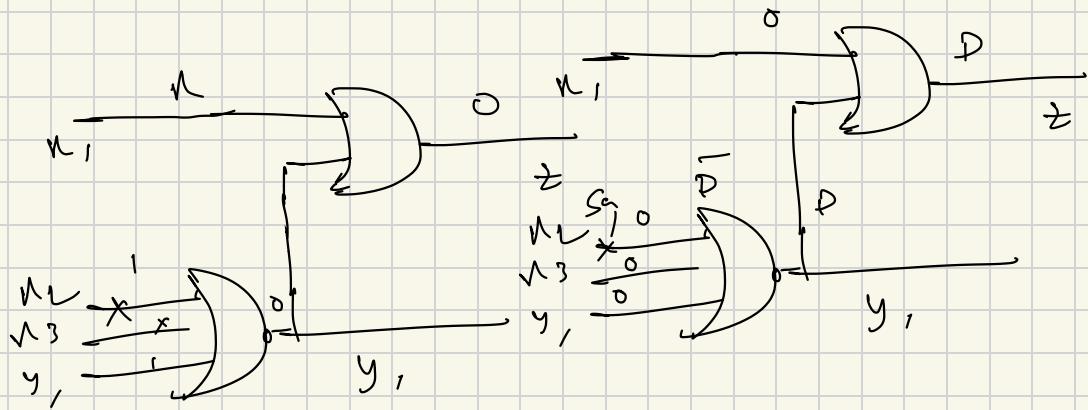
(ii) $n_1 = 0$



Sequence = $n_1, n_2, n_3 = 0, 1, x$
or
 $\begin{cases} 0 \\ 1 \end{cases}$

$$(x) \rightarrow 001, 011$$

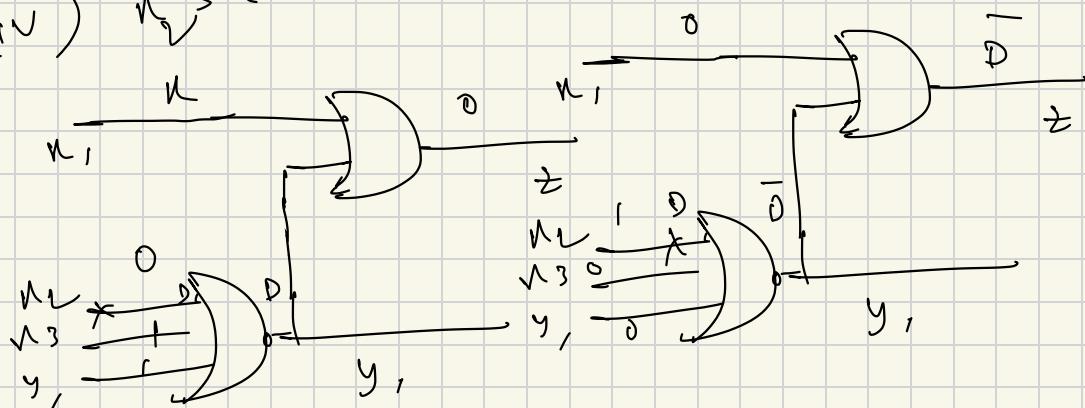
(iii) $n_2 \text{sa}_1$



Sequence $(n_1, n_2 \rightarrow n_3) =$

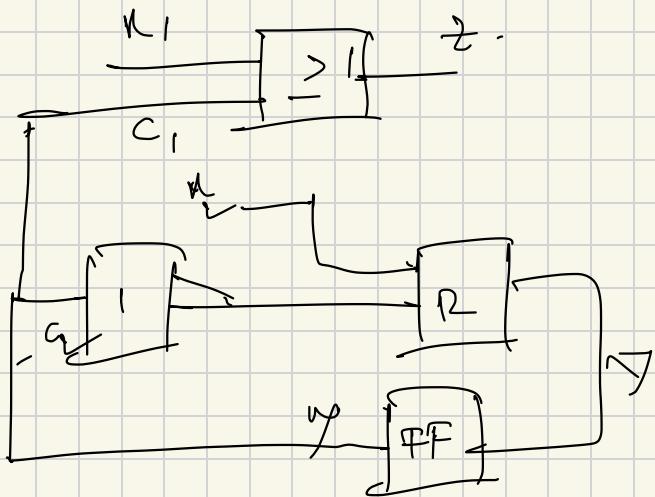
$x1x, 000$

(iv) $n_2 \text{sa}^0$

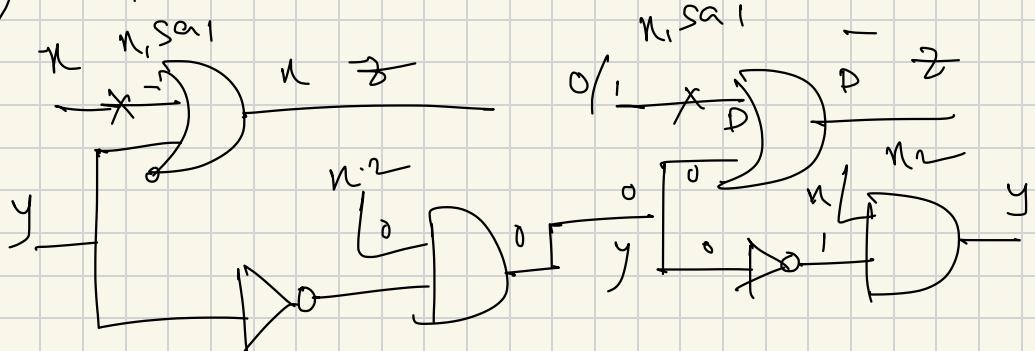


Sequence = $x1^n, 0^m$

5.27

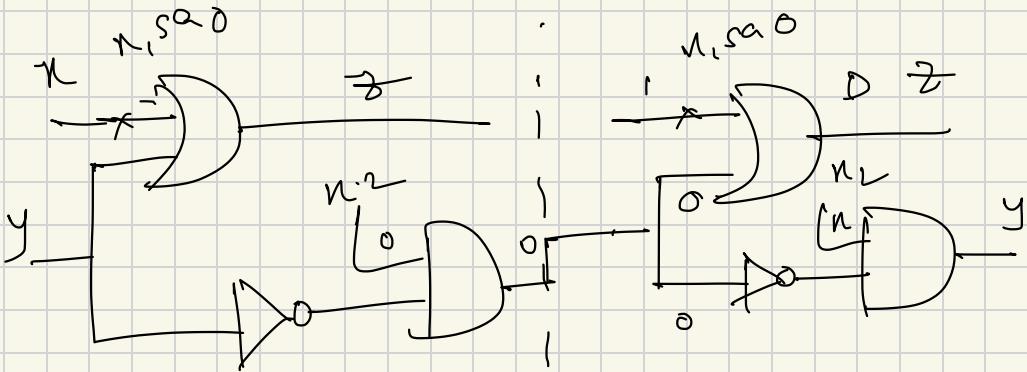


(i) n_1, sa_1



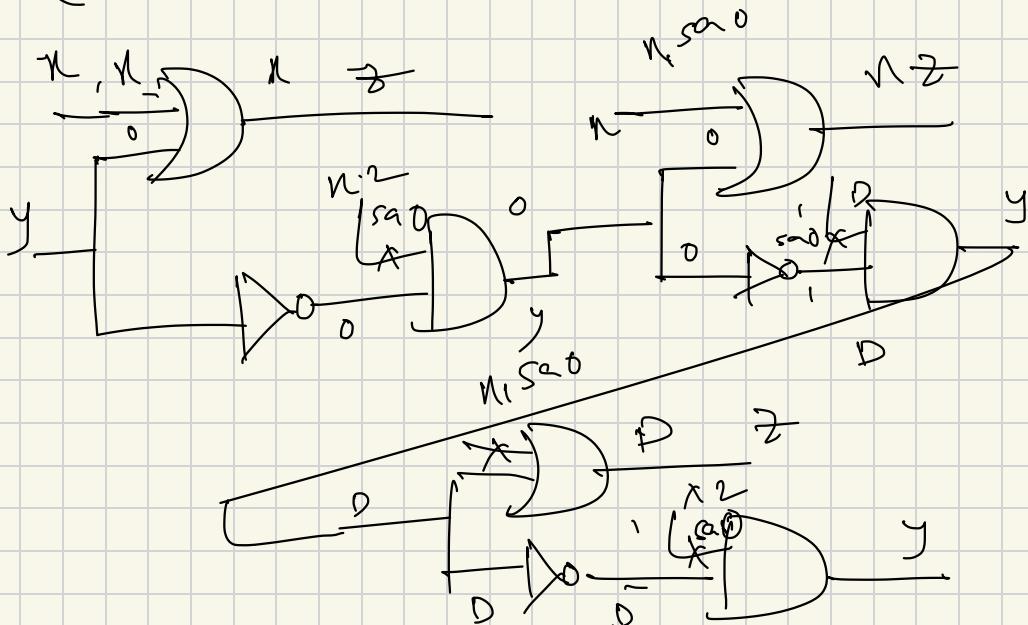
Pattern = $\{x0 \quad 10x\}$

(ii) $n_1, n_2, 0$



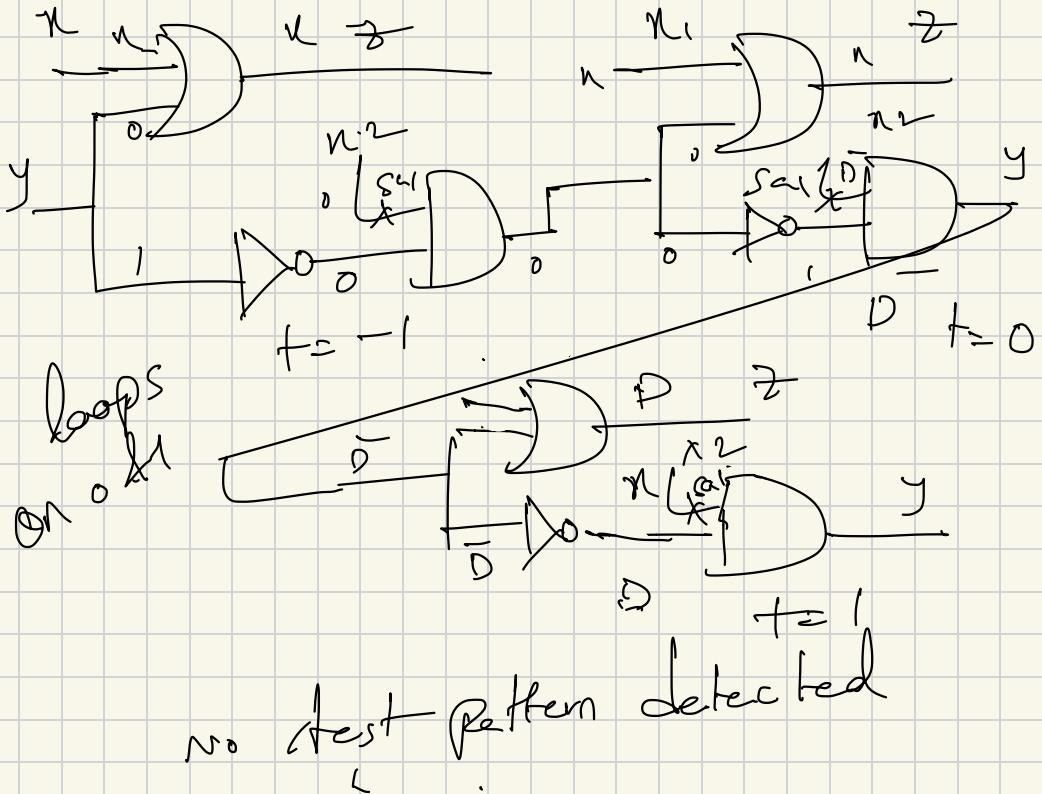
$$\text{Pattern} = \overline{x_0} \quad 1x$$

(iii)



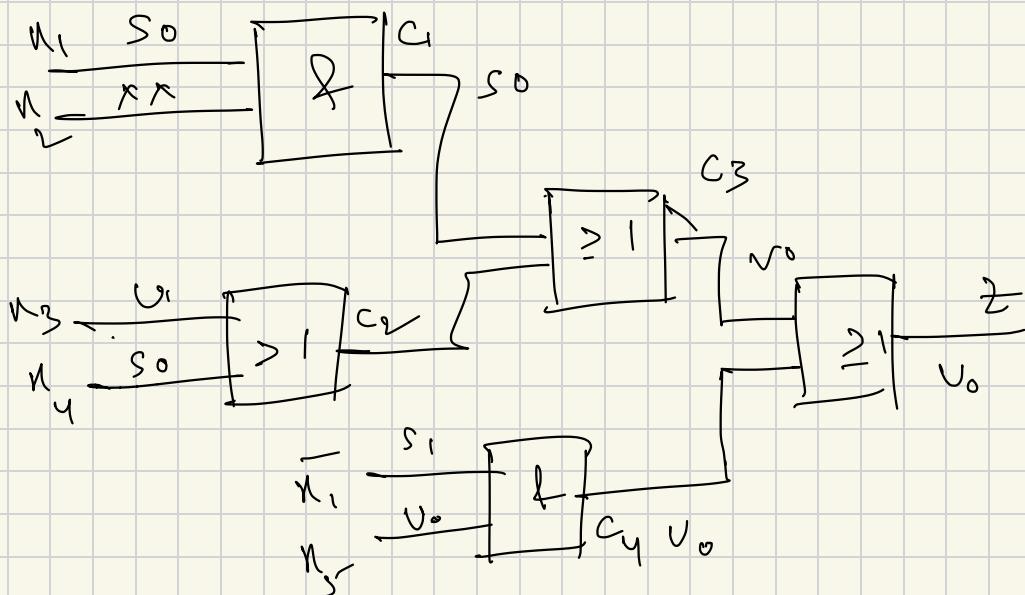
$$\text{Pattern} = n_1, n_2 = x_0 \quad x_1 \quad 0x$$

(iv) n_1 SAI



8.1.3

(i) $\kappa_3 c_2 c_3 t$
Robust

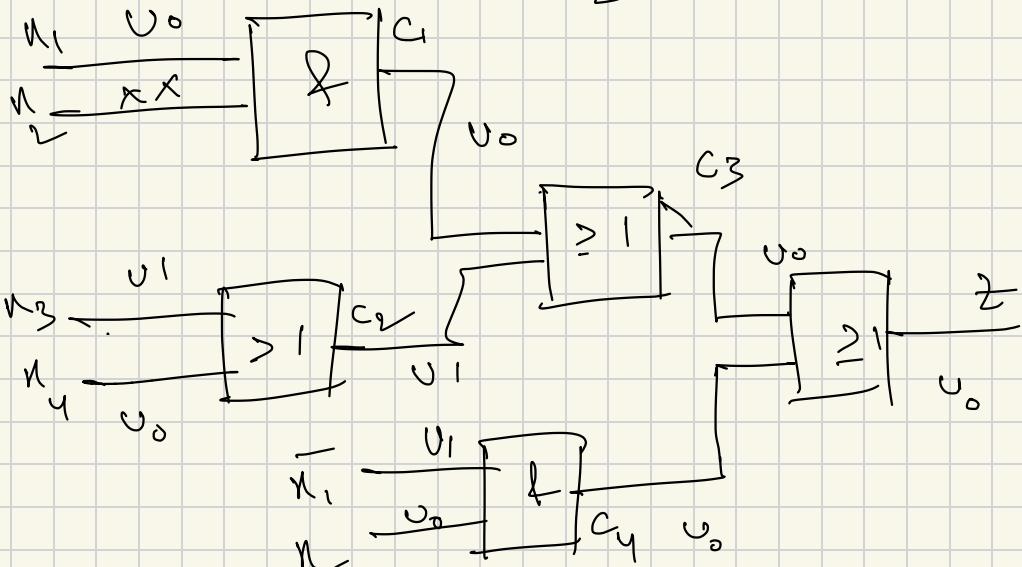


$\uparrow \kappa_3 c_2 c_3 t$

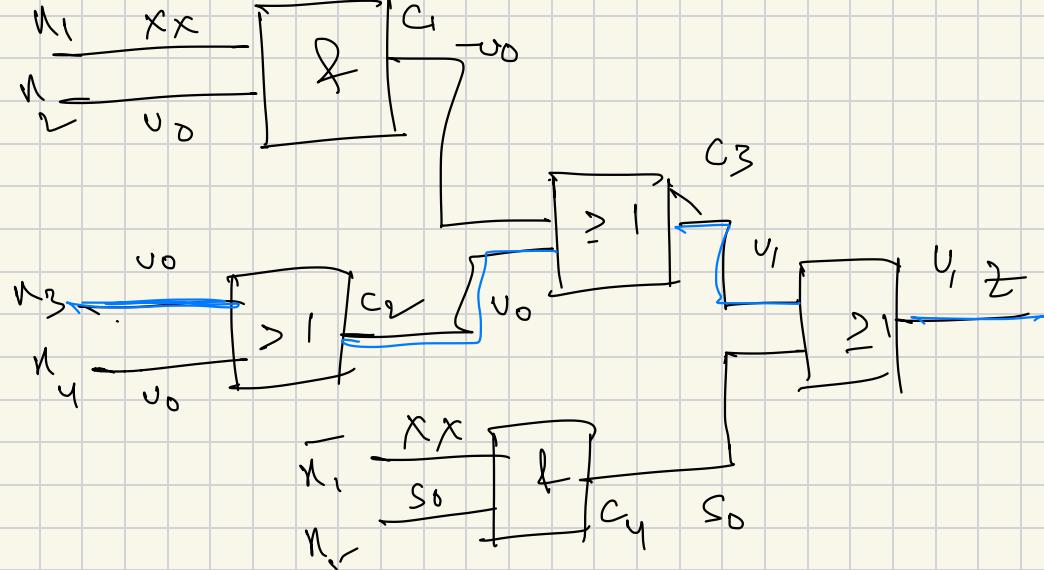
Pattern = $0 \times 0 0 x, 0 \times 1 0 0$

Non Robust

$\uparrow n_3 c_2 c_3 t$.

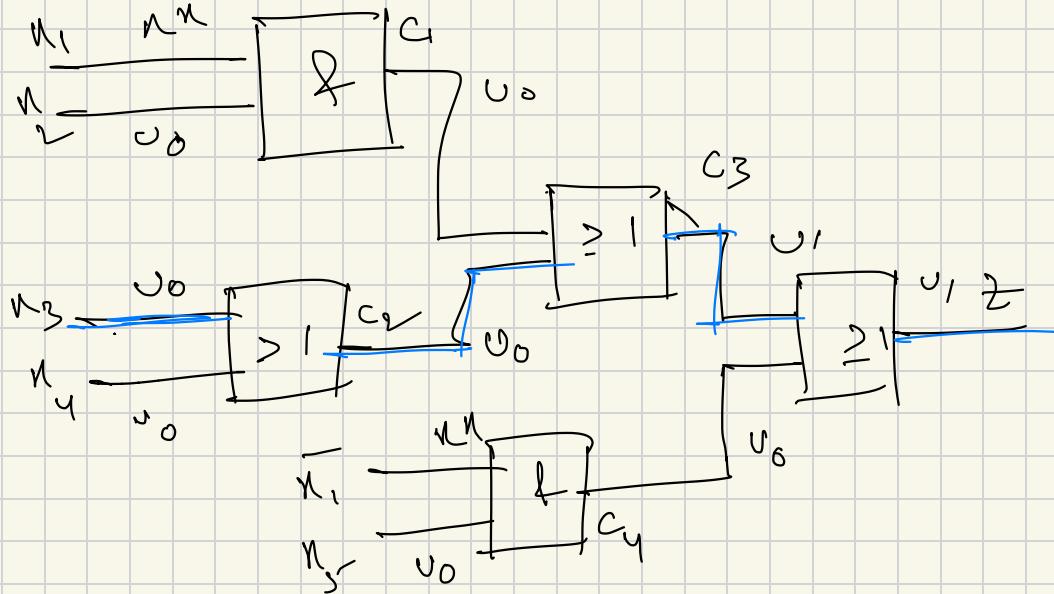


ii) Robust pattern



$\downarrow n_3 c_2 c_3 t$, pattern = $xx1x0, x0000$

Non Robust pattern

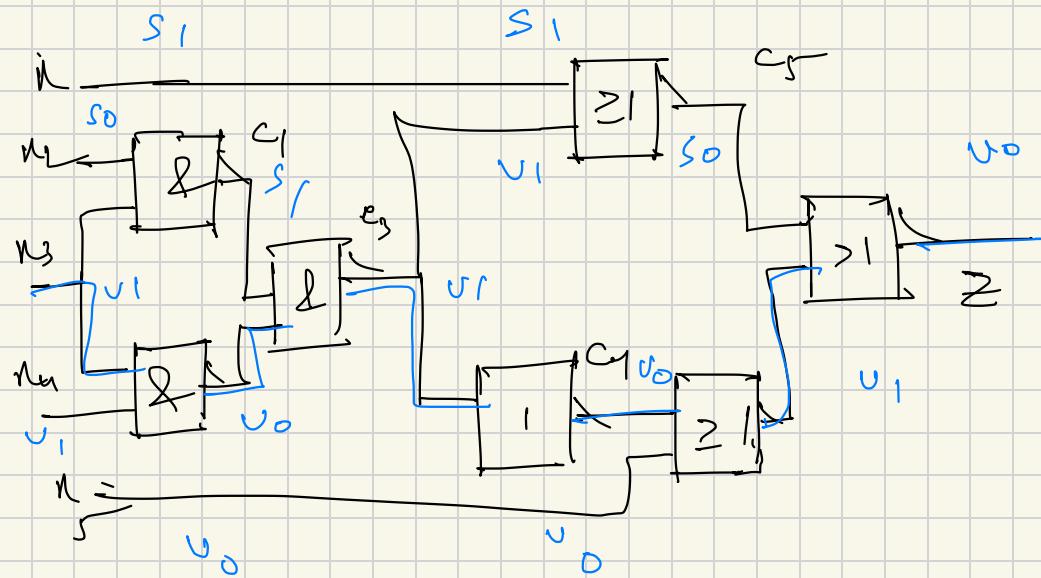


$\downarrow n_3 \wedge n_2 \wedge n_1 \neq$

Pattern = $xx1xx, x0000.$

8.20

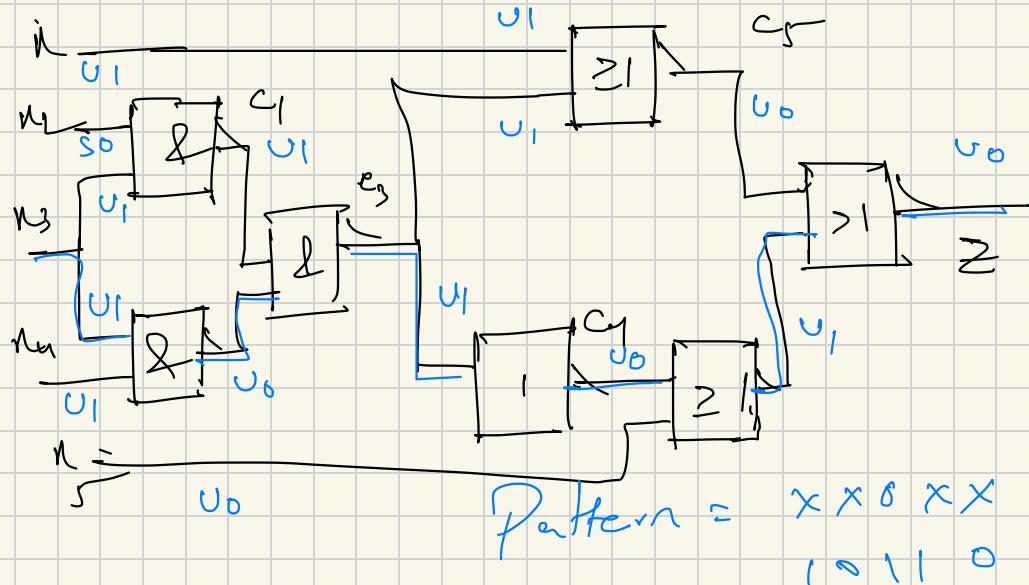
Robust Pattern



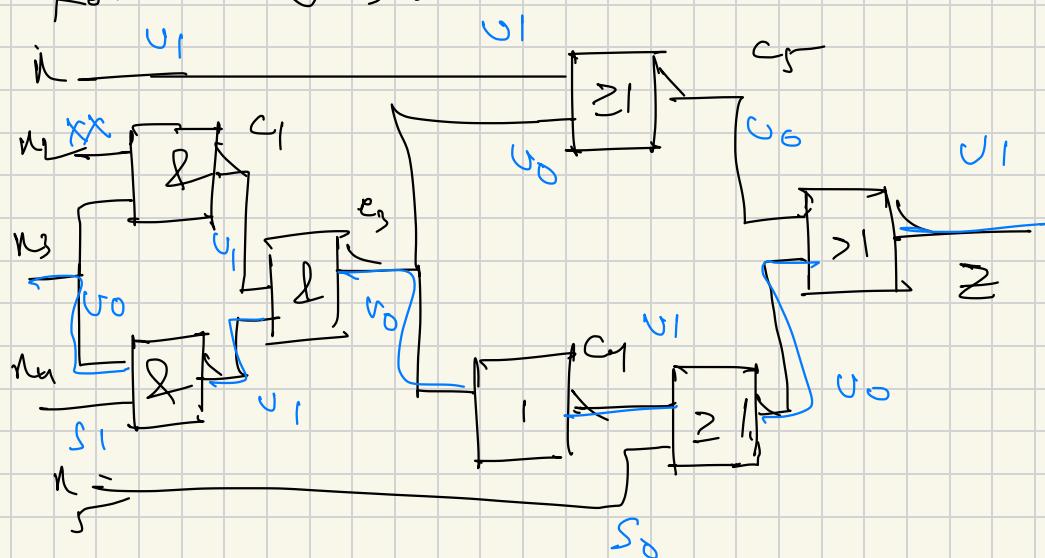
Pattern = $100 \times x$

10110

non Robust pattern = $\uparrow n_3 c_2 c_3 c_4 c_6 \uparrow$



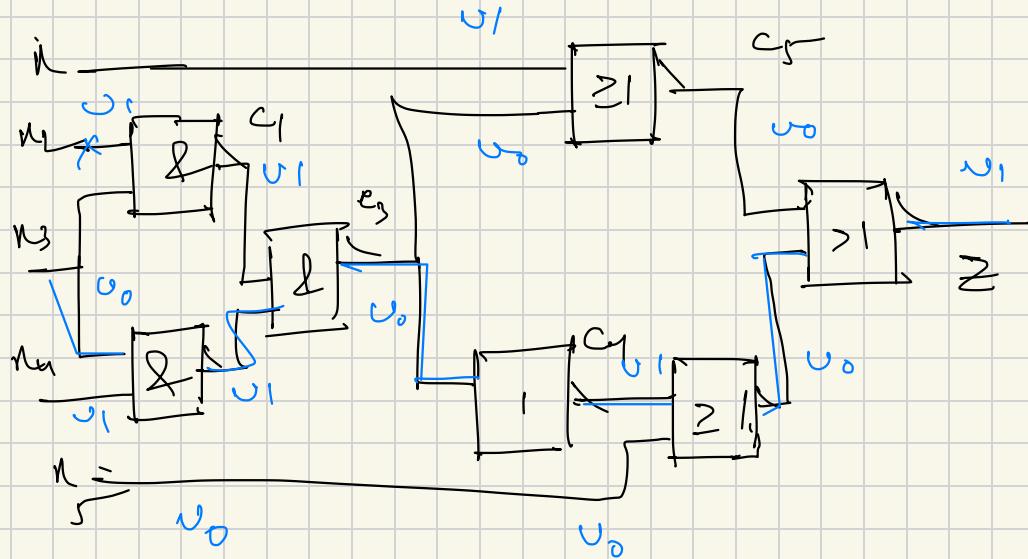
Robust $\downarrow n_3 c_2 c_3 c_4 c_6 \uparrow$



Pattern = $\begin{matrix} x & \wedge & 1 & 1 & 0 \\ 1 & x & 0 & 1 & 0 \end{matrix}$

Non Robust - Pattern

$\downarrow n_3 c_2 c_3 c_4 c_6 z$



$$\text{Pattern} = xx1xx$$

7x010

Question 3

**Figure 5.5 with DFF without rst and st
block, build, drc, atpg, faults and patterns**

```
module Dff_nsr(x1,x2,x3,clk,Q,y1n);
    input x1, x2,x3,clk;
    output Q,y1n;
    wire c1,y1;
    GTECH_OR2 (x1,c1,Q);
    GTECH_NOR3 (x2,x3, y1,c1);
    GTECH_FD1 (c1, clk, y1, y1n);

Endmodule
```

Testbench

```
`timescale 1ns/1ps

module Dff_3_1_tb();
    reg clk, x1, x2, x3;
    wire Q;

    Dff_nsr uut( .clk(clk), .x1(x1), .x2(x2), .x3(x3), .Q(Q));

    always #10 clk = ~clk;

    initial begin
        $dumpfile("dump.vcd");
```

```
$dumpvars;  
end  
  
initial begin  
clk <= 0;  
  
x1 <= 1; x2 <= 1; x3 <= 0;  
#10  
x1 <= 0; x2 <= 1; x3 <= 0;  
#10  
x1 <= 0; x2 <= 0; x3 <= 1;  
#10  
x1 <= 0; x2 <= 0; x3 <= 0;  
#10  
x1 <= 1; x2 <= 1; x3 <= 0;  
#10  
x1 <= 0; x2 <= 1; x3 <= 0;  
#10  
x1 <= 0; x2 <= 0; x3 <= 1;  
#10  
x1 <= 0; x2 <= 0; x3 <= 0;  
#10  
x1 <= 1; x2 <= 1; x3 <= 0;  
#10  
x1 <= 0; x2 <= 1; x3 <= 0;  
#10  
x1 <= 0; x2 <= 0; x3 <= 1;  
#10  
x1 <= 0; x2 <= 0; x3 <= 0;  
#10
```

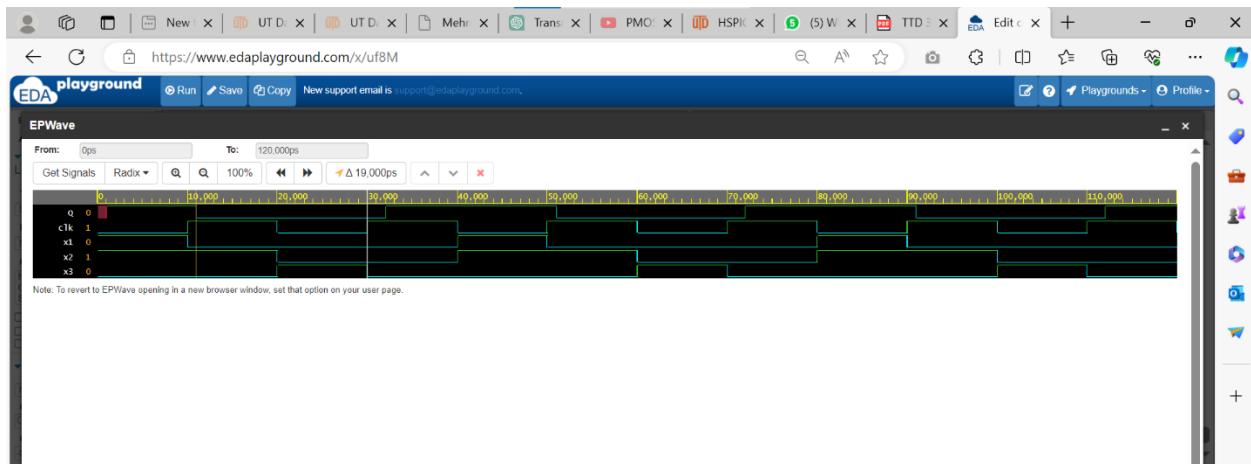
```
x1 <= 0; x2 <= 0; x3 <= 0;
```

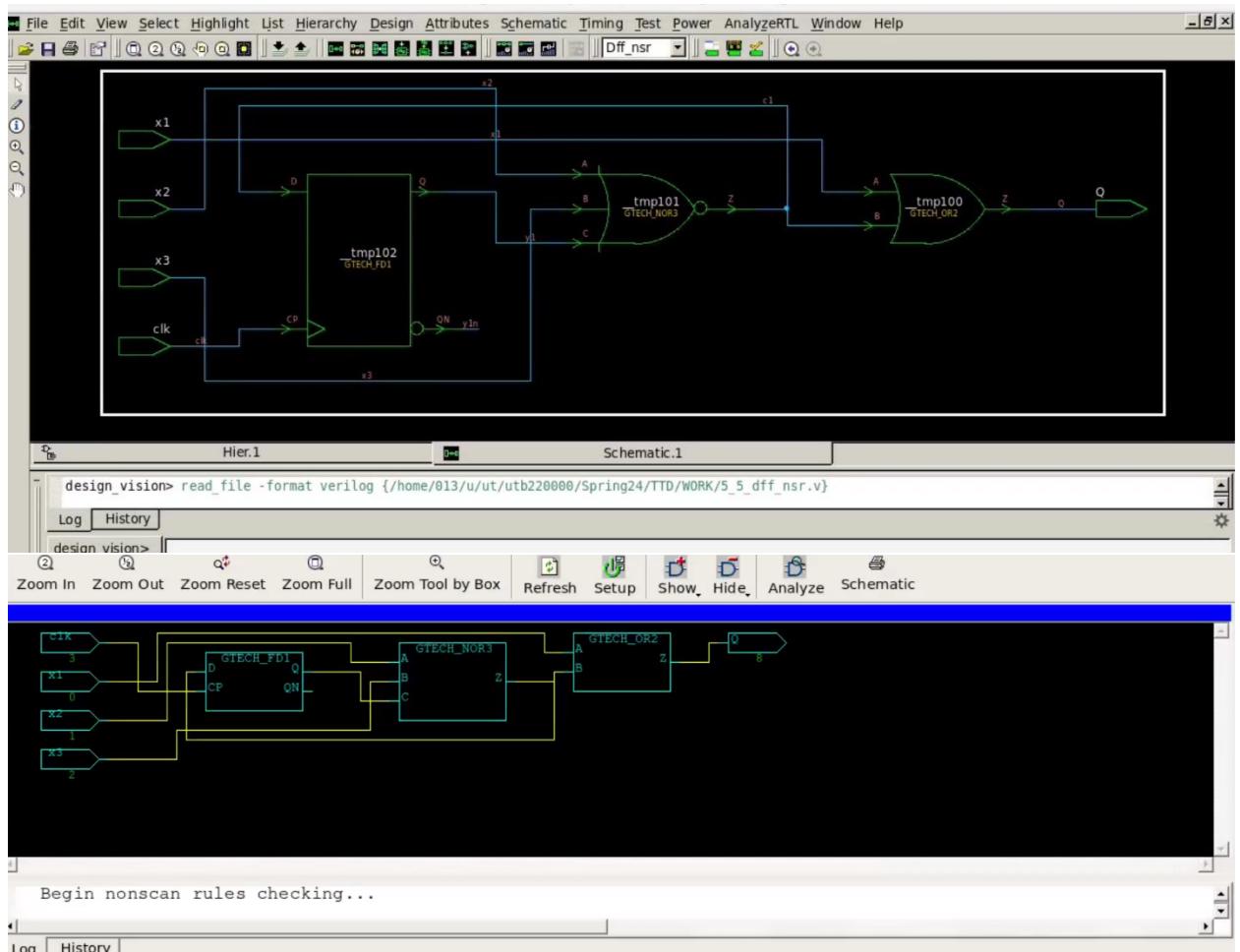
```
#10
```

```
$finish;
```

```
end
```

```
endmodule
```





```
Begin reading netlist ( /home/013/u/ut/utb220000/Spring24/TTD/WORK/gtech_lib.v )...
Warning: Rule N2 (unsupported construct) was violated 10 times.

Warning: Rule N5 (redefined module) was violated 106 times.

End parsing Verilog file /home/013/u/ut/utb220000/Spring24/TTD/WORK/gtech_lib.v with 0 errors.
End reading netlist: #modules=0, top=dff_sr, #lines=1976, CPU_time=0.00 sec, Memory=0MB
BUILD-T> read_netlist /home/013/u/ut/utb220000/Spring24/TTD/WORK/5_5_dff_nsr.v
Begin reading netlist ( /home/013/u/ut/utb220000/Spring24/TTD/WORK/5_5_dff_nsr.v )...
Warning: Rule N5 (redefined module) was violated 1 times.

End parsing Verilog file /home/013/u/ut/utb220000/Spring24/TTD/WORK/5_5_dff_nsr.v with 0 errors.
End reading netlist: #modules=0, top=dff_sr, #lines=11, CPU_time=0.00 sec, Memory=0MB
BUILD-T>
```



```
-----  
Begin DRC dependent learning...  
Fast-sequential depth results: control=0(0), observe=0(0), detect=0(0), CPU time=0.00 sec  
DRC dependent learning completed, CPU time=0.00 sec.  
-----
```

```
DRC Summary Report
```

```
-----  
Warning: Rule C2 (unstable nonscan DFF when clocks off) was violated 1 times.
```

```
There were 1 violations that occurred during DRC process.  
Design rules checking was successful, total CPU time=0.00 sec.
```

```
TEST-T>
```



```
End reading netlist: #modules=0, top=dff_sr, #lines=11, CPU_time=0.00 sec, Memory=0MB
BUILD-T> run_build_model Dff_nsr
```

```
-----  
Begin build model for topcut = Dff_nsr ...
```

```
-----  
There were 3 primitives and 1 faultable pins removed during model optimizations  
Warning: Rule B10 (unconnected module internal net) was violated 1 times.
```

```
End build model: #primitives=9, CPU_time=0.00 sec, Memory=0MB
```

```
-----  
Begin learning analyses...  
End learning analyses, total learning CPU time=0.00 sec.
```

```
-----  
DRC-T>
```

```
| Log History |
```

```
DRC-T> |
```

```
| ready |
```

```
| Pin Data: None | Stop | Build | DRC | Test |
```

```
| engnx04a.utdallas.edu:/home/013... | TetraMAX - Synopsys Inc. | [Design Vision - TopLevel.1 (Dff... | 5.5_dff_nsr.v (~/Spring24/TTD/... |
```

```
| 1 / 2 |
```

1 NoMachine - uday

Activities Applications ▾ Places ▾ TetraMAX - Synopsys Inc. ▾ Thu 17:42

TetraMAX - Synopsys Inc.

File Edit View Netlist Rules Scan Primitives Faults Patterns Buses Constraints Locations

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Messages Netlist Build DRC Summary ATPG Write Pat. Write Testbench S

fault class	code	#faults
Detected	DT	30
Possibly detected	PT	0
Undetectable	UD	0
ATPG untestable	AU	0
Not detected	ND	0
total faults		30
test coverage		100.00%

Pattern Summary Report

#internal patterns	6
#basic_scan patterns	2
#full_sequential patterns	4

Log History

TEST-T> |||

eady |

engnx04a.utdallas.edu:/home/013... TetraMAX - Synopsys Inc. [Design Vision - Te

NoMachine - uday

Activities Applications Places TetraMAX - Synopsys Inc. Thu 17:43

Report Faults

```

File
C   sal  DS  Q  (_PO)  ( 1: 8/1/0, SCOAP=2/1/0 0/0/0/0 )
C   sa0  DS  GTECH_OR20/B  (GTECH_OR2)  ( 2: 6/0/2, SCOAP=2/1/0 0/0/0/0 )
M   sa0  DS  Q  (_PO)  ( 3: 8/0/0, SCOAP=2/1/0 0/0/0/0 )
M   sa0  DS  x1  (_PI)  ( 4: 0/0/0, SCOAP=1/1/1 0/0/0/0 )
M   sal  DS  GTECH_NOR31/Z  (GTECH_NOR3)  ( 5: 5/1/0, SCOAP=1/255/1 0/255/0/0 )
M   sa0  DS  x3  (_PI)  ( 6: 2/0/0, SCOAP=1/1/255 0/0/255/255 )
M   sa0  DS  GTECH_NOR31/Z  (GTECH_NOR3)  ( 7: 5/0/0, SCOAP=1/255/1 0/255/0/0 )
M   sa0  DS  GTECH_FD12/Q  (GTECH_FD1)  ( 8: 7/0/0, SCOAP=255/255/255 255/255/0/0 )
M   sa0  DS  x2  (_PI)  ( 9: 1/0/0, SCOAP=1/1/255 0/0/255/255 )
M   sa0  DS  GTECH_FD12/D  (GTECH_FD1)  ( 10: 7/0/4, SCOAP=255/255/255 255/255/0/0 )
M   sa0  DI  GTECH_FD12/CP  (GTECH_FD1)  ( 11: 4/0/1, SCOAP=1/1/255 0/0/255/255 )
M   sal  DS  GTECH_FD12/D  (GTECH_FD1)  ( 12: 7/1/4, SCOAP=255/255/255 255/255/0/0 )
M   sal  DI  GTECH_FD12/CP  (GTECH_FD1)  ( 13: 4/1/1, SCOAP=1/1/255 0/0/255/255 )

```

Exit

NoMachine - uday

Activities Applications Places TetraMAX - Synopsys Inc. Thu 17:44

Report Patterns

```

Time 0: force_all_pis = 1110
Time 140: measure_all_pos =1
Time 200: force_all_pis = 0101
Time 340: measure_all_pos =0
Pattern 3 (full_sequential)
Time 0: period = 100
Time 0: force_all_pis = 0100
Time 140: measure_all_pos =0
Time 200: force_all_pis = 1011
Time 340: measure_all_pos =1
Time 400: force_all_pis = 1000
Time 540: measure_all_pos =1
Time 600: force_all_pis = 0001
Time 740: measure_all_pos =0
Pattern 4 (full_sequential)
Time 0: period = 100
Time 0: force_all_pis = 0110
Time 140: measure_all_pos =0
Time 200: force_all_pis = 0001
Time 340: measure_all_pos =1
Pattern 5 (full_sequential)
Time 0: period = 100
Time 0: force_all_pis = 1100
Time 140: measure_all_pos =1
Time 200: force_all_pis = 0011
Time 340: measure_all_pos =0

```

engy04a.utdallas.edu/home/ TetraMAX - Synopsys Inc. Dassan Vision - TopLevel 1.D 5_5_dff.psv.lvs/Spring24.CT Report Patterns 1/

Figure 5.5 with DFF with rst and st

block, build, drc, atpg, faults and patterns

```

module dff_sr1(x1,x2,x3,clk,st,rst,Q);
input x1, x2,x3,clk,st,rst;
output Q;
wire c1,y1,y1n;

```

```
GTECH_OR2 g1(x1,c1,Q);
GTECH_NOR3 g2(x2,x3, y1,c1);
GTECH_FD3 g3(c1, clk, st,rst,y1,y1n );
```

```
Endmodule
```

Testbench

```
`timescale 1ns/1ps
```

```
module dff_sr_tb();
reg clk, x1, x2, x3, st, rst;
wire Q;
dff_sr1 uut( .clk(clk), .x1(x1), .x2(x2), .x3(x3), .st(st), .rst(rst), .Q(Q));
```

```
always #10 clk = ~clk;
```

```
initial begin
$dumpfile("dump.vcd");
$dumpvars;
end
```

```
initial begin
clk <= 0;
st <= 0;
rst <= 1;
x1 <= 1; x2 <= 1; x3 <= 0;
```

#10
x1 <= 0; x2 <= 1; x3 <= 0;

#10
st <= 1;
rst <= 0;
x1 <= 0; x2 <= 0; x3 <= 1;

#10
x1 <= 0; x2 <= 0; x3 <= 0;

#10
x1 <= 1; x2 <= 1; x3 <= 0;

#10
x1 <= 0; x2 <= 1; x3 <= 0;

#10
st <= 1;
rst <= 0;
x1 <= 0; x2 <= 0; x3 <= 1;

#10
x1 <= 0; x2 <= 0; x3 <= 0;

#10
x1 <= 1; x2 <= 1; x3 <= 0;

#10
x1 <= 0; x2 <= 1; x3 <= 0;

#10
st <= 1;
rst <= 0;
x1 <= 0; x2 <= 0; x3 <= 1;

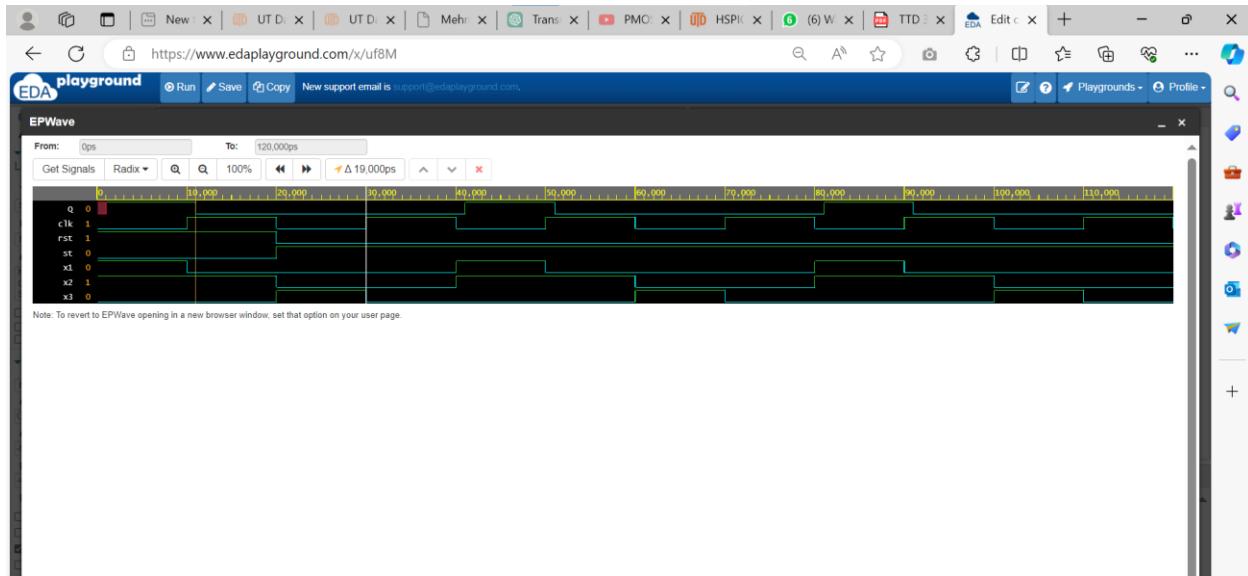
#10
x1 <= 0; x2 <= 0; x3 <= 0;

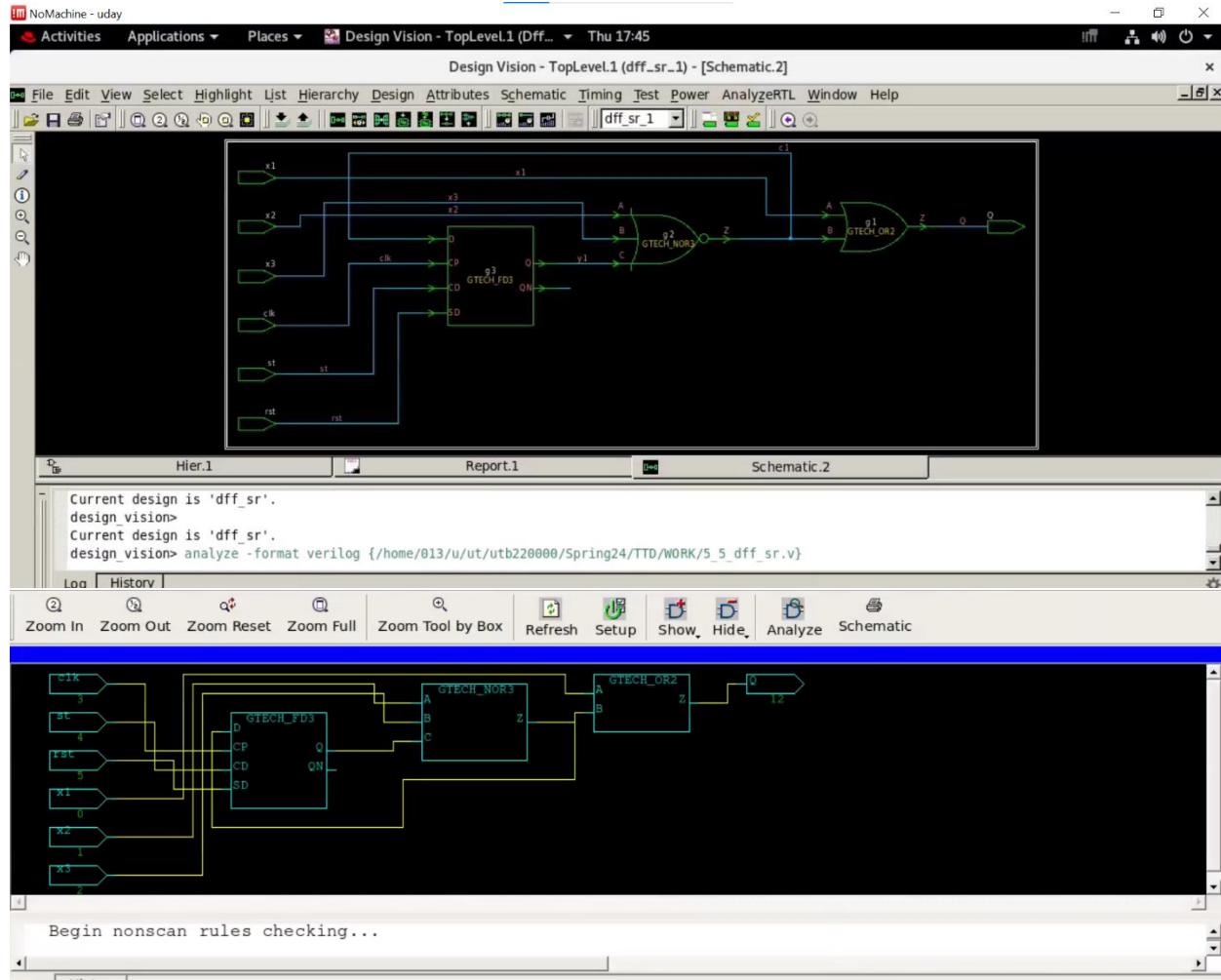
#10

```
$finish;
```

```
end
```

```
endmodule
```





```

NONSCAN BEHAVIOR: #CPU=1
Nonscan rules checking completed, CPU time=0.00 sec.

Begin DRC dependent learning...
Fast-sequential depth results: control=0(0), observe=0(0), detect=0(0), CPU time=0.00 sec
DRC dependent learning completed, CPU time=0.00 sec.

DRC Summary Report

Warning: Rule C2 (unstable nonscan DFF when clocks off) was violated 1 times.

There were 1 violations that occurred during DRC process.
Design rules checking was successful, total CPU time=0.00 sec.

TEST-T>

```

Log History TEST-T> Ready Pin Data: None Stop Build DRC Test 1 / 2

NoMachine - uday Activities Applications ▾ Places ▾ TetraMAX - Synopsys Inc. Thu 17:52

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File Edit View Netlist Rules Scan Primitives Faults Patterns Buses Constraints Loops Run Analyze Report Help

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Messages Netlist Build DRC Summary ATPG Write Pat. Write Testbench Simulation Fault Sim. Analyze

```

End parsing Verilog file /home/013/u/ut/utb220000/Spring24/TTD/WORK/5_5_dff_sr.v
End reading netlist: #modules=1, top=dff_srl, #lines=11, CPU_time=0.00 sec, Memory=0MB
BUILD-T> run_build_model dff_srl

Begin build model for topcut = dff_srl ...

There were 5 primitives and 1 faultable pins removed during model optimization:
Warning: Rule B10 (unconnected module internal net) was violated 2 times.

Warning: Rule N20 (underspecified UDP) was violated 1 times.

End build model: #primitives=13, CPU_time=0.00 sec, Memory=0MB

Begin learning analyses...
End learning analyses, total learning CPU time=0.00 sec.

DRC-T>

```

Log History DRC-T> Ready engnx04a.utdallas.edu:/home/013... TetraMAX - Synopsys Inc. Design Vision - TopLevel.1 (dff_sr... [5_5_dff_sr.v

NoMachine - uday

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TetraMAX - Synopsys Inc.

File Edit View Netlist Rules Scan Primitives Faults Patterns Buses Constraints Loops Run Analyze Report Help

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Messages Netlist Build DRC Summary ATPG Write Pat. Write Testbench Simulation Fault Sim. Analyze

```
-----  
fault class code #faults  
-----  
Detected DT 38  
Possibly detected PT 0  
Undetectable UD 0  
ATPG untestable AU 0  
Not detected ND 0  
-----  
total faults 38  
test coverage 100.00%  
-----  
Pattern Summary Report  
-----  
#internal patterns 8  
#basic_scan patterns 2  
#full_sequential patterns 6
```

Log History TEST-T> Ready

engnx04a.utdallas.edu:/home/013... TetraMAX - Synopsys Inc. Design Vision - TopLevel.1 (dff_sr.v) [5_5_dff_sr.v (~)

NoMachine - uday

Activities Applications Places TetraMAX - Synopsys Inc. Thu 17:54

Report Faults

```

sal DS Q (_PO) ( 1: 12/1/0, SCOAP=2/1/0 0/0/0/0 )
sa0 DS g1/B (GTECH_OR2) ( 2: 10/0/2, SCOAP=2/1/0 0/0/0/0 )
sa0 DS Q (_PO) ( 3: 12/0/0, SCOAP=2/1/0 0/0/0/0 )
sa0 DS x1 (_PI) ( 4: 0/0/0, SCOAP=1/1/1 0/0/0/0 )
sal DS g2/Z (GTECH_NOR3) ( 5: 9/1/0, SCOAP=1/255/1 0/255/0/0 )
sa0 DS x2 (_PI) ( 6: 1/0/0, SCOAP=1/1/255 0/0/255/255 )
sa0 DS x3 (_PI) ( 7: 2/0/0, SCOAP=1/1/255 0/0/255/255 )
sa0 DS g2/Z (GTECH_NOR3) ( 8: 9/0/0, SCOAP=1/255/1 0/255/0/0 )
sa0 DS g3/Q (GTECH_FD3) ( 9: 11/0/0, SCOAP=255/255/255 255/255/0/0 )
sal DS g3/SD (GTECH_FD3) ( 10: 8/1/1, SCOAP=1/1/255 0/0/255/255 )
sal DS g3/D (GTECH_FD3) ( 11: 11/1/4, SCOAP=255/255/255 255/255/0/0 )
sa0 DS g3/CP (GTECH_FD3) ( 12: 6/0/1, SCOAP=1/1/255 0/0/255/255 )
sa0 DS g3/D (GTECH_FD3) ( 13: 11/0/4, SCOAP=255/255/255 255/255/0/0 )
sa0 DS g3/CD (GTECH_FD3) ( 14: 7/0/1, SCOAP=1/1/255 0/0/255/255 )
sal DS g3/CP (GTECH_FD3) ( 15: 6/1/1, SCOAP=1/1/255 0/0/255/255 )
sa0 DS g3/SD (GTECH_FD3) ( 16: 8/0/1, SCOAP=1/1/255 0/0/255/255 )
sal DS g3/CD (GTECH_FD3) ( 17: 7/1/1, SCOAP=1/1/255 0/0/255/255 )

```

NoMachine - uday

Activities Applications Places TetraMAX - Synopsys Inc. Thu 17:56

Report Patterns

```

Time 0: force_all_pis = 110010
Time 140: measure_all_pos =1
Time 200: force_all_pis = 000110
Time 340: measure_all_pos =0
Pattern 4 (full_sequential)
Time 0: period = 100
Time 0: force_all_pis = 000101
Time 140: measure_all_pos =1
Pattern 5 (full_sequential)
Time 0: period = 100
Time 0: force_all_pis = 001001
Time 140: measure_all_pos =0
Time 200: force_all_pis = 000011
Time 340: measure_all_pos =1
Time 400: force_all_pis = 000111
Time 540: measure_all_pos =0
Pattern 6 (full_sequential)
Time 0: period = 100
Time 0: force_all_pis = 011011
Time 140: measure_all_pos =0
Time 200: force_all_pis = 000111
Time 340: measure_all_pos =1
Pattern 7 (full_sequential)
Time 0: period = 100
Time 0: force_all_pis = 010101
Time 140: measure_all_pos =0

```

engnx04a.utdallas.edu/home/... TetraMAX - Synopsys Inc. Design Vision - TopLevel.1 (df... 5_5_dff.sv (~/Spring24/T... Report Patterns 1 / 2

Question 6**Figure 8.13****Code**

```
module Q8_13(x1, x2, x3, x4, x5, z);
```

```
    input x1, x2, x3, x4, x5;
```

```
    output z;
```

```
    wire c1, c2, c3, c4, x1n;
```

```
    GTECH_NOT g1(x1, x1n);
```

```
    GTECH_AND2 g2(x1, x2, c1);
```

```
    GTECH_OR2 g3(x3, x4, c2);
```

```
    GTECH_NOR2 g4(c1, c2, c3);
```

```
    GTECH_AND2 g5(x1n, x5, c4);
```

```
    GTECH_OR2 g6(c3, c4, z);
```

```
Endmodule
```

TestBench

```
`timescale 1ns/1ps
```

```
module Q8_13_tb();
```

```
    reg x1, x2, x3, x4, x5;
```

```
    wire z;
```

```
    Q8_13 uut( .x1(x1), .x2(x2), .x3(x3), .x4(x4), .x5(x5), .z(z) );
```

```
initial begin
```

```

$dumpfile("dump.vcd");
$dumpvars;
end

initial begin
x1 <= 0; x2 <= 0;x3 <= 0 ;x4 <= 0;x5 <= 1;
#20
x1 <= 0; x2 <= 0;x3 <= 1 ;x4 <= 0;x5 <= 0;
#20
x1 <= 0; x2 <= 0;x3 <= 0 ;x4 <= 0;x5 <= 1;
#20
x1 <= 0; x2 <= 0;x3 <= 1 ;x4 <= 0;x5 <= 0;
#20
$finish;

end
endmodule

```

Design vision netlist

```

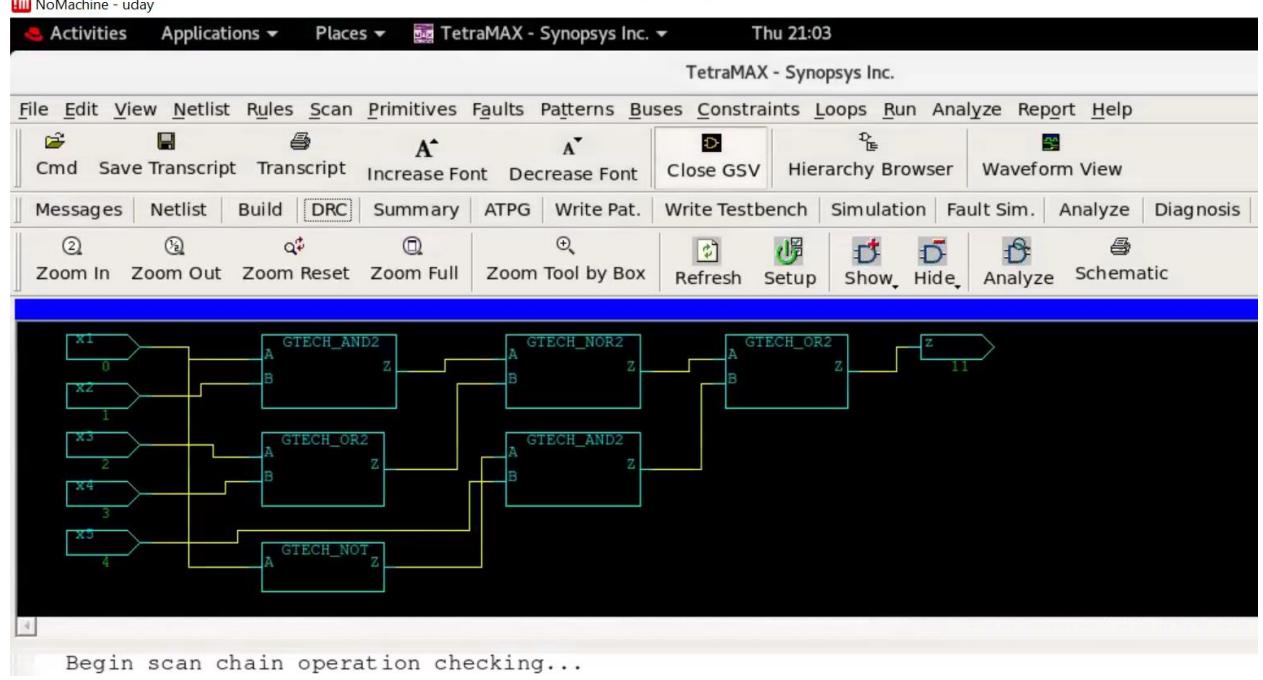
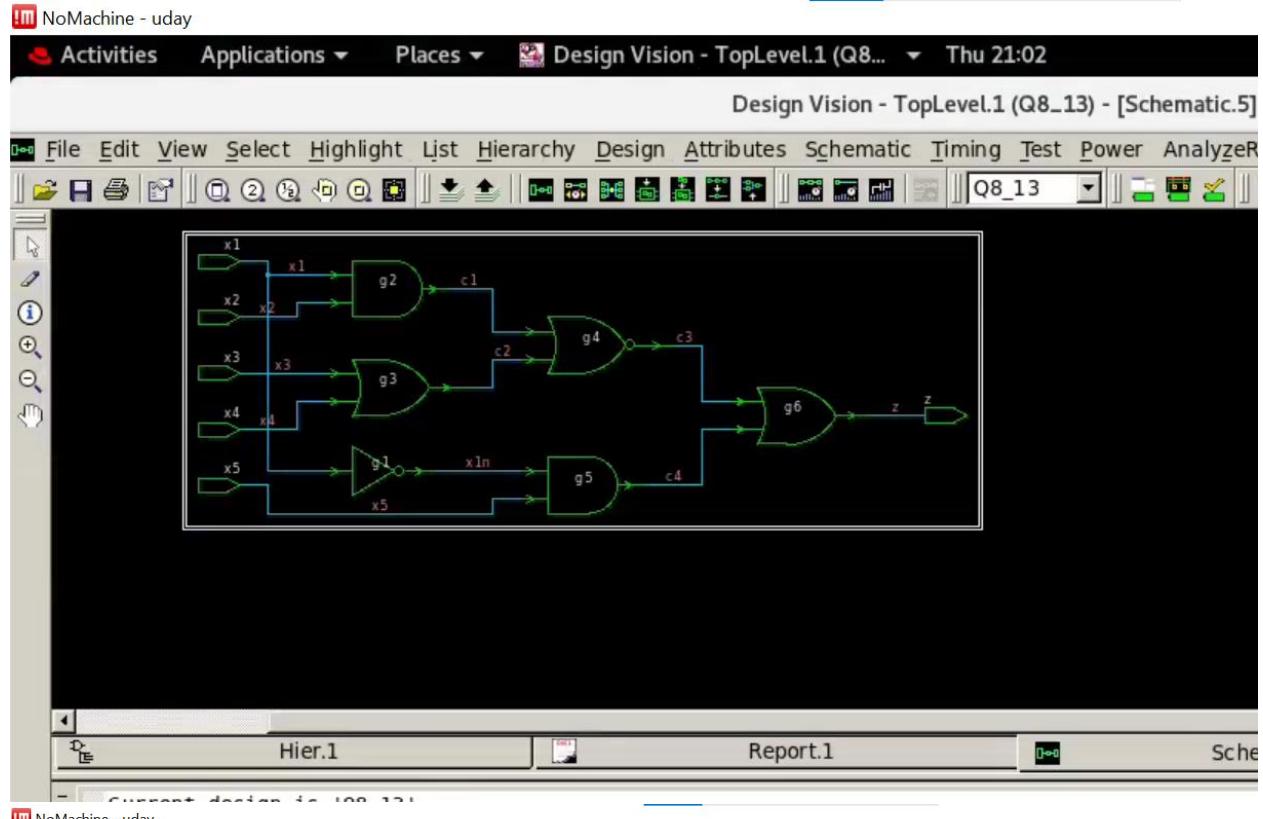
module Q8_13_1 ( x1, x2, x3, x4, x5, z );
input x1, x2, x3, x4, x5;
output z;
wire c1, c2, c3, c4, x1n;

GTECH_NOT g6 ( .A(x1), .Z(x1n) );
GTECH_AND2 g1 ( .A(x1), .B(x2), .Z(c1) );
GTECH_OR2 g2 ( .A(x3), .B(x4), .Z(c2) );
GTECH_NOR2 g3 ( .A(c1), .B(c2), .Z(z) );

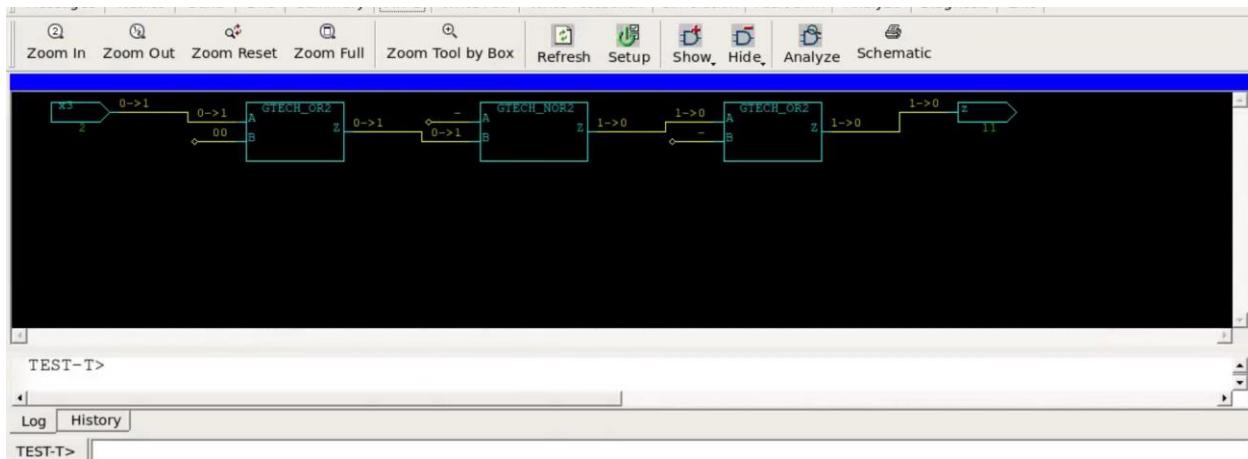
```

```
GTECH_AND2 g4 ( .A(x1n), .B(x5), .Z(c4) );
GTECH_OR2 g5 ( .A(c3), .B(c4), .Z(z) );
endmodule
```

Schematic



Robust



```
NoMachine - uday
Activities Applications ▾ Places ▾ Report Delay Paths ▾ Thu 21:47
TetraMAX - Synopsys Inc.

File Edit View Netlist Rules Scan Primitives Faults Patterns Buses Constraints Loops Run Analyze Report H
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Messages Netlist Build DRC Summary ATPG Write Pat. Write Testbench Simulation Fault Sim. Analy

fault class code #faults
-----
Detected DT 10
  detected_by_simulation DS (3)
  detected_robustly DR (7)
Possibly detected PT 0
Undetectable UD 0
ATPG untestable AU 0
Not detected ND 0
-----
total faults 10
test coverage 100.00%
fault coverage 100.00%
ATPG effectiveness 100.00%
-----
Pattern Summary Report
Log History
TEST-T>
Ready
engnx04a.ut... TetraMAX - S... Design Vision... Q8_13_1.v (...) Report Delay... Report Delay... Report
```

NoMachine - uday

Activities Applications Places TetraMAX - Report Delay Paths Thu 21:57

Report Delay Paths

```

$path {
    $name path1r ;
    // #launch_clocks=0, launch_node=PI (2)
    // #capture_clocks=0, capture_node=PO (11)
    // path is rising transition only
    // slow-to-rise fault class = DS
    $condition {
        x1 00 ; // 0 (PI)
        x4 00 ; // 3 (PI)
    }
    $transition {
        x3 ^ ; // 2 (PI)
        g2/Z ^ ; // 7 (OR)
        g3/Z v ; // 8 (NOR)
        g5/Z v ; // 10 (OR)
        z v ; // 11 (PO)
    }
}

$path {
    $name path1f ;
    // #launch_clocks=0, launch_node=PI (2)
    // #capture_clocks=0, capture_node=PO (11)
    // path is falling transition only
    // slow-to-fall fault class = DR
}

```

Pin Data: Delay Data Stop Build DRC Test

engnx0... TetraM... Design... Q8_13... Report... Report... Report... Report... Report... Report... 1/2

NoMachine - uday

Activities Applications Places TetraMAX - Report Delay Paths Thu 21:53

Report Patterns

Pattern 0 (fast_sequential)
Time 0: force_all_pis = 01000
Time 1: force_all_pis = 10100
Time 2: measure_all_pos = 0
Pattern 1 (fast_sequential)
Time 0: force_all_pis = 01011
Time 1: force_all_pis = 01100
Time 2: measure_all_pos = 0
Pattern 2 (fast_sequential)
Time 0: force_all_pis = 10100
Time 1: force_all_pis = 00111
Time 2: measure_all_pos = 1
Pattern 3 (fast_sequential)
Time 0: force_all_pis = 11011
Time 1: force_all_pis = 00000
Time 2: measure_all_pos = 1
Pattern 4 (fast_sequential)
Time 0: force_all_pis = 01001
Time 1: force_all_pis = 10010
Time 2: measure_all_pos = 0
Pattern 5 (fast_sequential)
Time 0: force_all_pis = 11011
Time 1: force_all_pis = 10000
Time 2: measure_all_pos = 1
Pattern 6 (fast_sequential)
Time 0: force_all_pis = 10001

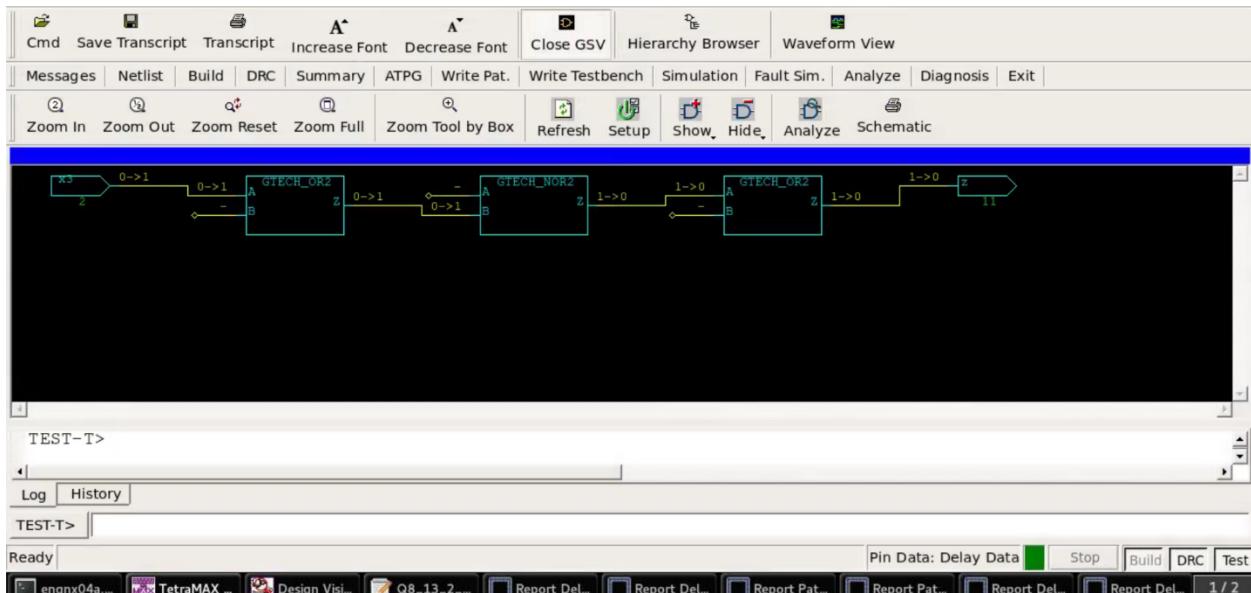
Report Patterns

Pattern	Fault num	Fault name	Fault type	Fault class	Launch clock
0	path1r	str	DS	-	
1	path5f	stf	DR	-	
2	path5r	str	DR	-	
3	path4f	stf	DS	-	
4	path4r	str	DS	-	
5	path3f	stf	DR	-	
6	path3r	str	DR	-	
7	path1f	stf	DR	-	
7	path2f	stf	DR	-	
8	path2r	str	DR	-	

Pin Data: Delay Data Stop Build DRC Test

engnx0... TetraM... Design... Q8_13... Report... Report... Report... Report... Report... Report... Report... Report... 1/2

Non Robust



NoMachine - uday

Activities Applications Places TetraMAX - Synopsys Inc. Thu 22:15

TetraMAX - Synopsys Inc.

File Edit View Netlist Rules Scan Primitives Faults Patterns Buses Constraints Loops Run Analyze Report Help

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Messages Netlist Build DRC Summary ATPG Write Pat. Write Testbench Simulation Fault Sim. Analyze Diagnosis Exit

```

End parsing Verilog file /home/013/u/ut/utb220000/Spring24/TTD/WORK/Q8_13_1.v with 0 errors.
End reading netlist: #modules=0, top=Q8_13_1, #lines=20, CPU_time=0.00 sec, Memory=0MB
BUILD-T> run_build_model Q8_13_1
-----
Begin build model for topcut = Q8_13_1 ...
-----
There were 0 primitives and 0 faultable pins removed during model optimizations
End build model: #primitives=12, CPU_time=0.00 sec, Memory=0MB
-----
Begin learning analyses...
End learning analyses, total learning CPU time=0.00 sec.
-----
DRC-T> run_drc
-----
Begin scan design rules checking...

```

NoMachine - uday

Activities Applications Places TetraMAX - Synopsys Inc. Thu 22:15

TetraMAX - Synopsys Inc.

File Edit View Netlist Rules Scan Primitives Faults Patterns Buses Constraints Loops Run Analyze Report Help

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Messages Netlist Build DRC Summary ATPG Write Pat. Write Testbench Simulation Fault Sim. Analyze Diagnosis Exit

```

Begin scan chain operation checking...
Scan chain operation checking completed, CPU time=0.00 sec.
-----
Begin nonscan rules checking...
Nonscan cell summary: #DFF=0 #DLAT=0 #RAM_outs=0 tla_usage_type=none
Nonscan rules checking completed, CPU time=0.00 sec.
-----
Begin DRC dependent learning...
Fast-sequential depth results: control=0(0), observe=0(0), detect=0(0), CPU time=0.00 sec
DRC dependent learning completed, CPU time=0.00 sec.
-----
DRC Summary Report
-----
No violations occurred during DRC process.
Design rules checking was successful, total CPU time=0.00 sec.
-----
TEST-T>

```

Log History

TEST-T>

Ready engnx04a.utdallas.edu:/home/013... TetraMAX - Synopsys Inc. Design Vision - TopLevel1 (Q8_13) Q8_13_1.v (~/Spring24/TTD/WO..

Pin Data: Delay Data Stop Build DRC Test

1 / 2

NoMachine - uday

Activities Applications Places Report Patterns Thu 22:37

TetraMAX - Synopsys Inc.

File Edit View Netlist Rules Scan Primitives Faults Patterns Buses Constraints Loops Run Analyze Report Help

Cmd Save Transcript Transcript Increase Font Decrease Font Open GSV Hierarchy Browser Waveform View

Messages Netlist Build DRC Summary ATPG Write Pat. Write Testbench Simulation Fault Sim. Analyze Diagnosis Exit

Collapsed Path_delay Fault Summary Report

fault class	code	#faults
Detected	DT	10
detected_by_simulation	DS	(3)
detected_robustly	DR	(7)
Possibly detected	PT	0
Undetectable	UD	0
ATPG untestable	AU	0
Not detected	ND	0
total faults		10
test coverage		100.00%
fault coverage		100.00%
ATPG effectiveness		100.00%

Log History TEST-T>

Ready

Pin Data: Delay Data Stop Build DRC Test

engnx04a... TetraMAX ... Design Visi... Q8_13_2... Report Del... Report Del... Report Pat... Report Pat... Report Del... Report Del... 1 / 2

NoMachine - uday

Activities Applications Places Report Patterns Thu 22:35

TetraMAX - Synopsys Inc.

File Loops Run Analyze Report Help

Hierarchy

Report Delay Paths

```
$path {
    $name path2r ;
    // #launch_clocks=0, launch_node=PI (2)
    // #capture_clocks=0, capture_node=PO (11)
    // path is rising transition only
    // slow-to-rise fault class = DR
    $transition {
        x3 ^ ; // 2 (PI)
        g2/Z ^ ; // 7 (OR)
        g3/Z v ; // 8 (NOR)
        g5/Z v ; // 10 (OR)
        z v ; // 11 (PO)
    }
}

$path {
    $name path2f ;
    // #launch_clocks=0, launch_node=PI (2)
    // #capture_clocks=0, capture_node=PO (11)
    // path is falling transition only
    // slow-to-fall fault class = DS
    $transition {
        x3 v ; // 2 (PI)
        g2/Z v ; // 7 (OR)
        g3/Z ^ ; // 8 (NOR)
    }
}
```

Pin Data: Delay Data Stop Build DRC Test

engnx04a... TetraMAX ... Design Visi... Q8_13_2... Report Del... Report Del... Report Pat... Report Pat... Report Del... Report Del... 1 / 2

NoMachine - uday

Activities Applications Places Report Patterns Thu 23:04

Report Delay Paths

```
$path {
    $name path3r ;
    // #launch_clocks=0, launch_node=PI (1)
    // #capture_clocks=0, capture_node=PO (11)
    // path is rising transition only
    // slow-to-rise fault class = DR
    $transition {
        x2 ^ ; // 1 (PI)
        g1/Z ^ ; // 6 (AND)
        g3/Z v ; // 8 (NOR)
        g5/Z v ; // 10 (OR)
        z v ; // 11 (PO)
    }
}

$path {
    $name path3f ;
    // #launch_clocks=0, launch_node=PI (1)
    // #capture_clocks=0, capture_node=PO (11)
    // path is falling transition only
    // slow-to-fall fault class = DR
    $transition {
        x2 v ; // 1 (PI)
        g1/Z v ; // 6 (AND)
        g3/Z ^ ; // 8 (NOR)
        g5/Z ^ ; // 10 (OR)
        z ^ ; // 11 (PO)
    }
}
```

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NoMachine - uday

Activities Applications Places Report Patterns Thu 23:04

Report Delay Paths

```
$path {
    $name path1r ;
    // #launch_clocks=0, launch_node=PI (0)
    // #capture_clocks=0, capture_node=PO (11)
    // path is rising transition only
    // slow-to-rise fault class = DR
    $transition {
        x1 ^ ; // 0 (PI)
        g1/Z ^ ; // 6 (AND)
        g3/Z v ; // 8 (NOR)
        g5/Z v ; // 10 (OR)
        z v ; // 11 (PO)
    }
}

$path {
    $name path1f ;
    // #launch_clocks=0, launch_node=PI (0)
    // #capture_clocks=0, capture_node=PO (11)
    // path is falling transition only
    // slow-to-fall fault class = DS
    $transition {
        x1 v ; // 0 (PI)
        g1/Z v ; // 6 (AND)
        g3/Z ^ ; // 8 (NOR)
        g5/Z ^ ; // 10 (OR)
    }
}
```

TetraMAX - Synopsys Inc. Design Vision - TopLevel.1 (Q8...) Q8_13_2_path.txt (~/Spring2... Report Delay Paths 1 / 2

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Activities Applications Places Report Patterns Thu 23:05

Report Delay Paths

```
$name path4r ;
// #launch_clocks=0, launch_node=PI (3)
// #capture_clocks=0, capture_node=PO (11)
// path is rising transition only
// slow-to-rise fault class = DR
$transition {
    x4 ^ ; // 3 (PI)
    g2/Z ^ ; // 7 (OR)
    g3/Z v ; // 8 (NOR)
    g5/Z v ; // 10 (OR)
    z v ; // 11 (PO)
}
}

$path {
    $name path4f ;
    // #launch_clocks=0, launch_node=PI (3)
    // #capture_clocks=0, capture_node=PO (11)
    // path is falling transition only
    // slow-to-fall fault class = DS
    $transition {
        x4 v ; // 3 (PI)
        g2/Z v ; // 7 (OR)
        g3/Z ^ ; // 8 (NOR)
        g5/Z ^ ; // 10 (OR)
        z ^ ; // 11 (PO)
    }
}
```

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NoMachine - uday

Activities Applications Places Report Patterns Thu 23:05

Report Delay Paths

```

$path {
    $name path5r ;
    // #launch_clocks=0, launch_node=PI (4)
    // #capture_clocks=0, capture_node=PO (11)
    // path is rising transition only
    // slow-to-rise fault class = DR
    $transition {
        x5 ^ ; // 4 (PI)
        g4/Z ^ ; // 9 (AND)
        g5/Z ^ ; // 10 (OR)
        z ^ ; // 11 (PO)
    }
}

$path {
    $name path5f ;
    // #launch_clocks=0, launch_node=PI (4)
    // #capture_clocks=0, capture_node=PO (11)
    // path is falling transition only
    // slow-to-fall fault class = DR
    $transition {
        x5 v ; // 4 (PI)
        g4/Z v ; // 9 (AND)
        g5/Z v ; // 10 (OR)
        z v ; // 11 (PO)
    }
}

```

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NoMachine - uday

Activities Applications Places Report Patterns Thu 22:38

Pattern	Fault num	Fault name	Fault type	Fault class	Launch clock
Pattern 0 (fast_sequential)					
Time 0: force_all_pis = 00000					
Time 1: force_all_pis = 10100					
Time 2: measure_all_pos = 0					
Pattern 1 (fast_sequential)					
Time 0: force_all_pis = 00101					
Time 1: force_all_pis = 00110					
Time 2: measure_all_pos = 0					
Pattern 2 (fast_sequential)					
Time 0: force_all_pis = 00110					
Time 1: force_all_pis = 00101					
Time 2: measure_all_pos = 1					
Pattern 3 (fast_sequential)					
Time 0: force_all_pis = 10111					
Time 1: force_all_pis = 01000					
Time 2: measure_all_pos = 1					
Pattern 4 (fast_sequential)					
Time 0: force_all_pis = 00000					
Time 1: force_all_pis = 10011					
Time 2: measure_all_pos = 0					
Pattern 5 (fast_sequential)					
Time 0: force_all_pis = 11011					
Time 1: force_all_pis = 10000					
Time 2: measure_all_pos = 1					
Pattern 6 (fast_sequential)					
Time 0: force_all_pis = 10000					

Pin Data: Delay Data Stop Build DRC Test

engnx0... TetraM... Design ... Q8_13... Report ... 1 / 2

Conclusion:

From the simulations, we have 100 percent coverage, patterns that are obtained by simulation matches with the descriptive deduction, and all the paths for robust and non robust have been covered.