Mini Stereo Digital Audio Processor

Presented By:

Uday Teja Bandaru (UTB220000)

Kodanda Rama Yaswanth Kumar Ramadugu (KXR230001)

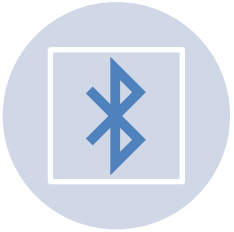
Aditya Bhaskaran (AXB230073)

Program: Computer Engineering (MS)

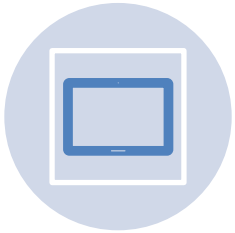
Date: 05/05/2025

Applications of MSDAP

Portable audio devices (MP3 players, hearing aids, wearables)



Bluetooth headsets and wireless earbuds



Smartphones and tablets (DSP for audio enhancement)

Voice-controlled IoT devices (noise suppression, echo cancellation)Automotive infotainment and stereo systems

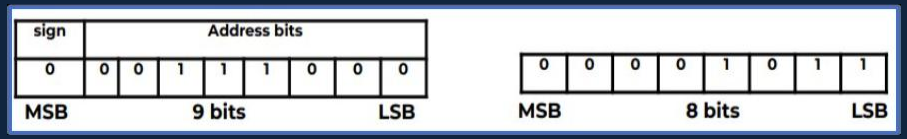
CONVOLUTION AND MSDAP ALGORITHM

$$y(n) = \sum_{k=0}^{N} h(k)x(n-k),$$

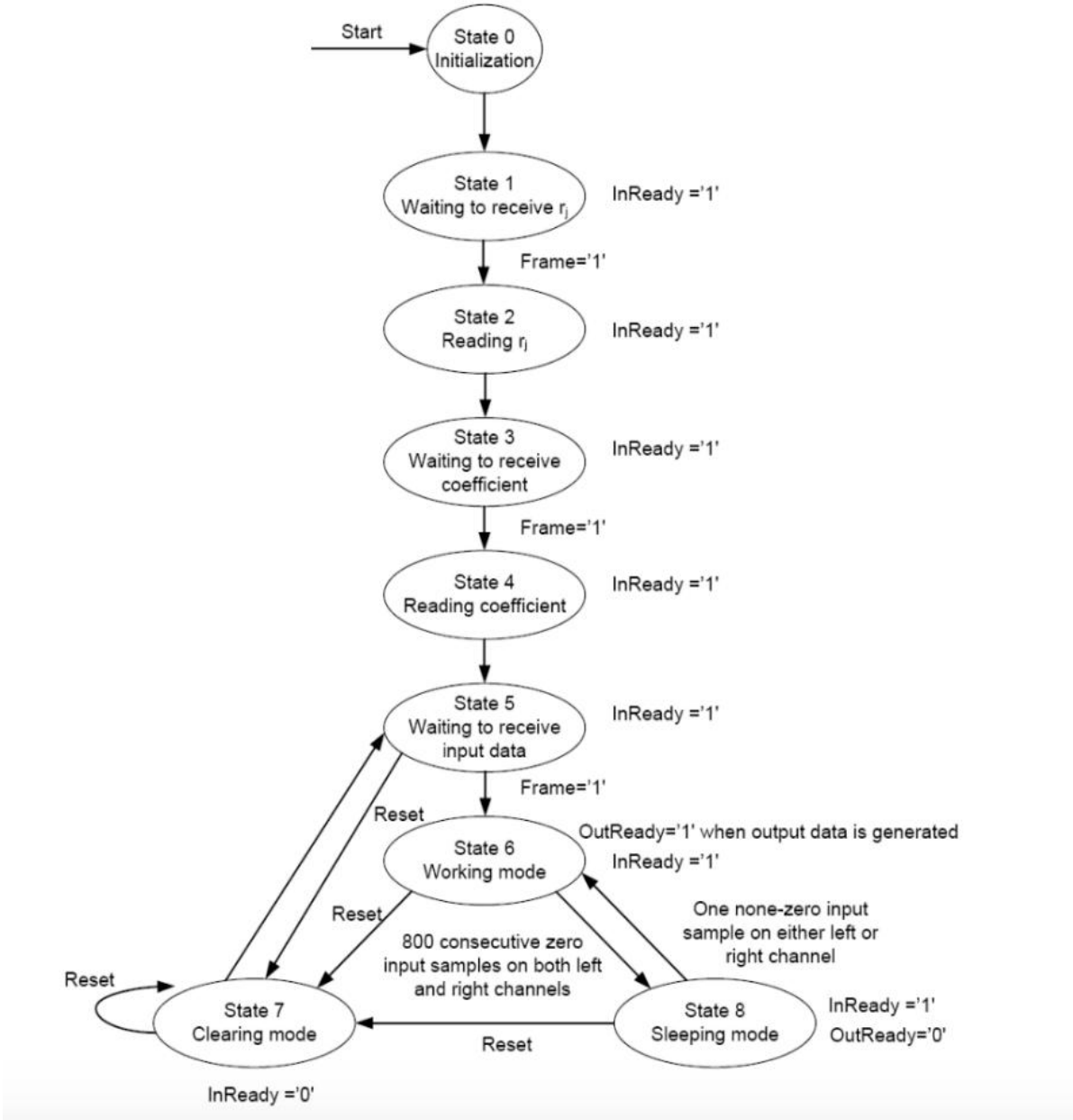
OPTIMIZING THE ALGORITHM FOR POWER AND AREA:

$$y(n) = 2^{-1}(u_{16} + 2^{-1}(u_{15} + \ldots . 2^{-1}(u_2 + 2^{-1}u_1) \ldots)$$

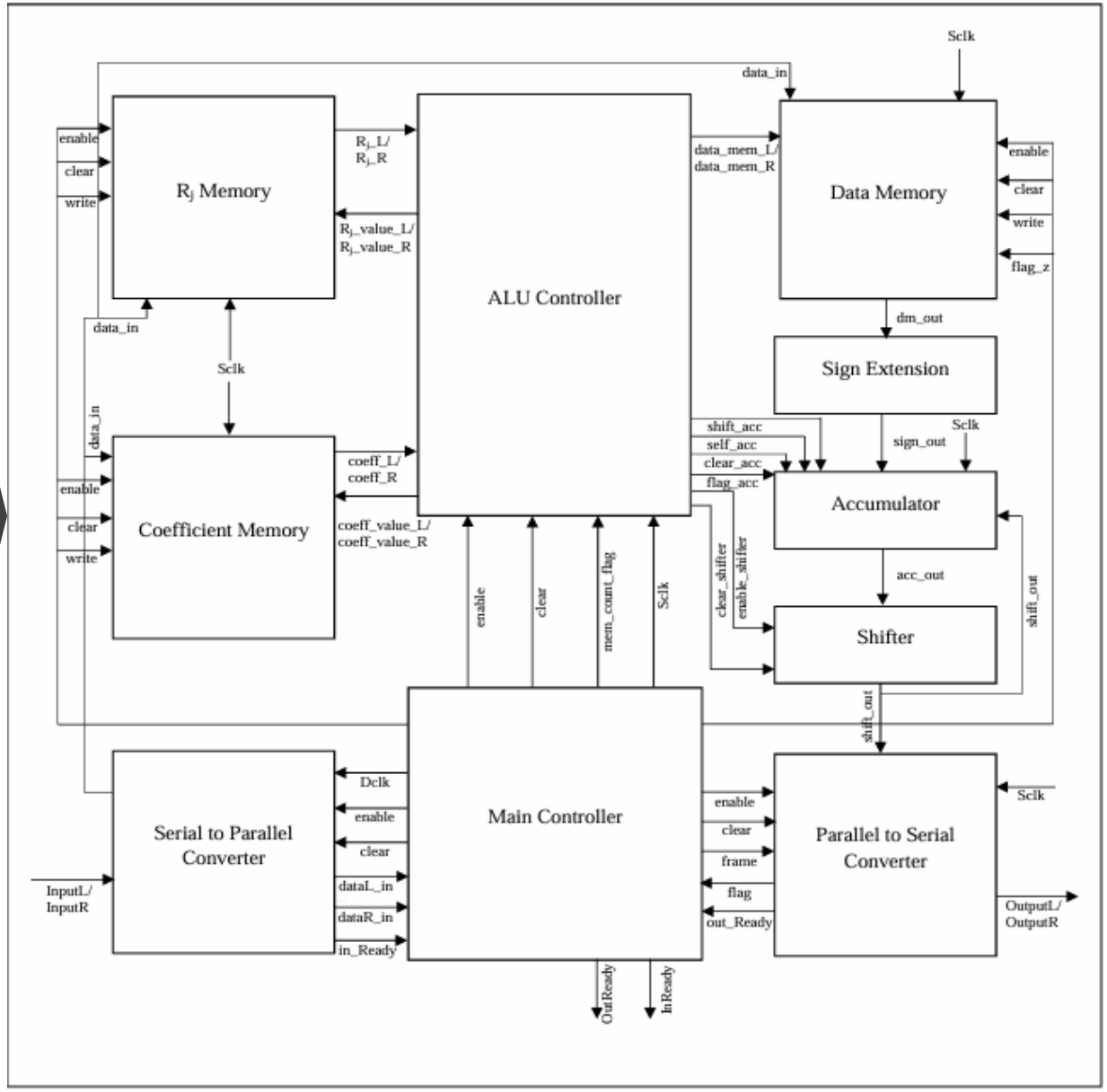
Data Format:



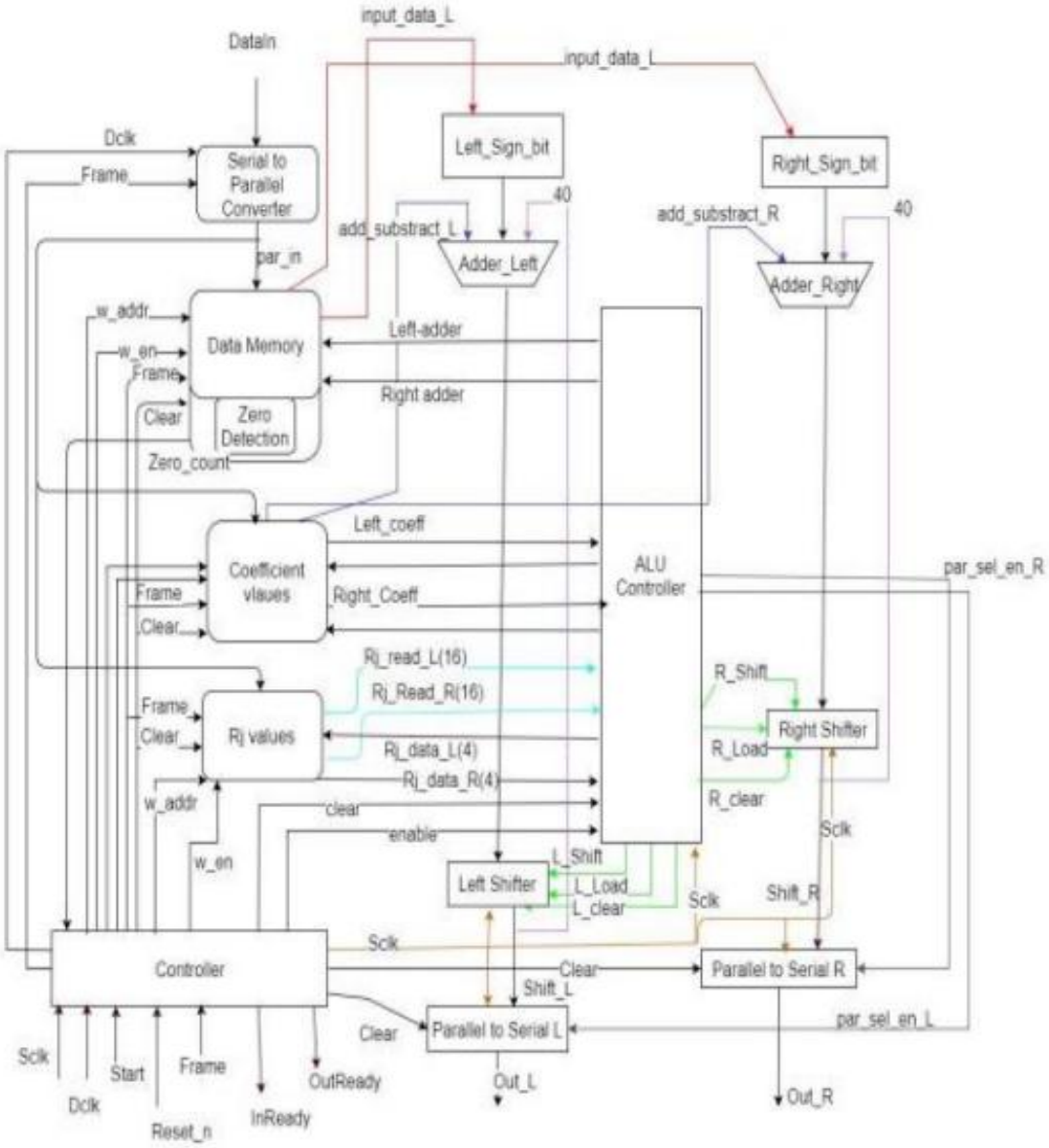
Main Controller



MSDAP Architecture(Original):



MSDAP
Architecture(Updated):



Architecture breakdown

1. Main Controller:

Receives control signals such as:

- Clock signals (CLK, SCLK) for synchronization.
- Start (START) & Reset (RESET) signals to control execution.
- Frame & Address signals for memory access.

Generates control signals for different processing blocks.

2. Memory Units:

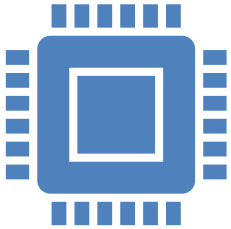
- S2P (Serial-to-Parallel) Converter - Converts incoming serial input data into parallel format.
- Register File (Ri 16x16) - Temporary storage for intermediate values.
- Coefficient Memory (COEFF 16x512) - Stores coefficient values required for calculations.
- FIFO Data Memory (10x256) - Buffers input data.

3. ALU Controller:

Manages arithmetic operations, including:

- Sign Control
- Shift Control
- Load Control
- Reset Handlin

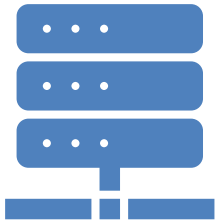
Specifications



Clock Frequencies

Sclk: 26.88 MHz (system clock for computation and control)

Dclk: 768 kHz (data clock for input/output, 16 bits per frame, frame rate = 48kHz).



Data Format

Input/Output: 16-bit 2's complement, MSB first, serial over 16 Dclk cycles.

Rj: 8-bit values, zero-padded to 16 bits.

Coefficients (uj): 8-bit values with a sign bit, zero-padded to 16 bits.

Module level Verilog

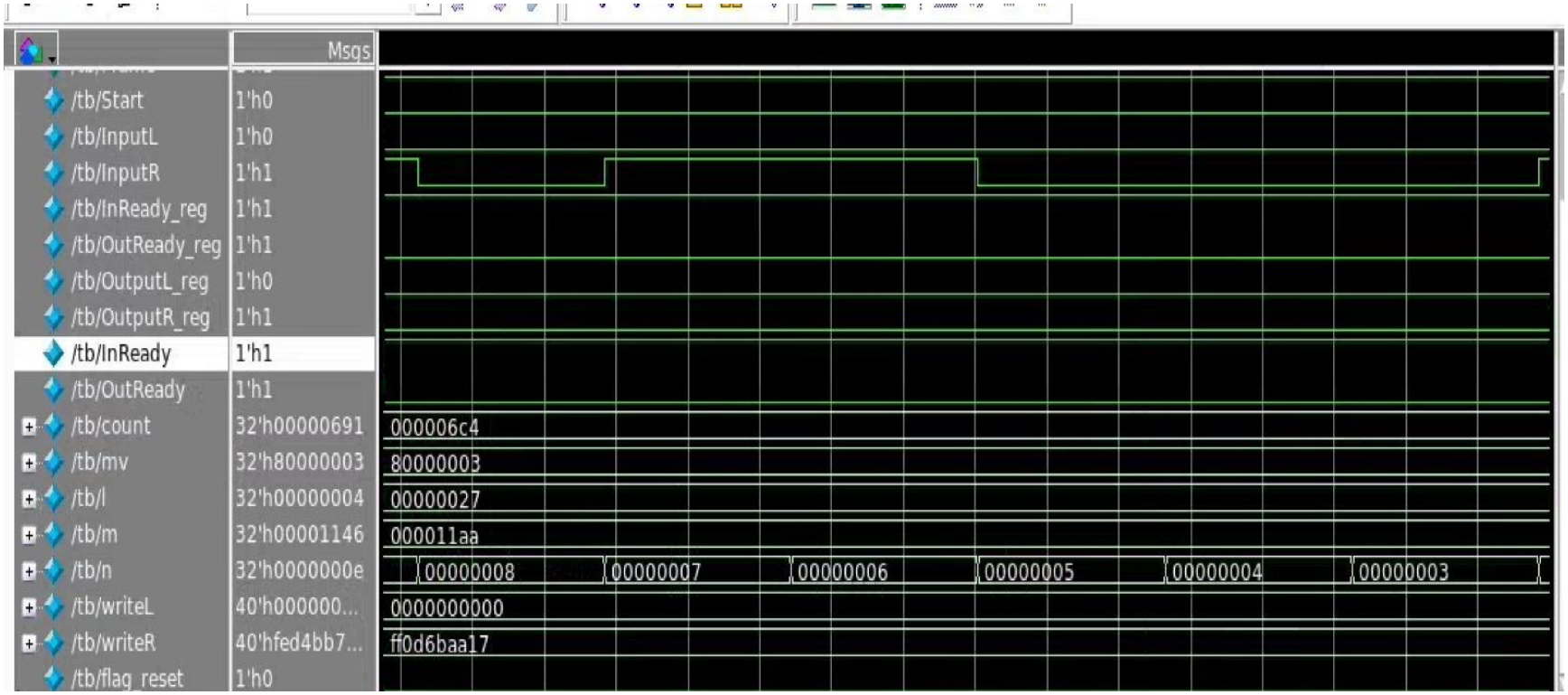
- **Top Level Verilog Code:**

```
module top(input Dclk, Sclk, Reset_n, Frame, Start, InputL, InputR,
                                output InReady, OutReady, OutputL, OutputR);


        //Wires for memories
        //wire rj_enable, coeff_enable, data_enable;            // For main controller
        //wire rjL_enable, coeffL_enable, inputL_enable;                // For ALU controller
        //wire rjR_enable, coeffR_enable, inputR_enable;
        //wire [3:0] rjwrite, rjL_addr, rjR_addr;
        //wire [8:0] coeffwrite, coeffL_addr, coeffR_addr;
        wire [7:0] datawrite, inputL_addr, inputR_addr;
        wire [15:0] rjdataL, coeffdataL, indataL;
        wire [15:0] rjdataR, coeffdataR, indataR;
        wire flag_zeroL, flag_zeroR;
        //wire [3:0] rj_addrR_muxed;
        //wire [3:0] dataL_addr;
        //wire [8:0] data_addrL_muxed, dataR_addr, datawrite_addr, data_addrR_muxed;
        // Left CO_MEM
        wire [8:0] RW0_addr_COL, RW0_wdata_COL, RW0_rdata_COL;
        wire       RW0_clk_COL, RW0_en_COL, RW0_Wmode_COL;


//-------------------------------------------------------------------------
// 1) Parameterize your three address?widths to match each memory macro:
//-------------------------------------------------------------------------

localparam ADDR_WIDTH_DATA  = 8;  // DATA_MEM expects an 8-bit address
localparam ADDR_WIDTH_COEFF = 9;  // CO_MEM expects a 9-bit address
localparam ADDR_WIDTH_RJ    = 4;  // R_MEM expects a 4-bit address

//-------------------------------------------------------------------------
// 2) Declare all of your wires at those widths:
//-------------------------------------------------------------------------

wire [ADDR_WIDTH_DATA-1:0]  dataL_addr,   dataR_addr,   datawrite_addr;
wire [ADDR_WIDTH_DATA-1:0]  data_addrL_muxed, data_addrR_muxed;

wire [ADDR_WIDTH_COEFF-1:0] coeffL_addr,  coeffR_addr,  coeffwrite;
wire [ADDR_WIDTH_COEFF-1:0] coeffL_addr_muxed, coeffR_addr_muxed;

wire [ADDR_WIDTH_RJ-1:0]    rjL_addr,     rjR_addr,     rjwrite;
wire [ADDR_WIDTH_RJ-1:0]    rj_addrL_muxed, rj_addrR_muxed;

// control signals
wire data_enable,   inputL_enable,   inputR_enable;
wire coeff_enable,  coeffL_enable,   coeffR_enable;
wire rj_enable,     rjL_enable,      rjR_enable;
```

- **Top Level Testbench Code:**

```
`timescale 1ns / 1ps

module tb;

        // Inputs
        reg Dclk;
        reg Sclk;
        reg Reset_n;
        reg Frame;
        reg Start;
        reg InputL;
        reg InputR;

        // Outputs
        wire InReady_reg;
        wire OutReady_reg;
        wire OutputL_reg;
        wire OutputR_reg;

        // Aliases
        wire InReady = InReady_reg;
        wire OutReady = OutReady_reg;

        // Testbench control
        integer count = 0;
        integer mv;

        // Input data memory
        reg [15:0] data [0:15055];

        // Parameters
        parameter Dclk_Time = 651;
```

Output Waveform



Genus Generated MSDAP Mapped.v

Open

MSDAP_mapped.v

~/Spring25/ASIC_DESIGN/Final_Project/MSDAP_1/Genus

```
// Generated by Cadence Genus(TM) Synthesis Solution 19.14-s108_1
// Generated on: May  5 2025 11:35:45 CDT (May  5 2025 16:35:45 UTC)

// Verification Directory fv/top

module CO_MEM(RW0_addr, RW0_clk, RW0_wdata, RW0_rdata, RW0_en,
     RW0_wmode);
  input [8:0] RW0_addr, RW0_wdata;
  input RW0_clk, RW0_en, RW0_wmode;
  output [8:0] RW0_rdata;
  wire [8:0] RW0_addr, RW0_wdata;
  wire RW0_clk, RW0_en, RW0_wmode;
  wire [8:0] RW0_rdata;
  wire [11:0] mem_0_0_O;
  wire [11:0] mem_0_1_O;
  wire [11:0] mem_0_2_O;
  wire [11:0] mem_0_3_O;
  wire UNCONNECTED, UNCONNECTED0, UNCONNECTED1, UNCONNECTED2,
       UNCONNECTED3, UNCONNECTED4, UNCONNECTED5, UNCONNECTED6;
  wire UNCONNECTED7, UNCONNECTED8, UNCONNECTED9, UNCONNECTED10;
  assign RW0_rdata[0] = 1'b0;
  assign RW0_rdata[1] = 1'b0;
  assign RW0_rdata[2] = 1'b0;
  assign RW0_rdata[3] = 1'b0;
  assign RW0_rdata[4] = 1'b0;
  assign RW0_rdata[5] = 1'b0;
  assign RW0_rdata[6] = 1'b0;
  assign RW0_rdata[7] = 1'b0;
  assign RW0_rdata[8] = 1'b0;
  SRAM1RW128x12 mem_0_0(.CE (1'b0), .WEB (1'b1), .OEB (1'b1), .CSB
```

Synthesized Design

Open

area.rpt

~/Spring25/ASIC/Final_Project/par/reports

Hinst Name	Module Name	Inst Count	Total Area
top		2863	24774.289
COL	CO_MEM	20	5903.010
COR	CO_MEM_1	63	5952.465
PISOL	PISO	332	612.127
PISOR	PISO_1	322	602.096
Sipo	SIPO	221	453.496
addL	adder	182	329.158
addR	adder_1	180	325.892
alu_ctrl	alu_controller	772	1250.847
data_memL	DATA_MEM	6	3732.385
data_memR	DATA_MEM_821	6	3737.984
main_ctrl	main_controller	320	555.673
rj_memL	R_MEM	4	174.356
rj_memR	R_MEM_822	4	177.155
shiftL	shift_accumulator	173	412.206
shiftR	shift_accumulator_1	176	412.672
u_mux_coeffR_addr	mux2to1_WIDTH9	14	24.961
u_mux_dataL_addr	mux2to1_WIDTH8	2	3.033
u_mux_dataR_addr	mux2to1_WIDTH8_1	2	3.033
u_mux_rjL_addr	mux2to1_WIDTH4	1	2.333
u_mux_rjR_addr	mux2to1_WIDTH4_1	1	2.333

Genus Power Report

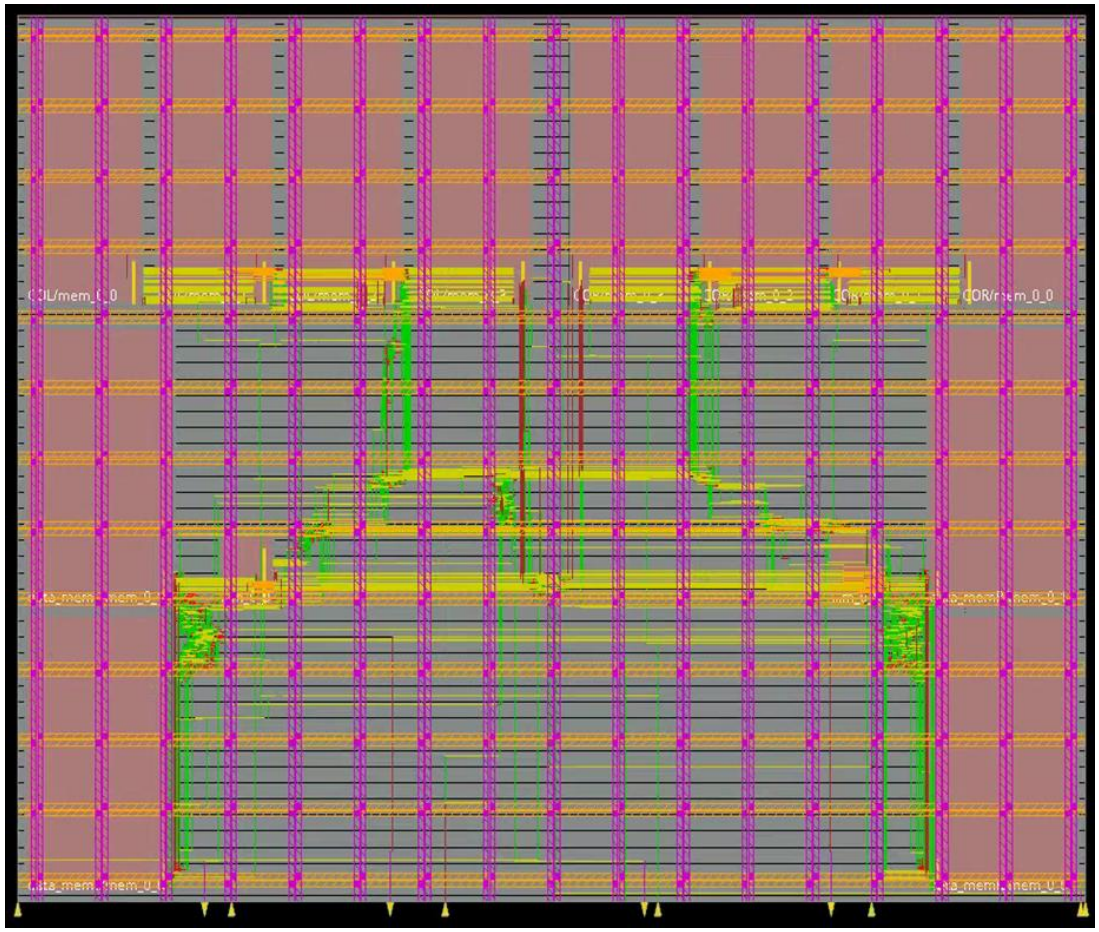
```
Instance: /top
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ------------------------------------------------------------------------------
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
    register     1.05803e-05  2.70993e-06  1.99405e-07  1.34896e-05  52.14%
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       logic     1.09744e-05  5.25411e-07  4.43273e-07  1.19431e-05  46.16%
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       clock     6.13981e-08  3.74900e-10  3.76504e-07  4.38277e-07   1.69%
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ------------------------------------------------------------------------------
    Subtotal     2.16161e-05  3.23572e-06  1.01918e-06  2.58710e-05  99.99%
  Percentage          83.55%       12.51%        3.94%      100.00% 100.00%
  ------------------------------------------------------------------------------
```

Genus Setup Report

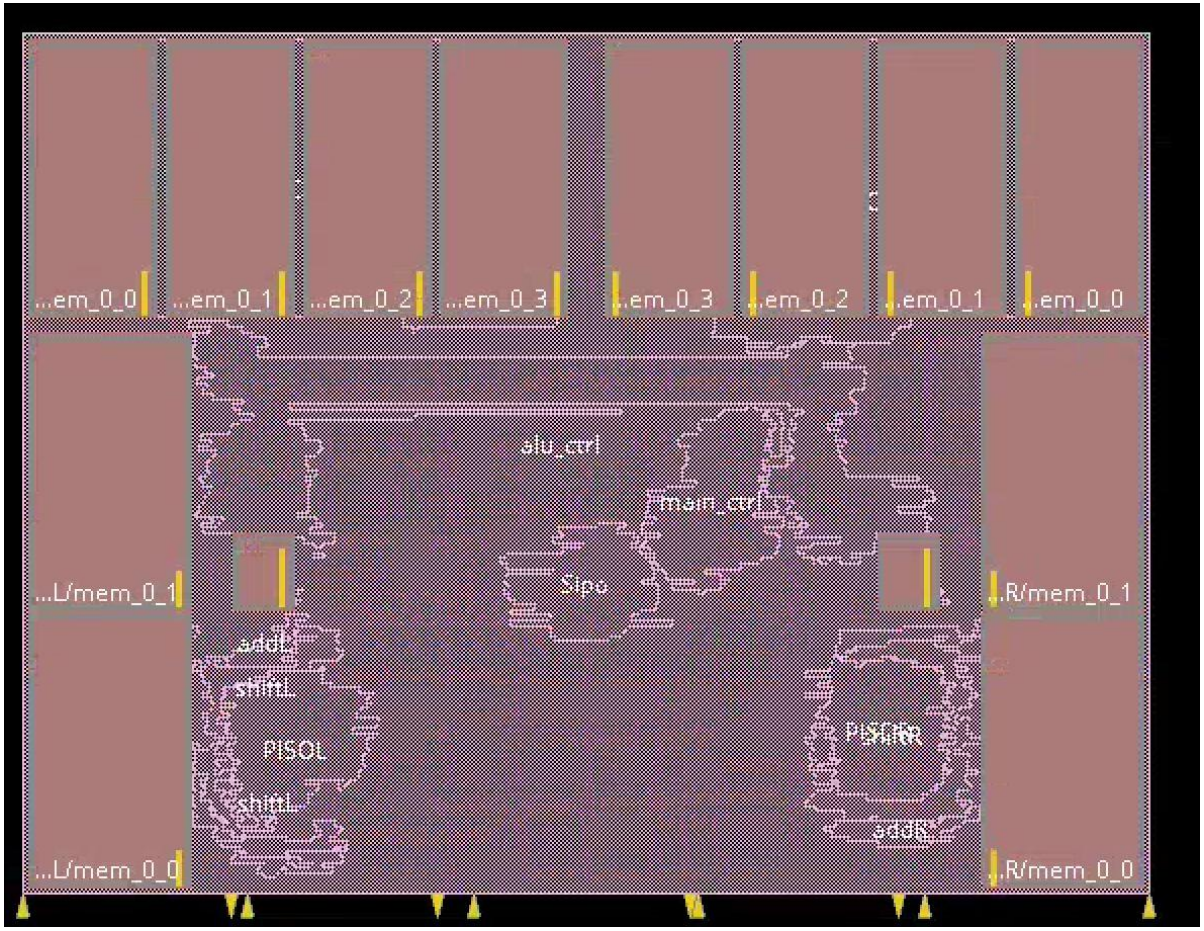
Open | setup.rpt | ~/Spring25/ASIC_DESIGN/Final_Project/MSDAP_1/Genus/reports | Save

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 19.14-s108_1
  Generated on:           May 05 2025  11:37:13 am
  Module:                 top
  Operating conditions:   PVT_0P63V_100C
  Interconnect mode:      global
  Area mode:              physical library
============================================================


Path 1: MET (16348 ps) Setup Check with Pin PISOR/count_bit_reg[5]/CLK->D
           View: PVT_0P63V_100C.setup_view
          Group: Sclk
     Startpoint: (F) alu_ctrl/p2sR_en_reg/CLK
          Clock: (F) Sclk
       Endpoint: (R) PISOR/count_bit_reg[5]/D
          Clock: (R) Sclk

                     Capture       Launch
        Clock Edge:+   33333        16667
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=   33333        16667

             Setup:-      18
       Uncertainty:-     100
     Required Time:=   33215
      Launch Clock:-   16667
         Data Path:-     201
             Slack:=   16348

#----------------------------------------------------------------------------------------------------------
```

Layout



Amoeba View


...em_0_0
...em_0_1
...em_0_2
...em_0_3
...em_0_3
...em_0_2
...em_0_1
...em_0_0
alu_ctrl
main_ctrl
...L/mem_0_1
...R/mem_0_1
sipo
addL
shiftL
PISOL
shiftL
addR
...L/mem_0_0
...R/mem_0_0

Schematic


Sclk
Dclk
Inputs
Reset_n
Start
ma...
alu_c...
shift_...
InReady
OutReady
Frame
OutputR
shift_a...

DRC

```
#############################################################
#  Generated by:      Cadence Innovus 19.11-s128_1
#  OS:                Linux x86_64(Host ID engnx06a.utdallas.edu)
#  Generated on:      Fri May  9 22:28:46 2025
#  Design:            top
#  Command:           check_drc -limit 2000 -out_file reports/drc.rpt
#############################################################

No DRC violations were found
```

LVS Check

Comparison Results ×

Layout Cell / Type	Source Cell	Count	Nets	Instances	Ports
top	top	202	152192L, 7566S (+144626)	155979L, 11353S (+144626)	11L, 13S (-2)
Discrepancies		202			
Incorrect Nets		100			
Incorrect Ports		2			
Incorrect Instances		100			

Cell top Summary (202 Discrepancies)

```
                  CELL COMPARISON RESULTS ( TOP LEVEL )


                #   #        ####################
                 # #         #                  #
                  #          #     INCORRECT    #
                 # #         #                  #
                #   #        ####################


  Error:    Different numbers of ports (see below).
  Error:    Different numbers of nets (see below).
  Error:    Different numbers of instances (see below).
  Warning:  Ambiguity points were found and resolved arbitrarily.

LAYOUT CELL NAME:         top
SOURCE CELL NAME:         top

------------------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:             11        13    *
 Nets:          160380     15850    *
 Instances:      85871     13558    *    MN (4 pins)
                 85871     13558    *    MP (4 pins)
                     8         8         SRAM1RW128x12 (37 pins)
                     4         4         SRAM1RW256x8 (30 pins)
                     2         2         SRAM2RW16x8 (50 pins)
                ------    ------
 Total Inst:    171756     27130


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------
```

Innovus Area Report

Hinst Name	Module Name	Inst Count	Total Area
top		2938	19839.732
COL	CO_MEM	71	5865.933
COR	CO_MEM_1	71	5865.685
PISOL	PISO	316	37.777
PISOR	PISO_1	314	37.704
Sipo	SIPO	230	29.466
addL	adder	182	20.514
addR	adder_1	180	20.368
alu_ctrl	alu_controller	751	76.355
data_memL	DATA_MEM	6	3722.675
data_memR	DATA_MEM_757	6	3722.092
main_ctrl	main_controller	332	36.027
mux_coeffL_addr	mux_coeff_2to1_WIDTH9	17	1.648
mux_coeffR_addr	mux_coeff_2to1_WIDTH9_1	10	1.225
rj_memL	R_MEM	4	169.063
rj_memR	R_MEM_758	4	168.772
shiftL	shift_accumulator	176	26.346
shiftR	shift_accumulator_1	181	26.667
u_mux_rjL_addr	mux_rj_2to1_WIDTH4	5	0.627
u_mux_rjR_addr	mux_rj_2to1_WIDTH4_1	6	0.685

Innovus Hold Report

```
#####################################################################
#  Generated by:      Cadence Innovus 19.11-s128_1
#  OS:                Linux x86_64(Host ID engnx06a.utdallas.edu)
#  Generated on:      Fri May  9 22:23:39 2025
#  Design:            top
#  Command:           report_timing -early -max_paths 3 > reports/hold.rpt
#####################################################################
Path 1: VIOLATED (-0.500 ps) Hold Check with Pin Sipo/frame_stat_reg/CLK->D
              View: PVT_0P77V_0C.hold_view
             Group: Dclk
       Startpoint: (R) Sipo/count_bit_reg[1]/CLK
            Clock: (F) Dclk
         Endpoint: (F) Sipo/frame_stat_reg/D
            Clock: (F) Dclk

                      Capture          Launch
       Clock Edge:+  651000.000       651000.000
      Src Latency:+     -51.803          -51.803
      Net Latency:+      59.553 (P)       49.428 (P)
          Arrival:=  651007.750       650997.625

             Hold:+       9.438
      Uncertainty:+     100.000
      Cppr Adjust:-       0.000
    Required Time:=  651117.188
     Launch Clock:=  650997.625
        Data Path:+     119.062
            Slack:=      -0.500
    +-------------------------------------------------------------------------------------------------------------------------+
    |        Timing Point         | Flags |   Arc    | Edge |          Cell           | Fanout | Trans | Delay | Arrival |
    |                             |       |          |      |                         |        |  (ps) |  (ps) |   (ps)  |
    |-----------------------------+-------+----------+------+-------------------------+--------+-------+-------+---------|
    | Sipo/count_bit_reg[1]/CLK   |       | CLK      | R    | (arrival)               |     38 | 25.200 |       | 650997.625 |
    | Sipo/count_bit_reg[1]/QN    |       | CLK->QN  | R    | ASYNC_DFFHx1_ASAP7_75t_SL |      1 | 25.200 | 29.900 | 651027.500 |
    | Sipo/FE_PHC76_count_bit_1/Y |       | A->Y     | R    | HB4xp67_ASAP7_75t_SRAM  |      4 | 11.600 | 58.688 | 651086.188 |
    | Sipo/g1957__8428/Y          |       | A->Y     | R    | OR2x2_ASAP7_75t_SL      |      4 | 34.700 | 15.438 | 651101.625 |
    | Sipo/g2598__5107/Y          |       | B->Y     | F    | NAND2xp5_ASAP7_75t_SL   |      3 |  7.900 |  0.500 | 651102.125 |
    | Sipo/g2548__5115/Y          |       | B->Y     | R    | NAND2xp5_ASAP7_75t_SL   |      3 | 10.900 |  9.688 | 651111.812 |
    | Sipo/g2540/Y                |       | A->Y     | F    | INVxp67_ASAP7_75t_SL    |      1 | 14.900 |  4.875 | 651116.688 |
    | Sipo/frame_stat_reg/D       |       | D        | F    | ASYNC_DFFHx1_ASAP7_75t_SL |      1 |  8.300 |  0.000 | 651116.688 |
    +-------------------------------------------------------------------------------------------------------------------------+
Path 2: VIOLATED (-0.491 ps) Hold Check with Pin rj_memR/mem_0_0/CE1->A1[0]
              View: PVT_0P77V_0C.hold_view
             Group: Sclk
       Startpoint: (R) main_ctrl/rj_enable_reg/CLK
            Clock: (R) Sclk
         Endpoint: (F) rj_memR/mem_0_0/A1[0]
            Clock: (R) Sclk
```

Innovus Power Report

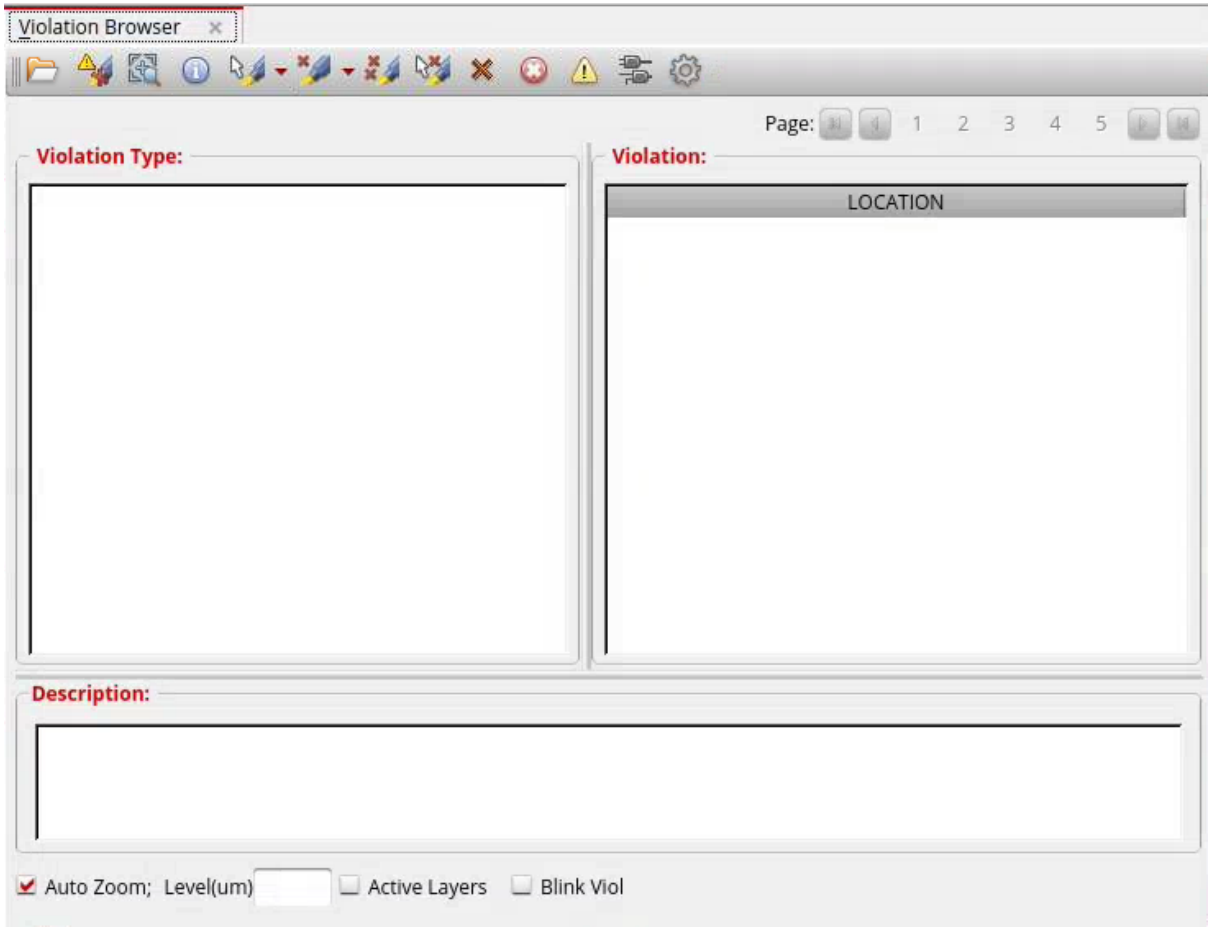
```
Total Power
----------------------------------------------------------------------------------------------
Total Internal Power:         0.03127723            16.4202%
Total Switching Power:        0.01104359             5.7978%
Total Leakage Power:          0.14815900            77.7820%
Total Power:                  0.19047983
----------------------------------------------------------------------------------------------

Group                            Internal    Switching      Leakage        Total   Percentage
                                 Power       Power          Power          Power   (%)
----------------------------------------------------------------------------------------------
Sequential                        0.01284    0.0003923      0.03964      0.05288        27.76
Macro                                   0    0.0001015            0    0.0001015      0.05327
IO                                      0            0            0            0           0
Combinational                    0.006596     0.005932      0.08953       0.1021       53.58
Clock (Combinational)             0.01184     0.004618      0.01898      0.03544       18.61
Clock (Sequential)                      0            0            0            0           0
----------------------------------------------------------------------------------------------
Total                             0.03128      0.01104       0.1482       0.1905         100
----------------------------------------------------------------------------------------------

Rail                    Voltage  Internal    Switching      Leakage        Total   Percentage
                                 Power       Power          Power          Power   (%)
----------------------------------------------------------------------------------------------
VDD                        0.63   0.03128      0.01104       0.1482       0.1905         100

Clock                            Internal    Switching      Leakage        Total   Percentage
                                 Power       Power          Power          Power   (%)
----------------------------------------------------------------------------------------------
Dclk                            1.615e-05    7.582e-06   0.0008641    0.0008879       0.4661
Sclk                              0.01182      0.00461     0.01812      0.03455        18.14
----------------------------------------------------------------------------------------------
Total (excluding duplicates)      0.01184     0.004618      0.01898      0.03544       18.61
----------------------------------------------------------------------------------------------
Clock: Dclk
Clock Period: 0.033333 usec
Clock Toggle Rate:      1.5361 Mhz
Clock Static Probability:  0.5000

Clock: Sclk
Clock Period: 0.033333 usec
Clock Toggle Rate:     60.0001 Mhz
Clock Static Probability:  0.5000
```

Innovus Setup Report

```
#############################################################
#  Generated by:      Cadence Innovus 19.11-s128_1
#  OS:                Linux x86_64(Host ID engnx06a.utdallas.edu)
#  Generated on:      Fri May  9 22:23:37 2025
#  Design:            top
#  Command:           report_timing -late -max_paths 3 > reports/setup.rpt
#############################################################
Path 1: MET (15064.346 ps) Setup Check with Pin shiftL/shift_reg_reg[39]/CLK->D
              View: PVT_0P63V_100C.setup_view
             Group: Sclk
        Startpoint: (R) data_memL/mem_0_0/CE
             Clock: (R) Sclk
          Endpoint: (F) shiftL/shift_reg_reg[39]/D
             Clock: (F) Sclk

                      Capture        Launch
       Clock Edge:+  16666.650         0.000
      Src Latency:+   -120.687      -107.774
      Net Latency:+    115.101 (P)   118.900 (P)
          Arrival:=  16661.064        11.126

            Setup:-      8.393
      Uncertainty:-    100.000
      Cppr Adjust:+      0.000
    Required Time:=  16552.672
     Launch Clock:=     11.126
        Data Path:+   1477.200
            Slack:=  15064.346
```

Timing Point	Flags	Arc	Edge	Cell	Fanout	Trans (ps)	Delay (ps)	Arrival (ps)
data_memL/mem_0_0/CE		CE	R	(arrival)	1	39.800		11.136
data_memL/mem_0_0/O[0]		CE->O[0]	R	SRAM1RW256x8	2	39.800	202.000	213.136
addL/sub_9_38_Y_add_10_30_g1375__2346/Y		A->Y	R	XOR2xp5_ASAP7_75t_SL	2	33.100	41.500	254.636
addL/sub_9_38_Y_add_10_30_g1265__8246/Y		B->Y	F	MAJIxp5_ASAP7_75t_SL	2	106.500	34.200	288.836
addL/sub_9_38_Y_add_10_30_g1263__5122/Y		C->Y	R	MAJIxp5_ASAP7_75t_SL	2	59.900	33.000	321.836
addL/sub_9_38_Y_add_10_30_g1260__2802/Y		C->Y	F	MAJIxp5_ASAP7_75t_SL	2	71.400	23.400	345.235
addL/sub_9_38_Y_add_10_30_g1258__1617/Y		C->Y	R	MAJIxp5_ASAP7_75t_SL	2	59.500	29.700	374.935
addL/sub_9_38_Y_add_10_30_g1255__6783/Y		A->Y	F	MAJIxp5_ASAP7_75t_SL	2	64.900	24.700	399.634
addL/sub_9_38_Y_add_10_30_g1253__5526/Y		A->Y	R	MAJIxp5_ASAP7_75t_SL	2	55.200	31.900	431.534
addL/sub_9_38_Y_add_10_30_g1250__4319/Y		A->Y	F	MAJIxp5_ASAP7_75t_SL	1	65.400	16.000	447.534
addL/FE_PHC279_sub_9_38_Y_add_10_30_n_152/Y		A->Y	F	HB4xp67_ASAP7_75t_SRAM	2	43.100	159.200	606.733
addL/sub_9_38_Y_add_10_30_g1248__6260/Y		A->Y	R	MAJIxp5_ASAP7_75t_SL	2	63.700	33.700	640.434
addL/sub_9_38_Y_add_10_30_g1245__2398/Y		A->Y	F	MAJIxp5_ASAP7_75t_SL	2	66.000	24.800	665.233
addL/sub_9_38_Y_add_10_30_g1243__5477/Y		A->Y	R	MAJIxp5_ASAP7_75t_SL	2	52.400	31.200	696.433
addL/sub_9_38_Y_add_10_30_g1240__7410/Y		A->Y	F	MAJIxp5_ASAP7_75t_SL	1	62.800	15.000	711.433
addL/FE_PHC362_sub_9_38_Y_add_10_30_n_158/Y		A->Y	F	HB3xp67_ASAP7_75t_SRAM	2	39.400	123.300	834.732

DRC Check


Violation Browser
Page: 1 2 3 4 5
Violation Type:
Violation:
LOCATION
Description:
Auto Zoom; Level(um)
Active Layers
Blink Viol

Thank You