EEDG/CE 6303: Testing and Testable Design (Spring'2024)

Department of Electrical & Computer Engineering

The University of Texas at Dallas

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Cover Page for All Submissions

(Assignment, Project, Codes/Simulations/CAD, Examinations, etc.)

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Submission Materials for (e.g. Homework #, Project #): Homework 4

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Homework-4

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(14.5)

Let us take the following MATS+ scheme

$\{ \Updownarrow(w_0) ; \Uparrow(r_0, w_1) ; \Downarrow(r_1 w_0) \}$

Expansion B-cell word the following schematic is applied

$\{ \Updownarrow(w_a) ; \Uparrow(r_a, w_b) ; \Downarrow(r_b, w_a) \}$

where b is Complement of 'a', 'a' & 'b' are called background words also called as

$\{ \Updownarrow(w_{00 \ldots 0}) ; \Uparrow(r_{00 \ldots 0}, w_{11 \ldots}) \Downarrow(r_{11 \ldots}, w_{00 \ldots 0}) \}$

since SAF is related to single cell, SAFs can be detected by

$(v_{x \ldots x} \ldots w_{x \ldots x})$ and

$(v_{x \ldots x} \ldots w_{x \ldots x})$ are satisfied with

M_1 & M_2 it can detect AF's

Consider the following

$\{ \Updownarrow . w_{0000}) ; \Uparrow (r_{0000}, w_{1111}) ; \Downarrow (r_{1111}, w_{0000})$

these can detect SA0 & SA1

14.6) Restrictions of march tests are

1. the RA → WA is incremented upon the completion of Read/write operation, so $\Uparrow$ is used in march elements

2. march can only contain a single Read and/or a single write operation i.e., only march elements of the pattern

$\Uparrow (r_x), \Uparrow (w_x), \Uparrow (r_x, w_y), \Uparrow (w_y, r_x);$

$x, y = 0/1$

So not all AFs and not all CF's will be detected.

(14.7)

1-bit memory, so if we take following

A[0]=0, A[1]=1, A[2]=0 .... A[256]=0 ...

1=(1028)A ...

Read A[I] and write Complement.

A[0]=0, A[1]=1, A[2]=0 ... A[256]=0 ....

A[1028]=1

Read A[I]

→ To detect linked AFs, $(r_x \ldots w_x)$

or $(\overline{r_0}, \ldots w_x)$ is used. if

(r_0, w_1) is used only.

A[0], A[2] were detected. So

All AFs cannot be covered.

→ for stuck at fault : SA0 : $\{\Uparrow w_0 ; \Uparrow (w_1, r_1)\}$

is used and SA1.

$\{\Uparrow w_1, \Uparrow (w_0, r_0)\}$ is used.

So All SAFs Can be detected.

→ since, only 1 transition, All TFs Cannot be detected.

→ All the CFst Cannot be detected by this test. like $\langle 0, 1 \rangle$ Cannot be detected.

(14.8)

→ linked CFids of the form

$\langle \uparrow ; \downarrow \rangle a_1 v \# \langle \uparrow ; \uparrow \rangle a_2 v$

this holds that $a_1 < v$ & $a_2 < v$; also this contains $a_1 < a_2$ & $a_2 < a_1$. this fault is detected by

$\{\Updownarrow(w_0) ; \Uparrow(r_0, w_1) ; \Uparrow(r_1, w_0, w_1)\}$

→ $\langle \uparrow ; \downarrow \rangle \# \langle \uparrow ; \uparrow \rangle$ holds that for $\langle \uparrow ; \downarrow \rangle \# \langle \uparrow ; \uparrow \rangle$ the a-cells take any relative. to v-cell, this can be detected, by $\{\Uparrow(w_0) ; \Uparrow(r_0, w_1) ; \Uparrow(r_1, w_0, w_1) ; \Downarrow(r_1, w_0, w_1) ; \Uparrow(w_0) ; \Downarrow(r_0, w_1)\}$

2)

Faults	Sensitizes	Detects
AF	M_2, M_1	M_3, M_4
SAF	M_0, M_1	M_1, M_2
TF	M_1, M_2	M_2, M_3
$CF_{in}(a<v, <\uparrow;\downarrow>)$	M_1	M_1
$CF_{in}(a<v, <\downarrow;\uparrow>)$	M_2	M_2
$CF_{in}(a>v <\uparrow;\updownarrow>)$	M_3	M_3
$CF_{in}(a>v <\downarrow;\updownarrow>)$	M_4	M_4
$CF_{in}(a<v, <\uparrow;0>)$	M_3	M_4
$CF_{in}(a<v; <\uparrow;1>)$	M_1	M_1
$CF_{in}(a<v <\downarrow;0>)$	M_2	M_2
$CF_{in}(a<v, <\downarrow;1>)$	M_4	M_5
$CF_{in}(a>v, <\uparrow;0>)$	M_1	M_4
$CF_{in}(a>v, <\uparrow;1>)$	M_5	M_3
$CF_{in}(a>v, <\downarrow;0>)$	M_4	M_4
$CF_{in}(a>v, <\downarrow;\uparrow>)$	M_2	M_3
$CF_{st}(a<v, <0;0>)$	M_2	M_2

Faults	sensitizes	Detects
$cfst(a<v, \langle 0;1 \rangle)$	M_4	M_5
$cfst(a<v, \langle 1;0 \rangle)$	M_3	M_4
$cfst(a<v, \langle 1;1 \rangle)$	M_1	M_1
$cfst(a>v, \langle 0;0 \rangle)$	M_4	M_4
$cfst(a>v, \langle 0;1 \rangle)$	M_2	M_3
$cfst(a>v, \langle 1;0 \rangle)$	M_1	M_2
$cfst(a>v; \langle 1;1 \rangle)$	M_3	M_3
linked CFid	cannot	cannot

3) March X

{ M_0 : $\Updownarrow(w0)$; M_1 : $\Uparrow(r0, w1, r1)$;

M_2 $\Downarrow(r1, w0, r0)$: M_3 ; $\Updownarrow(r0)$

1) AFs : (rx, wx) and $rx, wx)$ should be satisfied. Conditions are met by M_1 and M_2. so faults are detected.

2) SAFs : for SA0 M_1 satisfies M_2 will detect for SA1 M_2 will satisfies and M_3 will detect.

3) TFs → $<\uparrow/0>$: w_1 sensitizes and detects. M_1 sensitizes and M_2 detect it

→ $<\downarrow/1>$: w_0 sensitizes it and ~~to~~ detects it

M_2 sensitize and M_3 detect

All TFs detected.

(iv) unlinked CFs : ① CF_{ii}

In $<\uparrow; \updownarrow>$: Aggressor goes from 0 to 1 and its complemented.

Case-1 :- $v > a$

In this case, M_1 sensitize it (w_1) and M_1 will detect it (r_0)

Case-2 :- $a > v$

Here, fault will sensitize M_1 and M_2 detects it.

② $<\downarrow; \updownarrow>$:- Aggressor has falling condition 1 to 0 and victim is complemented

Case-1 :- $a > v$

M_2 will sensitize (w_0) and detective (r_1)

Case-2 :- $v > a$

M_2 sensitize and M_3 detect

All CFs detected

2) CFid

subtypes are

$<\uparrow;\uparrow>$; $<\uparrow;\downarrow>$, $<\downarrow;\uparrow>$, $<\downarrow;\downarrow>$

→ $<\uparrow;\uparrow>$ = agressor 0 to 1 and victim also 0 to 1

① ; $v > a$

M_1 sensitize and detect

② ; $a > v$

not detected

→ $<\uparrow;\downarrow>$

Agg → 0 to 1 victim → 1 to 0

$v > a$ → M_1 (sens) and M_2 (Detect)

$a > v$ → M_1 (sens) and M_2 (detect)

→ $<\downarrow;\uparrow>$

Agg → 1 to 0 victim → 0 to 1

$v > a$ → M_2 (S) M_3 (D)

$a > v$ → M_2 (S) M_3 (D)

→ <⇓;⇓>

Ag → 1 to 1 victim → 1 to 0

v > a → $M_2(S)$, no detect

a > v → $M_2(S)$, M_3 detect

③ CFsts :-

for static Coupling faults, we can use state validation table.

i → Agressor j → victim.

(i) j > i

Match element	states S_{ij} before op	op	state S_{ij} after op
M_0	—	w_0 into i	—
	—	w_0 into j	S_{00}
M_1	S_{00}	r_0 from i	S_{00}
	S_{00}	w_1 into i	S_{10}
	S_{10}	r_0 from j	S_{10} Liner
	S_{00}	w_1 into j	S_{11}
M_2	S_{11}	r_1 from j	S_{11}
	S_{11}	w_0 into j	S_{10}
	S_{10}	r_1 from i	S_{10}
	S_{10}	w_0 into i	S_{00}
M_3	S_{00}	r_0 from i	S_{00}
	S_{00}	r_0 from j	S_{00} L_2

$L-1$ detects $\langle 1;1 \rangle$
$L-2$ detect $\langle 0;1 \rangle$
$\langle 1;0 \rangle$ no detect
$\langle 0;0 \rangle$ no detect.

(2) $i > j$

M_0	—	w_0 from j	—
	—	w_0 into i	S_{00}
M_1	S_{00}	r_0 from j	S_{00}
	S_{00}	w_1 into j	S_{01}
	S_{01}	r_0 from 1	S_{01}
	S_{01}	w_1 from i	S_{11}
M_2	S_{11}	r_1 from i	S_{11}
	S_{11}	w_0 into i	S_{01}
	S_{01}	r_1 from j	S_{01}
	S_{01}	w_0 from j	S_{00}
M_3	S_{00}	r_0 from i	S_{00}
	S_{00}	r_0 from j	S_{00}

$\langle 0;1 \rangle$ will be detected
Few CFst are detected

⑤ linked cfid :-

Case-1 :- $<a_1, v>$ $(\uparrow ; \uparrow)$ S-sensitizes

D-detect

$<a_2, v>$ $(\uparrow ; \downarrow)$

$\rightarrow a_1 < a_2 < v$

$(\uparrow ; \uparrow)$ $(\uparrow ; \downarrow)$ not detected

a_1 a_2 v

$\rightarrow a_2 < a_1 < v$

$(\uparrow ; \downarrow)$ $(\uparrow ; \uparrow)$

M_1 c sensitizes and detect.

$\rightarrow a_1 < v < a_2$

$(\uparrow ; \uparrow)$ $(\uparrow ; \downarrow)$ a_2

a_1 v

$M_1 \rightarrow S$ $M_2 (D)$

$\rightarrow a_2 < v < a_1$

$(\uparrow ; \downarrow)$ $(\uparrow ; \uparrow)$ not detected

a_2 v a_1

$\rightarrow v < a_1 < a_2$

$(\uparrow ; \uparrow)$ $(\uparrow ; \downarrow)$ $M_1 (S)$ $M_2 (D)$

v a_1 a_2

Case-2 :-

(a, v) $(\downarrow ; \downarrow)$

(a_2, v) $(\downarrow ; \uparrow)$

→ $a_1 < a_2 < v$

$(\downarrow ; \downarrow)$ $(\downarrow ; \uparrow)$ not detected.

a_1 a_2

→ $a_2 < a_1 < v$

$(\downarrow ; \uparrow)$ $(\downarrow ; \downarrow)$

a_2 a_1 v

$M_1(S)$ $M_2, M_3(D)$

→ $a_1 < v < a_2$

$(\downarrow ; \downarrow)$ a_2 $(\downarrow ; \uparrow)$ not detect

→ $a_2 < v < a_1$

$(\downarrow ; \uparrow)$ $(\downarrow ; \uparrow)$

$M_1(S)$ → not detected.

→ $v < a_2 < a_1$

$(\downarrow ; \uparrow)$ $(\downarrow ; \downarrow)$ not detected

v a_2 a_1

few CFid faults detected.

Q4)

This Paper “Memory Test Optimization: An Industrial Evaluation of DRAM Tests” relates to the methodology and application of DRAM chips as this study consists of testing vast range of DRAM chips with 48 vector test combinations of stress and its dependencies. This gives weightage to the perfect stress combination for effective fault coverage. Moreover, tests should be according to the specific technology in usage to nullify the defects. This covers all combinations of march, base cell, repetitive, electric etc. which covers specific types of faults.

Observations reveal that voltage and temperature influence’s fault coverage to some extent, a vast list of base tests are included with their stress condition combinations and percentage of fault coverage that will be turned out. As we are dealing with DRAM majority of faults are caused by the leakage currents at the capacitor and refresh failures, loss of data due to gate level switching, stuck at faults at critical juncture etc. as influenced by high temperatures, so High Temperature (HT) test reveals or covers most of them. Analysis also points out different types of address stresses, timing stresses factor the fault detection in the chips, faults between the cells in the same lines are more likely to show the least effectiveness by address complement stress. After optimization of the stress test times, comparison of results at high and room temperature are noticed, mostly theoretically calculated fault coverage for tests has the highest fault coverage in the actual test result even though there is a clarification needed in modelling the stresses and deduce the fault coverage of that stress test vectors.

To Check in the specific test grouping, 32 DUTs in the HT testing group—which we refer to as single faults—and 37 DUTs in the RT testing category can only be identified by a single test and lots of single tests detect the number of DUTs. Since these tests will be necessary to reach an FC of 100%, it requires us to examine the DUTs identified by a single test.

The study looks to enhance the DRAM testing process through test time savings and ultimately cost savings. This focused on the more challenging uncovering problems, even though some errors might be discovered after multiple tests. Consequently, the plot only contains the problematic DUTs that were discovered by twelve out of around more than eight hundred tests. It highlights the careful balancing act between comprehensive testing and feasibility, implying that further study be conducted to reduce test durations while reducing the problems if any.