

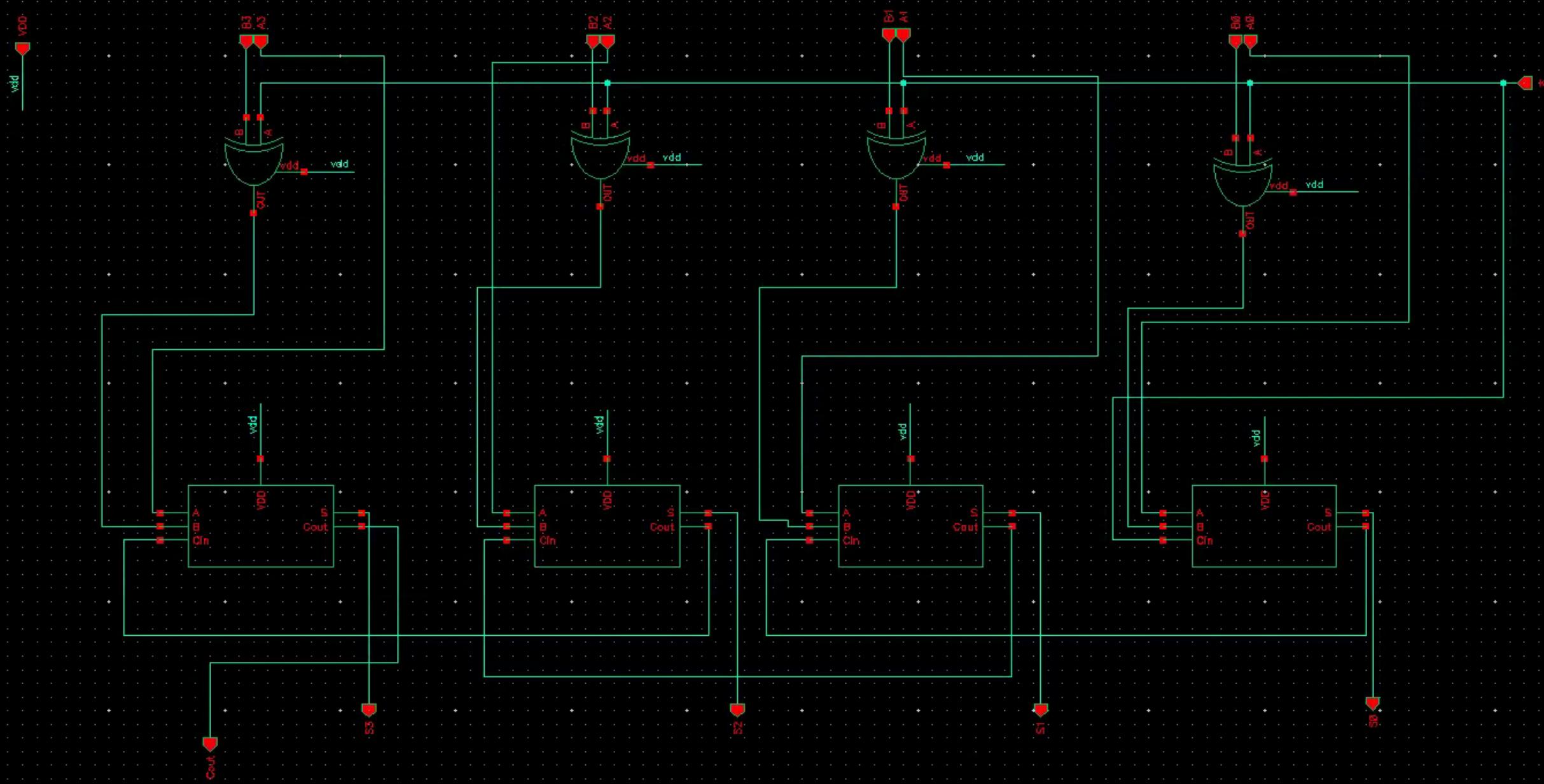
VLSI DESIGN (CE 6325)

4- Bit Microprocessor

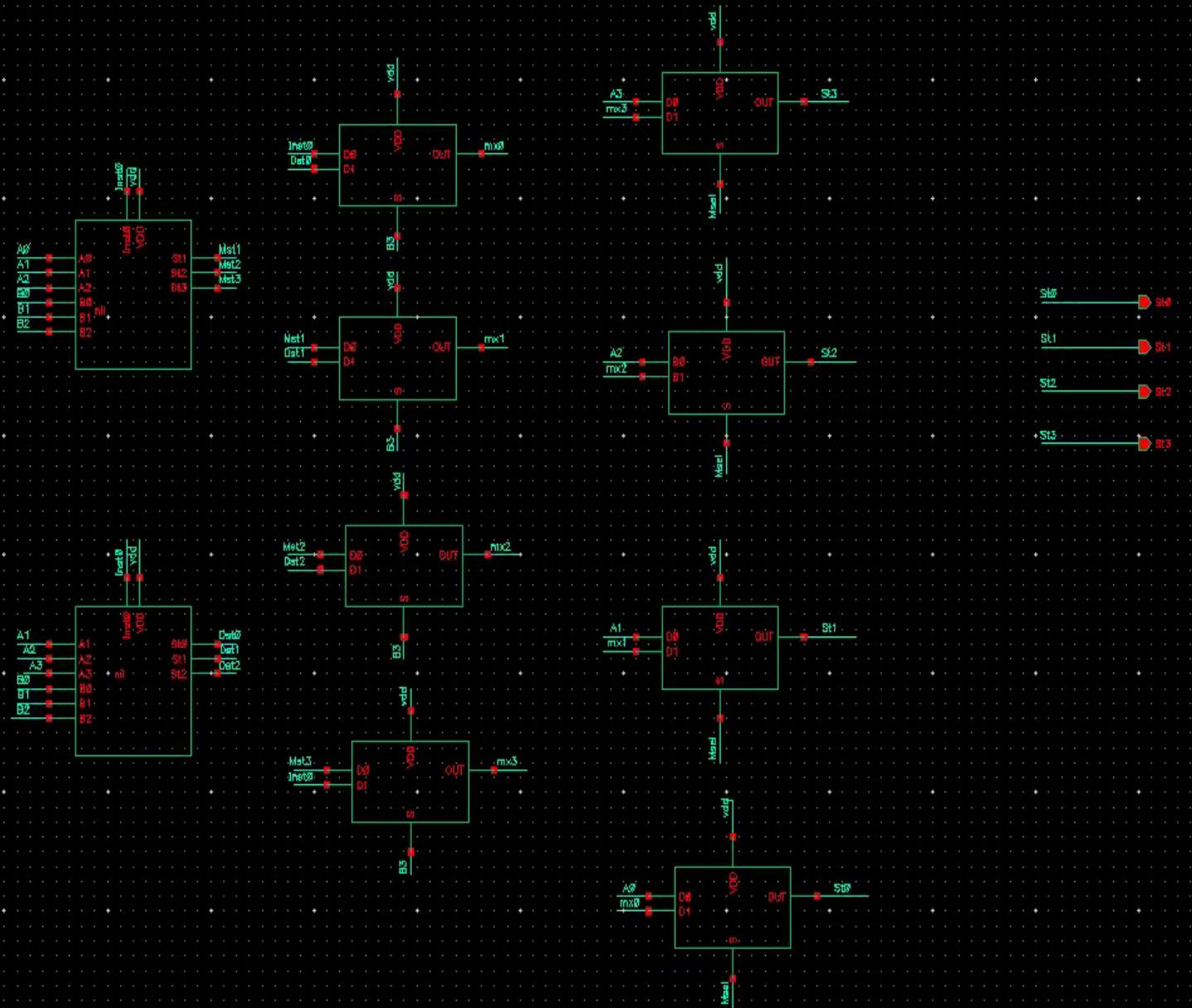
Team Members:
Kodanda Rama Yaswanth Kumar Ramadugu
(KXR230001)
Uday Teja Bandaru (UTB220000)

Initial Schematic:

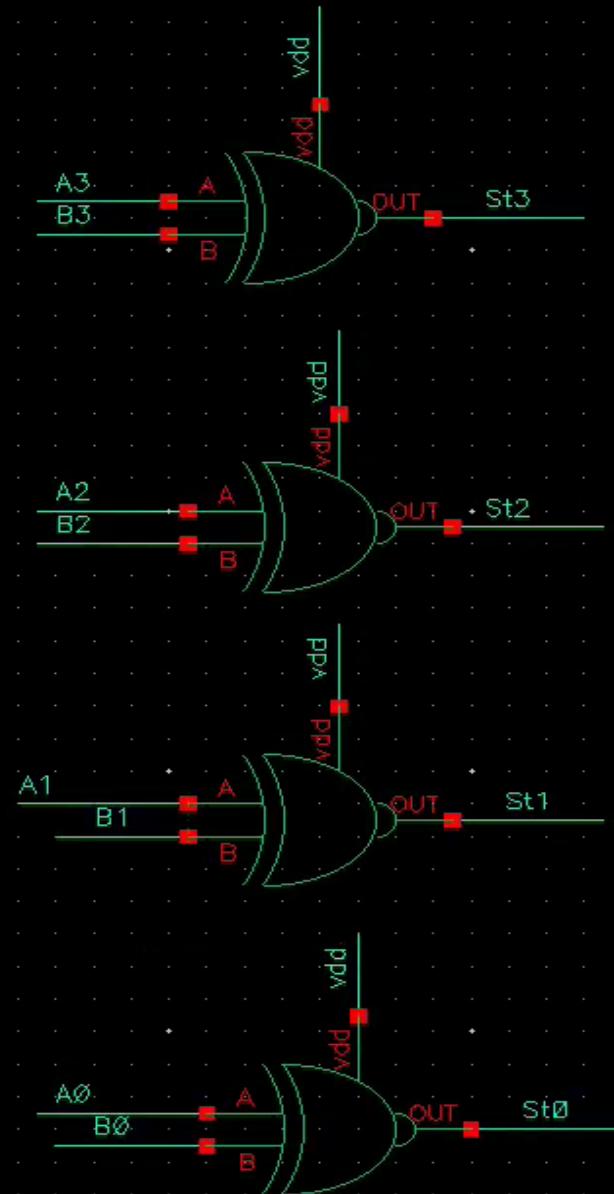
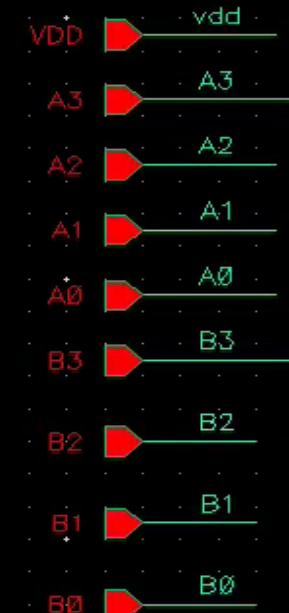
Add/Sub Block



Mul/ Div Block



XNOR Block



Verilog Code:

```
module Top_alu (
    input [3:0] A,           // First 4-bit input word
    input [1:0] Inst,        // Mode selection inputs
    input RESET,            // Reset input
    input clk,              // Clock input
    output reg [3:0] OUT    // Output word
);
wire [3:0] sum;
wire IInst;
add_sub_4_bit add_sub (
    .a(OUT),
    .b(A), // Connect to the reg
    .k(Inst[0]), // Use the least significant bit of Inst for the subtraction mode
    .sum(sum),
    .cout()
);
assign IInst = Inst[1] & Inst[0];
// Synchronous process triggered by rising edge of clock or RESET
always @(posedge clk) begin
    if (RESET) begin
        OUT <= 4'b0000;
    end else begin
        // ALU operation based on mode selection
        case({Inst[1] & Inst[0], Inst[1]})
            2'b00: OUT <= sum; // ADD mode, B is OUT from previous operation
            2'b01: begin
                // MUL/DIV mode
                case(A[3])
                    1'b0: begin // Multiplication
                        case(A[2:0])
                            3'b100: OUT <= {A[2] & OUT[0], 3'b000};
                            3'b010: OUT <= {A[1] & OUT[1], A[1] & OUT[0], 2'b00};
                            3'b001: OUT <= {A[0] & OUT[2], A[0] & OUT[1], A[0] & OUT[0], 1'b0};
                            default: OUT <= 4'b0000; // No Multiplication
                        endcase
                    end
                    1'b1: begin // Division
                        case(A[2:0])
                            3'b100: OUT <= {3'b000, A[2] & OUT[3]};
                            3'b010: OUT <= {2'b00, A[1] & OUT[3], A[1] & OUT[2]};
                            3'b001: OUT <= {1'b0, A[0] & OUT[3], A[0] & OUT[2], A[0] & OUT[1]};
                            default: OUT <= 4'b0000; // No division
                        endcase
                    end
                endcase
            end
            default: OUT <= ~(A ^ OUT); // XNOR mode, B is OUT from previous operation
        endcase
    end
end
```

```
end
endmodule
module add_sub_4_bit (
    input [3:0] a,
    input [3:0] b,
    input k, // Deciding bit: 0 for addition, 1 for subtraction
    output [3:0] sum,
    output cout
);
// Intermediate signals
wire [3:0] s;
wire c0, c1, c2;
wire [3:0]w1;
assign w1[0] = b[0] ^ k;
assign w1[1] = b[1] ^ k;
assign w1[2] = b[2] ^ k;
assign w1[3] = b[3] ^ k;

full_adder_1bit fa0 (.a(a[0]), .b(w1[0]), .cin(k), .sum(s[0]), .cout(c0));
full_adder_1bit fa1 (.a(a[1]), .b(w1[1]), .cin(c0), .sum(s[1]), .cout(c1));
full_adder_1bit fa2 (.a(a[2]), .b(w1[2]), .cin(c1), .sum(s[2]), .cout(c2));
full_adder_1bit fa3 (.a(a[3]), .b(w1[3]), .cin(c2), .sum(s[3]), .cout(cout));

// Output sum
assign sum = s;
endmodule

module full_adder_1bit (
    input a,
    input b,
    input cin,
    output sum,
    output cout
);

// Intermediate signals
wire s1, c1, c2;

// First stage: Add A, B, and Cin
xor xor1 (s1, a, b);
nand nand1 (c1, s1, cin);
nand nand2 (c2, a, b);
nand nand3 (cout, c1, c2);

// Second stage: Add Sum from first stage and Cin
xor xor2 (sum, s1, cin);
endmodule
```

Design Vision

NoMachine - Yash Activities Terminal Mon 11:25 engnx03a.utdallas.edu:/home/011/k/kx/kxr230001/Spring24/vlsi/design_vision

File Edit View Search Terminal Tabs Help

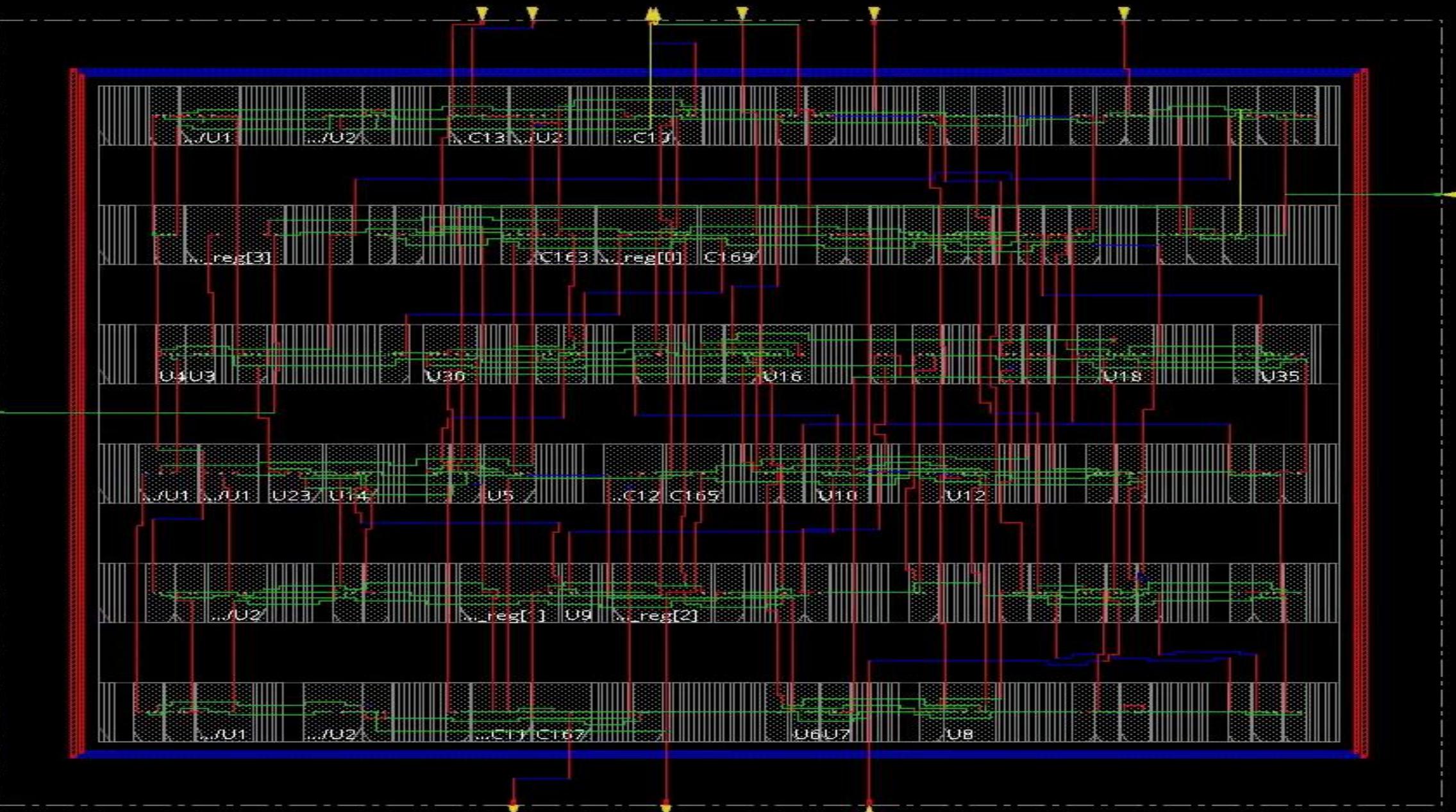
engnx03a.utdallas.edu:/hom... engnx03a.utdallas.edu:/hom... engnx03a.utdallas.edu:/hom... engnx03a.utdallas.edu:/hom... engnx03a.utdallas.edu:/hom... engnx03a.utdallas.edu:/hom...

add_sub/C10	XOR	standard_celllib	0.000000
add_sub/C11	XOR	standard_celllib	0.000000
add_sub/C12	XOR	standard_celllib	0.000000
add_sub/C13	XOR	standard_celllib	0.000000
add_sub/fa0/U1	XOR	standard_celllib	0.000000
add_sub/fa0/U2	XOR	standard_celllib	0.000000
add_sub/fa0/nand1	NAND	standard_celllib	0.000000
add_sub/fa0/nand2	NAND	standard_celllib	0.000000
add_sub/fa0/nand3	NAND	standard_celllib	0.000000
add_sub/fa1/U1	XOR	standard_celllib	0.000000
add_sub/fa1/U2	XOR	standard_celllib	0.000000
add_sub/fa1/nand1	NAND	standard_celllib	0.000000
add_sub/fa1/nand2	NAND	standard_celllib	0.000000
add_sub/fa1/nand3	NAND	standard_celllib	0.000000
add_sub/fa2/U1	XOR	standard_celllib	0.000000
add_sub/fa2/U2	XOR	standard_celllib	0.000000
add_sub/fa2/nand1	NAND	standard_celllib	0.000000
add_sub/fa2/nand2	NAND	standard_celllib	0.000000
add_sub/fa2/nand3	NAND	standard_celllib	0.000000
add_sub/fa3/U1	XOR	standard_celllib	0.000000
add_sub/fa3/U2	XOR	standard_celllib	0.000000

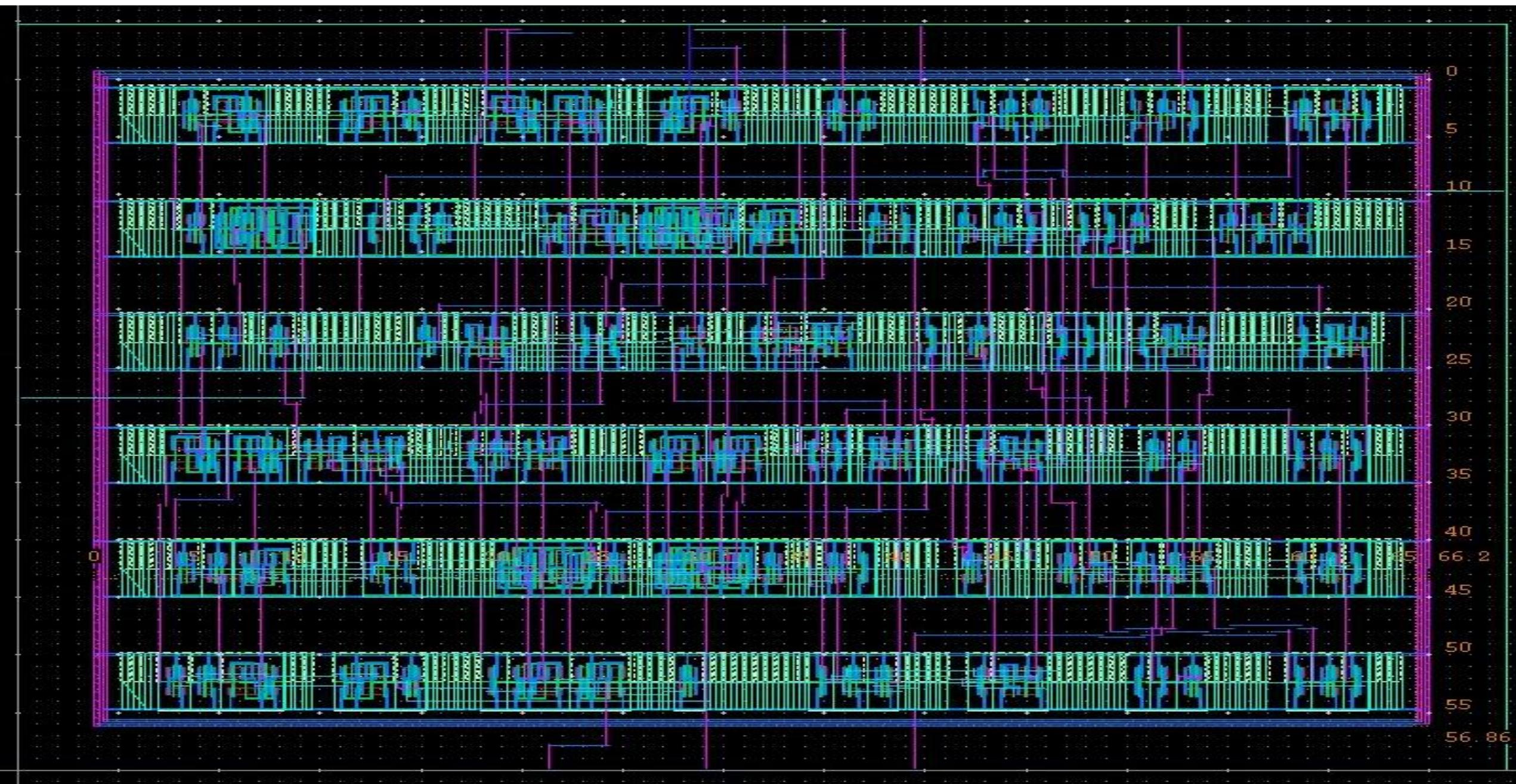
Total 117 cells			0.000000

```
design_vision> write -hierarchy -format verilog -output /home/011/k/kx/kxr230001/Spring24/vlsi/design_vision/f4_synth.v
Writing verilog file '/home/011/k/kx/kxr230001/Spring24/vlsi/design_vision/f4_synth.v'.
Warning: Verilog 'assign' or 'tran' statements are written out. (V0-4)
{engnx03a:~/Spring24/vlsi/design_vision} cd innovus
bash: cd: innovus: No such file or directory
```

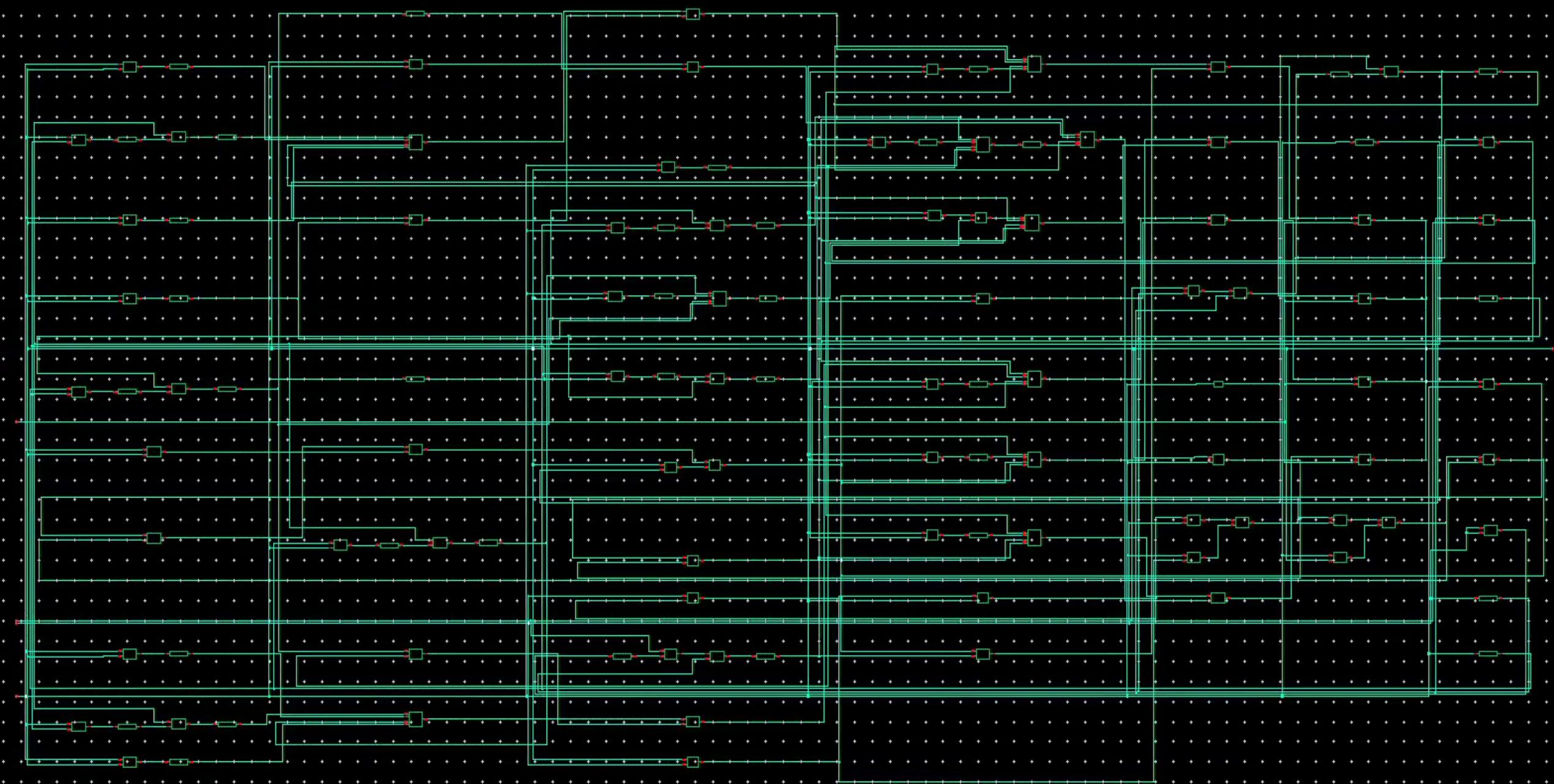
Innovus



Layout



Schematic



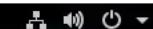
DRC

NoMachine - Yash



Activities Calibre

Tue 12:39



Calibre - RVE v2013.2_18.13 : Top_alu.drc.results

x

File View Highlight Tools Window Setup

Help

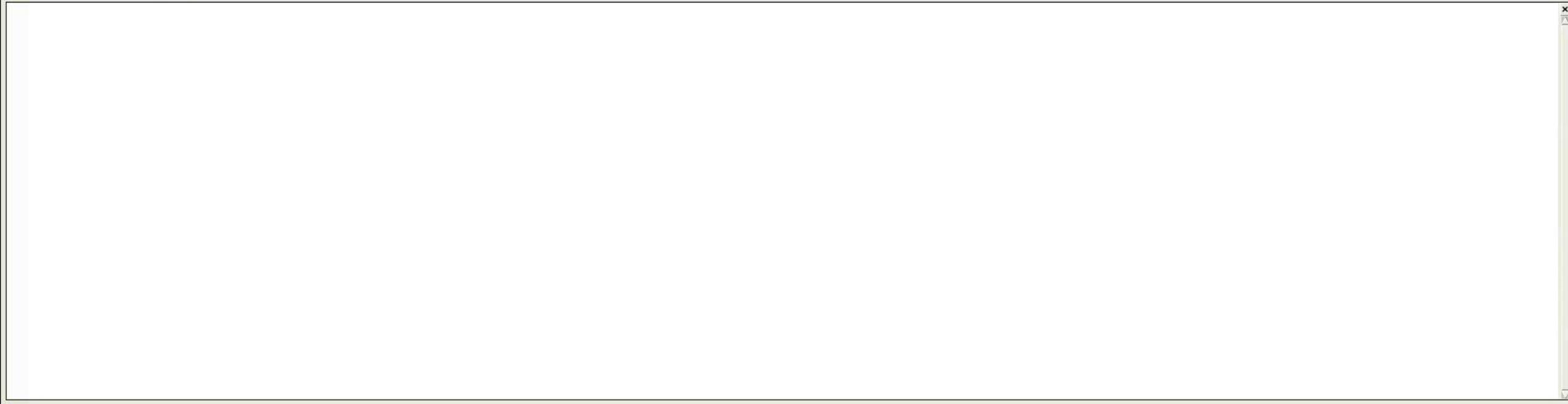


Search

Show Unresolved Top_alu, 0 Results (in 0 of 2078 Checks)

x

Check / Cell /	Results



LVS

NoMachine - Yash

Activities Calibre

Tue 12:41

Calibre - RVE v2013.2_18.13 : svdb Top_alu

File View Highlight Tools Window Setup Help

Navigator Comparison Results

Results Extraction Results Comparison Results

ERC ERC Results ERC Summary

Reports Extraction Report LVS Report

Rules Rules File

View Info Finder Schematics

Setup Options

Comparison Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
Top_alu	Top_alu	157L, 157S	217L, 217S	14L, 14S

Cell Top_alu Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

CORRECT #
#####

LAYOUT CELL NAME: Top_alu
SOURCE CELL NAME: Top_alu

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	14	14	
Nets:	309	310	*
Instances:	291 291	291 291	MN (4 pins) MP (4 pins)
Total Inst:	582	582	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	14	14	
Nets:	157	157	
Instances:	13	13	MN (4 pins)

PEX

NoMachine - Yash

Activities Calibre Interactive - PEX v2013.2_18.13 ▾



Calibre Interactive - PEX v2013.2_18.13

File Transcript Setup

Rules
Inputs
Outputs
Run Control
Transcript
Run PEX
Start RVE

```
--- OUTPUT NETLIST FILE NAME Top_alu.pex.netlist
--- OUTPUT PARASITIC MODEL FILE NAME Top_alu.pex.netlist.pex
--- PROCESSING PARASITIC MODELS
--- OUTPUT PARASITIC MODEL INSTANCE FILE NAME Top_alu.pex.netlist.TOP_ALU.pxi

--- NETWORK REDUCTION BEGIN:
--- READING FROM PDB...
--- BEGIN REDUCING NETS...
Ignore R=0.0238825 from (203,210) on layer 2909: self-loop at 205 after short removal
--- DONE REDUCING NETS...
--- WRITING TO PDB...
--- NETWORK REDUCTION COMPLETE: CPU TIME = 0 REAL TIME = 0 LVHEAP = 424/426/467 MALLOC = 359/359/359

----- PDB NET SUMMARY -----
pdb file name = svbdb/TOP_ALU.pdb
root cell name = TOP_ALU
total nets = 309
top-level nets = 309
non-top-level nets = 0
degenerate nets = 0
merged nets = 0
error nets = 0

----- CALIBRE xRC WARNING / ERROR Summary -----
xRC Warnings = 0
xRC Errors = 0

----- CALIBRE xRC::FORMATTER COMPLETED - Tue Apr 30 12:43:00 2024
--- TOTAL CPU TIME = 2 REAL TIME = 2 LVHEAP = 39/85/467 MALLOC = 295/295/359 ELAPSED TIME = 6
```

3 Warnings]

This Linux release is not supported for use with Calibre products.
This Linux release is not supported for use with Calibre products.
This Linux release is not supported for use with Calibre products.

Tue 12:43

PEX Netlist File - Top_alu.pex.netlist

```
* File: Top_alu.pex.netlist
* Created: Tue Apr 30 12:42:57 2024
* Program "Calibre xRC"
* Version "v2013.2_18.13"
*
*.include "Top_alu.pex.netlist.pex"
*.subckt Top_alu GND! OUT<2> OUT<1> OUT<3> OUT<0> VDD! A<2> A<1> A<0> CLK A<3>
+ RESET INST<0> INST<1>
*
* INST<1> INST<1>
* INST<0> INST<0>
* RESET RESET
* A<3> A<3>
* CLK CLK
* A<0> A<0>
* A<1> A<1>
* A<2> A<2>
* VDD VDD
* OUT<0> OUT<0>
* OUT<3> OUT<3>
* OUT<1> OUT<1>
* OUT<2> OUT<2>
* VSS VSS
X00_noxref N GND! D0_noxref_pos N_VDD! D0_noxref_neg DIODENWX AREA=1.5797e-10
+ PERIM=0.000125916
X01_noxref N GND! D0_noxref_pos N_VDD! D1_noxref_neg DIODENWX AREA=1.59646e-10
+ PERIM=0.000127196
X02_noxref N GND! D0_noxref_pos N_VDD! D2_noxref_neg DIODENWX AREA=1.60012e-10
+ PERIM=0.000127476
X03_noxref N GND! D0_noxref_pos N_VDD! D3_noxref_neg DIODENWX AREA=1.60274e-10
+ PERIM=0.000127676
X04_noxref N GND! D0_noxref_pos N_VDD! D4_noxref_neg DIODENWX AREA=1.5797e-10
+ PERIM=0.000125916
X05_noxref N GND! D0_noxref_pos N_VDD! D5_noxref_neg DIODENWX AREA=1.60588e-10
+ PERIM=0.000127916
XXU55/MMNO N N37_XU55/MMNO d N M7_XU55/MMNO g N GND! XU55/MMNO_s
+ N_GND! D0_noxref_pos NFET L=6.5e-08 W=6e-07 AD=1.35e-13 AS=1.062e-13
+ PD=1.65e-06 PS=1.554e-06 NRD=0.25 NRS=0.17 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0
+ PAR=1 PTWELL=0 SA=2.25e-07 SE=1.77e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0
+ PANW5=0 PANW6=5.98e-15 PANW7=1.3e-14 PANW8=1.3e-14 PANW9=7.02e-15 PANW10=0
XXU59/MMNO N N60_XU59/MMNO d N M2_XU59/MMNO g N GND! XU59/MMNO_s
+ N_GND! D0_noxref_pos NFET L=6.5e-08 W=6e-07 AD=1.35e-13 AS=1.062e-13
+ PD=1.65e-06 PS=1.554e-06 NRD=0.25 NRS=0.17 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0
+ PAR=1 PTWELL=0 SA=2.25e-07 SE=1.77e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0
+ PANW5=0 PANW6=5.98e-15 PANW7=1.3e-14 PANW8=1.3e-14 PANW9=7.02e-15 PANW10=0
XXI_4/MMNO N N21_XI_4/MMNO d N A<2> XI_4/MMNO g N_GND! XI_4/MMNO_s
+ N_GND! D0_noxref_pos NFET L=6.5e-08 W=6e-07 AD=1.35e-13 AS=1.062e-13
+ PD=1.65e-06 PS=1.554e-06 NRD=0.25 NRS=0.17 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0
+ PAR=1 PTWELL=0 SA=1.77e-07 SE=2.25e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0
+ PANW5=0 PANW6=5.98e-15 PANW7=1.3e-14 PANW8=1.3e-14 PANW9=7.02e-15 PANW10=0
XXU44/MMNO N M47_XU44/MMNO d N N48_XU44/MMNO g N_GND! XU44/MMNO_s
+ N_GND! D0_noxref_pos NFET L=6.5e-08 W=6e-07 AD=1.35e-13 AS=1.062e-13
+ PD=1.65e-06 PS=1.554e-06 NRD=0.25 NRS=0.17 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0
+ PAR=1 PTWELL=0 SA=1.77e-07 SE=2.25e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0
+ PANW5=0 PANW6=5.98e-15 PANW7=1.3e-14 PANW8=1.3e-14 PANW9=7.02e-15 PANW10=0
XXC60/MMNO N N48_XC60/MMNO d N N21_XC60/MMNO_g XC60/NET12_N_GND! D0_noxref_pos
+ NFET L=6.5e-08 W=6e-07 AD=1.98e-13 AS=7.05e-14 PD=1.86e-06 PS=8.35e-07
+ NRD=0.425 NRS=0.195833 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0
+ SA=3.3e-07 SB=4.75e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0
+ PANW6=5.98e-15 PANW7=1.3e-14 PANW8=1.3e-14 PANW9=7.02e-15 PANW10=0
XXC60/MMNO N N21_XC60/MMNO d N A<1> XC60/MMNO_g N_GND! D0_noxref_pos
+ NFET L=6.5e-08 W=6e-07 AD=7.05e-14 AS=1.05e-13 PD=8.35e-07 PS=1.55e-06
+ NRD=0.195833 NRS=0.166667 M=1 NF=1 CNR_SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0
+ SA=6.3e-07 SB=1.75e-07 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0
+ PANW6=5.98e-15 PANW7=1.3e-14 PANW8=1.3e-14 PANW9=7.02e-15 PANW10=0
XXC142/MMNO N M7_XC142/MMNO d N A<1> XC142/MMNO_g XC142/NET12
+ N_GND! D0_noxref_pos NFET L=6.5e-08 W=6e-07 AD=1.98e-13 AS=7.05e-14
```

Edit Row 7 Col 22

TPL File

Hspice Terminal

NoMachine - Yash Activities Terminal ▾ Wed 13:51 engnx03a.utdallas.edu:/home/011/k/ko/kxr230001/Spring24/vlsi/fpexrun

```
File Edit View Search Terminal Help

# nodes      = 11812 # elements      = 43535
# resistors = 10878 # capacitors = 32017 # inductors      = 0
# mutual_conds = 0 # vccs      = 0 # vcvss      = 0
# cccs       = 0 # ccvs      = 0 # volt_srcs      = 9
# curr_srcs = 0 # diodes     = 19 # bjts      = 0
# jfets      = 0 # mosfets    = 612 # U elements      = 0
# T elements = 0 # W elements   = 0 # B elements      = 0
# S elements = 0 # P elements    = 0 # VA device      = 0
# vector_srcs = 0 # N elements   = 0

***** Runtime Statistics (seconds) *****
analysis      time  # points  tot. iter conv.riter
op point     0.32      1        38
transient    21.83    25201    12783    3690 rev=      318
readin       2.05
errchk       0.31
setup        0.19
output       0.00

peak memory used      536.70 megabytes
total cpu time        24.70 seconds
total elapsed time    32.48 seconds
job started at        13:51:11 05/01/2024
job ended at          13:51:43 05/01/2024

>info:      ***** hspice job concluded
lic: Release hspice token(s)
lic: total license checkout elapse time:      0.12(s)

End of pVA simulation reached at time 0 on Wed May 1 13:51:44 2024      GTM/In-use: 61.0000/49.6116 MB

      pVA malloc      4.840 Mbytes      100792 times
      pVA calloc      79.544 Mbytes      547191 times
      pVA realloc     3.622 Mbytes      1826 times
      pVA valloc      0.000 Mbytes      0 times
      pVA alloca      0.000 Mbytes      0 times

      pVA TOT-MEM    88.006 Mbytes      649809 times
      pVA free        132695 times
      pVA strdup      0.000 Mbytes      0 times

pVA concluded on Wed May 1 13:51:44 2024      GTM/In-use: 61.0000/49.6116 MB
{engnx03a:~/Spring24/vlsi/fpexrun} ▾
```

Type here to search

Energy values in Hspice terminal:

```
NoMachine - Yash
Activities Terminal Mon 12:45
engnx03a.utdallas.edu:/home/011/k/kx/kxr230001/Spring24/vlsi/fpexprun

File Edit View Search Terminal Tabs Help
engnx03a.utdallas.edu:/hom... engnx03a.utdallas.edu:/hom... engnx03a.utdallas.edu:/hom... engnx03a.utdallas.edu:/hom... engnx03a.utdallas.edu:/hom... engnx03a.utdallas.edu:/hom...
+821:11      = 50.5774p 821:19      = 63.2267p 821:27      = 23.7118p
+821:31      = 53.2133p 821:35      = 57.0593p 821:51      = 23.6891p
+821:55      = 25.3963p 821:59      = 24.0102p 821:63      = 23.6877p
+821:64      = 23.6890p 821:66      = 23.6866p 821:70      = 23.6862p
+821:72      = 23.6636p 821:78      = 14.1214p 821:79      = 17.6624p
+821:85      = 23.6861p 821:111     = 25.3783p

*****
$generated from generate_tb.py

***** transient analysis tnom= 25.000 temp= 25.000 *****
iavg0=-316.9078u from= 0.          to= 9.6600n
iavg1= -2.4004u from= 0.          to= 9.6600n
iavg2= 98.3444n from= 0.          to= 9.6600n
iavg3= -2.6479u from= 0.          to= 9.6600n
iavg4= -1.3293u from= 0.          to= 9.6600n
iavg5=-613.0571n from= 0.          to= 9.6600n
iavg6= -3.4013u from= 0.          to= 9.6600n
iavg7= -46.5831n from= 0.          to= 9.6600n
iavg8= 96.3798n from= 0.          to= 9.6600n
vavg1= 967.7019m from= 0.          to= 9.6600n
vavg2= 228.5714m from= 0.          to= 9.6600n
vavg3= 396.2733m from= 0.          to= 9.6600n
vavg4= 396.2733m from= 0.          to= 9.6600n
vavg5= 453.4161m from= 0.          to= 9.6600n
vavg6= 624.8447m from= 0.          to= 9.6600n
vavg7= 514.2857m from= 0.          to= 9.6600n
vavg8= 57.1429m from= 0.          to= 9.6600n
energy0= -3.6736p
energy1= -22.4388f
energy2= 217.1444a
energy3= -10.1363f
energy4= -5.0887f
energy5= -2.6852f
energy6= -20.5305f
energy7=-231.4246a
energy8= 53.2017a
energy10=-414.9373f

***** job concluded
*****
$generated from generate_tb.py

***** job statistics summary tnom= 25.000 temp= 25.000 *****
***** Machine Information *****
CPU:
model name      : AMD EPYC 7F32 8-Core Processor
cpu MHz        : 3692.862
```

.mt0

NoMachine - Yash

Activities Text Editor ▾

Open ▾



```
$DATA1 SOURCE='HSPICE' VERSION='0-2018.09-2 linux64' PARAM_COUNT=0
.TITLE '$generated from generate_tb.py'
iavg0          iavg1          iavg2          iavg3
iavg4          iavg5          iavg6          iavg7
iavg8          vavg1          vavg2          vavg3
vavg4          vavg5          vavg6          vavg7
vavg8          energy0         energy1         energy2
energy3         energy4         energy5         energy6
energy7         energy8         energy10        temper
alter#
-3.169e-04    -2.400e-06    9.834e-08    -2.648e-06
-1.329e-06    -6.131e-07    -3.401e-06   -4.658e-08
 9.638e-08    0.9677         0.2286         0.3963
 0.3963         0.4534         0.6248         0.5143
 5.714e-02    -3.674e-12    -2.244e-14   2.171e-16
-1.014e-14    -5.089e-15    -2.685e-15   -2.053e-14
-2.314e-16    5.320e-17    -4.149e-13   25.0000
```

.sp (Setup File)

```
$Generated from generate_tb.py
$ .include "/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"
.include Top_alu.pex.netlist
.option post runlvl=5

.param Tc=0.46n $CLK period
.param Di=5p $Input delay after rising edge of clock

xi GND! OUT<3> OUT<1> OUT<0> OUT<2> VDD! INST<0> CLK A<3> A<1>
+ A<2> A<0> INST<1> RESET Top_alu

vdd VDD! GND! 1.2v

vINST<0> INST<0> GND! PWL(0ps 0v Di 0v 'Di+0*Tc+50ps' 0v 'Di+1*Tc' 0v 'Di+2*Tc+50ps' 0v 'Di+3*Tc' 0v 'Di+4*Tc+50ps' 1.2v 'Di+5*Tc' 1.2v
'Di+6*Tc' 1.2v 'Di+7*Tc+50ps' 0v 'Di+8*Tc' 0v 'Di+9*Tc+50ps' 0v 'Di+10*Tc' 0v 'Di+11*Tc' 0v 'Di+12*Tc+50ps' 0v
'Di+13*Tc' 0v 'Di+14*Tc+50ps' 0v 'Di+15*Tc' 0v 'Di+16*Tc+50ps' 1.2v 'Di+17*Tc' 1.2v 'Di+18*Tc' 1.2v)
vINST<1> INST<1> GND! PWL(0ps 0v Di 0v 'Di+0*Tc+50ps' 0v 'Di+1*Tc' 0v 'Di+2*Tc+50ps' 0v 'Di+3*Tc+50ps' 0v 'Di+4*Tc' 0v 'Di+5*Tc+50ps' 0v
'Di+6*Tc' 0v 'Di+7*Tc+50ps' 0v 'Di+8*Tc' 0v 'Di+9*Tc+50ps' 1.2v 'Di+10*Tc' 1.2v 'Di+11*Tc' 0v 'Di+12*Tc' 0v
'Di+13*Tc' 1.2v 'Di+14*Tc+50ps' 1.2v 'Di+15*Tc' 1.2v 'Di+16*Tc+50ps' 1.2v 'Di+17*Tc' 1.2v 'Di+18*Tc' 1.2v)
vA<3> A<3> GND! PWL(0ps 0v Di 0v 'Di+0*Tc+50ps' 0v 'Di+1*Tc' 0v 'Di+2*Tc+50ps' 0v 'Di+3*Tc+50ps' 0v 'Di+4*Tc' 0v 'Di+5*Tc' 0v 'Di+6*Tc+50ps' 0v
'Di+7*Tc' 0v 'Di+8*Tc+50ps' 0v 'Di+9*Tc+50ps' 0v 'Di+10*Tc' 0v 'Di+11*Tc+50ps' 0v 'Di+12*Tc' 0v
'Di+13*Tc+50ps' 0v 'Di+14*Tc' 0v 'Di+15*Tc+50ps' 1.2v 'Di+16*Tc' 1.2v 'Di+17*Tc+50ps' 1.2v 'Di+18*Tc'
1.2v)
vA<2> A<2> GND! PWL(0ps 0v Di 0v 'Di+0*Tc+50ps' 0v 'Di+1*Tc' 0v 'Di+2*Tc+50ps' 0v 'Di+3*Tc+50ps' 1.2v 'Di+4*Tc' 1.2v 'Di+5*Tc+50ps' 0v 'Di+6*Tc' 0v
'Di+7*Tc' 0v 'Di+8*Tc+50ps' 0v 'Di+9*Tc+50ps' 0v 'Di+10*Tc+50ps' 0v 'Di+11*Tc+50ps' 0v 'Di+12*Tc' 0v
'Di+13*Tc' 0v 'Di+14*Tc+50ps' 0v 'Di+15*Tc' 0v 'Di+16*Tc+50ps' 1.2v 'Di+17*Tc' 1.2v 'Di+18*Tc' 1.2v)
vA<1> A<1> GND! PWL(0ps 0v Di 0v 'Di+0*Tc+50ps' 0v 'Di+1*Tc' 0v 'Di+2*Tc+50ps' 0v 'Di+3*Tc+50ps' 0v 'Di+4*Tc' 0v 'Di+5*Tc+50ps' 1.2v
'Di+6*Tc' 1.2v 'Di+7*Tc' 0v 'Di+8*Tc+50ps' 0v 'Di+9*Tc+50ps' 0v 'Di+10*Tc+50ps' 0v 'Di+11*Tc+50ps' 0v 'Di+12*Tc+50ps' 0v
'Di+13*Tc' 0v 'Di+14*Tc+50ps' 0v 'Di+15*Tc' 0v 'Di+16*Tc+50ps' 1.2v 'Di+17*Tc' 1.2v 'Di+18*Tc' 0v)
vA<0> A<0> GND! PWL(0ps 0v Di 0v 'Di+0*Tc+50ps' 0v 'Di+1*Tc' 0v 'Di+2*Tc+50ps' 0v 'Di+3*Tc+50ps' 1.2v 'Di+4*Tc' 1.2v 'Di+5*Tc+50ps' 1.2v
'Di+6*Tc' 1.2v 'Di+7*Tc+50ps' 1.2v 'Di+8*Tc+50ps' 1.2v 'Di+9*Tc+50ps' 1.2v 'Di+10*Tc' 1.2v 'Di+11*Tc+50ps' 1.2v 'Di+12*Tc+50ps' 1.2v
'Di+13*Tc' 0v 'Di+14*Tc+50ps' 1.2v 'Di+15*Tc' 0v 'Di+16*Tc+50ps' 1.2v 'Di+17*Tc' 0v 'Di+18*Tc+50ps' 1.2v 'Di+19*Tc' 0v)
vRESET RESET GND! PWL(0ps 0v Di 0v 'Di+0*Tc+50ps' 1.2v 'Di+1*Tc' 1.2v 'Di+2*Tc+50ps' 0v 'Di+3*Tc' 0v 'Di+4*Tc+50ps' 0v 'Di+5*Tc' 0v 'Di+6*Tc+50ps' 0v
'Di+7*Tc' 0v 'Di+8*Tc+50ps' 0v 'Di+9*Tc+50ps' 0v 'Di+10*Tc' 0v 'Di+11*Tc+50ps' 0v 'Di+12*Tc' 0v
'Di+13*Tc+50ps' 0v 'Di+14*Tc' 0v 'Di+15*Tc+50ps' 0v 'Di+16*Tc' 0v 'Di+17*Tc+50ps' 0v 'Di+18*Tc' 0v
'Di+19*Tc' 0v)
vCLK CLK GND! PWL(0ps 0v Di 0v 'Di+0*Tc+50ps' 0v 'Di+1*Tc' 0v 'Di+2*Tc+50ps' 1.2v 'Di+3*Tc+50ps' 0v 'Di+4*Tc' 0v 'Di+5*Tc+50ps' 1.2v
'Di+6*Tc' 1.2v 'Di+7*Tc+50ps' 0v 'Di+8*Tc+50ps' 1.2v 'Di+9*Tc+50ps' 0v 'Di+10*Tc' 1.2v 'Di+11*Tc+50ps' 0v 'Di+12*Tc' 1.2v
'Di+13*Tc' 0v 'Di+14*Tc+50ps' 0v 'Di+15*Tc' 0v 'Di+16*Tc+50ps' 0v 'Di+17*Tc' 0v 'Di+18*Tc+50ps' 0v 'Di+19*Tc' 0v)
.tr 10ps '21*Tc' $Run for number of input clock cycles plus 2
```

vRESET RESET GND! PWL(0ps 0v Di 0v 'Di+0*Tc+50ps' 1.2v 'Di+1*Tc' 1.2v 'Di+1*Tc+50ps' 0v 'Di+2*Tc' 0v 'Di+2*Tc+50ps' 0v 'Di+3*Tc' 0v 'Di+3*Tc+50ps' 0v 'Di+4*Tc' 0v 'Di+4*Tc+50ps' 0v 'Di+5*Tc' 0v 'Di+5*Tc+50ps' 0v 'Di+6*Tc' 0v 'Di+6*Tc+50ps' 0v 'Di+7*Tc' 0v 'Di+7*Tc+50ps' 0v 'Di+8*Tc' 0v 'Di+8*Tc+50ps' 0v 'Di+9*Tc' 0v 'Di+9*Tc+50ps' 0v 'Di+10*Tc' 0v 'Di+10*Tc+50ps' 0v 'Di+11*Tc' 0v 'Di+11*Tc+50ps' 0v 'Di+12*Tc' 0v 'Di+12*Tc+50ps' 0v 'Di+13*Tc' 0v 'Di+13*Tc+50ps' 0v 'Di+14*Tc' 0v 'Di+14*Tc+50ps' 0v 'Di+15*Tc' 0v 'Di+15*Tc+50ps' 0v 'Di+16*Tc' 0v 'Di+16*Tc+50ps' 0v 'Di+17*Tc' 0v 'Di+17*Tc+50ps' 0v 'Di+18*Tc' 0v 'Di+18*Tc+50ps' 0v 'Di+19*Tc' 0v)

vCLK CLK GND! PWL(0ps 0v Di 0v 'Di+0*Tc+50ps' 0v 'Di+1*Tc' 1.2v 'Di+2*Tc+50ps' 0v 'Di+3*Tc' 1.2v 'Di+4*Tc+50ps' 0v 'Di+5*Tc' 0v 'Di+5*Tc+50ps' 1.2v 'Di+6*Tc' 1.2v 'Di+6*Tc+50ps' 0v 'Di+7*Tc' 0v 'Di+7*Tc+50ps' 1.2v 'Di+8*Tc' 1.2v 'Di+8*Tc+50ps' 0v 'Di+9*Tc' 1.2v 'Di+9*Tc+50ps' 1.2v 'Di+10*Tc' 1.2v 'Di+10*Tc+50ps' 0v 'Di+11*Tc' 0v 'Di+11*Tc+50ps' 1.2v 'Di+12*Tc' 1.2v 'Di+12*Tc+50ps' 0v 'Di+13*Tc' 1.2v 'Di+13*Tc+50ps' 1.2v 'Di+14*Tc' 1.2v 'Di+14*Tc+50ps' 0v 'Di+15*Tc' 1.2v 'Di+15*Tc+50ps' 0v 'Di+16*Tc' 1.2v 'Di+16*Tc+50ps' 0v 'Di+17*Tc' 0v 'Di+17*Tc+50ps' 0v 'Di+18*Tc' 0v 'Di+18*Tc+50ps' 0v 'Di+19*Tc' 0v)

.tr 10ps '21*Tc' \$Run for number of input clock cycles plus 2

.measure tran iavg0 avg i(vdd) from=0 to=21*Tc \$average current in one clock cycle

.measure tran iavg1 avg i(vA<0>) from=0 to=21*Tc

.measure tran iavg2 avg i(vA<1>) from=0 to=21*Tc

.measure tran iavg3 avg i(vA<2>) from=0 to=21*Tc

.measure tran iavg4 avg i(vA<3>) from=0 to=21*Tc

.measure tran iavg5 avg i(vINST<1>) from=0 to=21*Tc

.measure tran iavg6 avg i(vINST<0>) from=0 to=21*Tc

.measure tran iavg7 avg i(vCLK) from=0 to=21*Tc

.measure tran iavg8 avg i(vRESET) from=0 to=21*Tc

.measure tran vavg1 avg v(A<0>) from=0 to=21*Tc

.measure tran vavg2 avg v(A<1>) from=0 to=21*Tc

.measure Atran vavg3 avg v(A<2>) from=0 to=21*Tc

.measure tran vavg4 avg v(A<3>) from=0 to=21*Tc

.measure tran vavg5 avg v(INST<0>) from=0 to=21*Tc

.measure tran vavg6 avg v(INST<1>) from=0 to=21*Tc

.measure tran vavg7 avg v(CLK) from=0 to=21*Tc

.measure tran vavg8 avg v(RESET) from=0 to=21*Tc

.measure energy0 param='1.2*iavg0*21*Tc'

.measure energy1 param='vavg1*iavg1*21*Tc'

.measure energy2 param='vavg2*iavg2*21*Tc'

.measure energy3 param='vavg3*iavg3*21*Tc'

.measure energy4 param='vavg4*iavg4*21*Tc'

.measure energy5 param='vavg5*iavg5*21*Tc'

.measure energy6 param='vavg6*iavg6*21*Tc'

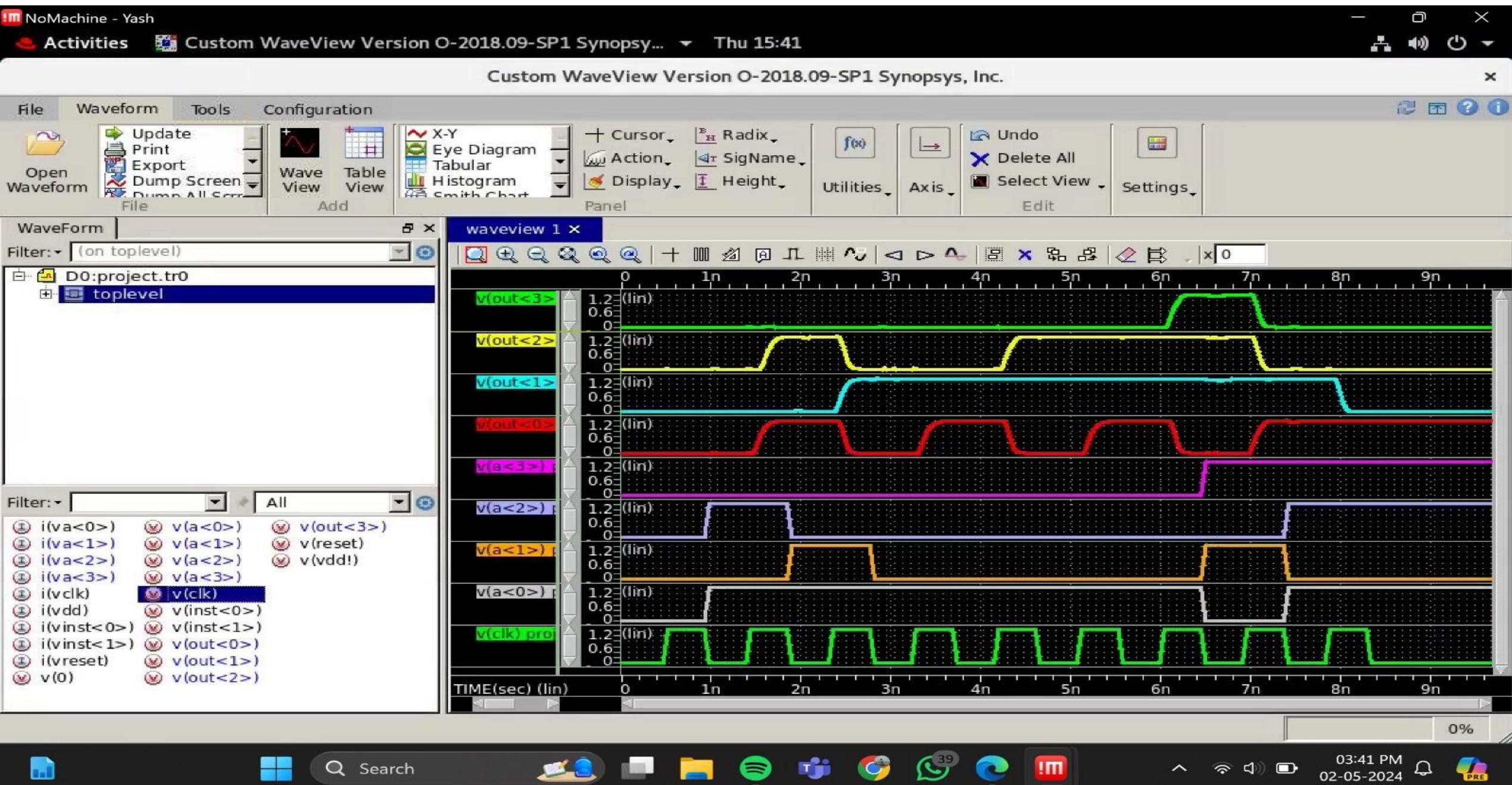
.measure energy7 param='vavg7*iavg7*21*Tc'

.measure energy8 param='vavg8*iavg8*21*Tc'

.measure energy10 param='(energy0+energy1+energy2+energy3+energy4+energy5+energy6+energy7+energy8)/9'|

.end

Output Waveform



AEDP Calculation:

- Cell Height= 56.86 μ m
- Cell Width= 66.20 μ m
- Area=Cell Height *Cell Width=56860nm*66200nm=3,764,132,000 nm².
- Energy(fJ)=(Current*Voltage*total time required for all operations including the reset operation)= -414.9373fJ
- Delay(ps)=460ps (Minimum possible clock period)
- AEDP(fJ.ps. nm²)=Area (nm²)* Energy (fJ)* Delay (ps) =3,764,132,000nm² * - 414.9373fj * 460
- **AEDP in (fj.ps. nm²)= 0.71846423fj.ps.nm²**

• ***Thank You***

