DSD LAB

Week 1

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CSE C3

Roll Number 64

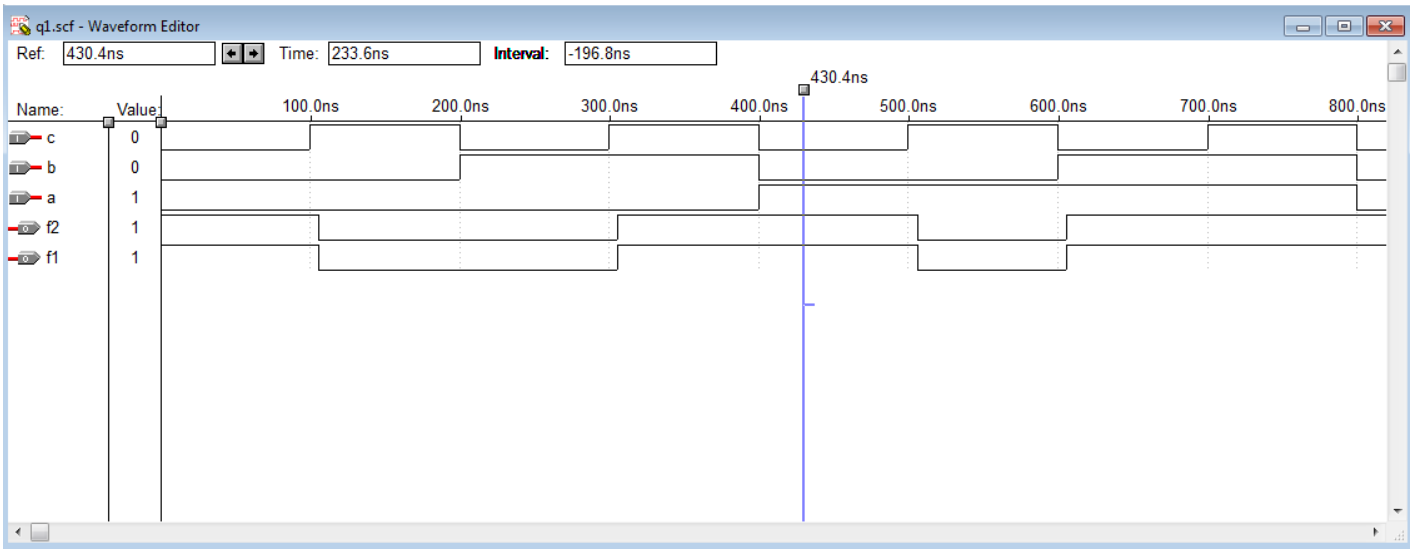
Q1.

1. Write Verilog code to describe the following functions
   f1 =ac'+bc+b'c'
   f2 = (a+b'+c)(a+b+c')(a'+b+c')
   Check whether f1 and f2 in question 1 are functionally equivalent or not.

Source Code:

```
module q1(a,b,c,f1,f2);
input a,b,c;
output f1,f2;
assign f1=(a & ~c) | (b & c) | (~b & ~c);
assign f2=(a | ~b | c) & (a| b| ~c) & (~a | b | ~c);
endmodule
```

Output Waveform:



Therefore, it is clear that f1 & f2 are functionally equivalent as their waveforms are the same.

Q2.

2. Simplify the following functions using K-map and implement the circuit using logic gates. Write Verilog code and simulate the circuit
   a) $f(A,B,C,D) = \sum m(1,3,4,9,10,12) + D(0,2,5,11)$
   b) $f(A,B,C,D) = \prod M(6,9,10,11,12) + D(2,4,7,13)$

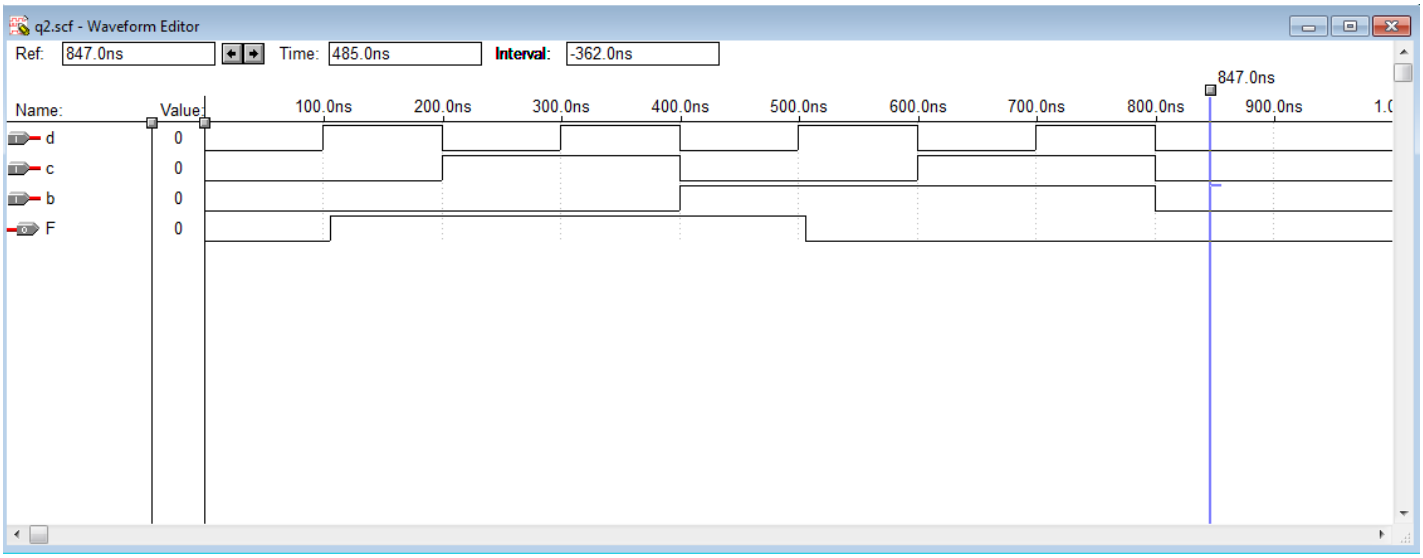
a.) The simplified expression comes as :

F=BC'D' + B'D + B'C

Source Code:

```
module q2(a,b,c,d,F);
input a,b,c,d;
output F;
assign F=(b & ~c & ~d) | (~b & d) | (~b & c);
endmodule
```

Output Waveform:



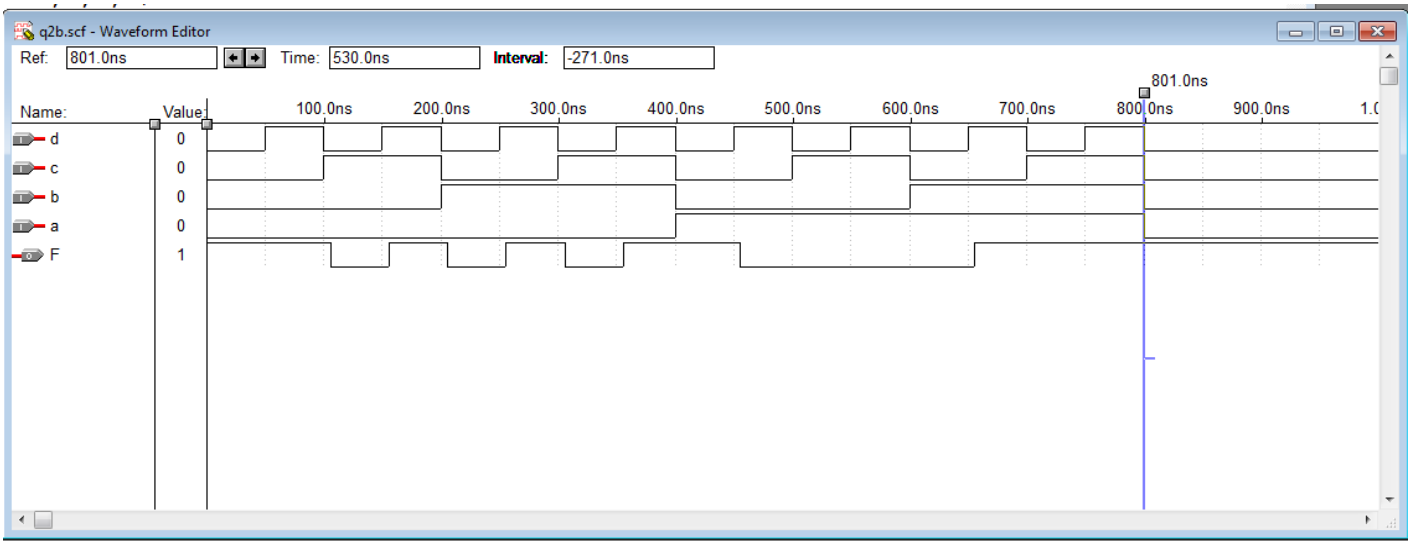
b.) The simplified expression comes as :

F=(A’ + B + D’)(A’ + B + C’)(A + C’ + D)(B’ + C + D)

Source Code:

```
module q2b(a,b,c,d,F);
input a,b,c,d;
output F;
assign F=(~a | b | ~d) & (~a | b | ~c) & (a | ~c | d) & (~b | c | d);
endmodule
```

Output Waveform:



Q3.

3. Minimize the following expression using K-map and simulate using only NAND gates.

$f(A,B,C,D)= \pi M(2,6,8,9,10,11,14)$

The expression simplifies to :

F=A'C' + A'D + BC' + BD

Source Code:

```
module q3(a,b,c,d,F);
input a,b,c,d;
output F;
assign F=~(~(~a & ~c) & ~(~a & d) & ~(b & ~c) & ~(b & d));
endmodule
```

Output Waveform: