DSD LAB

Week 4

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CSE C3

Roll Number 64

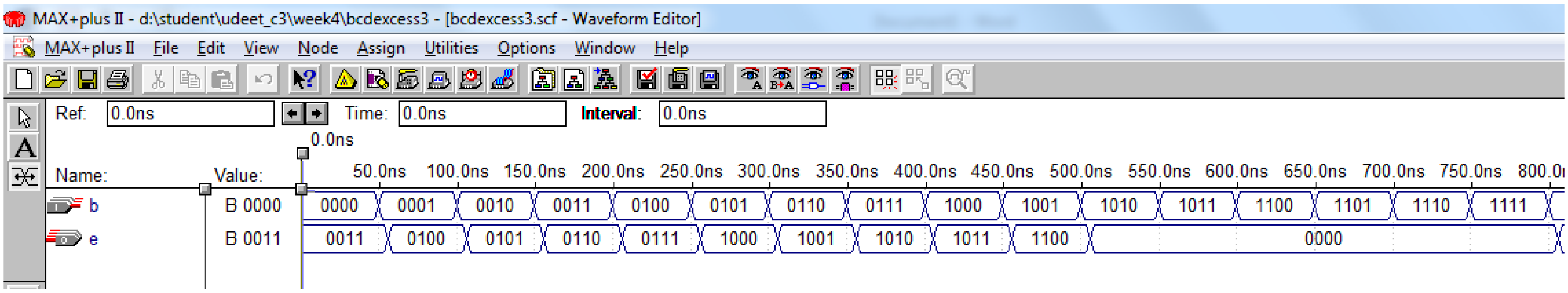
1.Write and simulate the Verilog code for a BCD to Excess 3 code converter using 8 to 1 multiplexers and other necessary gates.

Source Code:

```
module bcdexcess3(b,e);
input [3:0]b;
output [3:0]e;
wire z,one;
wire [7:0]w3,w2,w1,w0;
assign z=0;
assign one=1;
assign w3={z,z,z,one,one,b[0],z,z};
assign w2={z,z,z,b[0],z,~b[0],one,b[0]};
assign w1={z,z,z,~b[0],b[0],~b[0],b[0],~b[0]};
assign w0={z,z,z,~b[0],~b[0],~b[0],~b[0],~b[0]};
mux8to1 stage1(w0,b[3:1],e[0]);
mux8to1 stage2(w1,b[3:1],e[1]);
mux8to1 stage3(w2,b[3:1],e[2]);
mux8to1 stage4(w3,b[3:1],e[3]);
endmodule
```

```
module mux8to1(w,s,f);
input [7:0]w;
input [2:0]s;
output f;
function mux;
input [7:0]x;
input [2:0]ss;
case(ss)
0:mux=x[0];
1:mux=x[1];
2:mux=x[2];
3:mux=x[3];
4:mux=x[4];
5:mux=x[5];
6:mux=x[6];
7:mux=x[7];
endcase
endfunction
assign f=mux(w[7:0],s[2:0]);
endmodule
```

Output Waveform:



MAX+plus II - d:\student\udeet_c3\week4\bcdexcess3 - [bcdexcess3.scf - Waveform Editor]

Ref: 0.0ns Time: 0.0ns Interval: 0.0ns

Name:	Value:	
b	B 0000	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111
e	B 0011	0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 0000

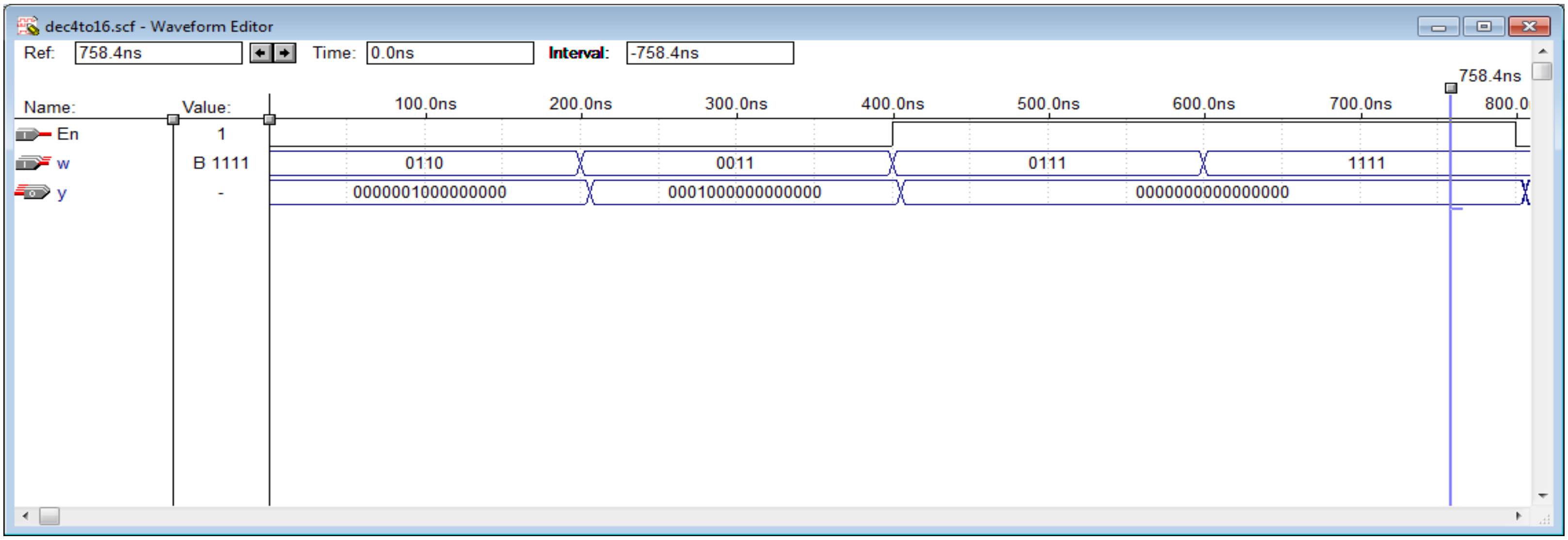
2. Write behavioral Verilog code for a 2 to 4 decoder with active low enable input and active high output using case statement. Using this, design a 4 to 16 decoder with active low enable input and active high output and write the Verilog code for the same.

Source Code:

```
module dec2to4(w,y,En);
input [1:0]w;
input En;
output [3:0]y;
reg [3:0]y;
always @(w or En)
begin
case({En,w})
3'b000:y=8;
3'b001:y=4;
3'b010:y=2;
3'b011:y=1;
default: y=0;
endcase
end
```

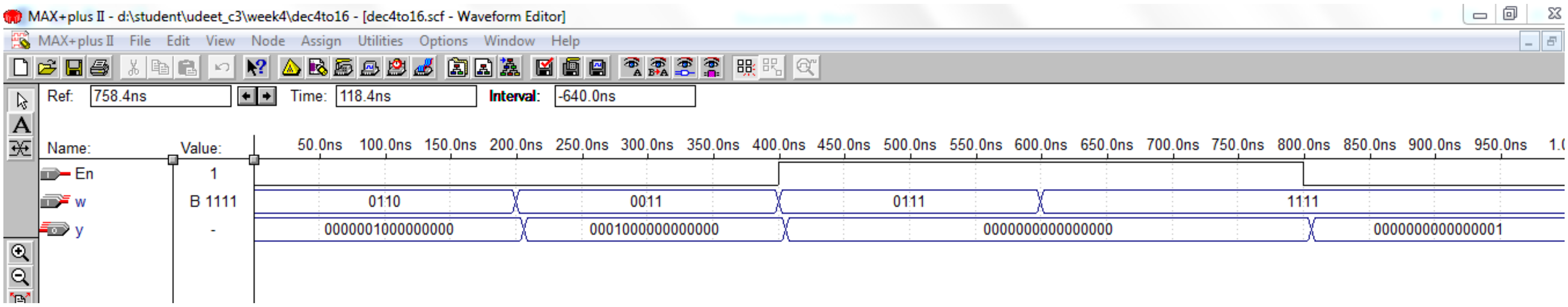
```
endmodule

module dec4to16(w,y,En);
input [3:0]w;
input En;
output [15:0]y;
wire [3:0]ey;
dec2to4 stage1(w[3:2],ey[3:0],En);
dec2to4 stage2(w[1:0],y[3:0],~ey[0]);
dec2to4 stage3(w[1:0],y[7:4],~ey[1]);
dec2to4 stage4(w[1:0],y[11:8],~ey[2]);
dec2to4 stage5(w[1:0],y[15:12],~ey[3]);
endmodule
```

Output Waveform:



dec4to16.scf - Waveform Editor

Ref: 758.4ns Time: 0.0ns Interval: -758.4ns



MAX+plus II - d:\student\udeet_c3\week4\dec4to16 - [dec4to16.scf - Waveform Editor]

Ref: 758.4ns Time: 118.4ns Interval: -640.0ns

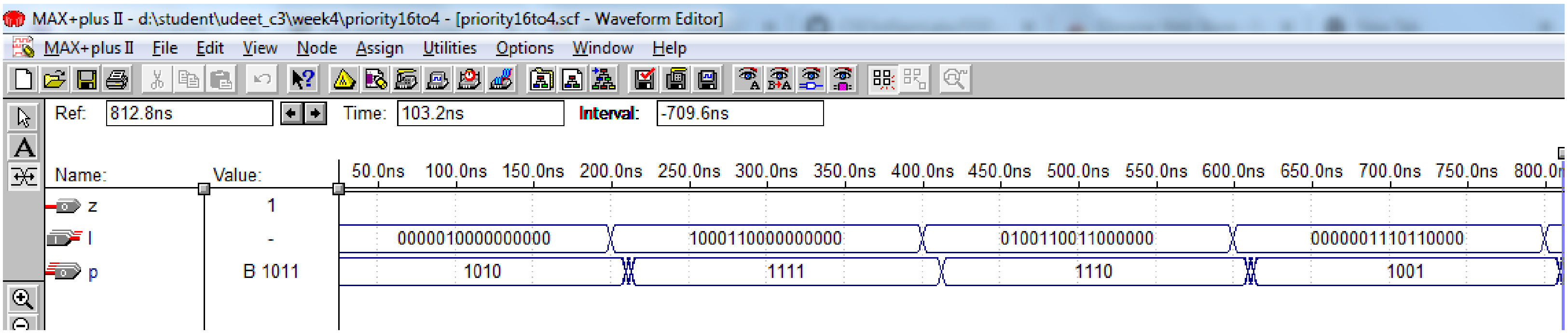
3. Write behavioral Verilog code for 16 to 4 priority encoder using for loop.

Source Code:

```
module priority16to4(l,p,z);
input [15:0]l;
output [3:0]p;
reg [3:0]p;
output z;
```

```
reg z;
integer i;
always @(l)
begin
z=0;
if(l==0)
p=0;
else
begin
for(i=0;i<16;i=i+1)
begin
if(l[i]==1)
p=i;
end
z=1;
end
end
endmodule
```

Output Waveform:


MAX+plus II - d:\student\udeet_c3\week4\priority16to4 - [priority16to4.scf - Waveform Editor]
MAX+plus II
File
Edit
View
Node
Assign
Utilities
Options
Window
Help

```
Ref: 812.8ns    Time: 103.2ns    Interval: -709.6ns

Name:   Value:   50.0ns 100.0ns 150.0ns 200.0ns 250.0ns 300.0ns 350.0ns 400.0ns 450.0ns 500.0ns 550.0ns 600.0ns 650.0ns 700.0ns 750.0ns 800.0n
z       1
l       -        0000010000000000   1000110000000000   0100110011000000   0000001110110000
p       B 1011   1010               1111               1110               1001
```