DSDL

Week 7

Udeet Mittal

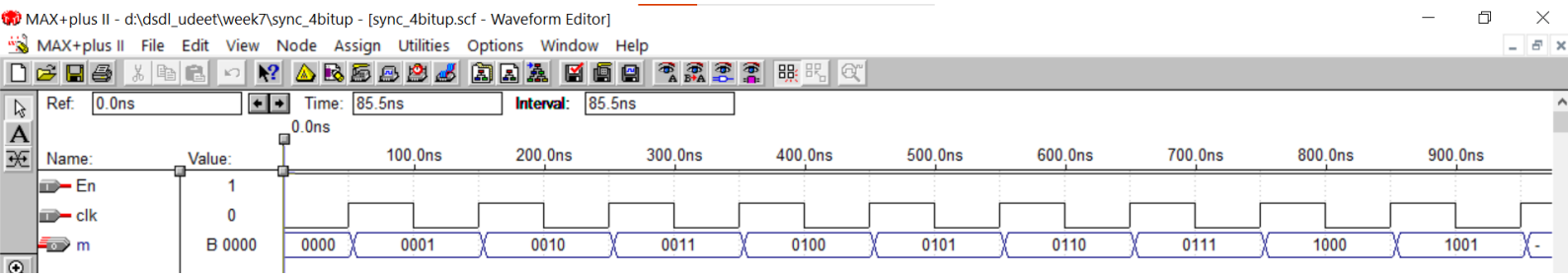
CSE C3

Roll Number 64

1.Design and simulate the following counters

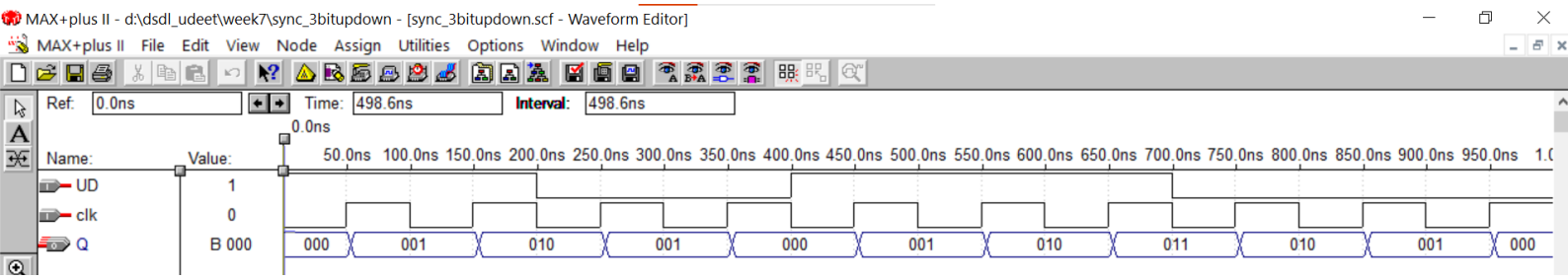
a)4 bit synchronous up counter

```
module tflipflop(T,clock,Q);
input T,clock;
output Q;
reg Q;
always @(posedge clock)
if(T)
Q<=~Q;
endmodule

module sync_4bitup(m,clk,En);
input En;
input clk;
output [3:0]m;
tflipflop stage1(En,clk,m[0]);
tflipflop stage2(En & m[0],clk,m[1]);
tflipflop stage3(En & m[1] & m[0],clk,m[2]);
tflipflop stage4(En & m[2] & m[1] & m[0],clk,m[3]);
endmodule
```



b)3 bit synchronous up/down counter with a control input up/$\overline{down}$. If up/$\overline{down}$= 1, then the circuit should behave as an up counter. If up/$\overline{down}$= 0, then the circuit should behave as a down counter.

```
module tflipflop(T,clock,Q);
input T,clock;
output Q;
reg Q;
always @(posedge clock)
if(T)
Q<=~Q;
endmodule

module sync_3bitupdown(clk,UD,Q);
input UD;
input clk;
output [2:0]Q;
wire control;
tflipflop stage1(1, clk, Q[0]);
tflipflop stage2((UD & Q[0])|(~UD & ~Q[0]), clk, Q[1]);
tflipflop stage3((UD & Q[0] & Q[1])|(~UD & ~Q[0] & ~Q[1]), clk, Q[2]);
endmodule
```


MAX+plus II - d:\dsdl_udeet\week7\sync_3bitupdown - [sync_3bitupdown.scf - Waveform Editor]
MAX+plus II File Edit View Node Assign Utilities Options Window Help
Ref: 0.0ns
Time: 498.6ns
Interval: 498.6ns
0.0ns
Name:
Value:
50.0ns 100.0ns 150.0ns 200.0ns 250.0ns 300.0ns 350.0ns 400.0ns 450.0ns 500.0ns 550.0ns 600.0ns 650.0ns 700.0ns 750.0ns 800.0ns 850.0ns 900.0ns 950.0ns
UD
1
clk
0
Q
B 000
000 001 010 001 000 001 010 011 010 001 000