

DSDL

Week 6

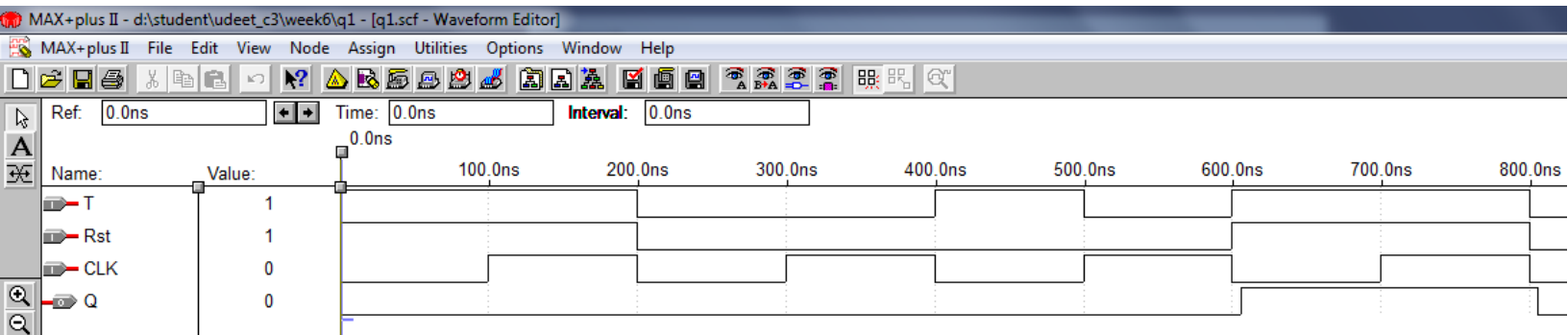
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CSE C3

Roll Number 64

1. Write behavioral Verilog code for a negative edge triggered T FF with asynchronous active low reset

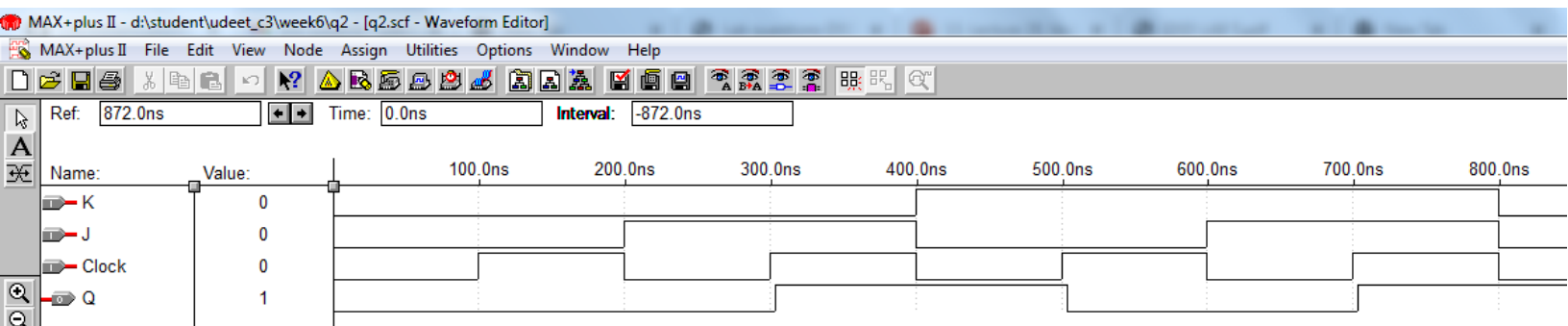
```
module q1(T, Rst, CLK, Q);  
input T, CLK, Rst;  
output Q;  
reg Q;  
always @(negedge CLK or negedge Rst)  
if(!Rst)  
Q <= 0;  
else  
if(T == 1)  
Q <= ~Q;  
else  
Q <= Q;  
endmodule
```



2. Write behavioral Verilog code for a positive edge-triggered JK FF with synchronous active high reset

```
module q2(J,K,Clock,Q);  
input J,K,Clock;  
output Q;  
reg Q;  
always @(posedge Clock)  
begin  
case ({J,K})  
0:Q<=Q;  
1:Q<=0;  
2:Q<=1;  
3:Q<=~Q;  
endcase  
end
```

endmodule



3. Design and simulate the following counters
- 4-bit ring counter.
 - 5 bit Johnson counter.

a.)

```
module q3a(clk,q);  
    input clk;  
    output[3:0]q;  
    wire [1:0]count;  
    wire en=1;  
    bitcounter2 one(clk,count[1:0]);  
    d2to4 two(en,count[1:0],q[3:0]);  
endmodule
```

```
module dff11(clk,d,q);  
    input clk,d;  
    output q;  
    reg q;  
    always@(posedge clk)
```

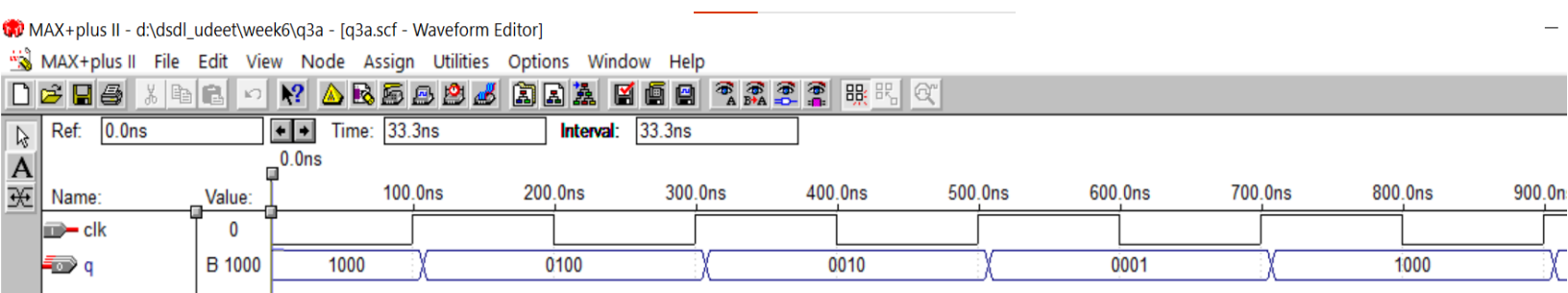
```
begin
q=d;
end
endmodule
```

```
module d2to4(en,w,y);
input en;
input [1:0]w;
output [3:0]y;
reg [3:0]y;
always@(en or w)
begin
y=0;
if(en==1)
case(w)
0:y[3]=1;
1:y[2]=1;
2:y[1]=1;
3:y[0]=1;
endcase
end
endmodule
```

```
module bitcounter2(clk,q);
input clk;
output[1:0]q;
dff11 ffo(clk,q[1]^q[0],q[1]);
```

```
dff1 ff1(clk,~q[0],q[0]);
```

```
endmodule
```



b.)

```
module q3b(clk,q);
```

```
input clk;
```

```
output [4:0]q;
```

```
dff1 ffo(clk,~q[4],q[0]);
```

```
dff1 ff1(clk,q[0],q[1]);
```

```
dff1 ff2(clk,q[1],q[2]);
```

```
dff1 ff3(clk,q[2],q[3]);
```

```
dff1 ff4(clk,q[3],q[4]);
```

```
endmodule
```

```
module dff1(clk,d,q);
```

```
input clk,d;
```

```
output q;
```

```
reg q;
```

```
always@(posedge clk)
```

```
begin
```

```
q=d;  
end  
endmodule
```

