VHDL-kode

1.1 – SigGenTop

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer: Ulrik Dan Hansen & Victor Strauss
--
-- Create Date:    13:19:32 08/03/2020
-- Design Name:
-- Module Name:    SigGenTop - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
```

```
22  ----------------------------------------------------------------------------
23  library IEEE;
24  use IEEE.STD_LOGIC_1164.ALL;
25
26  -- Uncomment the following library declaration if using
27  -- arithmetic functions with Signed or Unsigned values
28  --use IEEE.NUMERIC_STD.ALL;
29
30  -- Uncomment the following library declaration if instantiating
31  -- any Xilinx primitives in this code.
32  --library UNISIM;
33  --use UNISIM.VComponents.all;
34
35  entity SigGenTop is
36      Port ( Reset   : in std_logic;
37             Clk    : in std_logic;
38             SCK : in STD_LOGIC;
39            MOSI : in  STD_LOGIC;
40             SS : in  STD_LOGIC;
41             An     : out std_logic_vector(3 downto 0);
42             Cat    : out std_logic_vector(7 downto 0);
```

```
43          LED                         : out std_logic_vector(7 downto 0);
44          PWMOut : out std_logic);
45  end SigGenTop;
46
47  architecture Behavioral of SigGenTop is
48
49  -- Intern signals
50  signal Mclk, DispClk, SigEn: std_logic;
51  signal Disp: std_logic_vector(19 downto 0);
52  signal Ampl, Freq: std_logic_vector(7 downto 0);
53  signal Shape: std_logic_vector(1 downto 0);
54
55  begin
56  -- Sub-components
57  U0: entity WORK.DivClk
58      port map(Reset => Reset, Clk => Clk, TimeP => 4, Clk1 => Mclk);
59
60  U4: entity WORK.DivClk
61      port map(Reset => Reset, Clk => Clk, TimeP => 50e3, Clk1 => DispClk);
62
63  U1: entity WORK.SigGenControl
```

```
64      port map(Reset => Reset, SCK => SCK, Clk => MClk, MOSI => MOSI, SS => SS,
65                      Disp => Disp, Shape => Shape, Ampl => Ampl, Freq => Freq, SigEN => SigEN, LED => LED);
66
67  U2: entity WORK.SigGenDataPath generic map (PWMinc => '1')
68      port map(Reset => Reset, Clk => Mclk, Shape => Shape, Ampl => Ampl, Freq => Freq, SigEN=> SigEN, PWMOut => PWMOut);
69
70  U3: entity WORK.SevenSeg5
71      port map(Reset => Reset, Clk => DispClk, Data => Disp, An => An, Cat => Cat);
72
73  end Behavioral;
74
75  ***1.2 - U2 & U0 – ClkDiv***
76  ----------------------------------------------------------------------------------
77  -- Company:
78  -- Engineer: Ulrik Dan Hansen & Victor Strauss
79  --
80  -- Create Date:    13:29:35 08/03/2020
81  -- Design Name:
82  -- Module Name:    ClkDiv - Behavioral
83  -- Project Name:
84  -- Target Devices:
```

```
85  -- Tool versions:
86  -- Description:
87  --
88  -- Dependencies:
89  --
90  -- Revision:
91  -- Revision 0.01 - File Created
92  -- Additional Comments:
93  --
94  ----------------------------------------------------------------------------------
95
96  ----------------  Clock divider  ----------------------
97  library IEEE;
98  use IEEE.std_logic_1164.all;
99  use IEEE.STD_LOGIC_ARITH.ALL;
100 use IEEE.STD_LOGIC_UNSIGNED.ALL;
101
102 entity DivClk is
103     port ( Reset: in STD_LOGIC;     -- Global Reset (BTN1)
104            Clk: in STD_LOGIC;     -- Master Clock (50 MHz)
105            TimeP: in integer;     -- Time periode of the divided clock (50e6)
```

```
106             Clk1: out STD_LOGIC);   -- Divided clock1 (1 Hz)
107     end DivClk;
108
109     architecture DivClk_arch of DivClk is
110     --constant MaxCnt1: integer:= 14;
111     signal Cnt1: integer range 0 to 25000;  -- 24 bit counter
112     signal Clear1: STD_LOGIC;
113     signal Clk1_D: STD_LOGIC;
114
115     begin
116
117      -- T-register with enable and async.reset
118      Div1Reg: process(clk,Reset)
119      begin
120        if Reset = '1' then Clk1_D <= '0';     -- async. reset
121        elsif (clk'event and clk ='1') then
122          if Clear1= '1' then               -- enable
123            Clk1_D <= not Clk1_D;
124                                            end if;
125        end if;
126      end process Div1Reg;
```

```
127
128     Div1Dec: process(Cnt1, TimeP) -- Kombinatorisk
129     begin
130      Clear1 <= '0';
131      if Cnt1 = TimeP/2 then
132                          Clear1 <= '1';
133                         end if;
134     end process Div1Dec;
135
136     -- 24 bit up-counter with clear and async. reset
137     Div1Cnt:process(clk,Reset)
138     begin
139      if Reset = '1' then Cnt1 <= 1;       -- async. reset
140      elsif (clk'event and clk ='1') then
141                          if Clear1 = '1' then Cnt1 <= 1;   -- clear
142                                               else Cnt1 <= Cnt1 + 1; end if;
143      end if;
144     end process Div1Cnt;
145
146     Clk1 <= Clk1_D;
147
```

```
148 end DivClk_arch;
149
```

1.3 – U1 – SigSpiGenControl

```
151
152 ----------------------------------------------------------------------------
153 -- Company:
154 -- Engineer: Ulrik Dan Hansen & Victor Strauss
155 --
156 -- Create Date:    13:39:34 08/03/2020
157 -- Design Name:
158 -- Module Name:    SigGenControl - Behavioral
159 -- Project Name:
160 -- Target Devices:
161 -- Tool versions:
162 -- Description:
163 --
164 -- Dependencies:
165 --
166 -- Revision:
167 -- Revision 0.01 - File Created
168 -- Additional Comments:
```

```
169     --
170     ----------------------------------------------------------------------------
171     library IEEE;
172     use IEEE.STD_LOGIC_1164.ALL;
173     use IEEE.STD_LOGIC_ARITH.ALL;
174     use IEEE.STD_LOGIC_UNSIGNED.ALL;
175
176     entity SigGenControl is
177     Port ( Reset  : in std_logic;
178     Clk    : in std_logic;
179     SCK    : in std_logic;
180     MOSI    : in std_logic;
181     SS    : in std_logic;
182     Disp   : out std_logic_vector(19 downto 0);
183     Shape  : inout std_logic_vector(1 downto 0);
184     Ampl   : inout std_logic_vector(7 downto 0);
185     LED : out std_logic_vector(7 downto 0);
186     Freq   : inout std_logic_vector(7 downto 0);
187     SigEn  : out std_logic);
188     end SigGenControl;
189
```

```
190  architecture Behavioral of SigGenControl is
191
192  signal nextMOSI, nextA, nextF, Checksum: STD_LOGIC_VECTOR(7 downto 0);
193  signal nextS: STD_LOGIC_VECTOR(1 downto 0);
194  signal DispSel: STD_LOGIC_VECTOR(3 downto 0);
195  signal ShapeEN, AmplEN, FreqEN, RunEN, SSold, SSPuls: STD_LOGIC;
196  type StateType is (ShapeS, AmplS, FreqS, RunS, SyncS, ResetS, ChecksumS);
197  signal State, nState: StateType;
198
199  begin
200
201  -- Shift-register
202  SpiReg: process(Reset, SCK)
203
204  variable BUFFreg: STD_LOGIC_VECTOR(7 downto 0);
205
206  begin
207  if Reset = '1' then BUFFreg := X"00";
208                  elsif SCK'event and SCK = '1' then
209                  BUFFreg := BUFFreg(6 downto 0) & MOSI; -- Buffer mod venstre
210                  end if;
```

```
211     nextMOSI <= BUFFreg;
212     end process;
213
214     ShapeRegBUFF: process (Reset, Clk)
215     begin
216                     if Reset = '1' then nextS <= "00";
217                     elsif Clk'event and Clk = '1' then
218                                     if ShapeEN = '1' then
219                                     nextS <= nextMOSI(1 downto 0);
220                                     end if;
221                     end if;
222     end process;
223
224     ShapeReg: process (Reset, Clk)
225     begin
226                     if Reset = '1' then Shape <= "00";
227                     elsif Clk'event and Clk = '1' then
228                                     if RunEN = '1' then
229                                     Shape <= nextS;
230                                     end if;
231                     end if;
```

```
232     end process;
233
234     AmplRegBUFF: process (Reset, Clk)
235     begin
236                     if Reset = '1' then nextA <= X"00";
237                     elsif Clk'event and Clk = '1' then
238                                     if AmplEN = '1' then
239                                     nextA <= nextMOSI(7 downto 0);
240                                     end if;
241                     end if;
242     end process;
243
244     AmplReg: process (Reset, Clk)
245     begin
246                     if Reset = '1' then Ampl <= X"00";
247                     elsif Clk'event and Clk = '1' then
248                                     if RunEN = '1' then
249                                     Ampl <= nextA;
250                                     end if;
251                     end if;
252     end process;
```

```
253
254     FregRegBUFF: process (Reset, Clk)
255     begin
256                     if Reset = '1' then nextF <= X"00";
257                     elsif Clk'event and Clk = '1' then
258                                     if FreqEN = '1' then
259                                     nextF <= nextMOSI(7 downto 0);
260                                     end if;
261                     end if;
262     end process;
263
264     FregReg: process (Reset, Clk)
265     begin
266                     if Reset = '1' then Freq <= X"00";
267                     elsif Clk'event and Clk = '1' then
268                                     if RunEN = '1' then
269                                     Freq <= nextF;
270                                     end if;
271                     end if;
272     end process;
273
```

```
274     StateReg: process (Reset, Clk)
275     begin
276                         if Reset = '1' then State <= SyncS;
277                          elsif Clk'event and Clk = '1' then
278                                              State <= nState;
279                          end if;
280     end process;
281
282     SSReg: process(Reset, Clk)
283     begin
284                         if Reset = '1' then SSold <= '0';
285                         elsif Clk'event and Clk = '1' then
286                                              SSold <= SS;
287                         end if;
288     end process;
289
290     SSPuls <= SS and not SSold; -- Puls til tilstandsmaskinen
291
292
293     ------------ Display - multiplexer ------------------------
294
```

```
295  DispMux: Disp <= X"F1EAD" when DispSel = "0111" else -- 'rEAD' på display
296                   X"F1230" when DispSel = "0" else -- 'run' på display
297                    X"4F0" & Freq when DispSel = X"1" else -- 'f' samt HEX-tal
298                   X"4A0" & Ampl when DispSel = X"2" else -- 'A' samt HEX-tal
299                   X"450" & "000000" & Shape; -- 'S' samt samt HEX-tal
300
301  StateDec: process(SSpuls, State, Checksum, Reset, nextMOSI)
302  begin
303  ---------- Default ----------
304
305  LED <= "00000000";
306  Checksum <= X"00";
307  RunEN <= '0';
308  ShapeEN <= '0';
309  AmplEN <= '0';
310  FreqEn <= '0';
311  SigEN <= '0';
312  DispSel <= "0000";
313  nState <= SyncS;
314
315                   case state is
```

```
316
317     ---------- State Sync ----------
318
319                     when SyncS =>
320                                     LED <= "00000001";
321                                     DispSel <= "0111";
322
323                                     if SSPuls = '1' then
324                                                     if nextMOSI = "01010101" then -- 0x55
325                     nState <= ShapeS;
326                                                     else
327                                                     nState <= SyncS;
328                                     end if;
329                                     else
330                                     nState <= SyncS;
331                                     end if;
332
333     ---------- State Shape ----------
334
335                     when ShapeS =>
336                     RunEN <= '0';
```

```
337                     DispSel <= "0011";
338                     LED <= "00000011";
339
340                     if SSPuls =       '1' then
341                     ShapeEN <= '1';
342                     nState <= FreqS;
343                     else
344                     nState <= ShapeS;
345                     end if;
346
347     ------------- State Frekvens --------------
348
349
350                     when FreqS =>
351                     ShapeEN <= '0';
352                     DispSel <= "0001";
353                     LED <= "00000111";
354
355                     if SSPuls =       '1' then
356                     FreqEN <= '1';
357                     nState <= AmplS;
```

```
358                     else
359                     nState <= FreqS;
360                     end if;
361
362     ---------- State Amplitude ----------
363
364                     when AmplS =>
365                     FreqEN <= '0';
366                     DispSel <= "0010";
367                     LED <= "00001111";
368
369                     if SSPuls =       '1' then
370                     AmplEN <= '1';
371                     nState <= ResetS;
372                     else
373                     nState <= AmplS;
374                     end if;
375
376     ---------- State Reset ----------
377
378                     when ResetS =>
```

```
379                     AmplEn <='0';
380                     LED <= "00011111";
381
382                     if SSPuls =     '1' then
383                                     if nextMOSI = X"00"  then
384                                     nState <= SyncS;
385                                     elsif Checksum = X"00" then
386                                     nState <= ChecksumS;
387                                     else
388                                     nState <= ResetS;
389                                     end if;
390                                     else
391                                     nState <= ResetS;
392                                     end if;
393     ---------- State Checksum ------------
394
395                     when ChecksumS =>
396                     nState <= RunS;
397                     LED <= "00111111";
398
399     ---------- State Run ------------------
```

```
400
401             when RunS =>
402             SigEN <= '1';
403             RunEN <= '1';
404             DispSel <= "0000";
405             LED <= "01111111";
406
407             if SSPuls =     '1' then
408                             if nextMOSI = "01010101" then -- 0x55
409                             RunEN <= '0';
410                             nState <= ShapeS;
411                             else
412                             nState <= RunS;
413                             end if;
414             else
415             nState <= RunS;
416             end if;
417
418             when others =>
419             nState <= SyncS;
420
```

```
421     end case;
422     end process;
423     end Behavioral;
424
425     1.4 – U1 – SigGenDataPath
426     ----------------------------------------------------------------------------------
427     -- Company:
428     -- Engineer: Ulrik Dan Hansen & Victor Strauss
429     --
430     -- Create Date:    13:42:34 08/03/2020
431     -- Design Name:
432     -- Module Name:    SigGenDataPath - Behavioral
433     -- Project Name:
434     -- Target Devices:
435     -- Tool versions:
436     -- Description:
437     --
438     -- Dependencies:
439     --
440     -- Revision:
441     -- Revision 0.01 - File Created
```

```
442     -- Additional Comments:
443     --
444     ----------------------------------------------------------------------------------
445
446     -- SKAL IKKE ÆNDRES
447
448     library IEEE;
449     use IEEE.STD_LOGIC_1164.ALL;
450     use IEEE.STD_LOGIC_ARITH.ALL;
451     use IEEE.STD_LOGIC_UNSIGNED.ALL;
452
453     entity SigGenDatapath is
454       generic( PWMinc : std_logic := '1' ); -- HW=1, SIM=0010000
455       Port ( Reset  : in std_logic;
456              Clk    : in std_logic;
457              SigEN  : in std_logic;
458              Shape  : in std_logic_vector(1 downto 0);
459              Ampl   : in std_logic_vector(7 downto 0);
460              Freq   : in std_logic_vector(7 downto 0);
461              PWMOut : out std_logic);
462     end SigGenDatapath;
```

```
463
464     architecture Behavioral of SigGenDatapath is
465
466     signal SigCnt, nSigCnt, FreqCnt: std_logic_vector(11 downto 0);
467     signal Sig, SigSquare, SigSaw, SigSinus : std_logic_vector(7 downto 0);
468     signal SigAmpl: std_logic_vector(6 downto 0);
469     signal PWMcnt: std_logic_vector(6 downto 0) := "0000000";
470     signal PWM, PWMwrap : std_logic;
471
472     begin
473
474     FreqDec: FreqCnt <= "00" & Freq(7 downto 6) & Freq(5 downto 4) & '0' & Freq(3 downto 2) & '0' & Freq(1 downto 0);
475
476     FreqAdd: nSigCnt <= SigCnt + FreqCnt;
477
478
479     SigReg: process (Reset, Clk)
480     begin
481       if Reset = '1' then SigCnt <= X"000";
482       elsif Clk'event and Clk = '1' then
483         if PWMwrap = '1' then
```

```
484         SigCnt <= nSigCnt;
485       end if;
486     end if;
487   end process;
488
489   SinusDec : entity WORK.SinusLUT PORT MAP (clka => Clk, addra => SigCnt, douta => SigSinus);
490
491   PWMcount: process(Reset, Clk)
492   variable PWMcntvar: std_logic_vector(7 downto 0);
493   begin
494     if Reset = '1' then PWMcntvar := "00000000";
495     elsif Clk'event and Clk = '1' then
496       PWMcntvar := PWMcntvar + PWMinc;
497                                   if PWMcntvar > "10000000" then
498                                                 PWMcntvar := "00000000";
499                                   end if;
500     end if;
501     PWMcnt <= PWMcntvar(6 downto 0);
502   end process;
503
504   PWMdec: PWMwrap <= '1' when PWMcnt = "0000000" else '0';
```

```
505
506     SquareDec: SigSquare <= "00000000" when SigCnt < X"800" else "11111111";
507
508     SawDec: SigSaw <= SigCnt(11 downto 4);
509
510     SigMux: Sig <= X"FF" when Shape = "00" else
511                    SigSquare when Shape = "01" else
512                    SigSaw when Shape = "10" else
513                    SigSinus;
514
515
516     AmplDec: process(Ampl, Sig)
517     variable MulA, MulB, MulC: std_logic_vector(15 downto 0);
518     --variable MulC: std_logic_vector(6 downto 0);
519     begin
520       MulB := X"00" & Sig;
521       MulA := X"00" & Ampl;
522       MulC := X"0000";
523       for j in 0 to 15 loop
524         if MulA(j) = '1' then
525           MulC := MulC + MulB;
```

```
526         end if;
527         MulB := MulB(14 downto 0) & '0';
528       end loop;
529     --  MulC := MulC + 1;
530       SigAmpl <= MulC(15 downto 9);
531     --  SigAmpl <= "1111111";
532     end process;
533
534
535     PWMcomp: PWM <= '1' when PWMcnt <= SigAmpl else '0';
536
537     PWMon: PWMout <= PWM when SigEn = '1' else '0'; -- SigEN bliver aktiveret for at vise PWM-output
538
539     end Behavioral;
540
541     1.5 – U5 – SevenSeg5
542     ----------------------------------------------------------------------------
543     -- Company:
544     -- Engineer: Ulrik Dan Hansen & Victor Strauss
545     --
546     -- Create Date:    13:41:10 08/03/2020
```

```
547     -- Design Name:
548     -- Module Name:    SevenSeg5 - Behavioral
549     -- Project Name:
550     -- Target Devices:
551     -- Tool versions:
552     -- Description:
553     --
554     -- Dependencies:
555     --
556     -- Revision:
557     -- Revision 0.01 - File Created
558     -- Additional Comments:
559     --
560     ----------------------------------------------------------------------------
561     ----------  Driver to sevensegment display  ---------------
562     library IEEE;
563     use IEEE.STD_LOGIC_1164.ALL;
564     use IEEE.STD_LOGIC_ARITH.ALL;
565     use IEEE.STD_LOGIC_UNSIGNED.ALL;
566
567     entity SevenSeg5 is
```

```
568     Port ( Reset,Clk: in  std_logic;
569                            Data :   in  std_logic_vector (19 downto 0); -- Binary data
570            cat :    out std_logic_vector(7 downto 0);  -- Common cathodes
571            an :     out std_logic_vector(3 downto 0)); -- Common Anodes
572 end SevenSeg5;
573
574 architecture SevenSeg_arch of SevenSeg5 is
575 signal DispCount: integer range 0 to 3;
576 signal DataN: std_logic_vector (3 downto 0);
577 signal CatInt, CatData, CatSign: std_logic_vector (7 downto 0);
578 signal AnInt: std_logic_vector (3 downto 0);
579
580 begin
581
582
583                     DispCountReg: process(Reset, Clk)
584                     begin
585                      if Reset = '1' then
586                      DispCount <= 0;
587                      elsif Clk'event and Clk = '1' then
588                        if DispCount = 3
```

```
589                                 then DispCount <= 0;
590                                 else DispCount <= DispCount + 1; end if;
591         end if;
592                     end process DispCountReg;
593
594                     DispCountDec: process(DispCount, Data)
595                     begin
596                      case DispCount is
597                       when 0 =>
598                                 AnInt <= "1110";       --  Display 1 activated
599                                           DataN <= Data(3 downto 0);
600                       when 1 =>
601                                 AnInt <= "1101";       --  Display 2 activated
602                                           DataN <= Data(7 downto 4);
603                       when 2 =>
604                                 AnInt <= "1011";       --  Display 3 activated
605                                           DataN <= Data(11 downto 8);
606                       when others =>
607                                 AnInt <= "0111";       --  Display 4 activated
608                                           DataN <= Data(15 downto 12);
609         end case;
```

```
610         end process DispCountDec;
611
612        with DataN SELect      --  Activate segments acc. to Data
613         CatData <= "11000000" when "0000",   --0
614                    "11111001" when "0001",   --1
615                    "10100100" when "0010",   --2
616                    "10110000" when "0011",   --3
617                    "10011001" when "0100",   --4
618                    "10010010" when "0101",   --5
619                    "10000010" when "0110",   --6
620                    "11111000" when "0111",   --7
621                    "10000000" when "1000",   --8
622                    "10011000" when "1001",   --9
623                    "10001000" when "1010",   --A
624                    "10000011" when "1011",   --b
625                    "11000110" when "1100",   --C
626                    "10100001" when "1101",   --d
627                    "10000110" when "1110",   --E
628                    "10001110" when "1111",   --F
629                    "11111111" when others;  --blank
630
```

```
631       with DataN SELect      --  Activate segments acc. to Data
632         CatSign <= "11111111" when "0000",   --Blank
633                    "10101111" when "0001",   -- "r"
634                    "11100011" when "0010",   --"u"
635                    "10101011" when "0011",   --"n"
636                    "10011001" when "0100",   --4
637                    "10010010" when "0101",   --5
638                    "10000010" when "0110",   --6
639                    "11111000" when "0111",   --7
640                    "10000000" when "1000",   --8
641                    "10011000" when "1001",   --9
642                    "10001000" when "1010",   --A
643                    "10000011" when "1011",   --b
644                    "11000110" when "1100",   --C
645                    "10100001" when "1101",   --d
646                    "10000110" when "1110",   --E
647                    "10001110" when "1111",   --F
648                    "11111111" when others;  --blank
649
650     CatInt <= CatData when Data(DispCount+16) = '0' else CatSign;
651
```

```
652                     process(Reset, Clk)
653                     begin
654                       if Reset = '1' then Cat <= "00000000"; An <= "0000";
655                       elsif Clk'event and Clk = '1' then
656                         Cat <= CatInt;
657                         An <= AnInt;
658         end if;
659                     end process;
660
661   end SevenSeg_arch;
662
```

663 ***1.5 UCF fil***

```
664
665   #PACE: Start of PACE I/O Pin Assignments
666   # Define 7-seg display anode
667   NET "An<0>" LOC = F12;
668   NET "An<1>" LOC = J12;
669   NET "An<2>" LOC = M13;
670   NET "An<3>" LOC = K14;
671
672   ## Define BUTTON-signals
```

```
673     #NET "BTN0" LOC = G12;
674     #NET "BTN1" LOC = C11;
675     #NET "BTN2" LOC = M4;
676     #NET "BTN3" LOC = A7;
677
678     # Define 7-seg display cathode
679     NET "Cat<0>" LOC = L14;
680     NET "Cat<1>" LOC = H12;
681     NET "Cat<2>" LOC = N14;
682     NET "Cat<3>" LOC = N11;
683     NET "Cat<4>" LOC = P12;
684     NET "Cat<5>" LOC = L13;
685     NET "Cat<6>" LOC = M12;
686     NET "Cat<7>" LOC = N13;
687
688     # CLOCK-signal
689     NET "Clk"  LOC = B8;
690
691     # Define LED-switch LED
692     NET "LED[7]" LOC = G1;
693     NET "LED[6]" LOC = P4;
```

```
694 NET "LED[5]" LOC = N4;
695 NET "LED[4]" LOC = N5;
696 NET "LED[3]" LOC = P6;
697 NET "LED[2]" LOC = P7;
698 NET "LED[1]" LOC = M11;
699 NET "LED[0]" LOC = M5;
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701 # MCU-signals
702 NET "PWMOut"  LOC = B2;
703 NET "MOSI" LOC = A3;
704 NET "SCK" LOC = J3;
705 NET "SCK" CLOCK_DEDICATED_ROUTE = FALSE;
706 NET "SS" LOC = B5;
707
708 ## Define SW-signals
709 #Net "SW[7]" LOC = N3;
710 #Net "SW[6]" LOC = E2;
711 #Net "SW[5]" LOC = F3;
712 #Net "SW[4]" LOC = G3;
713 #Net "SW[3]" LOC = B4;
714 #Net "SW[2]" LOC = K3;
```

```
#Net "SW[1]" LOC = L3;
#Net "SW[0]" LOC = P11;

#PACE: Start of PACE Area Constraints
#PACE: Start of PACE Prohibit Constraints
#PACE: End of Constraints generated by PACE
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1.6 – COE-fil – sinus-look-up-table

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