## ARM Anditeches \* information set \* manisterset. \* exception model. \* Mentory madel. \* Robers , touce & profiling. RISC : Raduce Information Set Computer. Simple Inetructions simple Addressing medly Load Store Architecture Big Endia on (more Commonly) Little Endian. Micro applite frace. \* The build and devign of 9 processor is reflered

to as missio corclutechere.

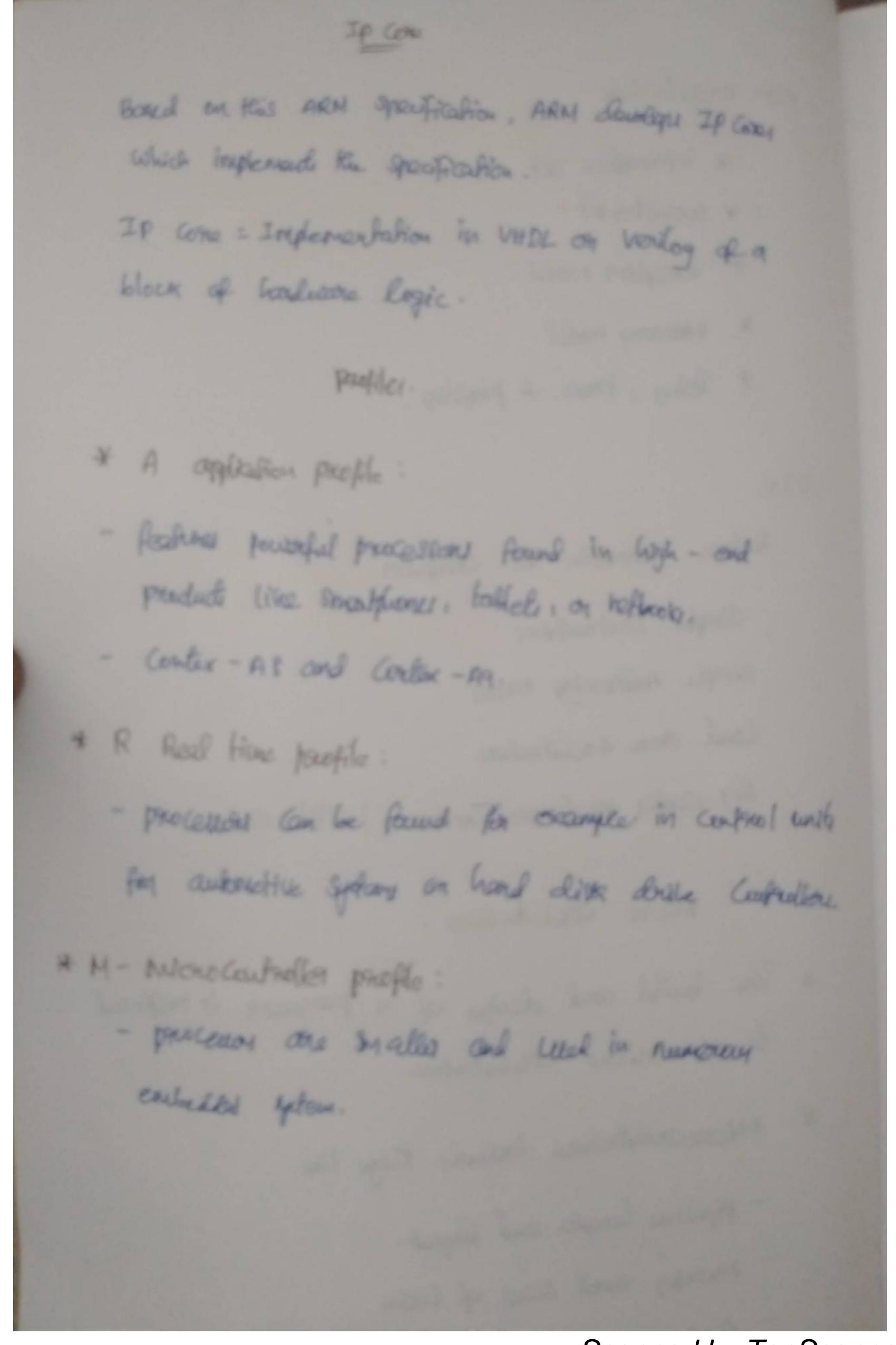
\* microcorditecture includes tringe like

- pipeline lengter and Bujant.

- Number and sizes of cades

- apple county for individual ineternation.

- Which optional features are implemented.



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