MEET UDESHI

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Indian Institute of Technology Bombay
Electrical Engineering Department
B.Tech - M.Tech Dual Degree
CGPA: 8.01/10

PUBLICATIONS

N. K. Boran, **M. Udeshi**, S. Rathore and V. Singh, "HIDC: Heterogeneous-ISA Dynamic Core Architecture" in Transactions on Embedded Computing Systems *(under review)*.

N. K. Boran, S. Rathore, **M. Udeshi** and V. Singh, "Fine-Grained Scheduling in Heterogeneous-ISA Architectures," in IEEE Computer Architecture Letters.

M. Udeshi, H. Garg, V. Baddi, P. Dwarakanath and S. Ladwa, "Low Power Object Tracking on AI100 using Kernelized Correlation Filters," as Video Paper in Qualcomm India QBuzz Conference 2021

WORK AND RESEARCH EXPERIENCE

ML Compiler Engineer — Jul'19 - Present

Qualcomm CR&D AI Software Group - AI100 Accelerator Compiler Team

- Worked on key aspects of AI100 compiler like multi-core, multi-thread data tiling, memory management, graph scheduling and operator fusion
- Innovated various **graph optimization techniques** applicable to 2D and 3D computer vision models, recommendation systems and autonomous driving tasks
- Currently developing an **automatic SIMD code generation** framework for ML operators based on dataflow analysis using **polyhedral optimization** methods
- Contributed to the open-source **Pytorch Glow** compiler framework
- Deployed power efficient object tracking pipeline using **Kernelized Correlation Filters (KCF)** algorithm on AI100

Master's Thesis - Hardware Cybersecurity — May'18 - Jun'19

Guide: Prof. Virendra Singh, CADSL, IIT Bombay

- Designed a **prefetcher disabling attack** to amplify cache side-channel leakage
- Achieved **99%** reduction in prefetches generated by **AES program**
- Implemented confidence measurement for **Gem5** stride and DCPT prefetcher
- Simulated a timing attack on the **re-order buffer** using **SNIPER** x86 simulator
- Implemented tools to reverse-engineer cache information of **Intel Skylake** cores

R&D Project - Heterogeneous-ISA Dynamic Core — May'17 - Jun'18

Guide: Prof. Virendra Singh, CADSL, IIT Bombay

- Implemented execution migration which helps HIDC switch between two ISAs
- Created a stack analysis and mapping framework for x86 and ARM using **LLVM**
- Proposed a granular function level migration strategy which reduces cost by **10x**
- Benchmarked the migration time between x86 and ARM using **Gem5** simulator

Zedroid - Android on Zedboard — Jan'18 - Apr'18

VLSI Design lab project under Prof. Sachin Patkar

- Ported and packaged Android OS for **Zynq** core
- Modified the OS init procedure for networking over **Android Debug Bridge**

Google Summer of Code — May'16 - Aug'16

Kivy: Python Native UI Framework

- Created the Tiled maps integration module for the **KivEnt** game engine
- Implemented an animation system in **Cython** using entity-component model

ACHIEVEMENTS

Awarded the **Recognition of Outstanding Contributions (ROCStar)** for work on the AI100 Accelerator ML compiler

Received a **Gold Medal** in Indian National Physics Olympiad

Scored **Advanced Performer (AP)** grade in CS101, awarded to top 3 students in a batch of 200

Secured all-India rank **275** in IIT JEE Advanced 2014 examination out of 1.3 million students

RESPONSIBILITIES

Teaching Assistant for Microprocessor course (EE309) and VLSI Design lab (EE705) from Aug'18 to Apr'19

Manager of Electronics Club, IIT Bombay from May'16 to May'17

SKILLS

Relevant Courses

Advanced Computer Architecture
VLSI Design
VLSI Testing and Verification
Electronic Design Lab
Image Processing
Neuromorphic Engineering

Programming

C/C++	★★★★★
Python	★★★★★
Cython/Pybind/SWIG	★★★★☆
VHDL	★★★☆☆

Frameworks

Pytorch Glow Compiler	★★★★★
LLVM Compiler	★★★★★
Halide	★★★★☆
Integer Set Library	★★★★☆
OpenCV	★★★☆☆

Tools

Gem5	★★★★★
SNIPER	★★★★☆
Vivado HLS	★★★☆☆
Quartus	★★★☆☆