MEET UDESHI

+91-9892713747 mudeshi1209@gmail.com
mudeshi.in udiboy1209

Research Interests: computer architecture, compilers, hardware security, accelerator design, hardware-software co-design

Indian Institute of Technology Bombay
Electrical Engineering Department
B.Tech - M.Tech Dual Degree
CGPA: 8.18/10

PUBLICATIONS

M. Udeshi, H. Garg, V. Baddi, P. Dwarakanath and S. Ladwa, "Low Power Object Tracking on AI100 using Kernelized Correlation Filters," in Qualcomm QBuzz Conference 2021 (won **Best Paper Award**)

N. K. Boran, S. Rathore, **M. Udeshi** and V. Singh, "Fine-Grained Scheduling in Heterogeneous-ISA Architectures," in IEEE Computer Architecture Letters, vol. 20, no. 1, pp. 9-12, 1 Jan.-June 2021

N. K. Boran, **M. Udeshi**, S. Rathore and V. Singh, "HIDC: Heterogeneous-ISA Dynamic Core Architecture" in Transactions on Embedded Computing Systems *(under review)*.

WORK AND RESEARCH EXPERIENCE

Senior Engineer, Qualcomm R&D Jul'19 - Present
ML Compiler Team for Cloud AI100 Accelerator

- Worked on key aspects of AI100 compiler like multi-core, multi-thread data tiling, memory management, graph scheduling and operator fusion
- Innovated various **graph optimization techniques** applicable to 2D and 3D computer vision models, recommendation systems and autonomous driving tasks
- Currently developing an **automatic SIMD code generation** framework for ML operators using dataflow analysis
- Contributed to the open-source **Pytorch Glow** compiler framework
- Deployed power efficient object tracking pipeline using **Kernelized Correlation Filters (KCF)** algorithm on AI100

Master's Thesis - Hardware Security Aug'18 - Jun'19
Guide: Prof. Virendra Singh, CADSL, IIT Bombay

- Designed a **prefetcher disabling attack** to amplify cache side-channel leakage
- Achieved **99%** reduction in prefetches generated by **AES program**
- Implemented confidence measurement for **Gem5** stride and DCPT prefetcher
- Simulated a timing attack on the **re-order buffer** using **SNIPER** x86 simulator
- Implemented tools to reverse-engineer cache information of **Intel Skylake** cores

R&D Project - Heterogeneous-ISA Dynamic Core Aug'17 - Jul'18
Guide: Prof. Virendra Singh, CADSL, IIT Bombay

- Implemented execution migration which helps HIDC switch between two ISAs
- Created a stack analysis and mapping framework for x86 and ARM using **LLVM**
- Proposed a granular function level migration strategy which reduces cost by **10x**
- Benchmarked the migration time between x86 and ARM using **Gem5** simulator

Software Development Intern Jul'17 - Aug'17
Amazon India - Transportation Financial Systems

- Implemented processing of **1 million+ receipts** using DynamoDB, SQS
- Automated server setup containing 30+ AWS resources in CloudFormation

Google Summer of Code May'16 - Aug'16
Kivy: Python Native UI Framework

- Created the Tiled maps integration module for the **KivEnt** game engine
- Implemented an animation system in **Cython** using entity-component model

ACHIEVEMENTS

Awarded the **Recognition of Outstanding Contributions (ROCStar)** for work on the AI100 compiler and KCF

Received a **Gold Medal** in Indian National Physics Olympiad

Scored **Advanced Performer (AP)** grade in CS101, awarded to top 3 students in a batch of 200

RESPONSIBILITIES

Teaching Assistant for Microprocessor course (EE309) and VLSI Design lab (EE705) from Aug'18 to Apr'19

Manager of Electronics Club, IIT Bombay from May'16 to May'17

Reviewer in the 46th International Physics Olympiad

SKILLS

Relevant Courses

Advanced Computer Architecture
VLSI CAD
VLSI Testing and Verification
Electronic Design Lab
Image Processing
Neuromorphic Engineering

Programming

C/C++	★★★★★
Python	★★★★★
Cython/Pybind/SWIG	★★★★☆
VHDL	★★★☆☆
Java	★★★☆☆

Frameworks

Pytorch Glow Compiler	★★★★★
LLVM Compiler	★★★★★
Halide	★★★★☆
Integer Set Library	★★★★☆
OpenCV	★★★☆☆

Tools

Gem5	★★★★★
SNIPER	★★★★☆
Vivado HLS	★★★☆☆
Quartus	★★★☆☆