COL 215-Digital Logic and System Design

UART Protocol Establishment for Serial Communication

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Specifications

We want to design a module on FPGA which will transmit an ASCII characters from board to PC at an agreed frequency say 9600 Baud rate.

This will happen by an agreed upon protocol between them.

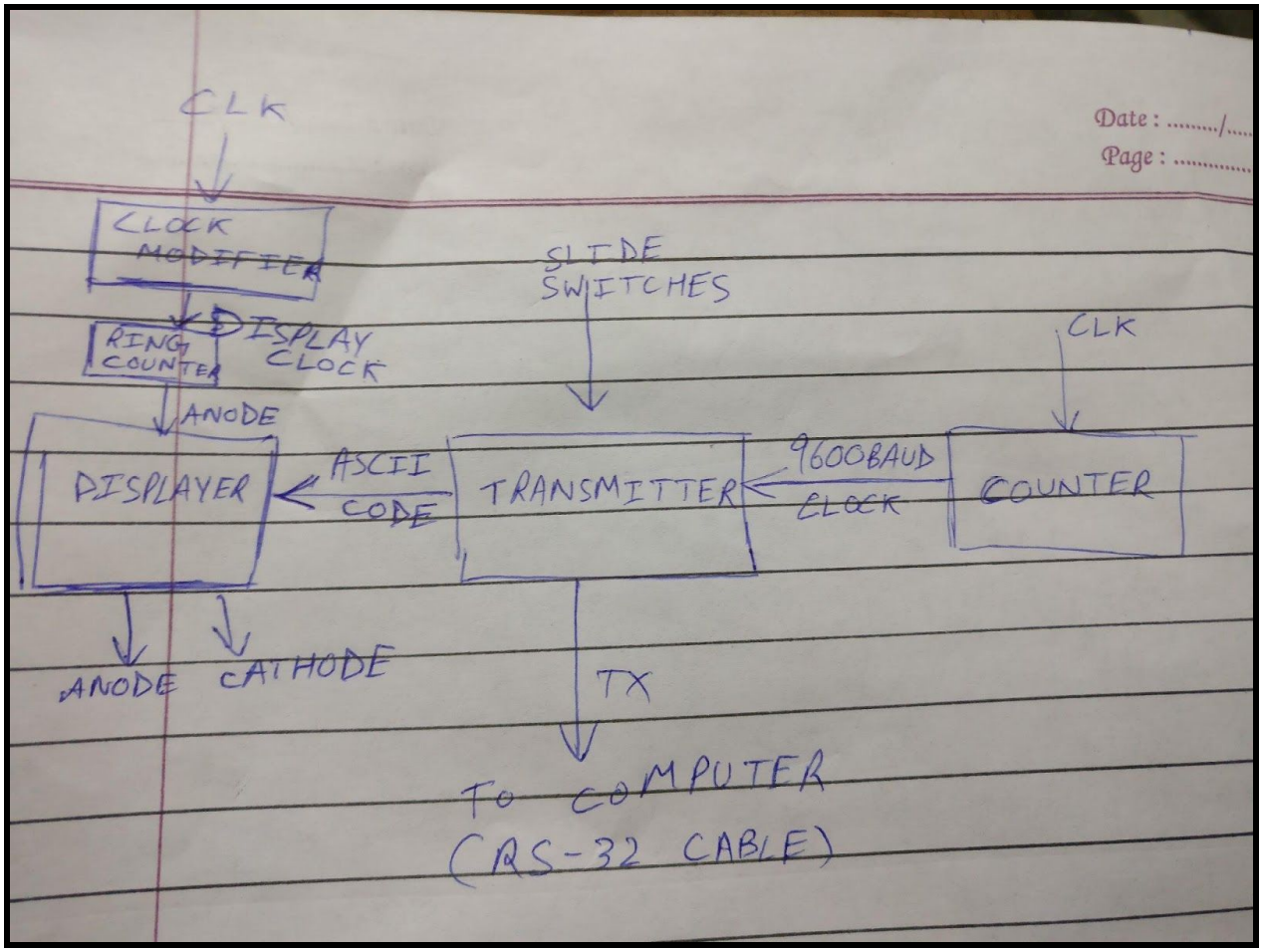
Overall Approach

To transmit an ASCII character we would need 8 bits at a time. To establish a protocol we would need some bit to know that the incoming of the character bits has started so this bit will be called a START BIT . Similarly we would need a STOP BIT to indicate an end of transmission and that Bit will be also be sent when there is no signal to be transmitted . Choices of start and stop can be 0 1 or 1 0 but , we'll go with the industry protocol standard of Start<=0 and Stop<=1 and there will be a stream of 1's when nothing is being sent, upon encountering the first 0 PC will start listening . The choice of whether to send start as 0 or 1 and to send MSB or LSB first will be dictated also by the protocol to receive programmed in the receiving end of PC.

Block Diagram

Transmitter has another counter of 10 bits which will select the bit that will be sent from the sequence (start + 8 bits + stop) and transmits the

configuration of switches to cable. The display unit will display the current value for the configuration of switches. To transmit the input,



we'll hit push button and send .

Test and Demonstration

We can do loopback testing of the wire . We will take input from the switches on FPGA , display the corresponding ASCII value on the Seven Segment Display and send the same value to PC's receiving terminal.

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