BRAC University

CSE340: Computer Architecture

Assignment 1; Total Marks:20

Please Note: Submit with a top sheet having your name, student id, section, assignment number and semester. Submission deadline is on the 6/3/24 by 5.00 pm.

1. Suppose gaming consoles PlayStation 5 and Xbox Series X use different implementations of AMD's Zen 2 architecture. The instructions they support can be divided into four classes according to their CPI (class A, B, C, and D).PlayStation has a clock rate of 2.7 GHz and the instruction classes have CPIs of 7, 2, 3, and 6 respectively whereas Xbox has a clock rate of 3.0 GHz and the instruction classes have CPIs of 5, 4, 2, and 1 respectively.

   Now suppose, a program has an instruction count of $1.0 * 10^6$, and the instructions are divided into classes as follows:

   30% class A,
   50% class B,
   10% class C, and
   10% class D.

Now answer the following questions:

   a. **Calculate** how many more clock cycles per instruction on average does the PlayStation take compared to the Xbox? **[1]**
   b. **Calculate** the difference between the execution time in these two consoles in milliseconds **[1]**
   c. If the program runs on a reference PC with an execution time of 120 milliseconds, **calculate the** SPECRatio for the PlayStation **[1]**

2. Suppose, you are a developer of a software company named 'HackerMan'. Your supervisor asked you to develop a password generator program, for MIPS architecture, that can not only generate passwords but also break them. After building the program, you observed that the program was taking 2100 seconds to execute and the password generation was taking 90% of the total run time.

After reporting to your boss fearfully, he said it was unacceptable and threatened to fire you unless you can increase the whole program's performance by a factor of 5 by optimizing the password generation.

Now, your job's future rests in your optimization skills and the results of your analysis. Let's start with the analysis.

   a. You need to improve the password generation operation by a factor of what, to meet the requirements. [1]
   b. **Compute** the new time of the program (in seconds) taken by the generation operation. **[1]**

3. What is the difference between Program Counter and $zero? In the case of 16-bit and 128-bit architecture, what would be the increment in memory address for sequential instruction execution? [2]

4. Let us consider the instruction ld x4, X(x5). Now, we have an array A and the base address of that array is 256 in decimal. If we are looking to load the contents of A [5], find the value of X in the ld instruction in the case of 256-bit architecture. [2]

5. Assume that the base address of the array *A* is in *X3*, and the values of *i* and *f* are stored in *X8* and *X9*. Then translate the following statement into RISC-V assembly code. [2]

   f = A[i];

6. Let us consider the set of instructions given below. Here, X and Y are in registers X4 and X5 respectively. The base address of the array Arr is in X7. Now, write the equivalent RISC-V code for the given set of instructions, identify the instruction type, and write the machine code for each instruction. [5]

   X = 15Y - 5;
   Arr[5] = 2X + Arr[10];

7. Calculate the branch destination address of the instruction beq X5, X6, 124 if the PC holds 0x1278A4B1. Show all the steps and write the calculated branch address in hex. [2]

8. Consider the instruction: ld X6, 64(X9). If the base address is 0x15632017. What is the memory address of the data that will be loaded to X6? [2]