

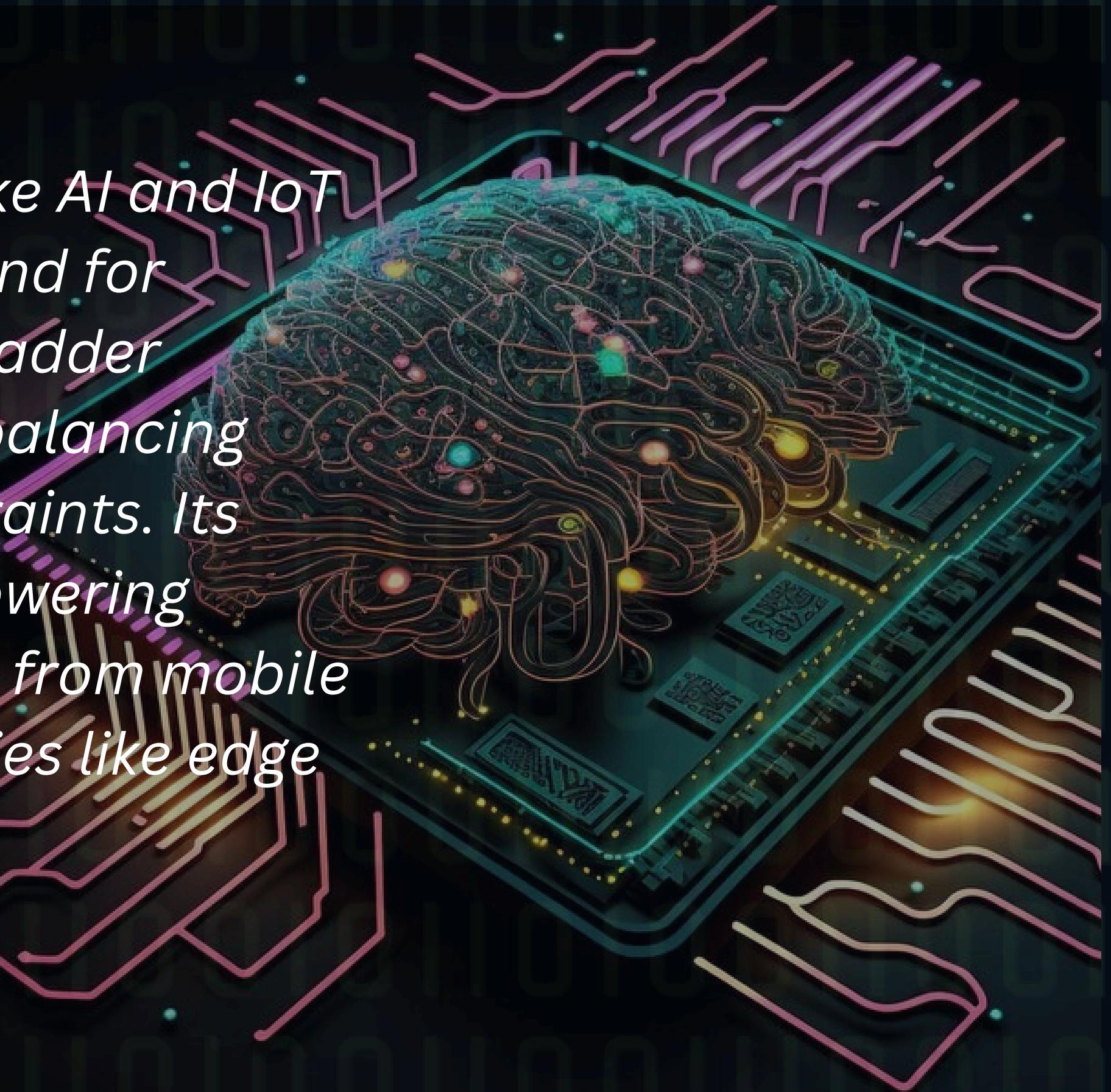
Design and Implementation of 32 bit carry skip adder .

Table of content

1. Motivation
2. Introduction
3. Working and Circuit Description
4. Result and discussion
5. Conclusion
6. References

Motivation

As data-centric applications like AI and IoT thrive, there's a pressing demand for efficient hardware. The 32-bit adder presents an optimal solution, balancing performance and space constraints. Its compact design is pivotal in powering modern computing paradigms, from mobile devices to emerging technologies like edge computing and IoT sensors.



Introduction

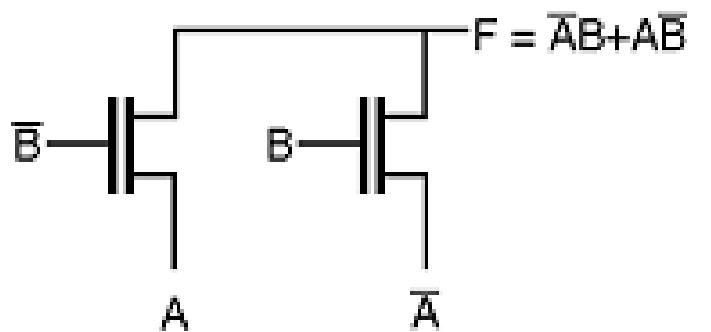
- The 32-bit full adder is a digital circuit designed to perform addition operations on binary numbers.
- Designed based on carry skip adder using transmission gate and pass transistor logic.
- CMOS implementation with 180nm technology
- It utilizes a minimalistic architecture comprising only 10 transistors per bit, effectively reducing carry propagation delay.
 - This enables faster computation speeds, making it a preferred choice for high-performance computing applications.



Working and Circuit Discription

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

Truth table of 'XOR' gate



'XOR' gate using pass transistor logic [7]

$$S = (X \oplus Y)' C_{in} + (X \oplus Y) C_{in}'$$
$$C_{out} = (X \oplus Y) C_{in} + (X \oplus Y)' X$$
$$C_{out}' = (X \oplus Y) C_{in}' + (X \oplus Y)' X'$$

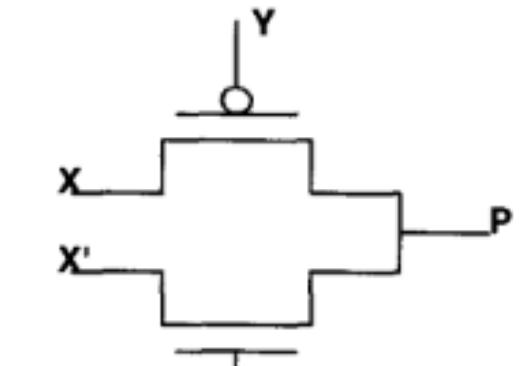


Fig. 1. The XOR circuit

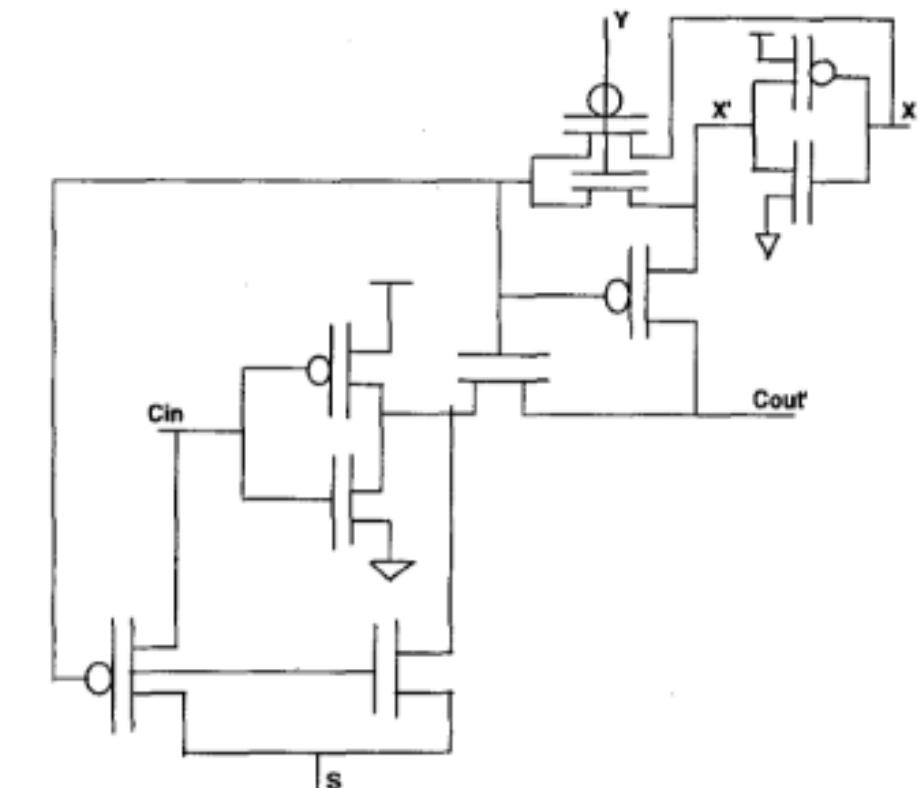
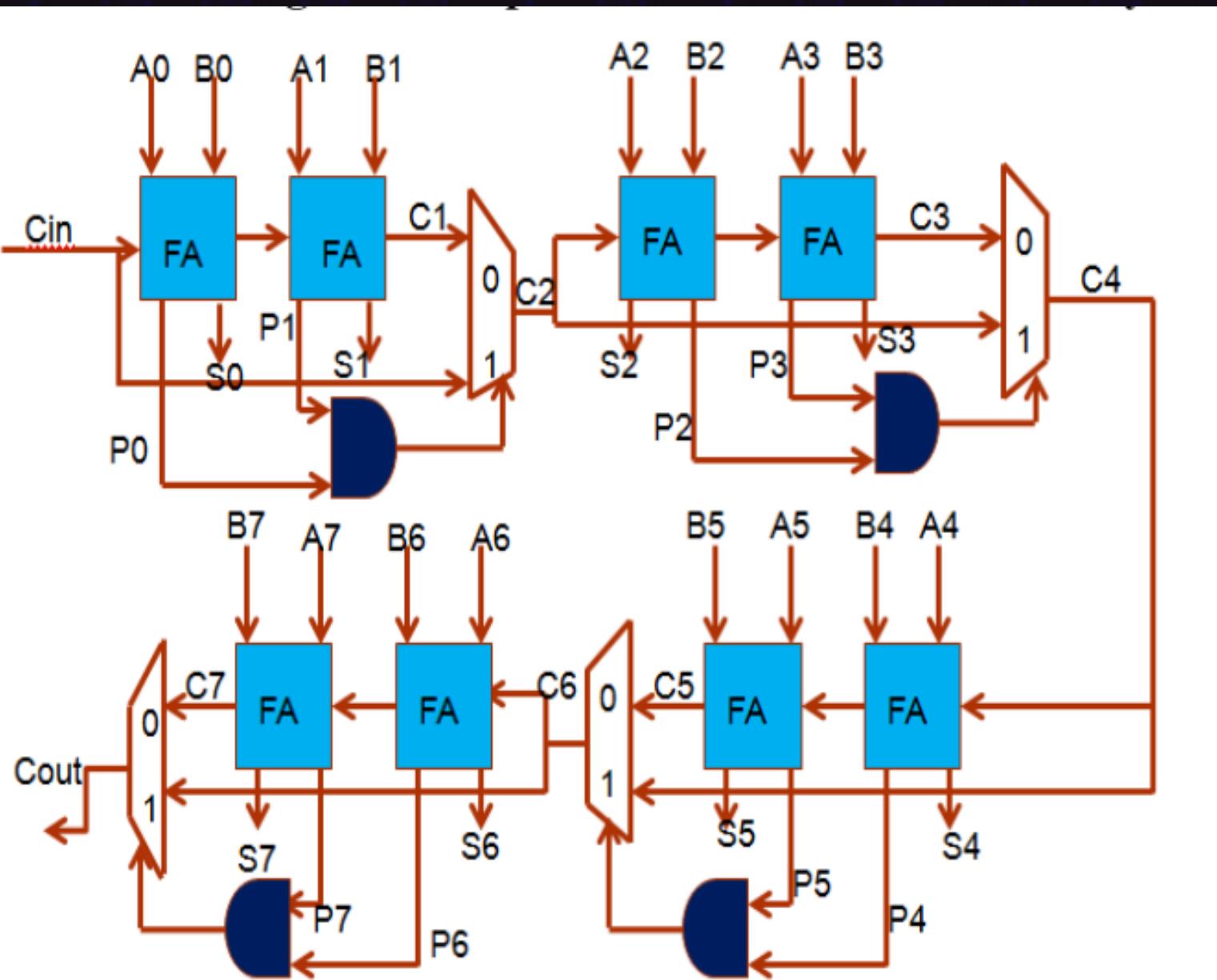


Fig. 2 The 10-transistor Full Adder Cell

[1]

[1]

Carry skip adder



[6] 8 bit carry skip adder

Carry Propagate: $P_i = A_i \oplus B_i$;
Sum: $S_i = P_i \oplus C_i$;
Carry Out: $C_{i+1} = A_i \cdot B_i + P_i \cdot C_i$

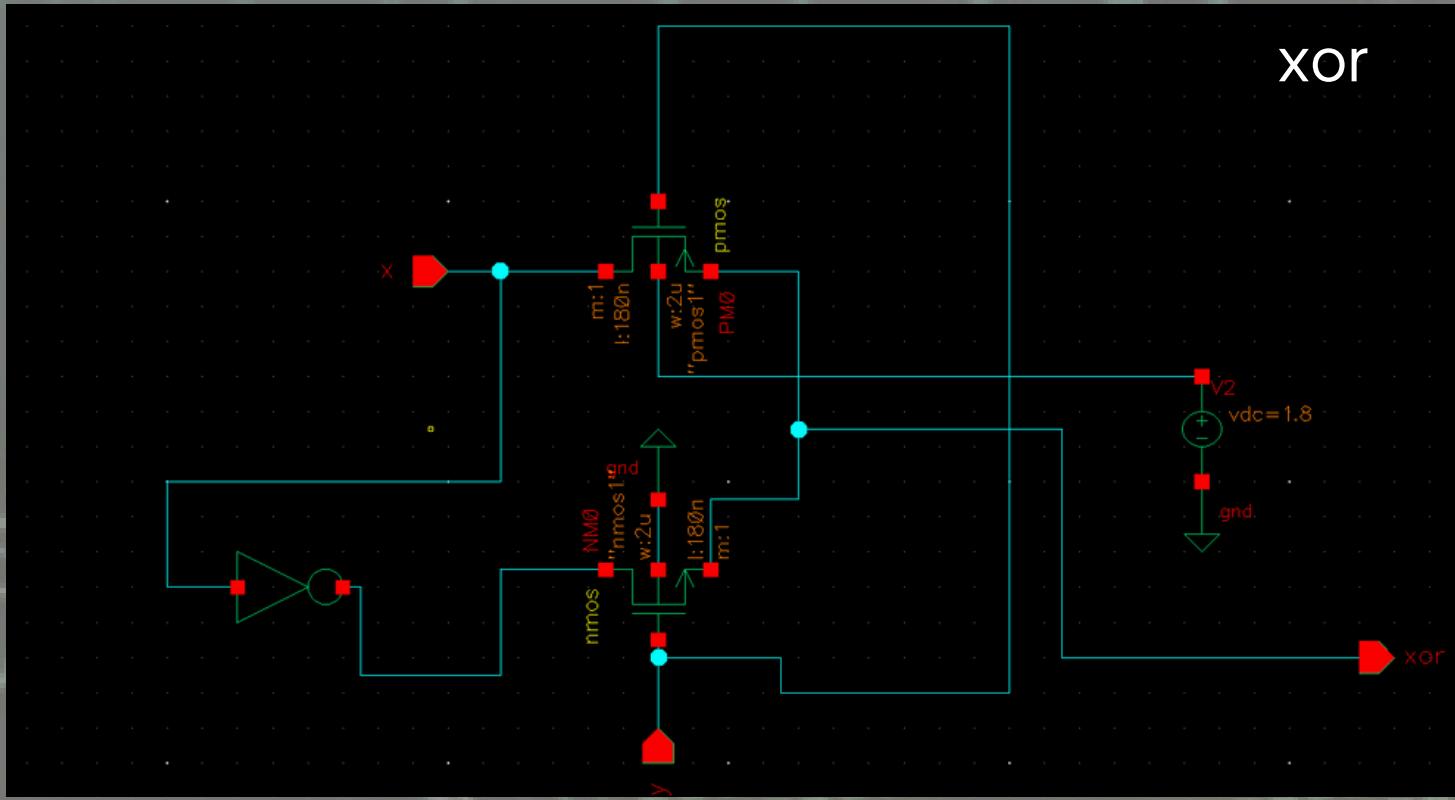
If $A_i = B_i$
then $P_i = 0$, which makes
carry out, C_{i+1} , depend only on A_i and B_i

- $C_{i+1} = A_i \cdot B_i$
- if $A_i = B_i = 0$, then $C_{i+1} = 0$
- if $A_i = B_i = 1$, then $C_{i+1} = 1$

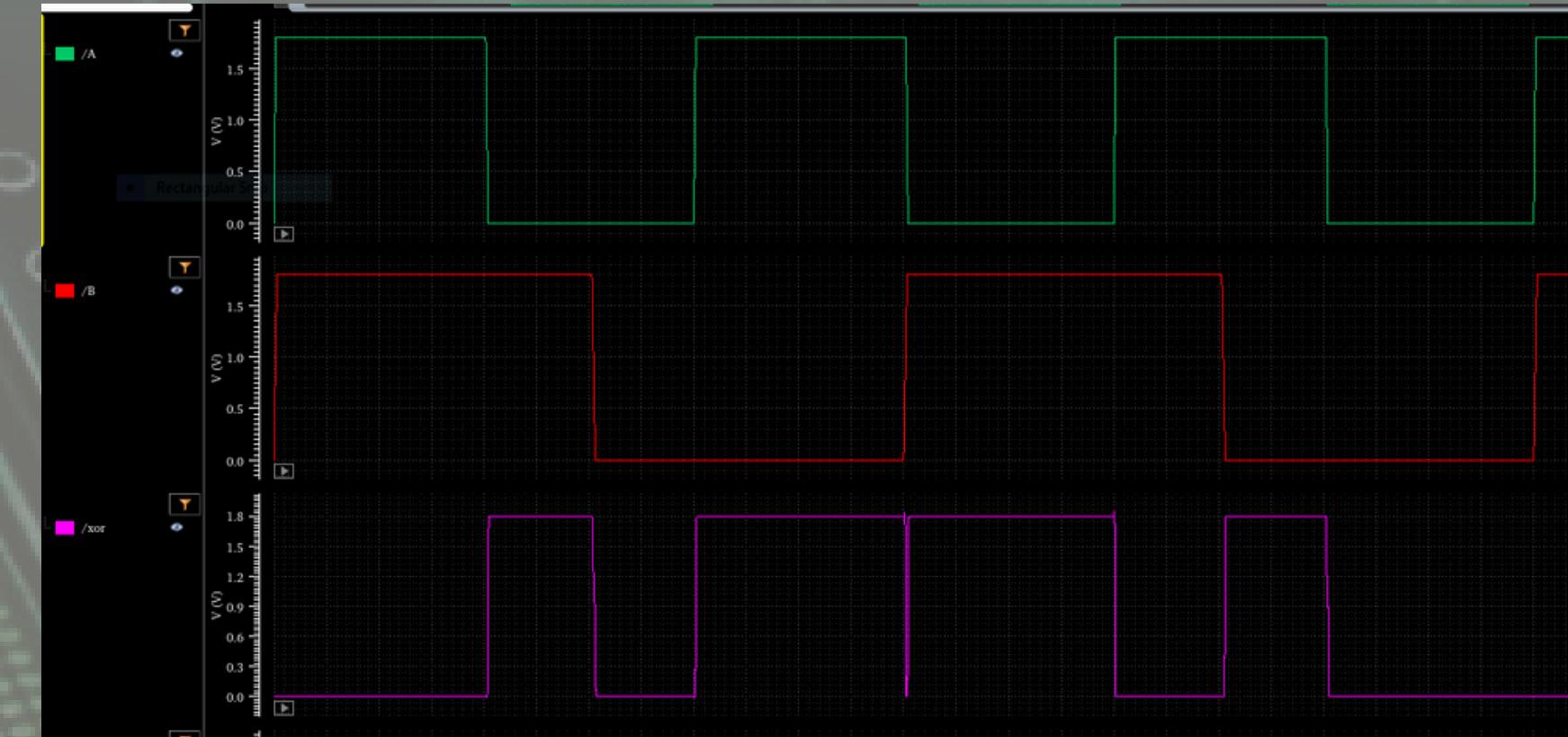
Else if A_i not equal B_i
then $P_i = 1$ and $C_{i+1} = C_i$

Results and discussion

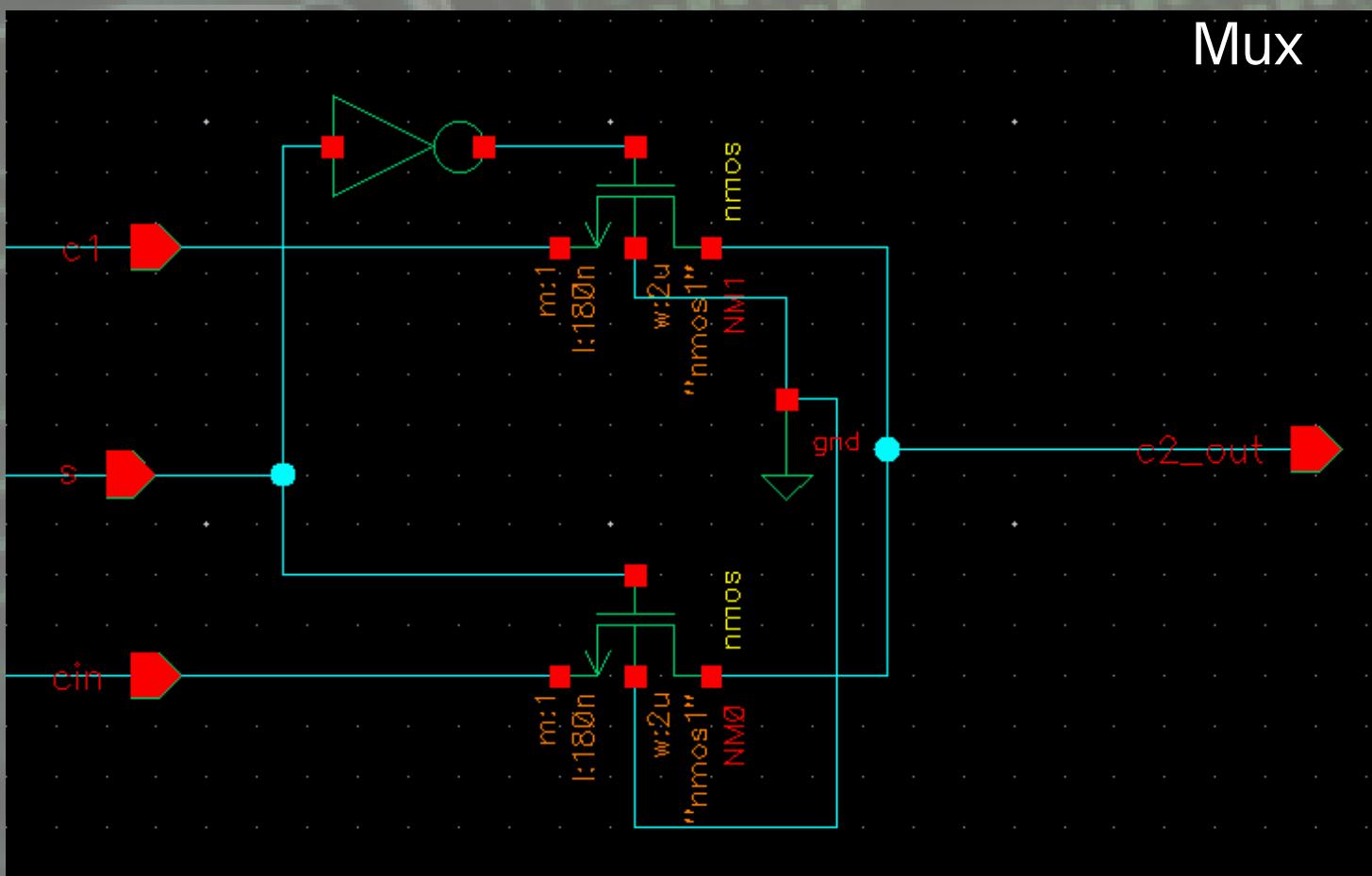
Schemactics



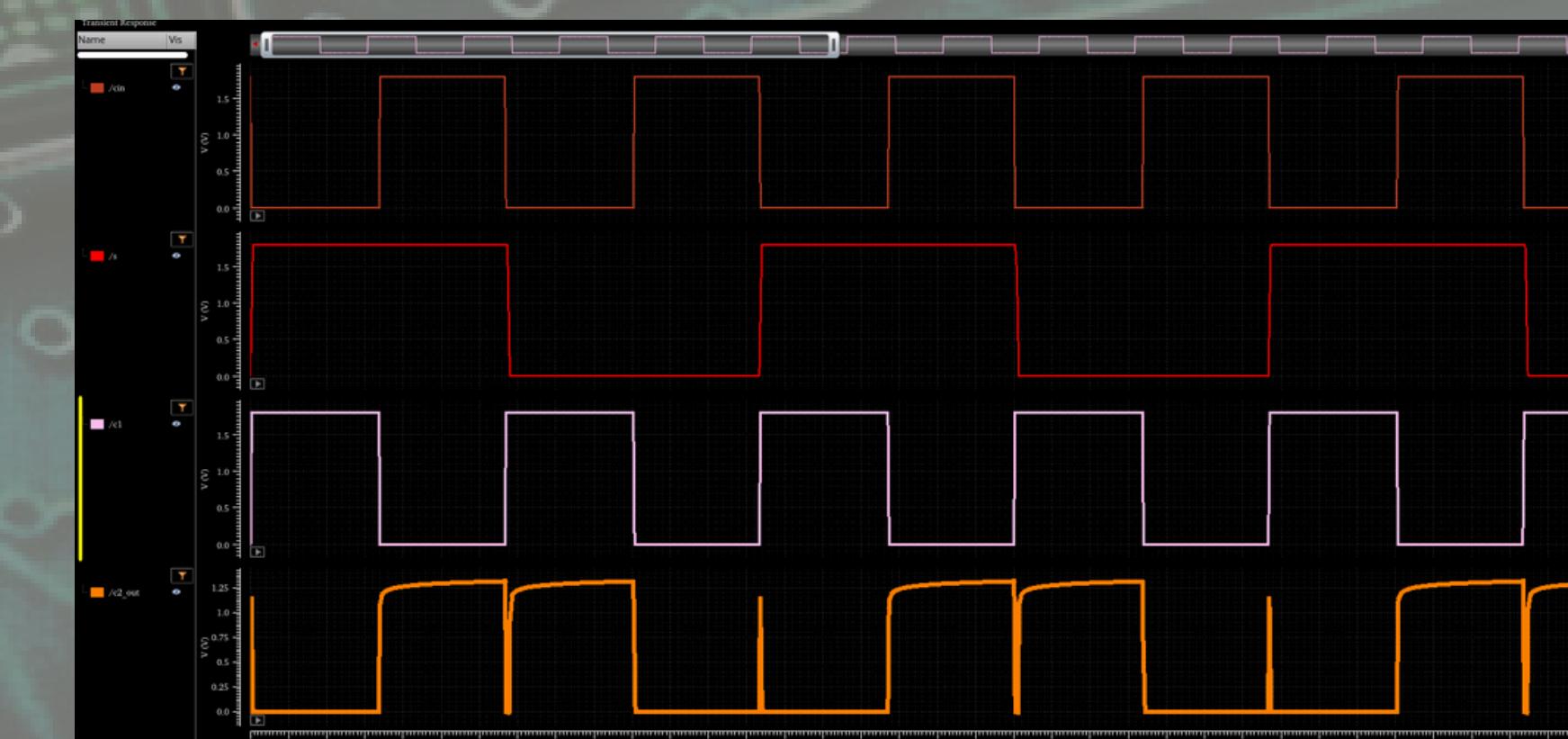
xor



Results

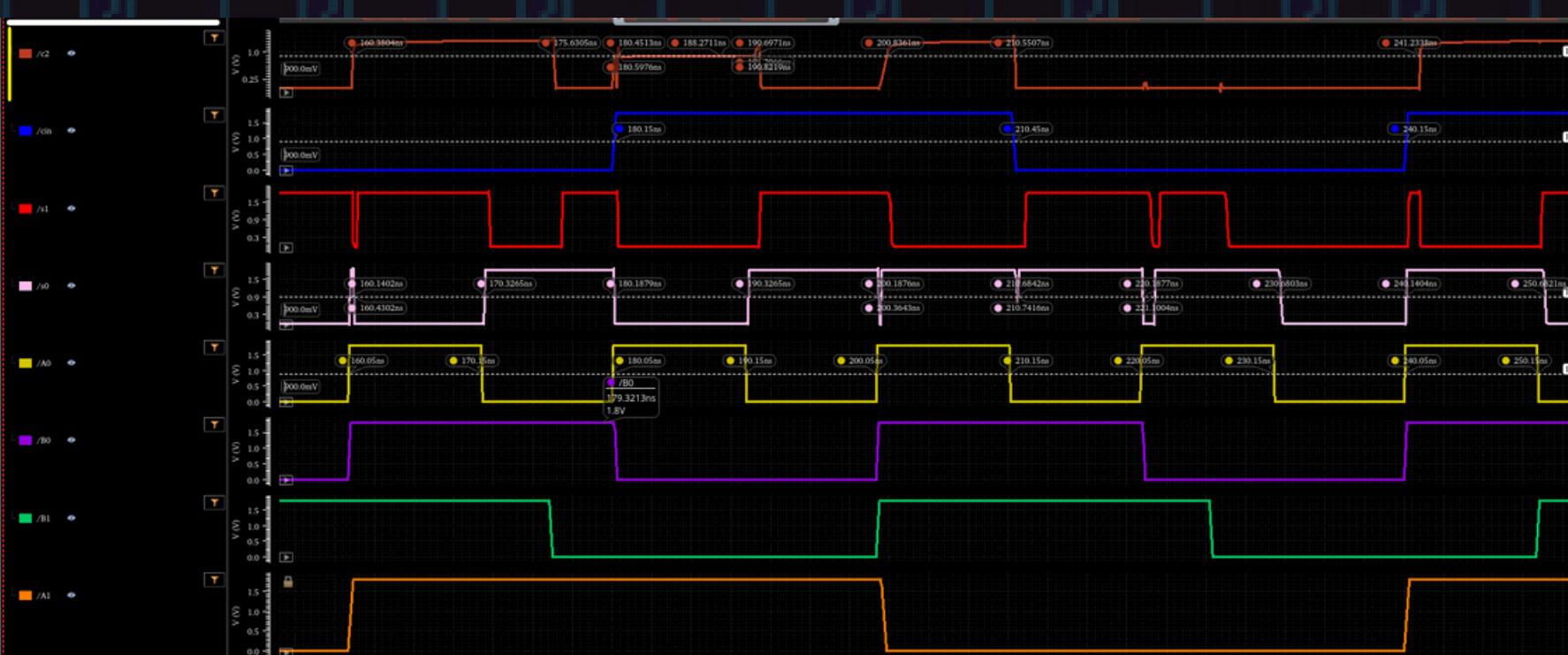
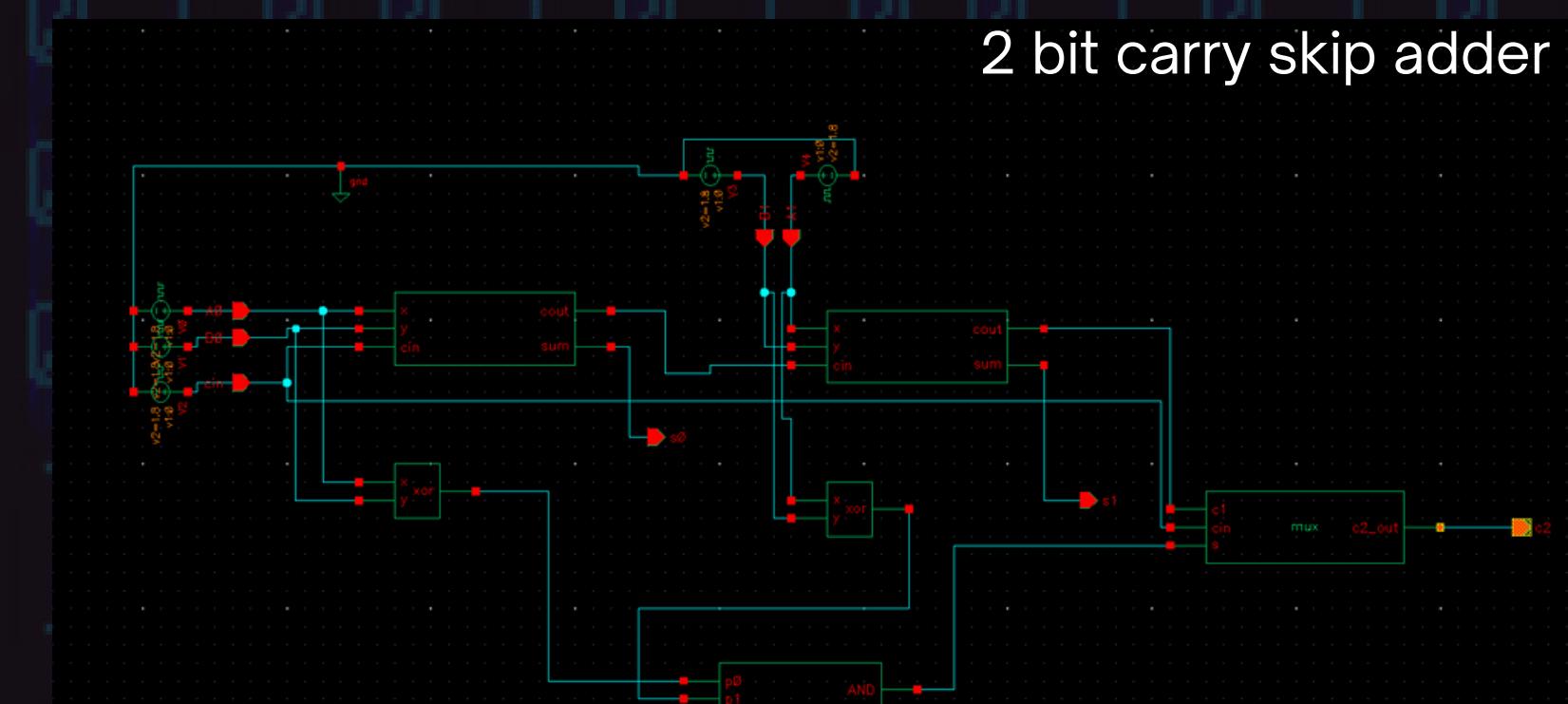
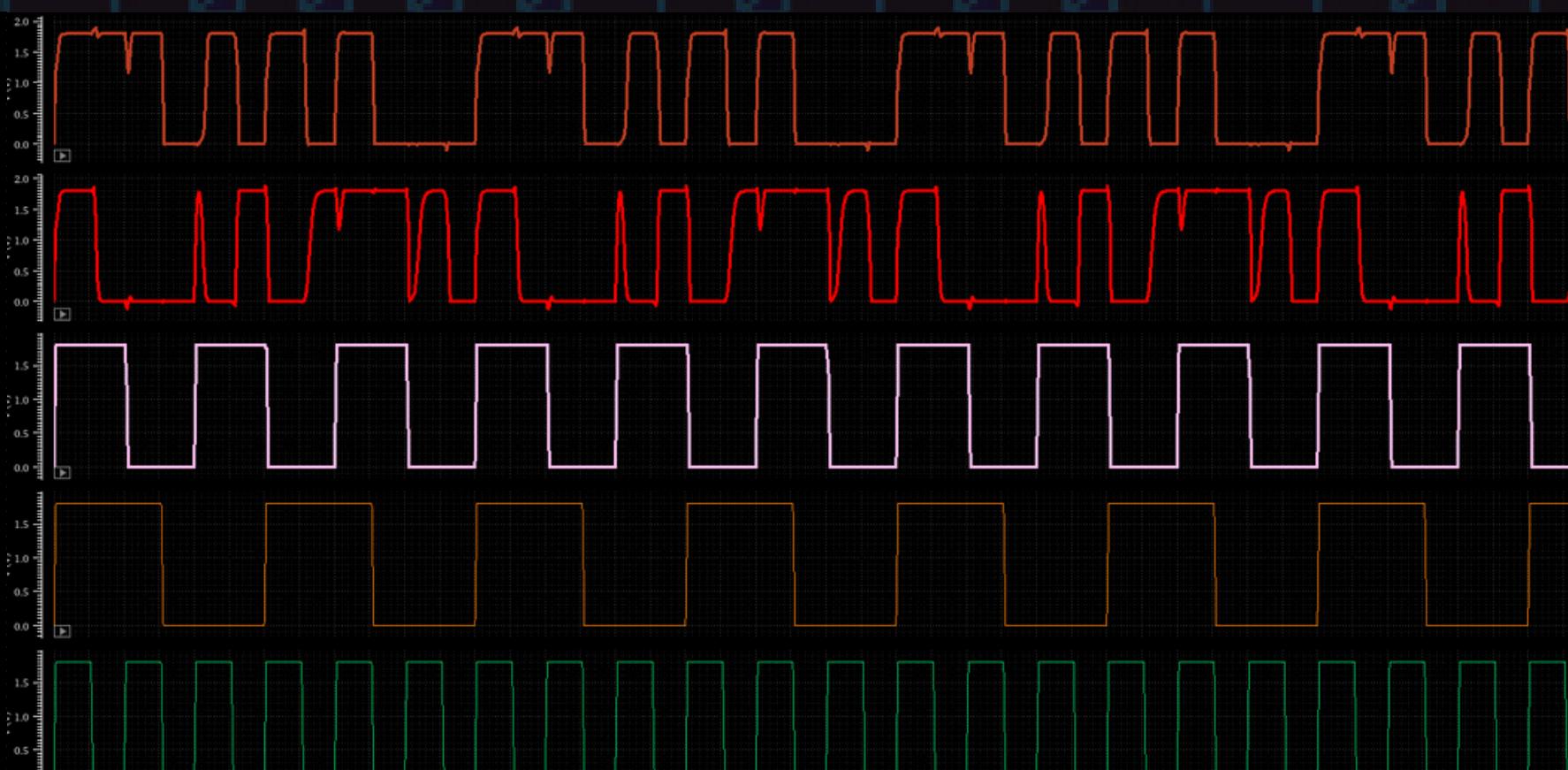
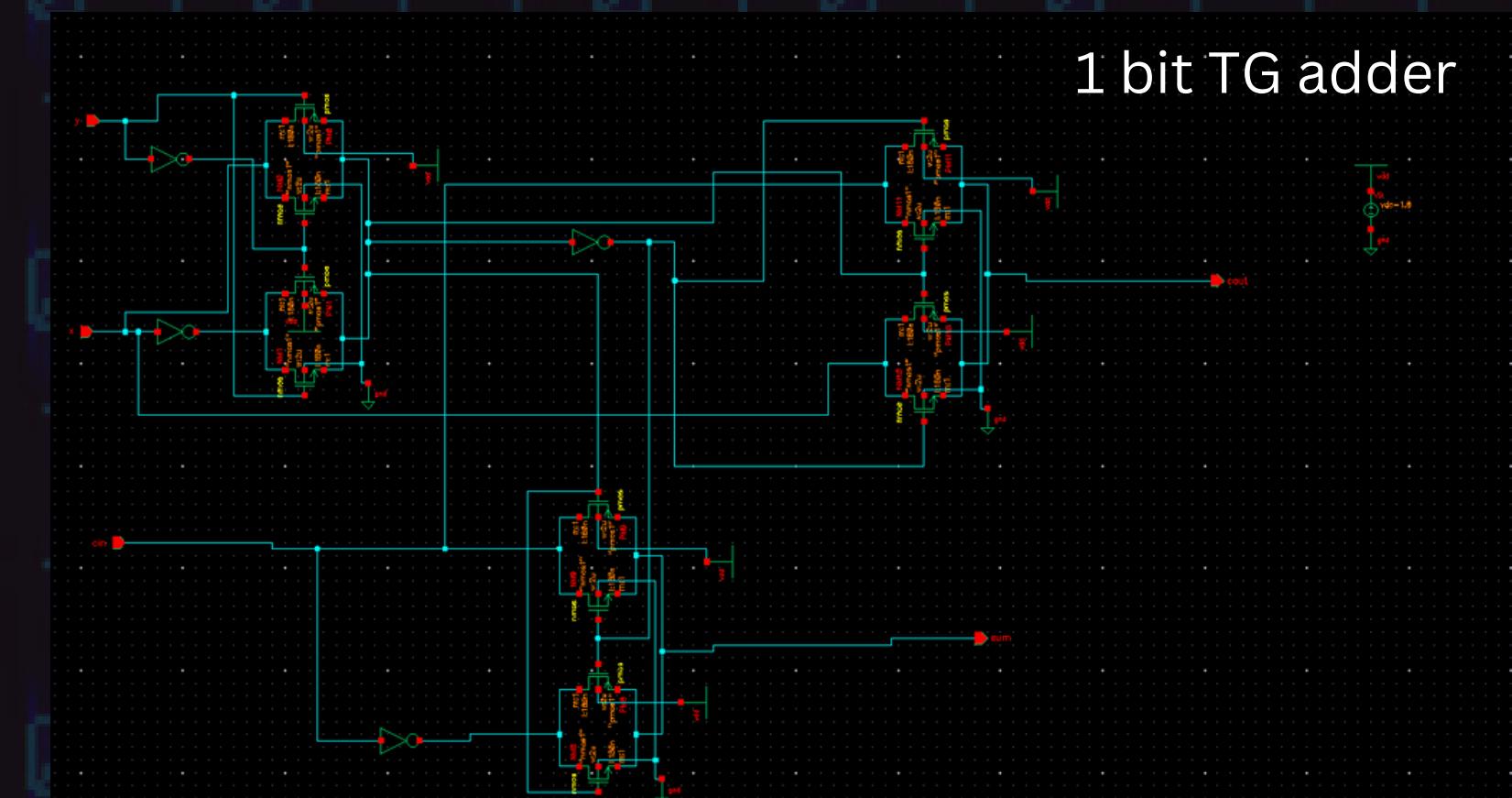


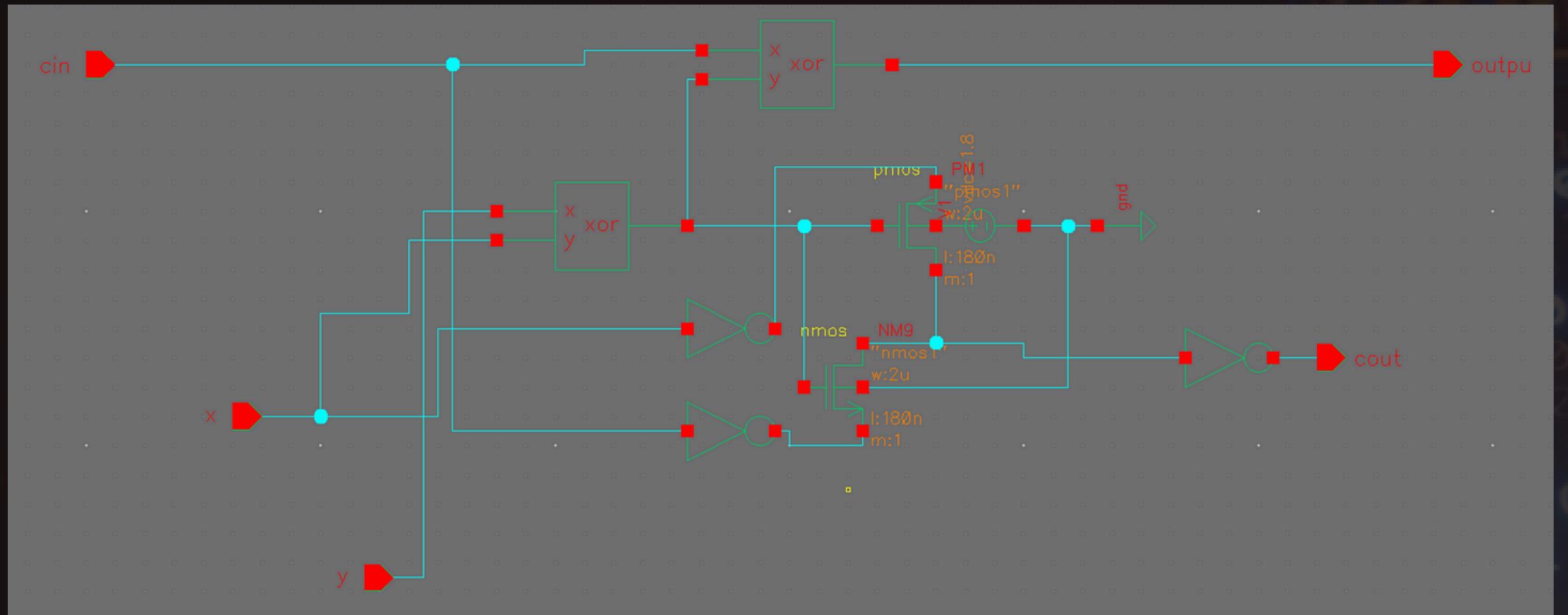
Mux



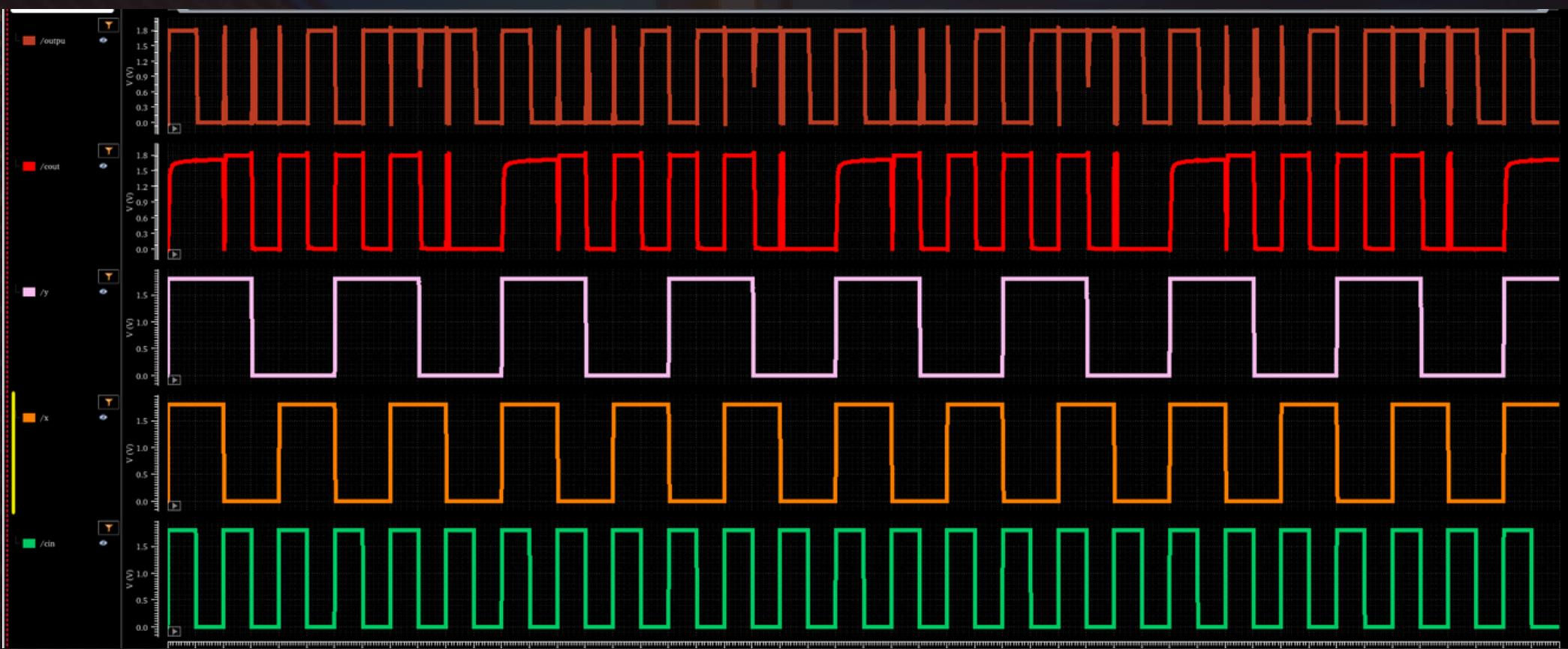
Schemactics

Results



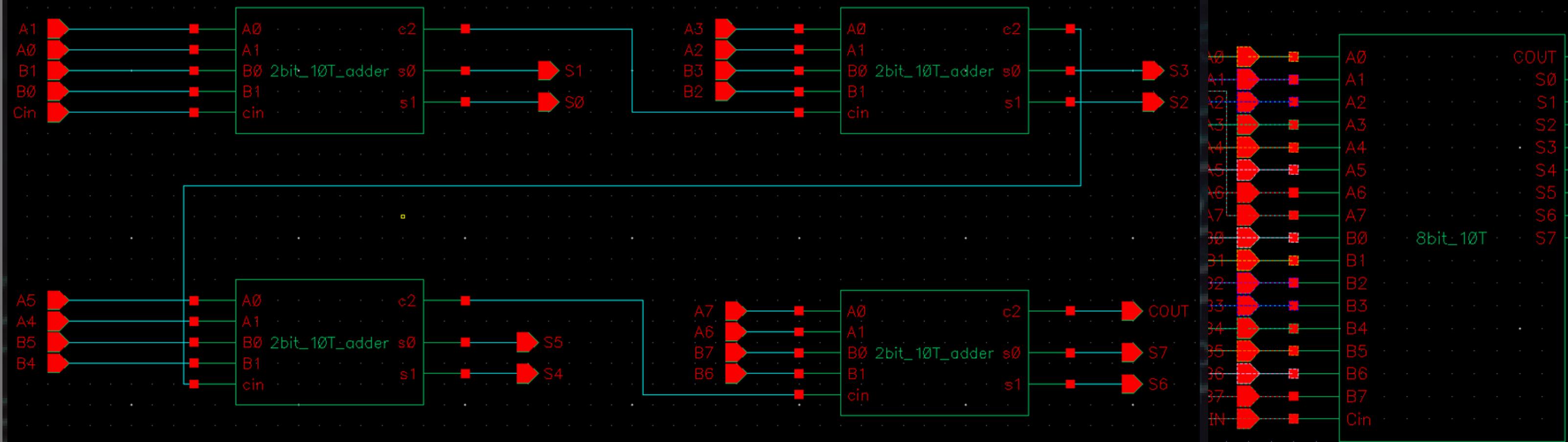


10T full adder

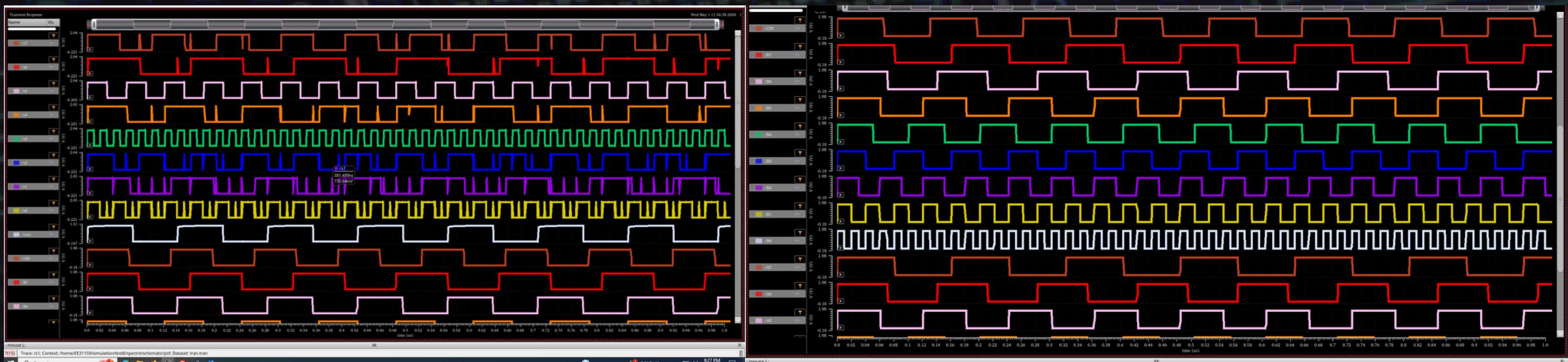


Schemactics

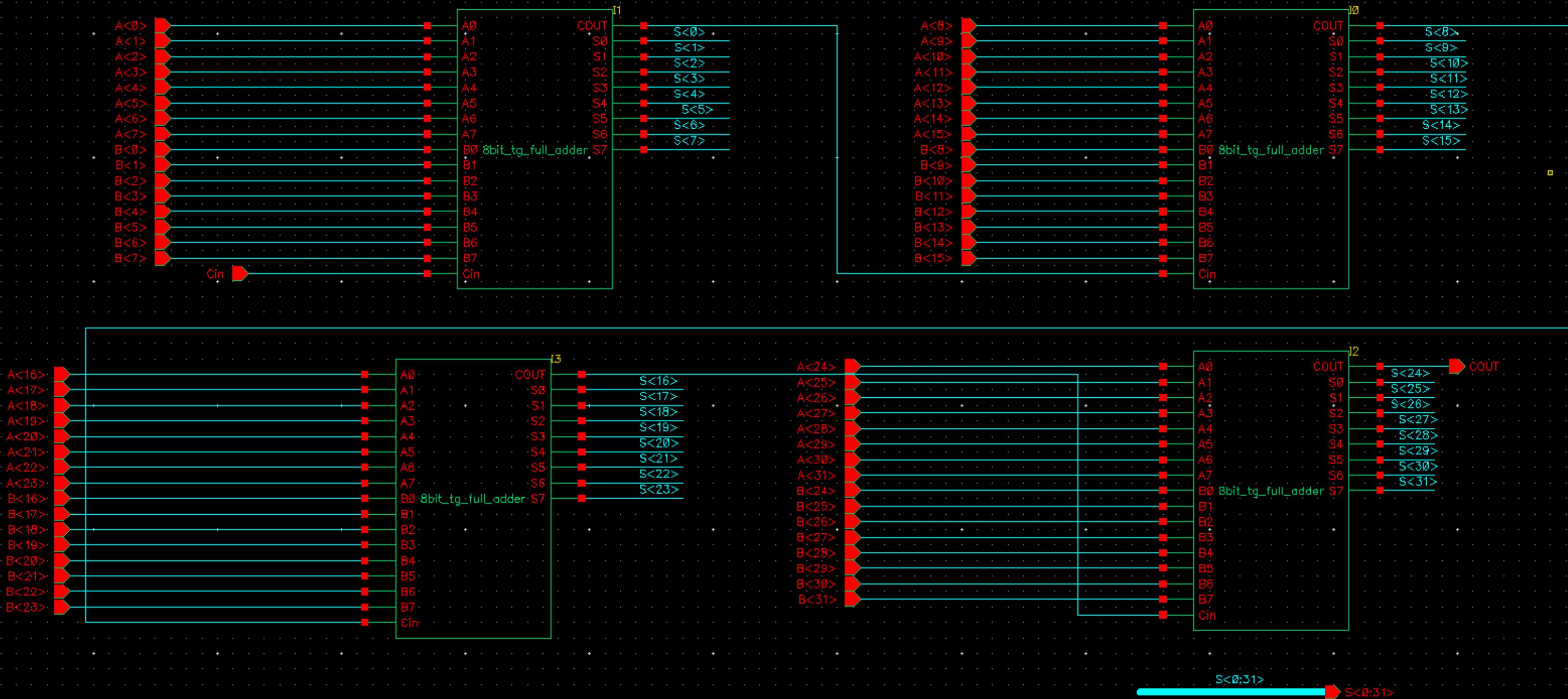
8 bit TG full adder

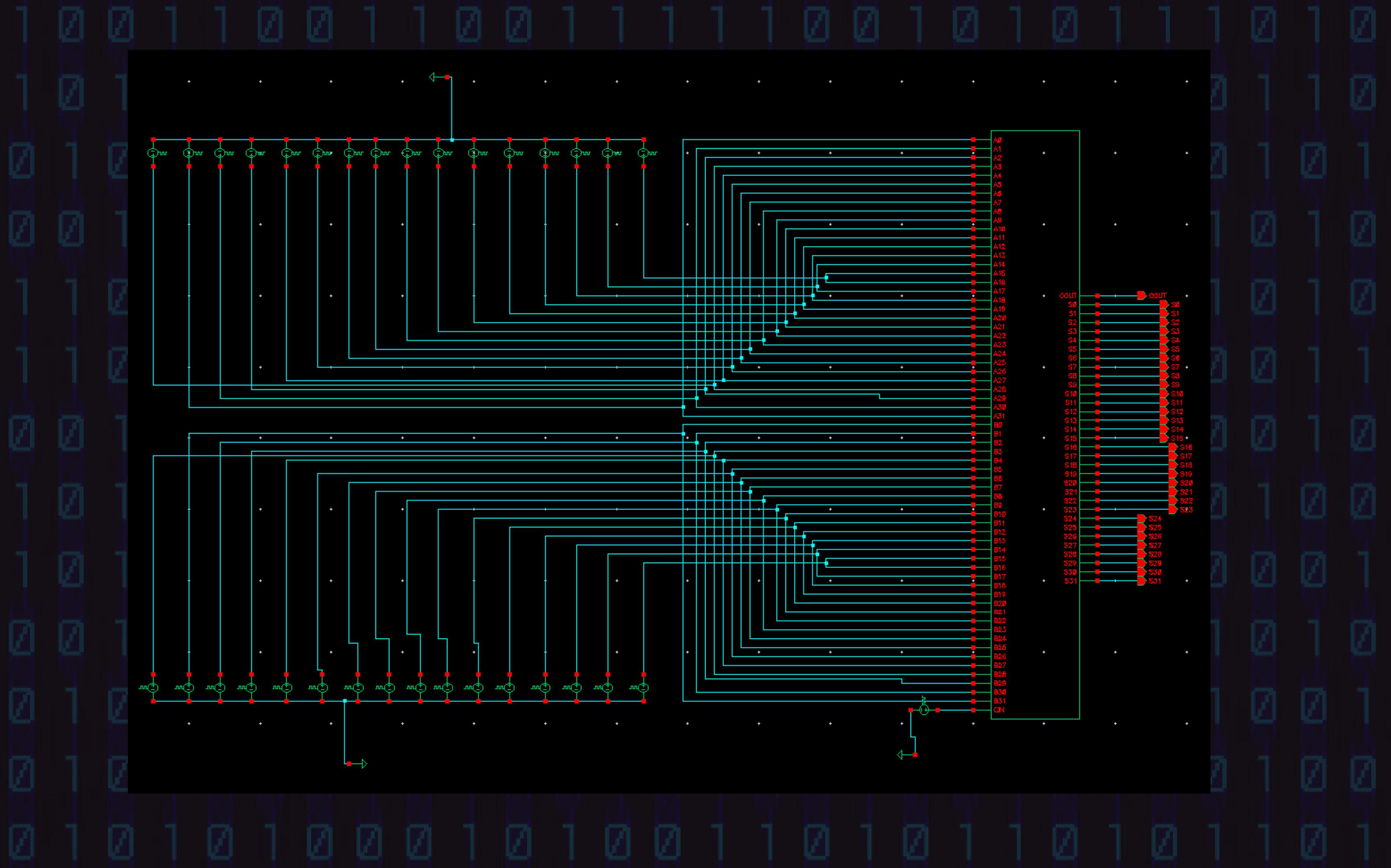


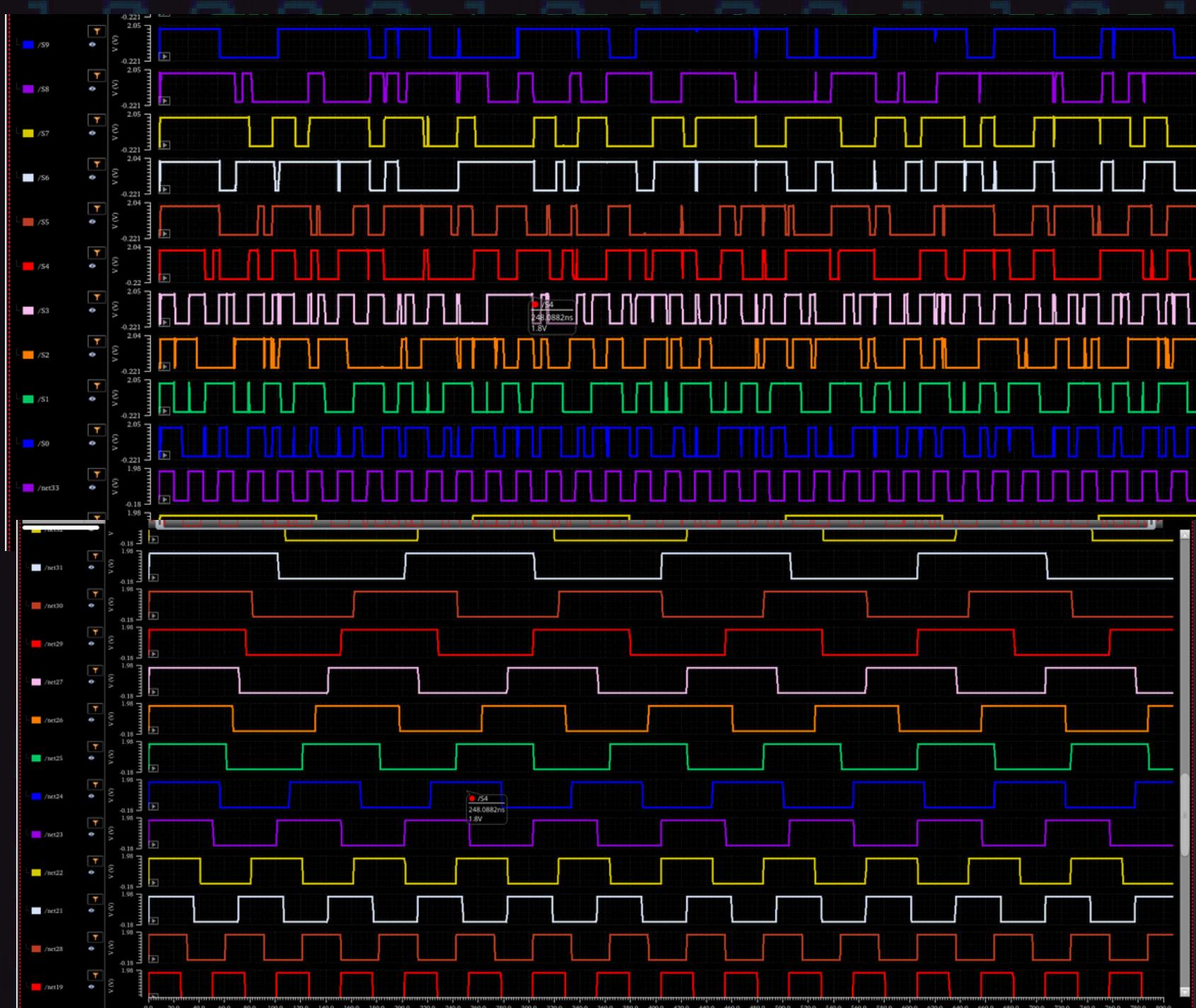
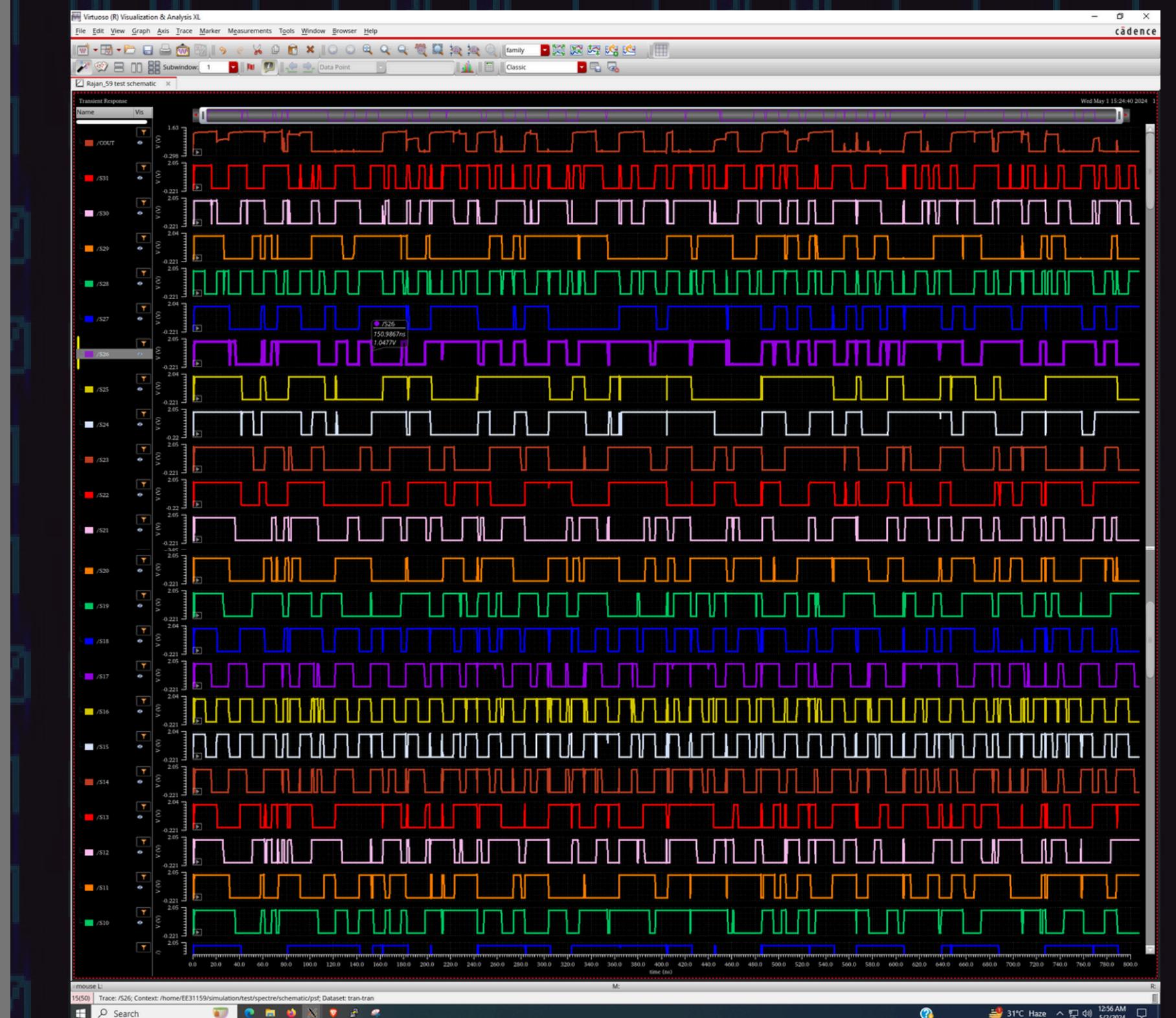
Results



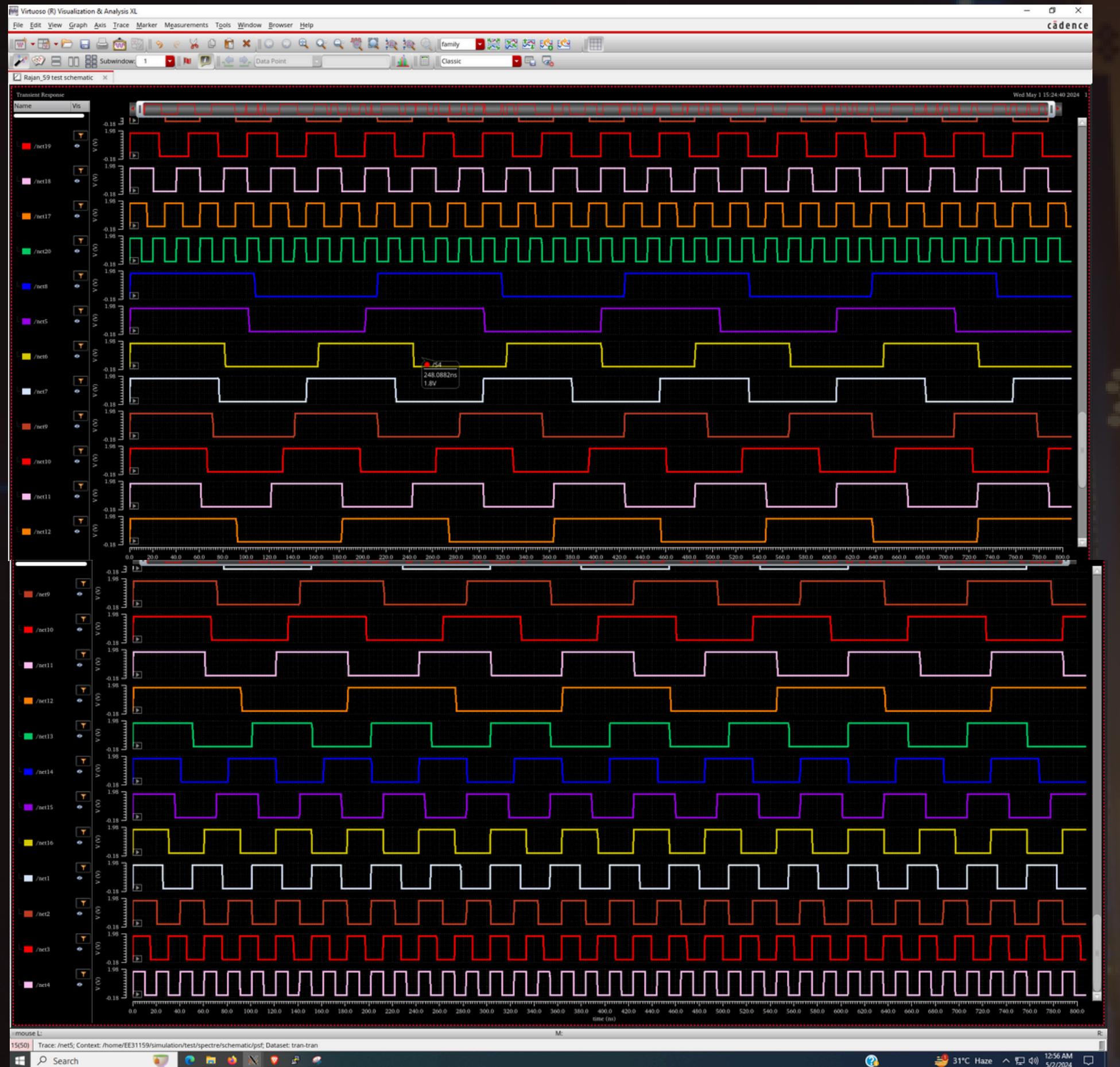
32-bit-TG full adder







output of 32 bit TG full adder



Input of 32 bit TG full adder

vdd=1.8V

Delay

Power

Power dealy
product

1bit TG full adder

0.163ns

143.01e^-6watt

23.320e^-6Ws

1bit 10T full adder

0.102ns

131.4e^-6watt

13.362e^-6Ws

2bit CSA full adder

0.208ns

156.6e^-6watt

32.5728e^-6Ws

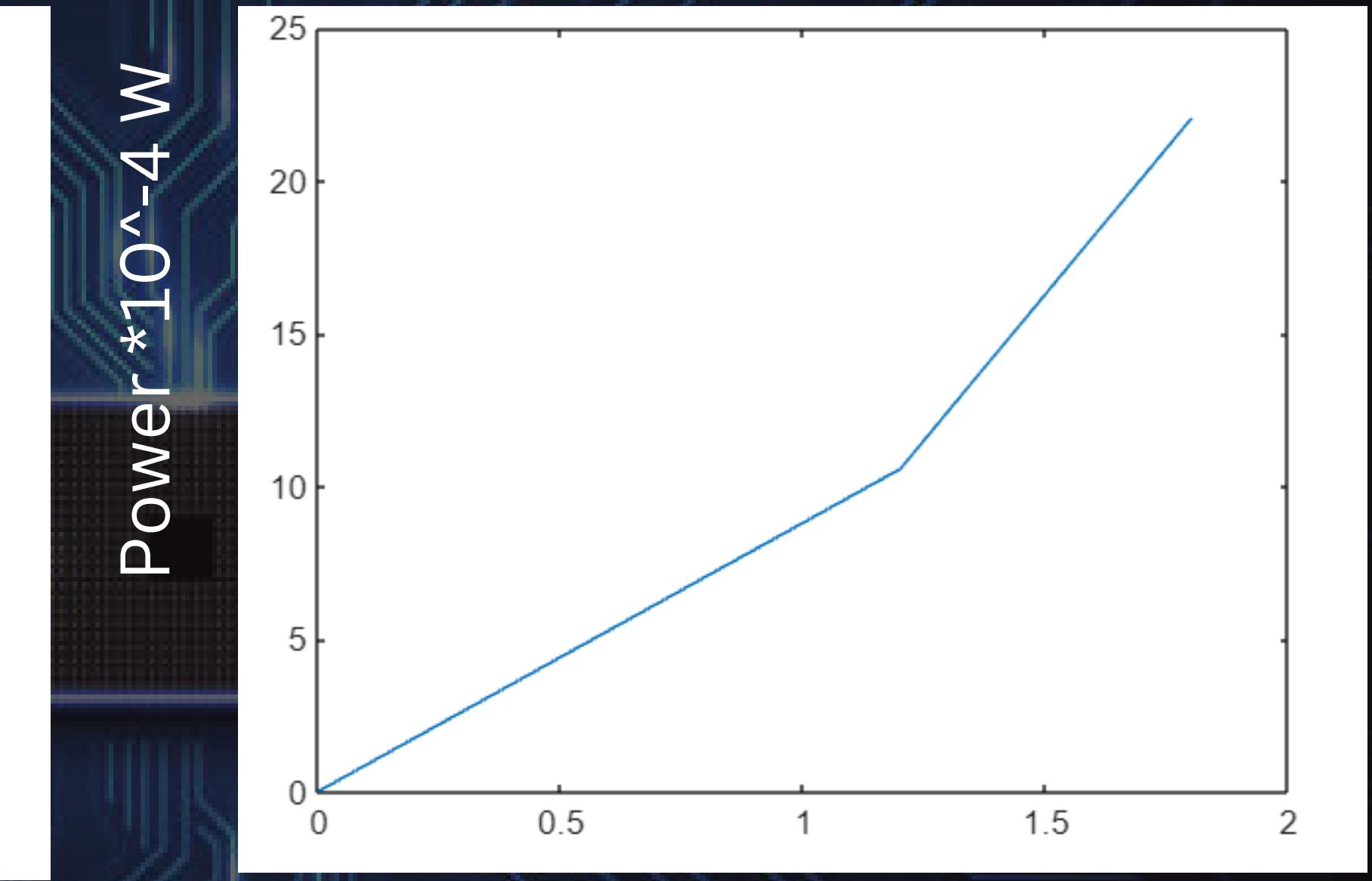
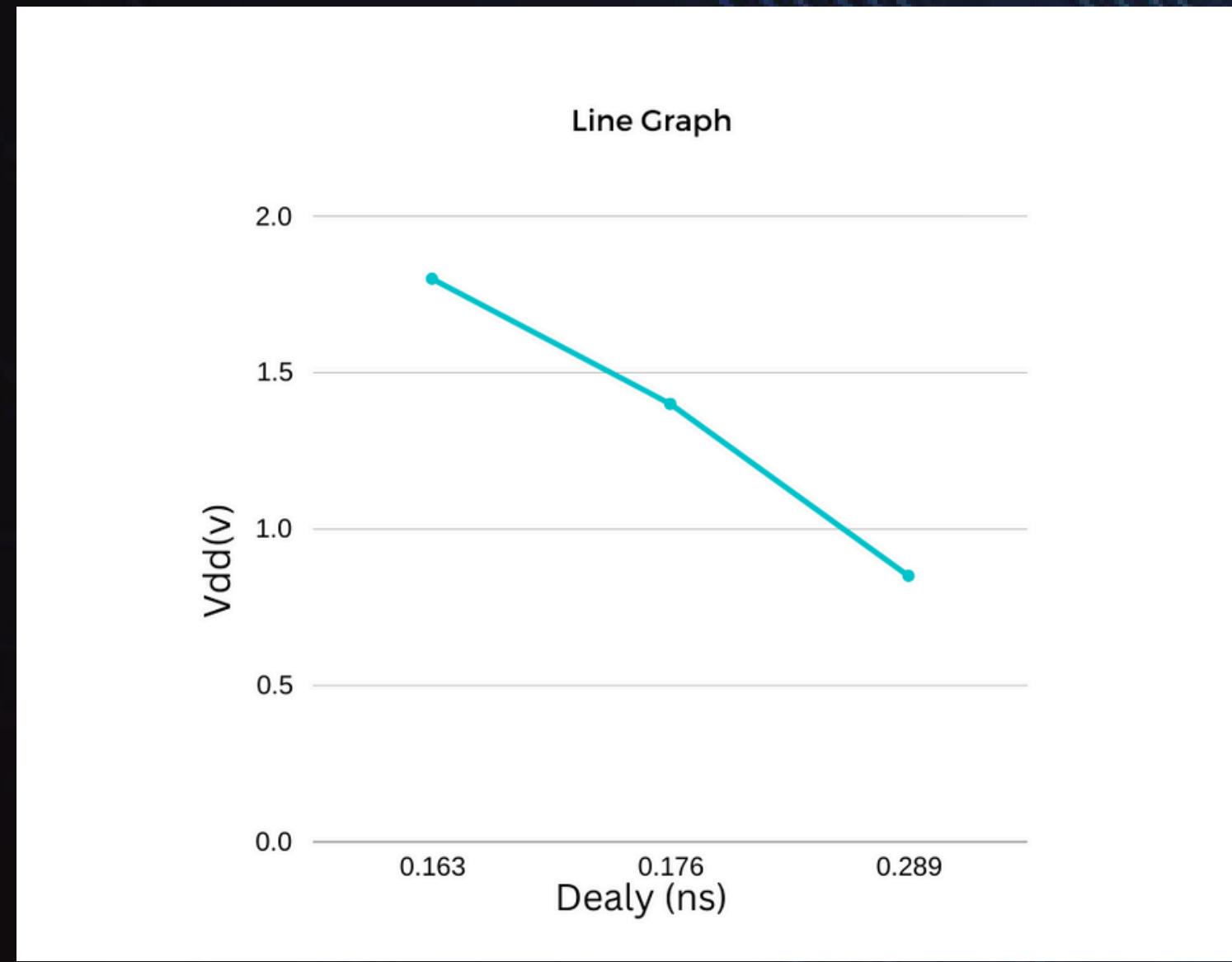
32bit CSA full adder

3.328ns

22.05e^-4watt

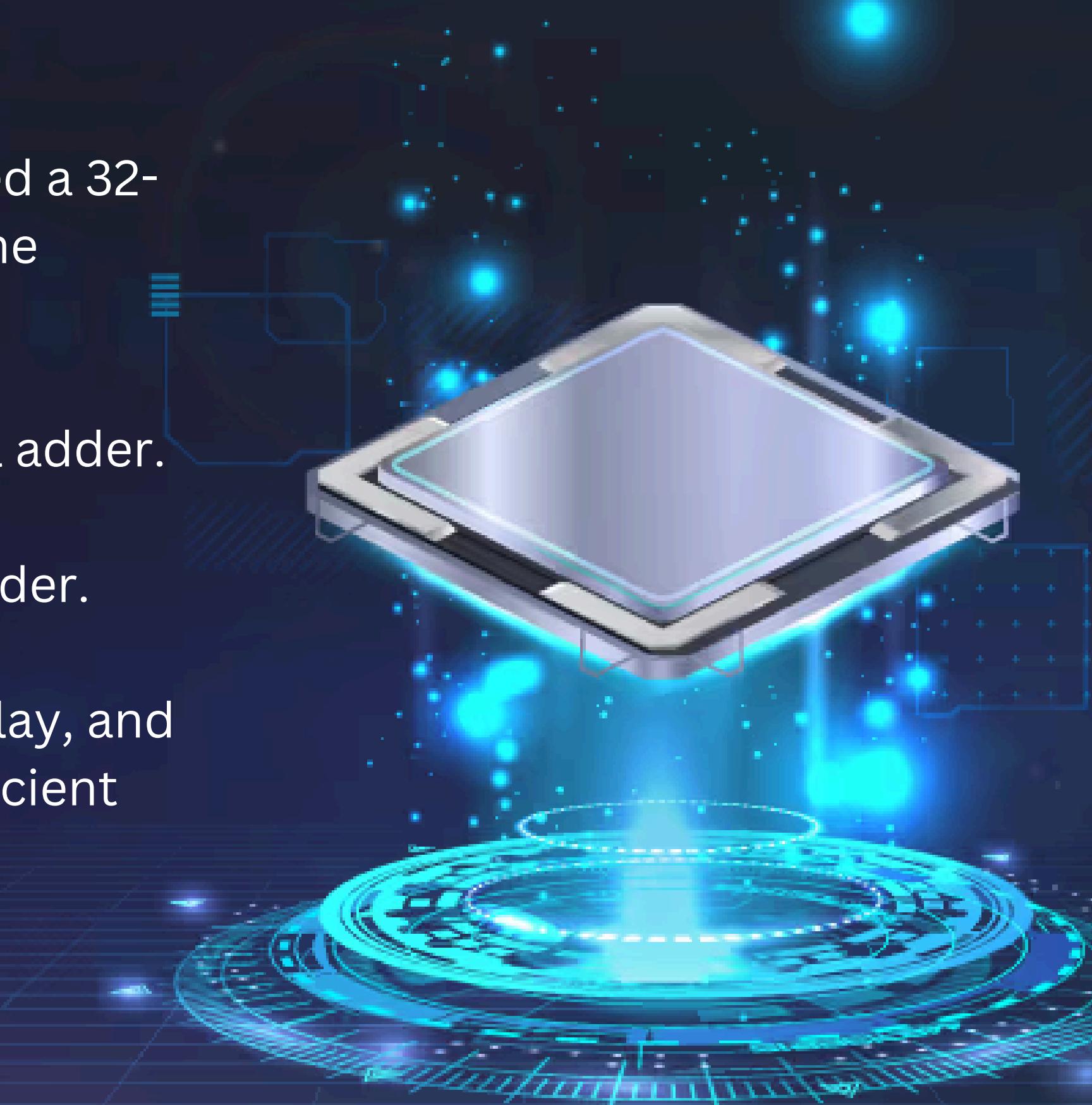
73.3824e^-6Ws

Graphs



Conclusion

- we successfully designed and implemented a 32-bit carry-skip adder using CMOS logic in the 180nm technology node.
- Compared 1 bit TG and pass transistor full adder.
- Achieved delay of 3.328ns for 32 bit TG adder.
- The primary goal was to minimize area, delay, and power consumption while maintaining efficient performance for binary addition.



Reference

[1] <https://ieeexplore.ieee.org/abstract/document/777801> by Hanan A Mahmoud and Magday A.Bayoumi

[2] <https://ieeexplore.ieee.org/document/4263414/references#references>

[3] A. Chandrakasan, R.Brodersen, “Low Power Digital CMOS circuits” , Kluwer Academic publishers, 1995

[4]. Bellauer and M. I. Elmasry, Low-Power Digital VLSI Design Circuits anSystems, KluwerAcademic Publishers, 1995.

[5] <https://ieeexplore.ieee.org/abstract/document/1333335?signout=success>

[6] <https://www.ijeast.com/papers/319-322,Tesma504,IJEAST.pdf>

[7] [Internet sources](#)

