Experiment No. - 1

TITLE :- Implementing SISO, SIPO, PISO shift registers

OBJECTIVE :- The objective of the experiment is to design and implement SISO, SIPO, PISO

APPARATUS REQUIRED :- IC 4013, connecting wires, logic trainer kit.

THEORY :-

Register> A register is a collection of f-flip-flop. A flip-flop is used to store single bit digital data. For storing a large number of bits, the storage capacity is increased by grouping more than one flip-flop. If, we want to store an n-bit word, we have to use an n-bit register containing a number of flip-flops.

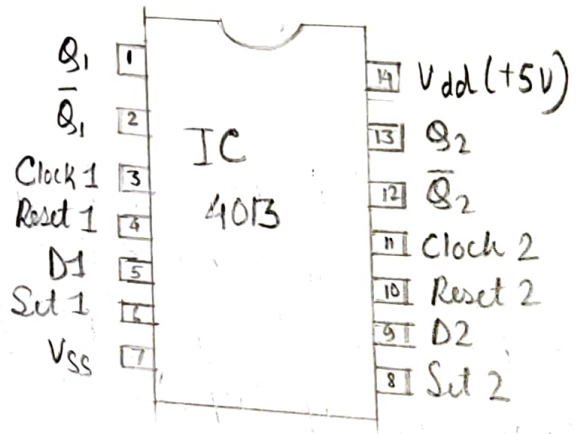
Types of Register>

SISO> Serial in Serial out (SISO) shift register are kind of a shift register where both data loading as well as data retrieval to/from the shift register occurs in serial-mode.

SIPO> A serial in parallel out shift register is similar to the serial in, serial out shift register is that it shifts data into internal storage element and shifts data out at the serial out, data out, pin. It is different in that if makes all the internal stages available as output.

PIPO) The shift register which was parallel input and generates parallel output is known as the parallel input, parallel output shift register. The shift register include three connections only the PI (parallel I/P), PO (parallel O/P) and the clock signal.

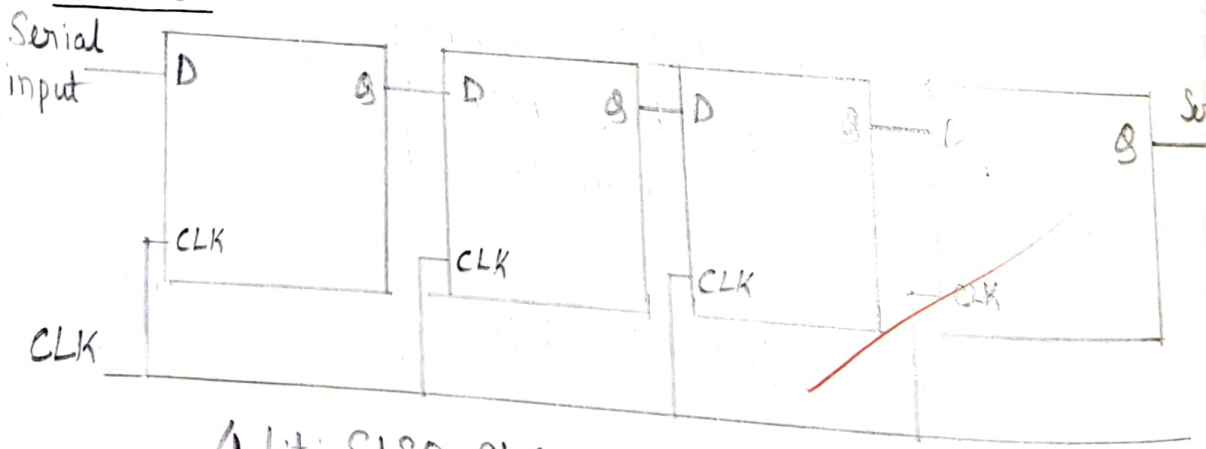
PIN DIAGRAM :-



D flip-flop

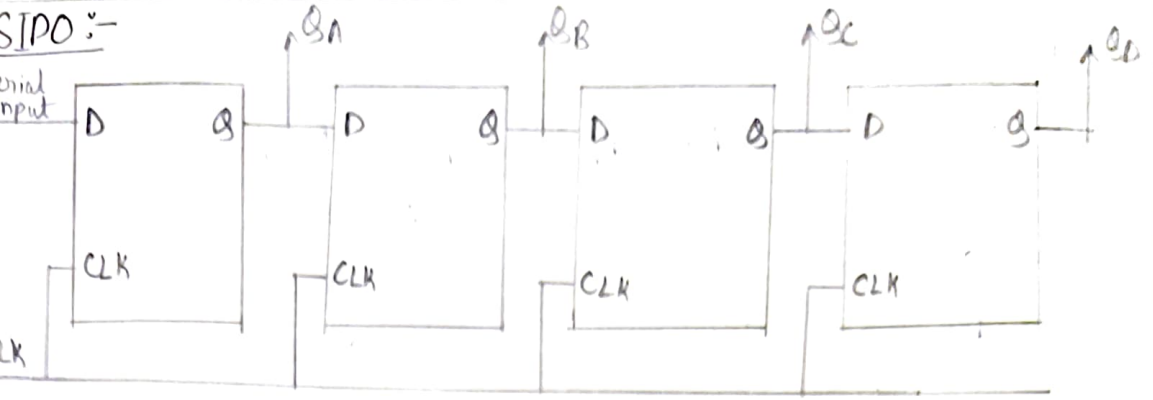
CIRCUIT DIAGRAM :-

SISO :-



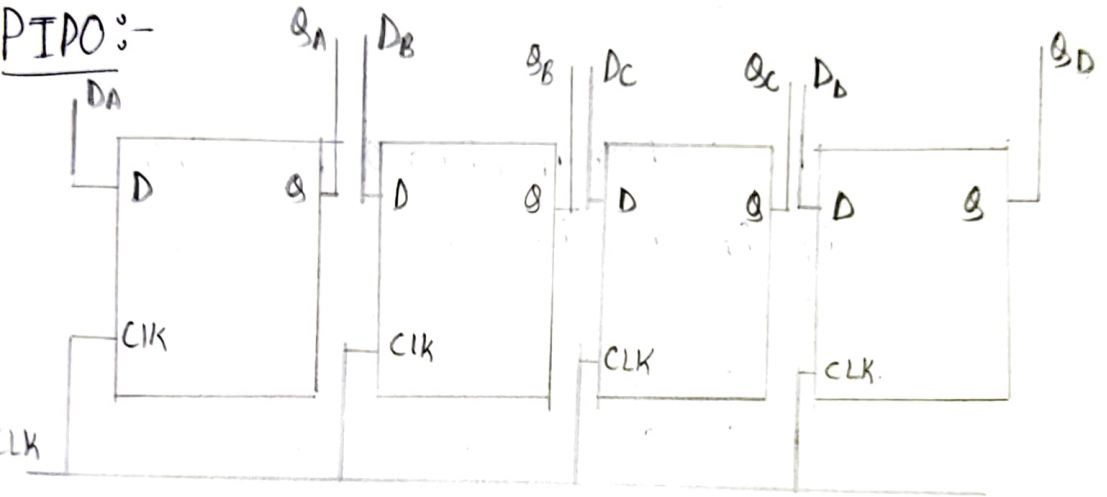
4 bit SISO shift register using D flip-flop

SIPO :-



4 bit SIPO shift register using D flip-flop.

PIPO :-



4 bit PIPO shift register using D flip-flop

~~PISO~~ :-

OBSERVATION TABLE :-

SISO

CLOCK	Serial Data Input (D)	Serial Data Output (Q)
0	0	0
1	1	0
2	0	0
3	0	0
4	0	1

SIPO>

CLOCK	Serial Data Input (D)	Parallel Data Output			
		Q_A	Q_B	Q_C	Q_D
0	0	0	0	0	0
1	1	1	0	0	0
2	0	0	1	0	0
3	0	0	0	1	0
4	0	0	0	0	1

PIPO>

Clock	Parallel Data Input				Data output Parallel			
	Q_A	Q_B	D_C	D_D	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0	0	0	0	0
1	1	0	0	0	1	0	0	0
2	1	1	0	0	1	1	0	0
3	1	1	1	0	1	1	1	0
4	1	1	1	1	1	1	1	1

CONCLUSION :- SISO, SIPO, PIPO registers have been implemented and designed and the truth table is verified.

EXPERIMENT NO. - 2

TITLE :- Design of an adder - subtractor composite circuit.

OBJECTIVE :- To design of an adder - subtractor composite circuit.

THEORY :- The 4-bit adder subtractorcomposite circuit performs the operations of both two 4-bit inputs $A_4A_3A_2A_1$ and $B_4B_3B_2B_1$. The Mode Select line (M) is connected with Cin of the least significant bit of the full-adder, is used to perform the operation of addition of subtraction. The XOR gates are used as controlled inverter.

Adders are part of the arithmetic and logic unit (ALU).

CIRCUIT DIAGRAM :-

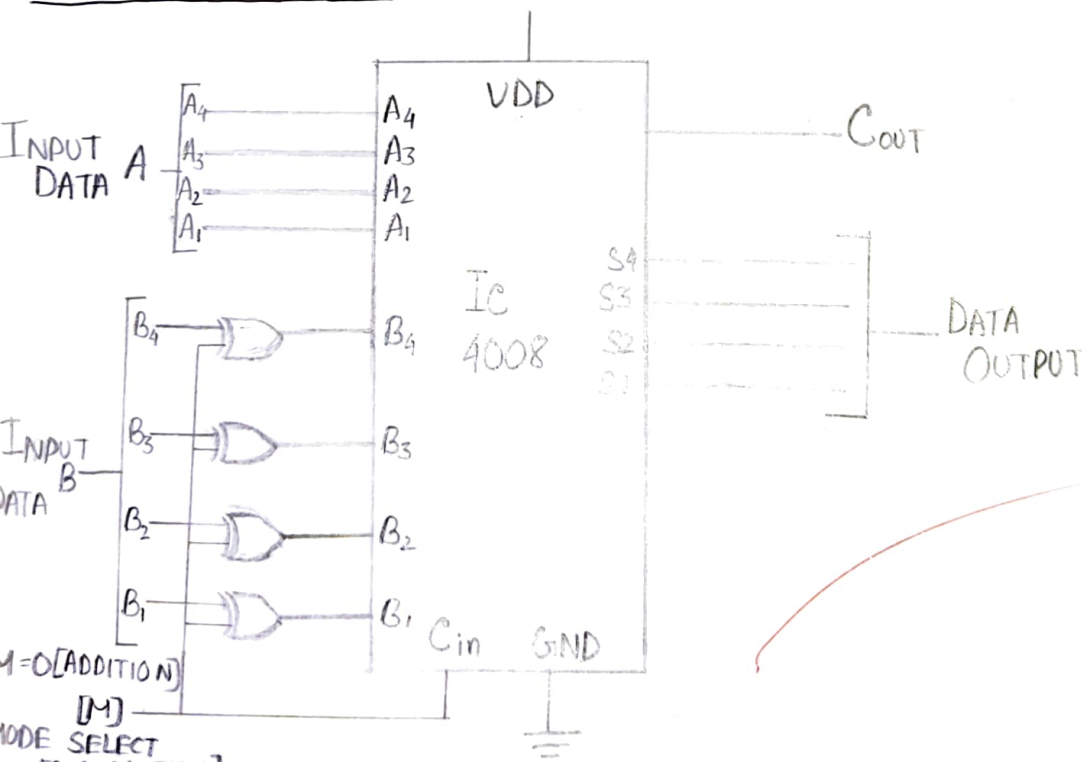
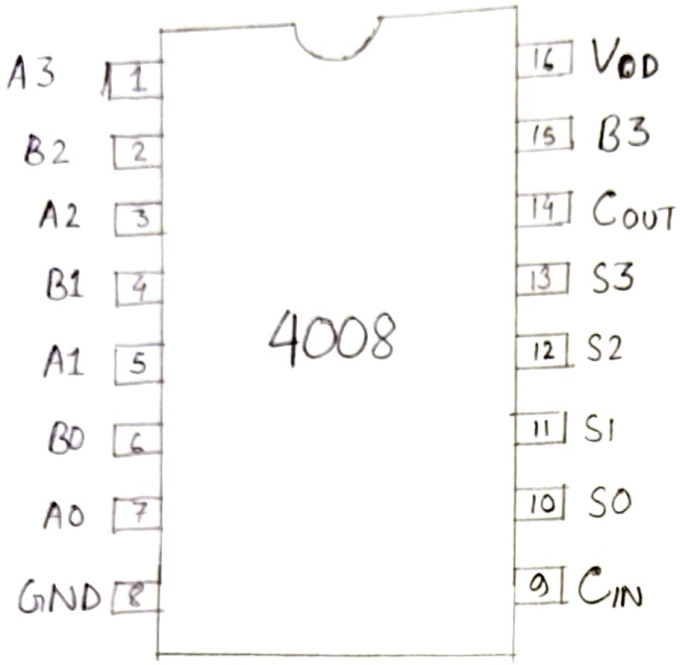


FIG: ADDER - SUBTRACTOR COMPOSITE CIRCUIT

PIN DIAGRAM OF 4-BIT BINARY FULL ADDER IC-4



INSTRUMENT & COMPONENT REQUIRED :-

SI NO.	ITEM	SPECIFICATION	QTY.
1	IC 4008	It is the IC of 4-bit binary full adder IC-4008.	1
2	IC 4070	It is the IC of XOR gate.	1
3	Bread board	It is to make quick electrical connections between components.	1
4	Electrical wires	Used to do a electrical experiment and connects thecomponents	10

VERIFICATION TABLE :-

MODE SELECTION	INPUT (A)				INPUT (B)				OUTPUT (S)				
	A_4	A_3	A_2	A_1	B_4	B_3	B_1	B_1	C_{OUT}	S_4	S_3	S_2	S_1
0	0	0	0	1	0	1	0	1	0	0	1	1	0
0	1	1	1	1	1	1	1	1	1	1	1	1	0
0	0	0	1	1	1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	1	0	0	0	1	0	1
1	1	1	1	1	1	1	1	0	0	0	0	0	1
1	1	1	0	0	1	0	0	0	0	0	1	0	0

CONCLUSION :-

We have implemented design and experiment of an adder-subtractor composite circuit using IC 4008 & IC 4070 with the help of circuit diagram successfully.

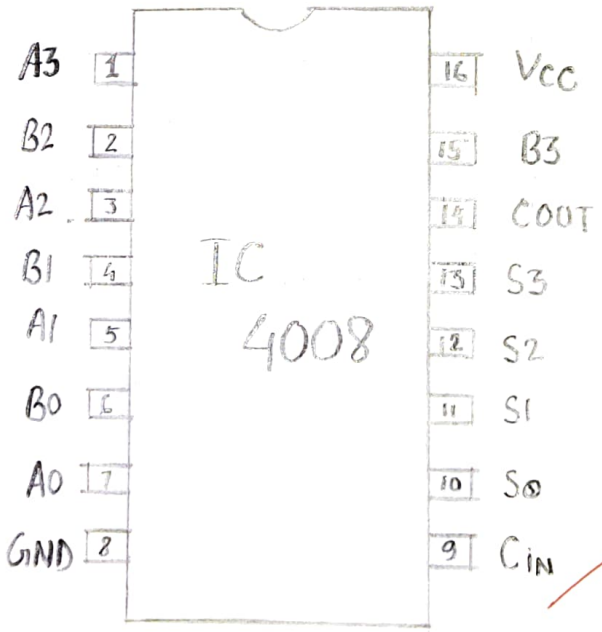
EXPERIMENT NO. - 3

TITLE :- Design of an BCD(Binary Coded Decimal) adder circuit.

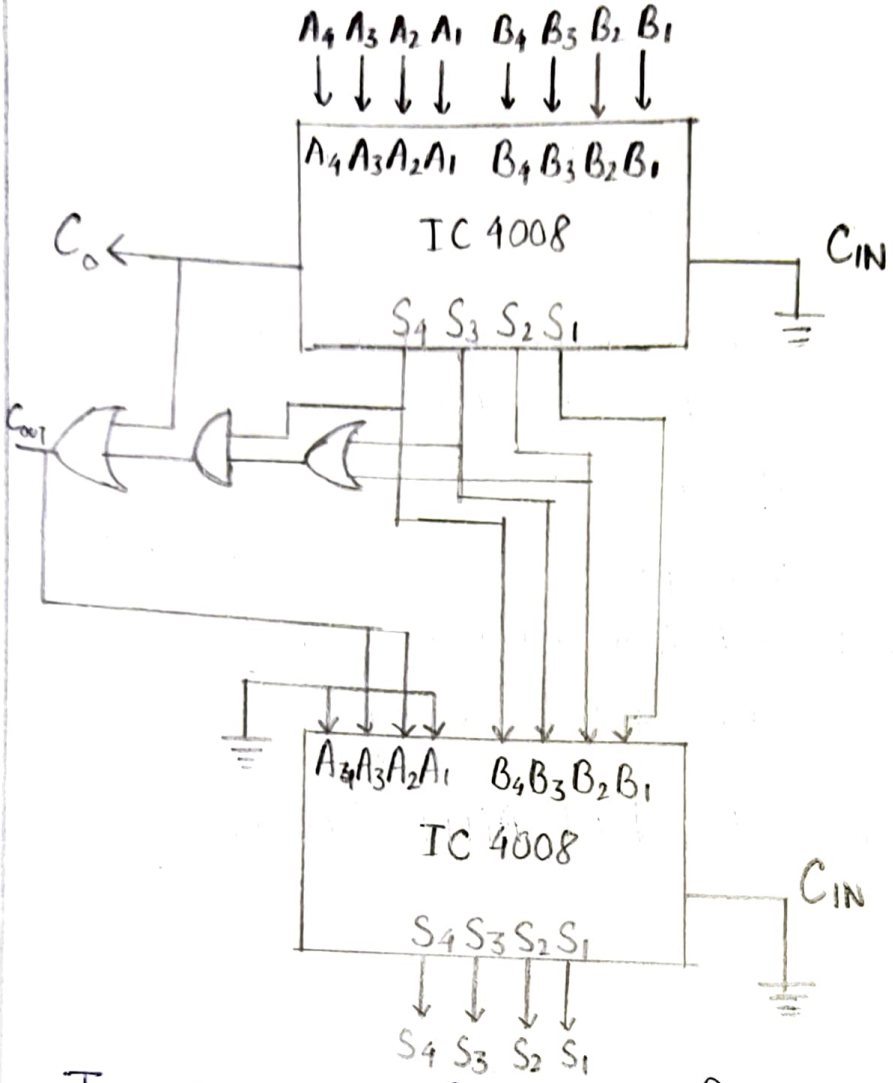
OBJECTIVE :- To design an BCD(Binary Coded Decimal) adder circuit.

THEORY :- A BCD adder is a circuit that adds two BCD digits in parallel and makes a sum digit also in BCD. BCD's full form is Binary Coded Decimal. The 4-bit BCD adder circuit performs the operations of both two 4-bit inputs $A_4A_3A_2A_1$ and $B_4B_3B_2B_1$. Here, with the BCD adder IC, we will use AND gate and OR gate.

PIN DIAGRAM OF 4-BIT BCD ADDER CIRCUIT :-



CIRCUIT DIAGRAM :-



INSTRUMENT & COMPONENT REQUIRED :-

Sl No.	ITEM	SPECIFICATION	QTY.
1	IC 4008	It is the IC of BCD adder circuit.	2
2	IC 4081	It is the IC of AND gate.	1
3	IC 4071	It is the IC of OR gate.	1
4	Bread board	It is to make electrical connections	1
5	Electrical wires	Used to do electrical experiment.	10

OBSERVATION TABLE :-

DECIMAL	BINARY SUM					BCD SUM				
	C	S_4	S_3	S_2	S_1	C	S_4	S_3	S_2	S_1
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	1
2	0	0	0	1	0	0	0	0	1	0
3	0	0	0	1	1	0	0	0	1	1
4	0	0	1	0	0	0	0	1	0	0
5	0	0	1	0	1	0	0	1	0	1
6	0	0	1	1	0	0	0	1	1	0
7	0	0	1	1	1	0	0	1	1	1
8	0	1	0	0	0	0	1	0	0	0
9	0	1	0	0	1	0	1	0	0	1
10	0	1	0	1	0	1	0	0	0	0
11	0	1	0	1	1	1	0	0	0	1
12	0	1	1	0	0	1	0	0	1	0
13	0	1	1	0	1	1	0	0	1	1
14	0	1	1	1	0	1	0	1	0	0
15	0	1	1	1	1	1	0	1	0	1

CONCLUSION :-

We have implemented design and experiment of a BCD (Binary Coded Decimal) adder circuit using IC4008, IC 4081, IC 4071 with the help of circuit diagram successfully.

EXPERIMENT No.:- CO-05 (A)

TITLE :- Design a composite Logic Unit using Multiplexer.

OBJECTIVE :- To design a composite Logic Unit using Multiplexer.

THEORY :- Logic microoperations are very useful for manipulating individual bits or a portion of a word stored in a register. They can be used to change bit values, delete group of bits, or insert new bit values into a register. These microoperations require different logic gates to be inserted for each bit or pair of bits in the register to perform the required operation. Although there are several logic microoperations, most computers use only - four AND, OR, XOR and NOT - from which all others can be derived.

FUNCTION TABLE :-

Selection Lines S_1	Selection Lines S_0	OUTPUT (F)	OPERATION
0	0	A'	NOT
0	1	$A \cdot B$	AND
1	0	$A + B$	OR
1	1	$F = A \oplus B$	XOR

PIN DIAGRAM :-

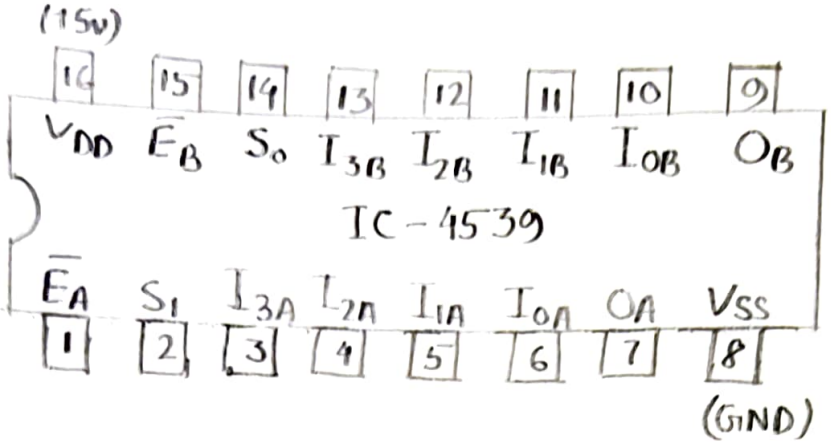


FIG: Pin diagram of Dual 4-input multiplexer

CIRCUIT DIAGRAM :-

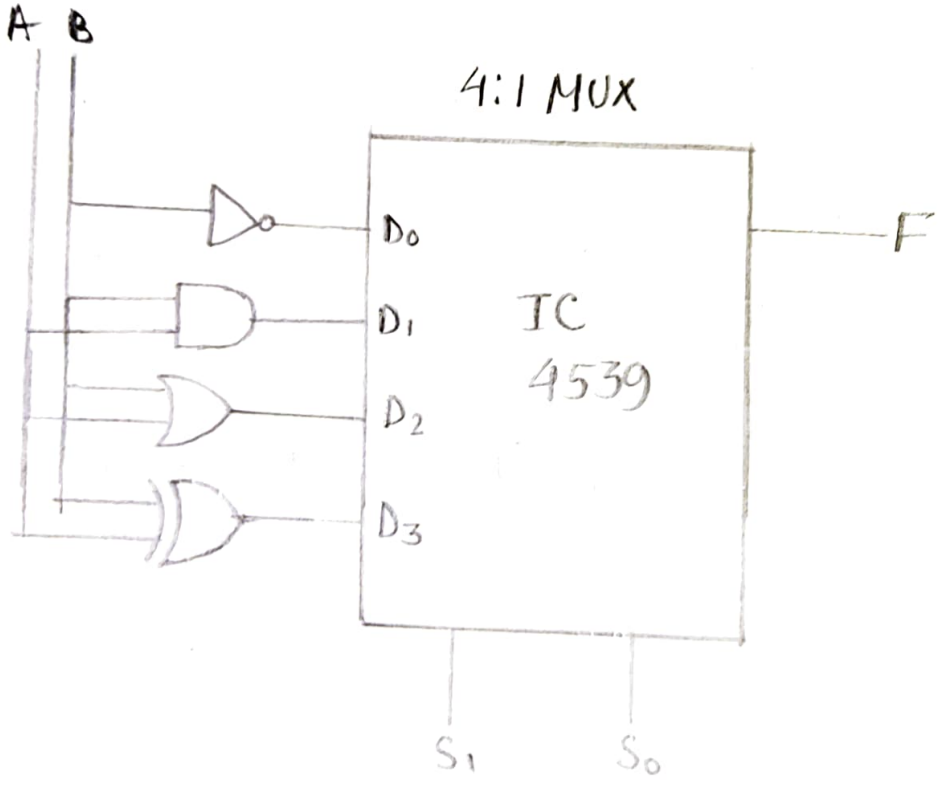


FIG: CIRCUIT DIAGRAM of COMPOSITE LOGIC UNIT USING MULTIPLEXER

INSTRUMENT & COMPONENT REQUIRED :-

SI NO.	ITEM	SPECIFICATION	QTY.
1	IC 4539	It is the IC of 4-bit composite arithmetic unit or ALU	2
2	IC 4081	It is the IC of AND gate	1
3	IC 4071	It is the IC of OR gate	1
4	IC 4069	It is the IC of NOT gate	1
5	IC 4070	It is the IC of XOR gate	1
6	Bread board	It is the equipment to make electrical connections	1
7	Electrical wires	Used to do electrical connections by making connection in bread board	15

VERIFICATION TABLE :-

Select Lines		Input		Output (Fi)	Operations
S_1	S_0	Ai	Bi		
0	0	0	0	D_0	NOT
0	1	0	1	D_1	AND
1	0	1	0	D_2	OR
1	1	1	1	D_3	XOR

CONCLUSION :-

We have implemented design and experimentation of a composite logic unit using multiplexer with the help of various components like NOT, AND, OR & XOR gate. We observed the experiment is successful ~~and~~ with the help of circuits and observation table.

EXPERIMENT No.:- CO-05(B)

TITLE :- Design a 4-bit composite Arithmetic Unit using Multiplexer.

OBJECTIVE :- To design a 4-bit composite Arithmetic Unit using Multiplexer.

THEORY :- The Arithmetic Unit (AU) also called the Arithmetic Logic Unit (ALU), is a part of the Central Processing Unit (CPU). It is often referred to as the Engine of the CPU because it allows the Computer to perform mathematical calculation such as addition, subtraction etc. The Arithmetic Unit comprised of many interconnected elements that are designed to perform specific task. The basic component of an ALU is the parallel adder. By controlling the data inputs to the adder, it is possible to obtain different types of arithmetic operations.

FUNCTION TABLE :-

Function Selection			Output of the MUX(Y)	OUTPUT(F)	Function Name
S_1	S_0	Cin			
0	0	0	B	F=A+B	Add B to A
0	0	1	B	F=A+B+1	Add B to A plus 1
0	1	0	B'	F=A+B'	Add 1's complement of B to A
0	1	1	B'	F=A+B'+1	Add 2's complement of B to A
1	0	0	0	F=A	Transfer A
1	0	1	0	F=A+1	Increment A

CONTD.

INSTRUMENT & COMPONENT REQUIRED :-

Function Selection			Output of the MUX(Y)	Output (F)	Function Name
S_1	S_0	Cin			
1	1	0	AB	F=A-1	Decrement A
1	1	1	AB	F=A	Transfer A

PIN DIAGRAM :-

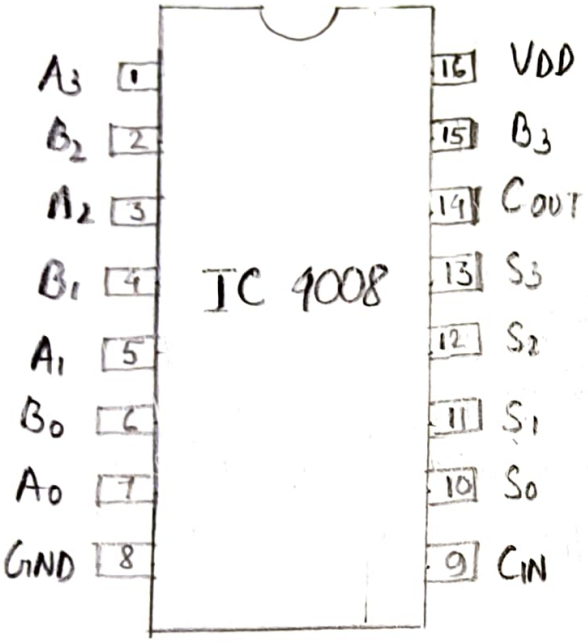


FIG. Pin diagram of 4-bit binary Full adder IC-4008

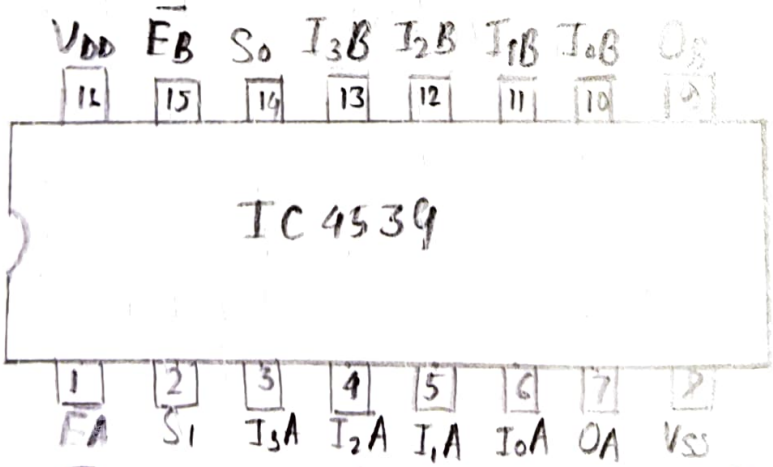


Fig TC 4539 (Dual 4-input Multiplexer)

INSTRUMENT & COMPONENTS REQUIRED :-

SI NO.	ITEM	SPECIFICATION	QTY.
1	IC 4539	It is the IC of 4-bit composite arithmetic unit or ALU	2
2	IC 4008	It is the IC of BCD adder circuit	1
3	IC 4069	It is the IC of NOT gate	1
4	Bread board	It is the equipment to make electrical connections	1
5	Logic trainer kit	The main component to do the experiments	1
6	Electrical wires	Used to do electrical connection with bread board, ICs, trainer kit	25

CIRCUIT DIAGRAM :-

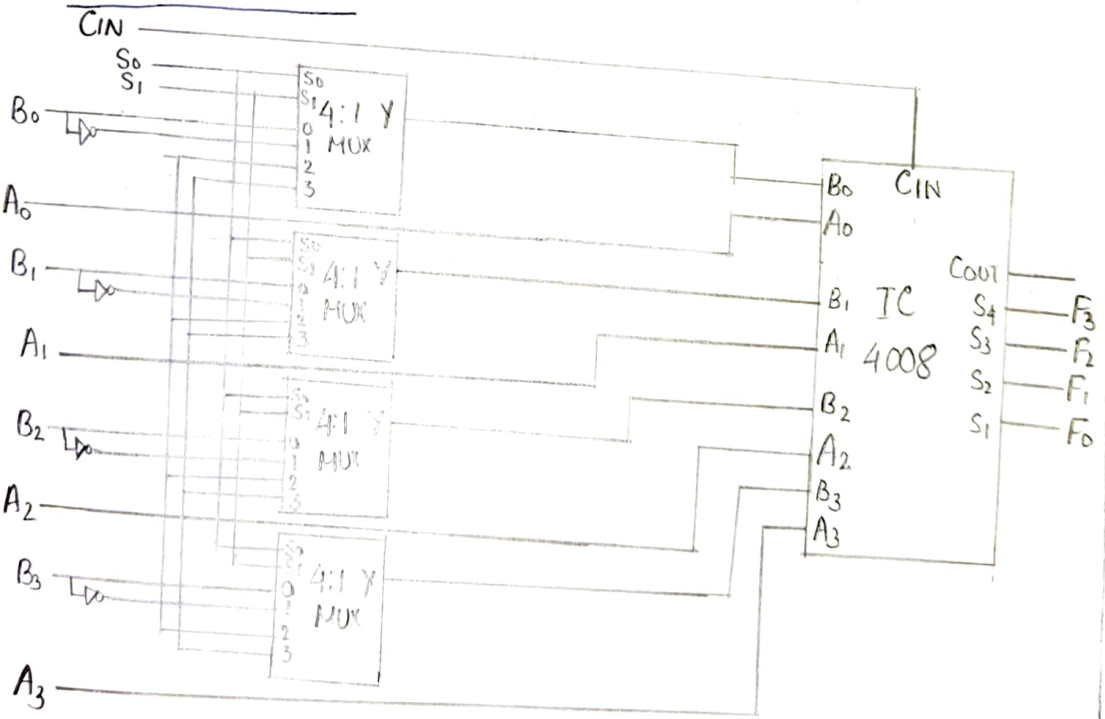


FIG. Circuit diagram of Composite Arithmetic Unit using MUX

VERIFICATION TABLE :-

Function	Select Inputs			Input (A)				Input (B)				Output (Y)				
	S_1	S_0	Cin	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	Cout	F_3	F_2	F_1	F_0
	0	0	0													
	0	0	1													
	0	1	0													
	0	1	1													
	1	0	0													
	1	0	1													
	1	1	0													
	1	1	1													

CONCLUSION :-

We have implemented design and experimentation of a composite ~~logic~~ arithmetic unit using multiplexer with the help of various components like NOT, BCD adder gate and we also observed the experiment is successful with the help of circuits and observation table.