**TECHNICAL REPORT**

([Document of Project A])

HISTOHRAM OF ORIENTED GRADIENT:

**[REPORT’S TITLE HERE]**

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Document History (lịch sử sửa đổi)

* **Version 01**

Blah…blah…

* **Version 00**

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# Specifications

# Overall Architectures of SISHOG



Figure 1 Overall Architecture

**Main components and functions:**

1. Cell Histogram Generation (CHG):
   1. reading pixel data via Control Center
   2. computing 9-bins and sum of bin square of a Cell
   3. writing result to local MEM
2. Window (**not completed definition**):
   1. reading output of 16x8 Cell from MEM
   2. computing window features
3. Control Center (**not completed definition**):
   1. memory: storing 9-bins and sum of bin square in order, …
   2. sending command signals and requirement data to CHG and Window module
   3. interacting to the outside modules of SISHOG for archiveing pixel data and write the output

# Cell Historgram Generation

## Overall

**Functions:**

Loading 100 pixels of a CELL

Computing 9-bins of CELL and sum of bin square cb =

Writing out in order: = 22 bytes

is integer number with 16-bits length, => 13 bit integer

is integer number with 32-bits lengths ⬄ 4 bytes

hog_arc

Figure 2 CHG Architecture for one component of a pixel

**Main signal/components:**

1. **counter** is used to generate control signals (representing current status of CHG), **counter** in [0..112], CHG’s status can be:

* Loading without enable pix2bin (no computing 2 bins of pixel), when counter is [0..21], [3-9][0-1], [102-end]
* Loading with enable pix2bin (computing 2 bins of pixels), when counter is in [22-30], [32-40],[42-40]…[92-100]
* Writing bin out [102-110]
* Reseting all banks when couter = MAX or rst = 1

|  |  |  |
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| **Signal** | **Function** | **How** |
| vld\_out | Valid output, active high | 1 when writing out  0, otherwise |
| rst\_bin\_bank | Reset bin\_bank, active high | 1 when reset all bank  0, otherwise |
| binpos\_wo | Current write out bin position, [0-8] | [0-8] when writing out  0, when others |
| pix2bin\_rst | Disable(0)/Enable(1) pix2bin | 1 when loading with enable pix2bin,  0, otherwise |

1. **pix\_bank** a shift register store 23 pixels of a CELL
2. **bin\_bank** a register store 9-bins of a CELL

At each cycle,

bin[i1] = bin[i1] + mag\_1

bin[i2] = bin[i2] + mag\_2

1. **pix2bin is** a component compute 2-bins of a pixels.

if pix2bin\_rst = 0, return mag\_1 = mag\_2 = 0;

else return 2 bin positions i1,i2 and 2 magnitudes mag\_1, mag\_2

## Feature vectors/bins of a pixel: pix2bin



Figure 3 pix2bin

⬄ 15-bit float number with 8-bit fractional part

# Control Center (not completed definition)

Control data flow and send commands to other modules

## Memmory

**Functions:**

Storing CHG in order

Each CHG contains 22 bytes ⬄ 22 memory cell

**CHG order in MEM:**

n = (image\_width / 8)

max = (image\_height / 8 ) - 1

CHG = 22 bytes

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| CHG(0) | CHG(1) | CHG(2) |  |  |  | CHG(n-1) |
| CHG(n) |  |  |  |  |  | CHG(2n-1) |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  | CHG(max) |

**An Image 3840 × 2160 requires:** MEM\_SIZE = 2.72 Mbytes for CHG per a component

# Window feature vectors/bins (not completed definition)

**Functions:**

Loading 16x8 CHG or 1x8 or 16x1 CHG via Control Center

Getting control singal from Control Center

Computing 3780 normalization bin

**Don’t care about window position**

**Detail interfaces (not completed definition):**

Clk, rst

Enable signal:

Mode signal: 16x8, 1x8, 16x1 corresponding to number of CHG need to be load and how to computing bin of window (how to reused load CHG, and computed bins)

Data interface ⬄ input data

**Detail of Mode:**

**16x8:** load total CHG in window, make sure that all local memory in Window is empty

**1x8*:***  Window is moving in Ox axis

**16x1:** Window is moving in Oy axis.

**16x8 CHG Memory in Window: storing 16x8 CHG in order: 1…16x8**

**16x1** at each clock: need 16 x (22/input data width) clock

16x8\_CHG = 16x8\_CHG[1..16x8] & new\_data

**16x8** at each clock: need 16 x 8 x (22/input data width) clock

16x8\_CHG = 16x8\_CHG[1..16x8] & new\_data

**1x8:** at clock ith

16x8\_CHG[(i\*9)..(i\*9 + 8)] = 16x8\_CHG[(i\*9 + 1) ..( i \*9 + 8)] & new\_data

**State of Window**

Loading CHG

Computing normalization bins

Hết !

DANH MỤC HÌNH VẼ

[Figure 1: Hình thứ nhất. **Error! Bookmark not defined.**](#_Toc224575542)

DANH MỤC BẢNG BIÊU

[Table 1: Tên bảng biểu **Error! Bookmark not defined.**](#_Toc224575555)