**LSI Contest 2017 Report**

***Human Detection by Histogram of Oriented Gradients***

# GENERAL INFORMATION

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| --- | --- |
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| Size of team member's T-shirt: | M |
| The tasks level of design: | Level 1 |

Table of content

[GENERAL INFORMATION 1](#_Toc473310415)

[Contents 2](#_Toc473310416)

[CONTENTS 3](#_Toc473310417)

[1. Purpose 3](#_Toc473310418)

[2. Architecture 3](#_Toc473310419)

[2.1. General Architecture 3](#_Toc473310420)

[2.2. Cell Input Generation 3](#_Toc473310421)

[2.3. Cell Histogram Generation 4](#_Toc473310422)

[2.4. Histogram Normalization 4](#_Toc473310423)

[2.5. SVM Classification 5](#_Toc473310424)

[2.6. Processing 5](#_Toc473310425)

[3. Originality point 6](#_Toc473310426)

[3.1. Scan image by shift register 6](#_Toc473310427)

[3.2. Using LUT (Look Up Table) when calculating magnitude gradient 6](#_Toc473310428)

[3.3. Calculating SVM Classification by combined serial and parallel 7](#_Toc473310429)

[4. C Code 8](#_Toc473310430)

[4.1. Introduction 8](#_Toc473310431)

[4.2. lsi\_2017.c 8](#_Toc473310432)

[4.3. helper.h 10](#_Toc473310433)

[4.4. human\_detection.h 12](#_Toc473310434)

[4.5. Cal\_HOG\_block.h 14](#_Toc473310435)

[5. The display of a simulation waveform which the design is operating 16](#_Toc473310436)

[6. Others 16](#_Toc473310437)

[6.1. Acknowledge 16](#_Toc473310438)

[6.2. Detail C code 17](#_Toc473310439)

[6.2.1. helper.c 17](#_Toc473310440)

[6.2.2. human\_detection.c 21](#_Toc473310441)

[6.2.3. Cal\_HOG\_block.c 30](#_Toc473310442)

# CONTENTS

# HOG, SVM introduction

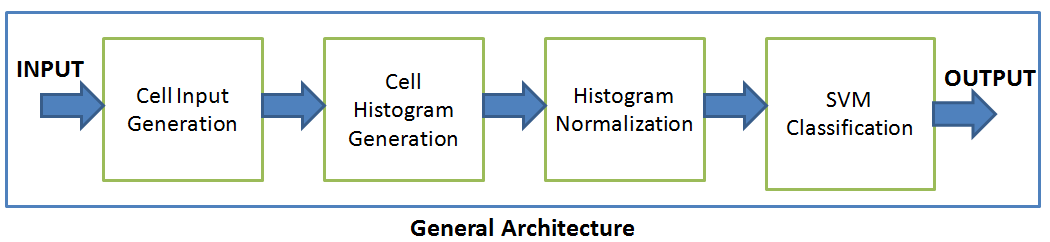
Gray data ->

# Purpose

My purpose is can simulation hardware of this project by HDL code. Currently, I designed hardware architecture and simulation it in C code. The most important in my architecture is optimized performance and timing.

# Architecture

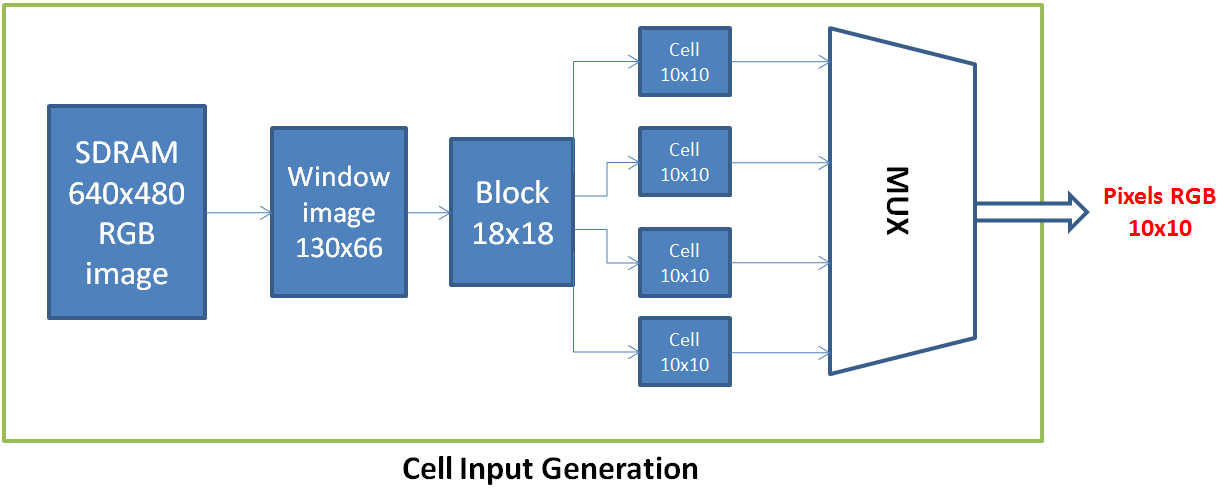
## General Architecture



OUTPUT will be compared with BIAS\_SVM to determine human in current window.

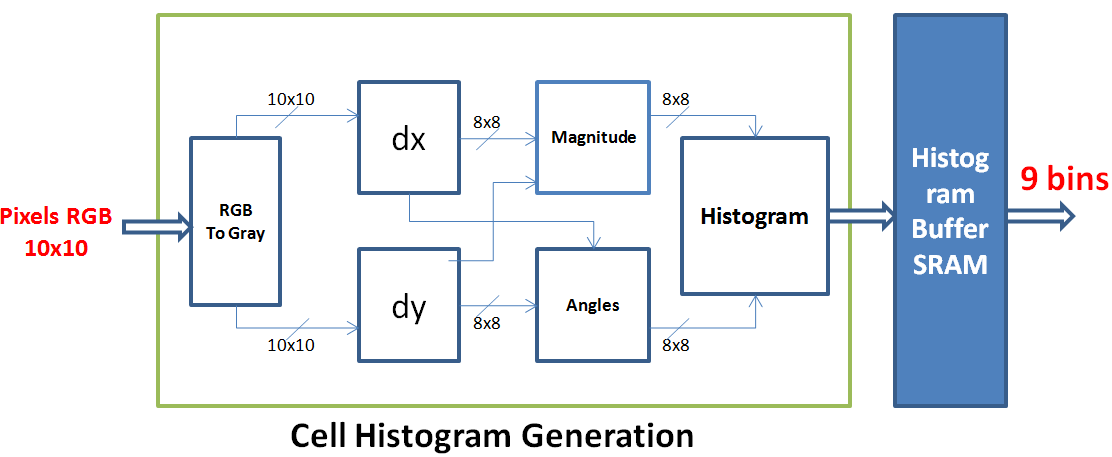
## Cell Input Generation

In the first processing, human detection is showed by these flowcharts:



In **Cell Input Generation,** I scan extend window of 128x64, I scan extend cell of 8x8 later.

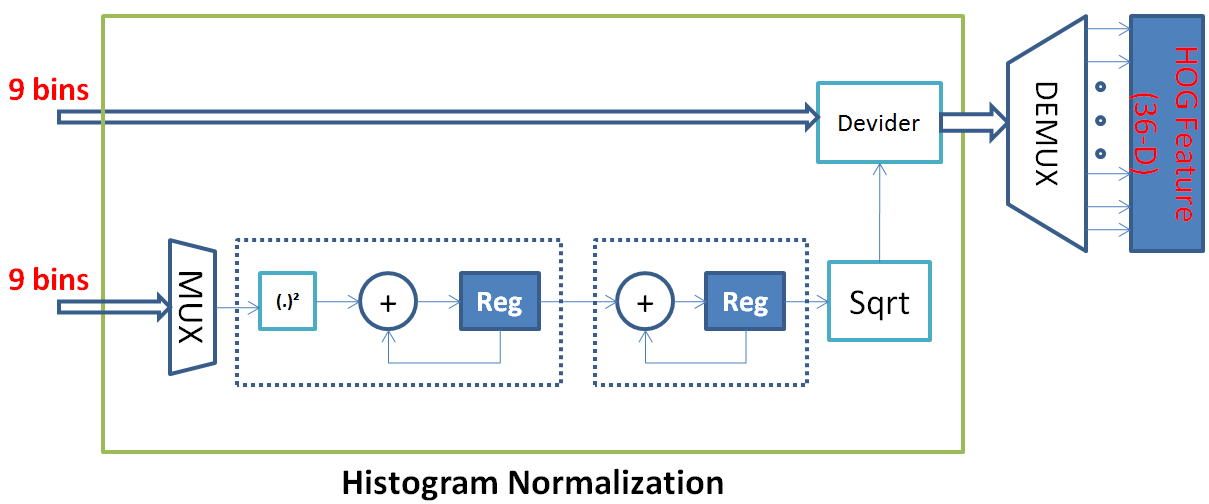
## Cell Histogram Generation



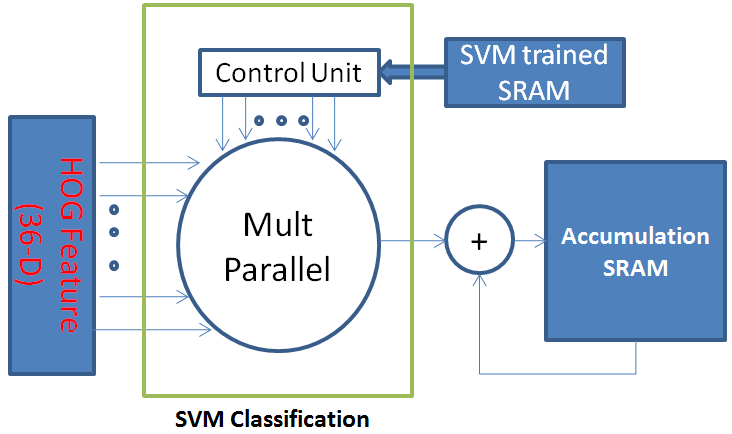
Because I will calculate derivative with respect to x and y, I do not use 8x8 but 10x10.

Then, HOGs are saved **BUFFER.**

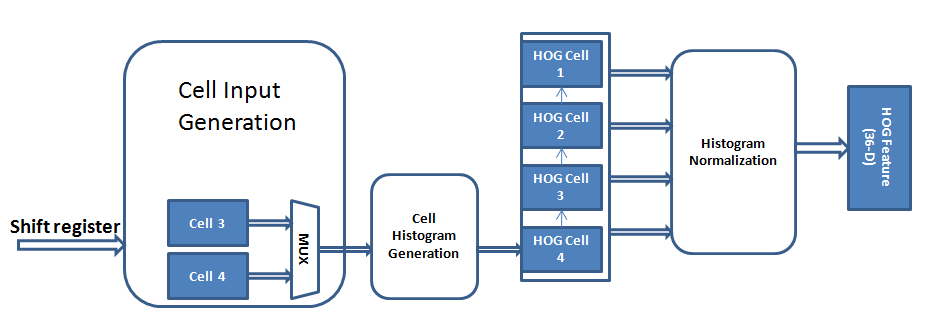
## Histogram Normalization



## SVM Classification



## Processing



The 1st processing, I calculate HOG Cell follow previous flowcharts.

Since the 2nd processing, I just calculate HOG Cell 3 and HOG Cell 4. Similarly, when shift window image, I keep HOG overlapping section and calculate HOG of next section.

# Originality point

I found 3 point to optimization:

## Scan image by shift register

Instead of scan window image and block image as usual, I shift register 8 pixel to pass next window.

## Using LUT (Look Up Table) when calculating magnitude gradient

When calculating magnitude gradient, I realize derivative and derivative usually valued in the range of 0 to 15.

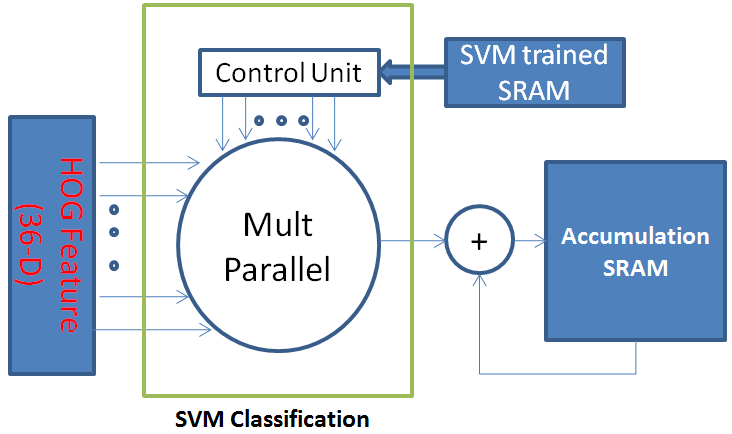
In expression:

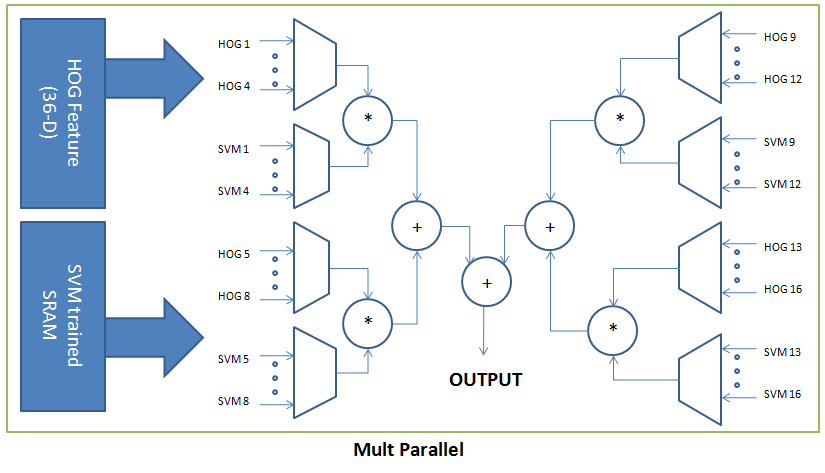
I use LUT to quickly calculate and , and I do not use a multiplier.

Pseudo code:

|  |  |
| --- | --- |
| if < 16  then  = LUT()  else  = | if < 16  then  = LUT()  else  = |

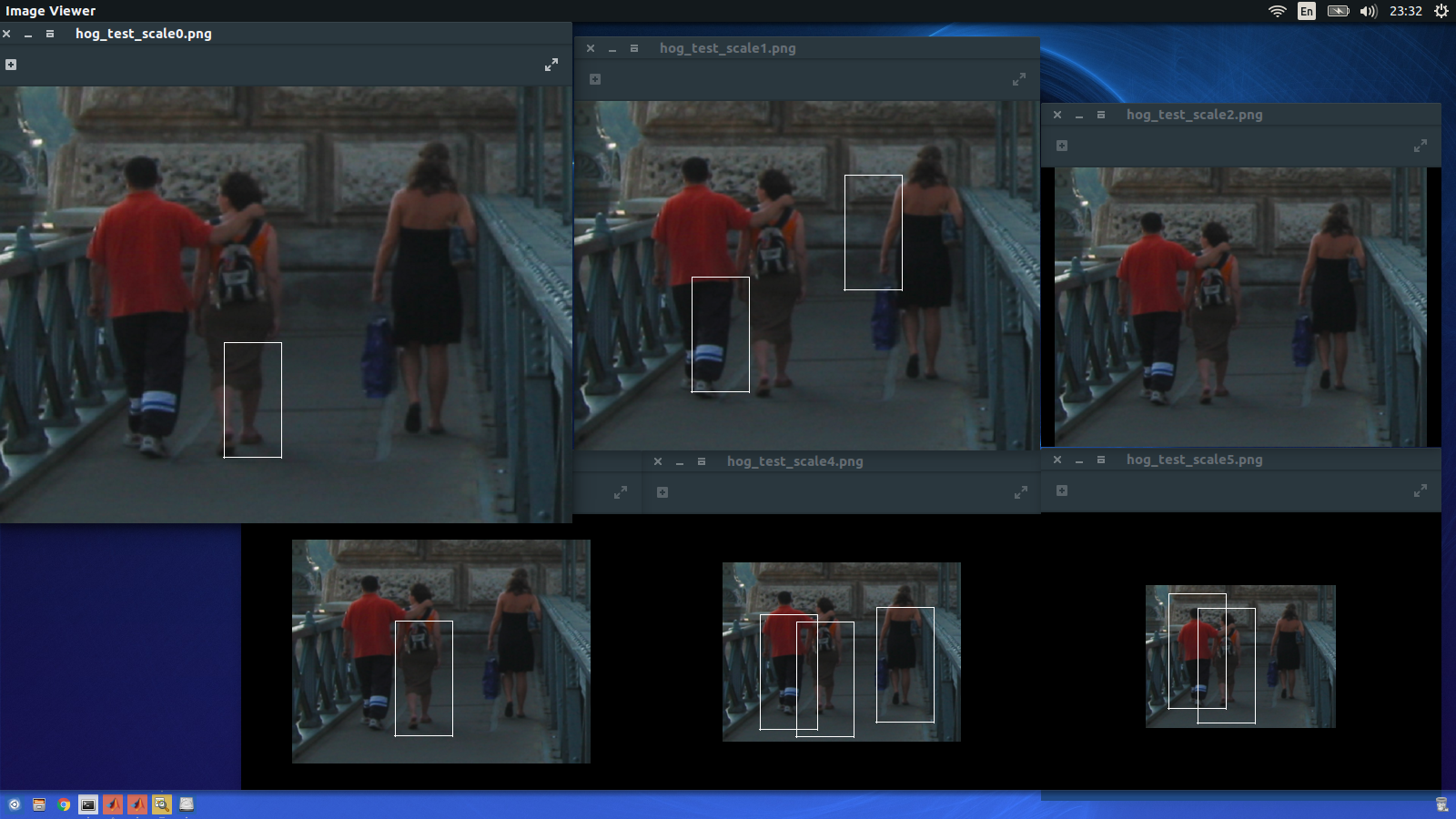
## Calculating SVM Classification by combined serial and parallel





I use 4 **multipliers** to calculate, increase size hardware but decrease timing

# The display of a simulation waveform which the design is operating



# Others

## Acknowledge

I sincerely thank you for my SISLAB (Laboratory for Smart Integrated Systems), especially Tu Teacher and Sinh-Ngoc Nguyen for supporting me in this project.

I do not have enough time to finish this project, but I will try my best if you give me one more chance.