BC-1503

Arquitetura de Computadores

Universidade Federal do ABC

Lógica Digital Binária

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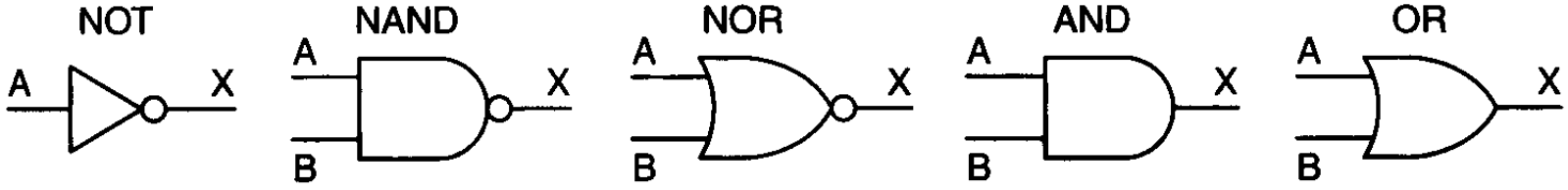
CONTEÚDO PROGRAMÁTICO:

- História e Evolução dos Computadores e Sistemas
- Estrutura de Computadores Digitais
- **Lógica Digital Binária**
- Processamento
- Instruções e linguagem de máquina
- Microprocessadores modernos: pipeline, super escalar, RISC
- Memórias cache e gerenciamento de memórias
- Arquitetura de computadores pessoais
- Arquitetura de Computadores Paralelos
- Sistemas Computacionais: desempenho e confiabilidade

Revisão Circuitos Digitais

PORTAS LÓGICAS E SUAS FUNÇÕES

Portas Lógicas:
- elementos básicos na implementação de circuitos digitais
- álgebra booleana: **George Boole** (1815-1864): Matemático e filósofo inglês
  Criador da álgebra booleana, que possibilitou o vínculo da lógica (filosofia) com a matemática.
- tabela da verdade



A	X
0	1
1	0

(a)

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

(b)

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

(c)

A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

(d)

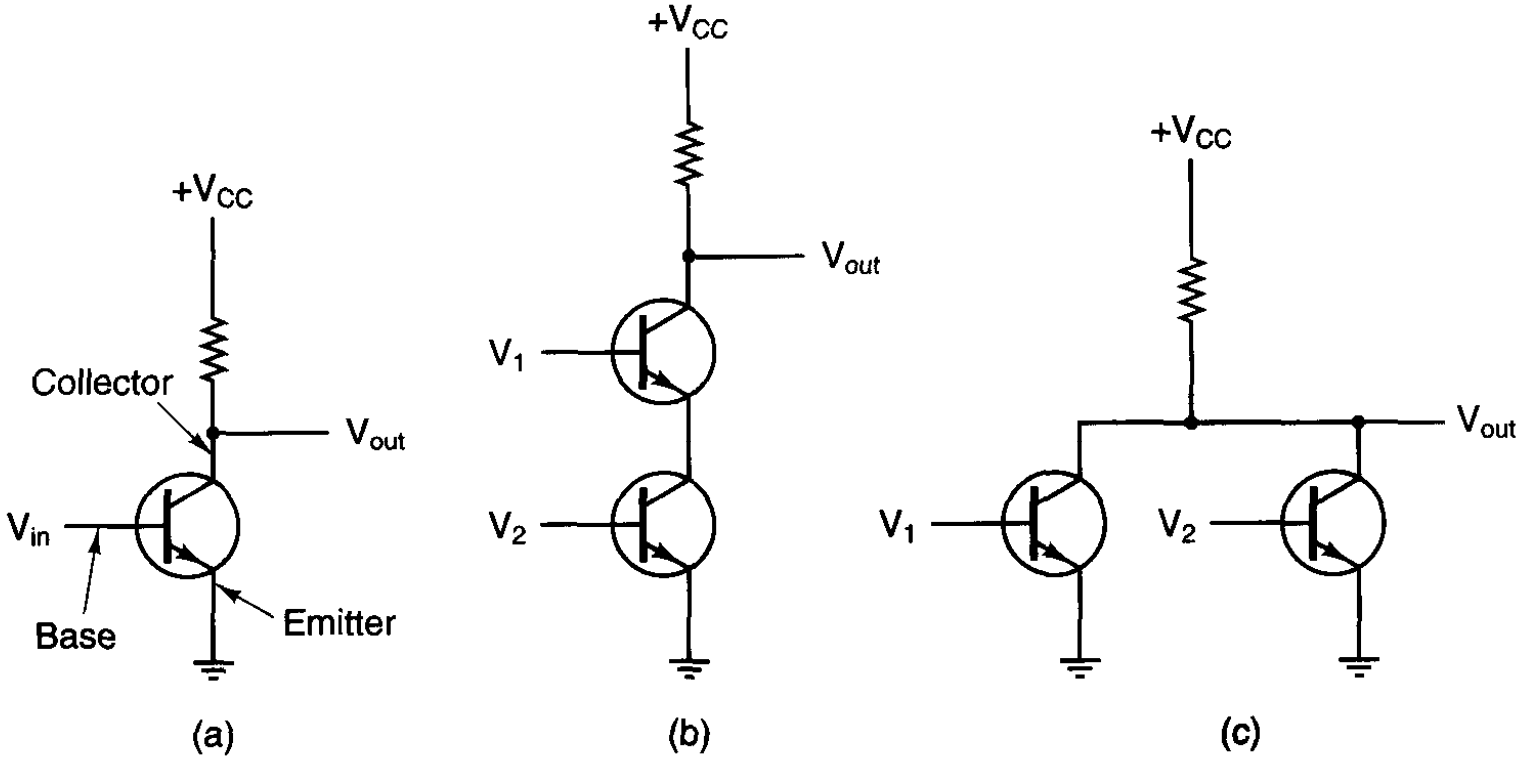
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

(e)

The symbols and functional behavior for the five basic gates.

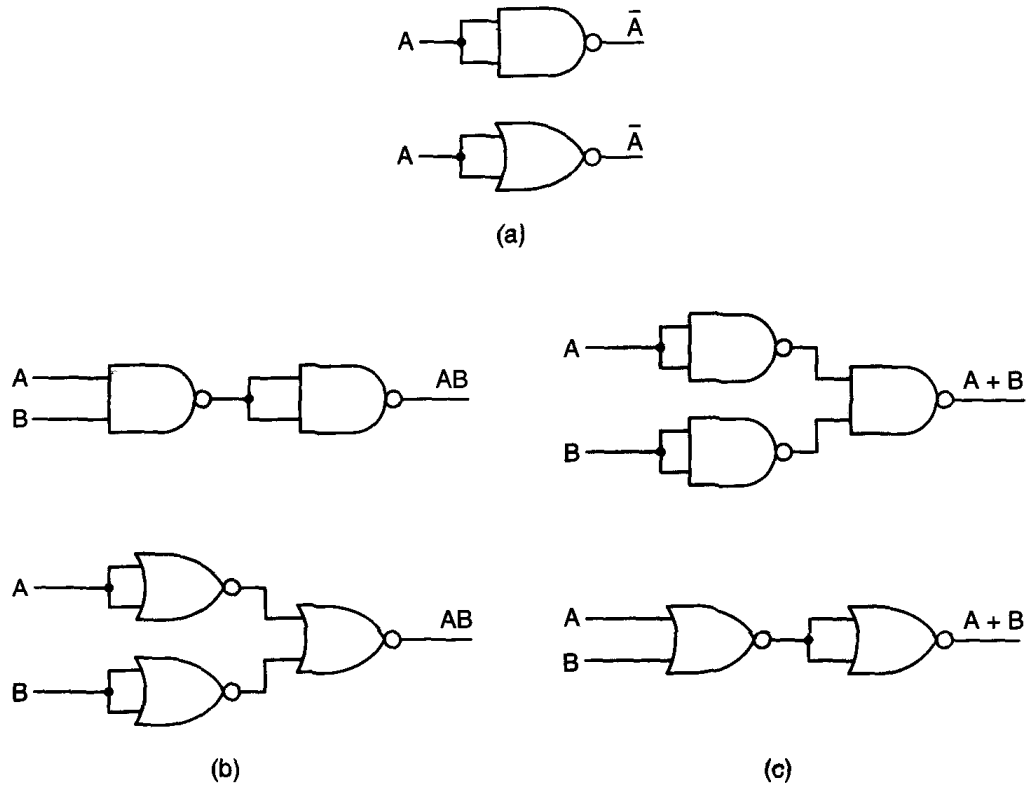
PORTAS LÓGICAS E O TRANSISTOR

Implementação das portas lógicas por transístores



(a) A transistor inverter. (b) A NAND gate. (c) A NOR gate.

CONSTRUÇÕES UTILIZANDO SOMENTE NAND OU NOR

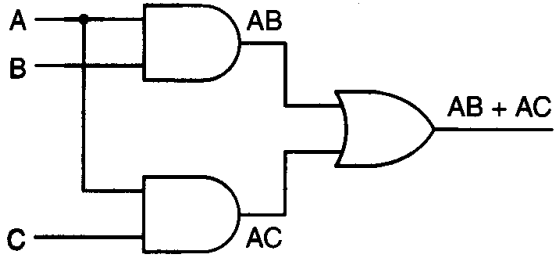


Construction of (a) NOT, (b) AND, and (c) OR gates using only NAND gates or only NOR gates.

Vantagem: utiliza um único tipo de circuito transistorizado

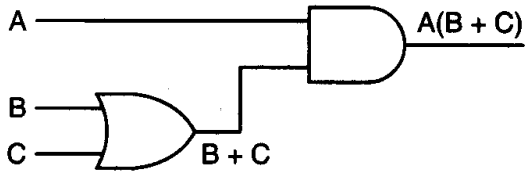
ÁLGEBRA BOOLEANA: EQUIVALÊNCIA DE EQUAÇÕES

Álgebra Booleana: exemplo de equivalência



A	B	C	AB	AC	AB + AC
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	1	1
1	1	0	1	0	1
1	1	1	1	1	1

(a)

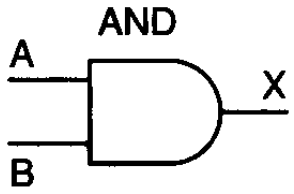


A	B	C	A	B + C	A(B + C)
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	0	1	0
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	1	1	1

(b)

Two equivalent functions. (a) $AB + AC$. (b) $A(B + C)$.

EQUIVALÊNCIA ELETRÔNICA COM A LÓGICA



(a): Implementação AND eletrônica
(b): Equivalente lógico positivo
(c): Equivalente lógico negativo

A	B	F
0V	0V	0V
0V	5V	0V
5V	0V	0V
5V	5V	5V

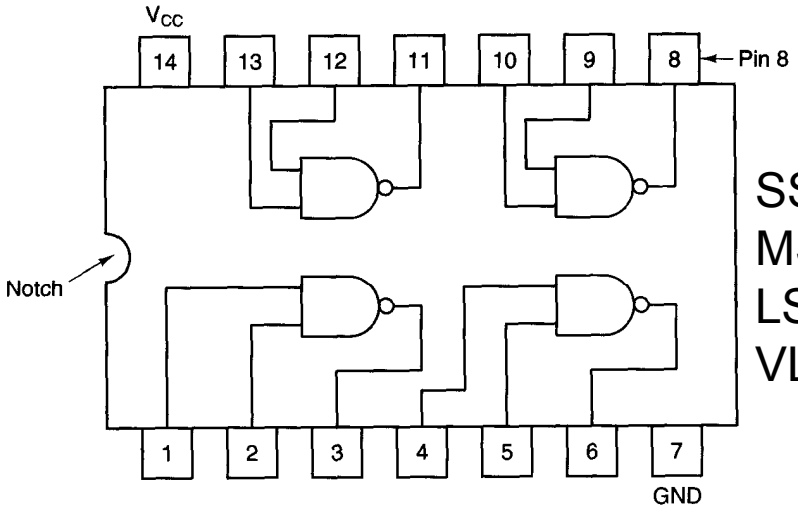
(a)

A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

(b)

A	B	F
1	1	1
1	0	1
0	1	1
0	0	0

(c)



An SSI chip containing four gates.

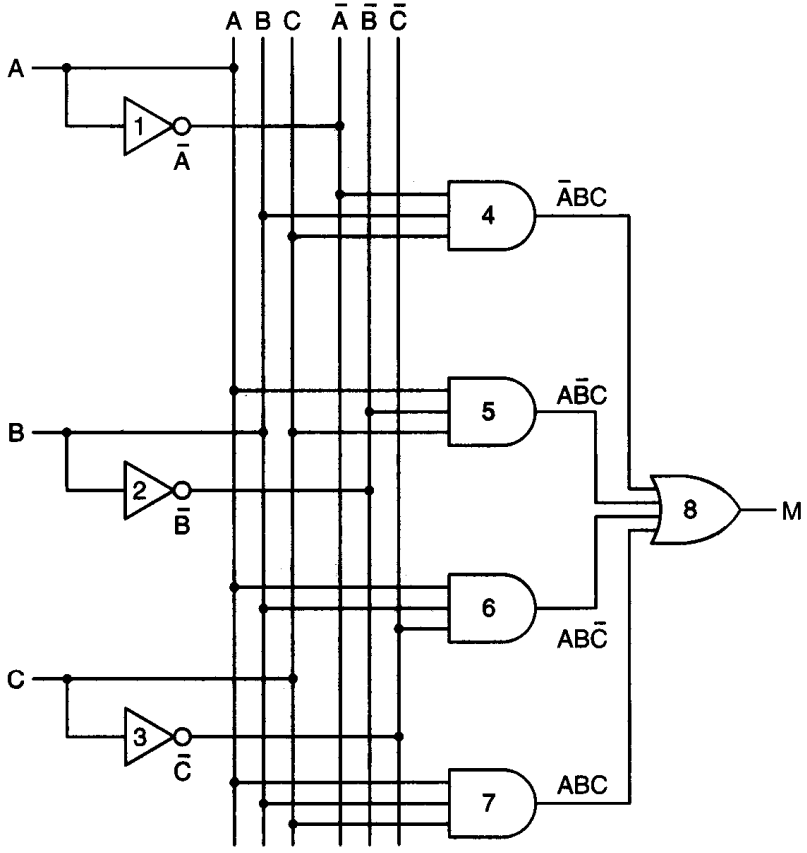
SSI: Small Scale Integrated: 1 a 10 portas
MSI: Medium Scale Integrated: 10 a 100 portas
LSI: Large Scale Integrated: 100 a 100 mil portas
VLSI: Very Large Scale Integrated: >100 mil portas

EXERCÍCIO DE ANÁLISE DE UM CIRCUITO LÓGICO

Identificar a função realizada pelo circuito lógico

A	B	C	M
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

(a)



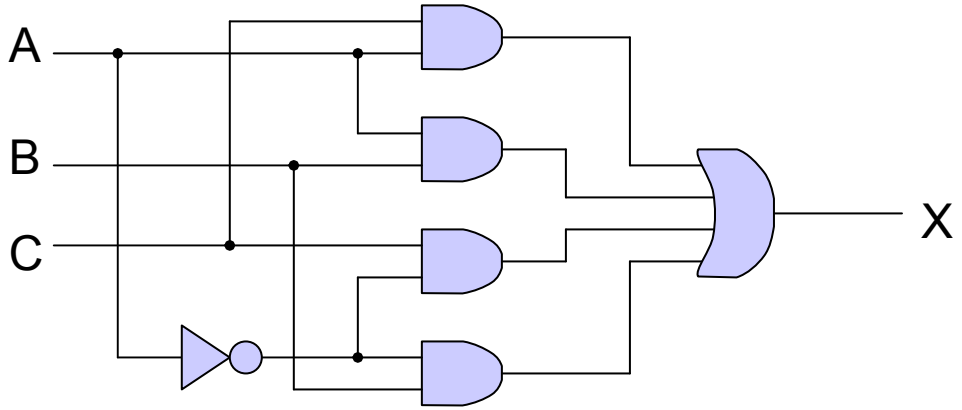
(b)

(a) The truth table for the majority function of three variables.
(b) A circuit for (a).

ÁLGEBRA BOOLEANA: NOTAÇÃO E PROPRIEDADES

Name	AND form	OR form
Identity law	$1A = A$	$0 + A = A$
Null law	$0A = 0$	$1 + A = 1$
Idempotent law	$AA = A$	$A + A = A$
Inverse law	$A\bar{A} = 0$	$A + \bar{A} = 1$
Commutative law	$AB = BA$	$A + B = B + A$
Associative law	$(AB)C = A(BC)$	$(A + B) + C = A + (B + C)$
Distributive law	$A + BC = (A + B)(A + C)$	$A(B + C) = AB + AC$

Exercício de Lógica Booleana



Dado e esquema lógico acima:
- elaborar a Tabela Verdade;
- escrever a equação booleana;
- fatorar / simplificar a equação booleana;
- elaborar novo esquema lógico a partir da equação simplificada
- conferir a Tabela Verdade

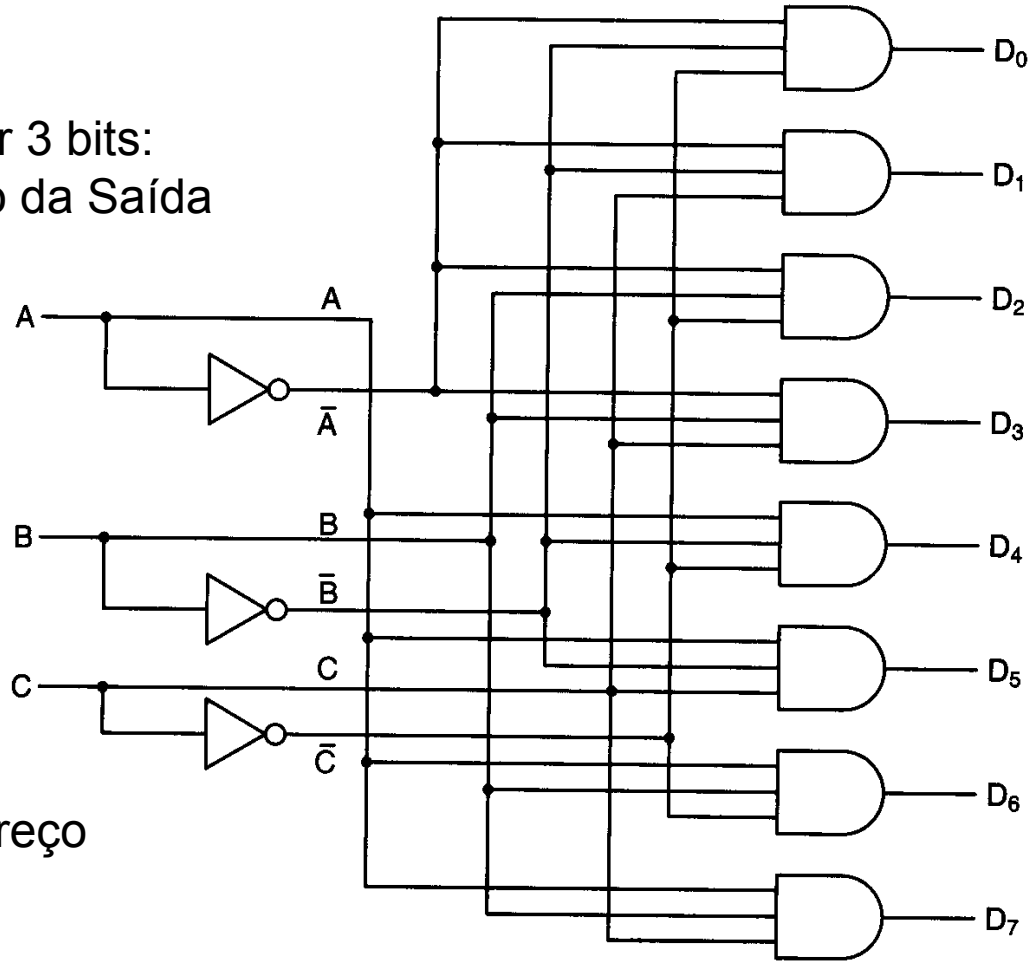
ULA: Unidade Lógica e Aritmética

DECODIFICAÇÃO OU DEMUTIPLEXADOR

Exemplo: Decodificador 3 bits:
Capacidade de seleção da Saída

A	B	C	Saídas
0	0	0	D0 = 1
0	0	1	D1 = 1
...	...	...	
1	1	1	D7 = 1

Decodificação de endereço de memória

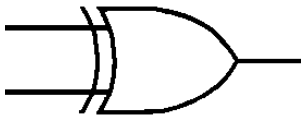


A 3-to-8 decoder circuit.

IMPLEMENTAÇÕES DO XOR (OU EXCLUSIVO)

Importante na implementação do Somador Binário

Símbolo XOR

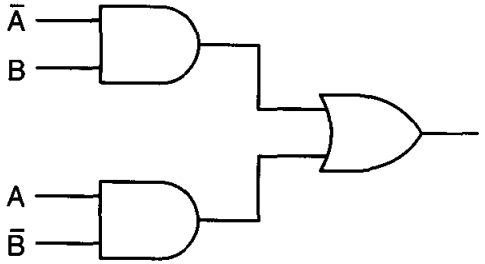


A	B	XOR
0	0	0
0	1	1
1	0	1
1	1	0

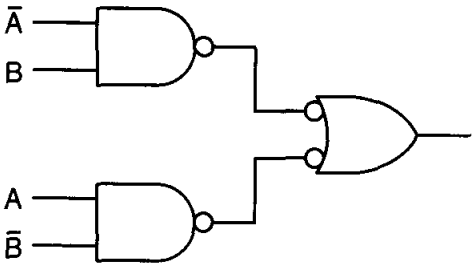
(a)

Bin				Dec	
0	1	0	1	5	A
0	1	1	0	6 +	B
1	0	1	1	11	

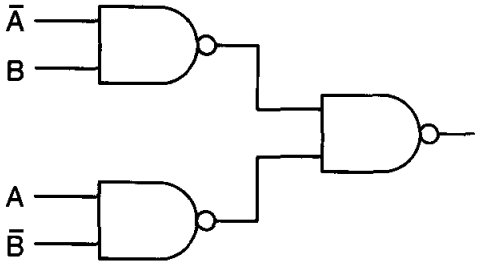
OU exclusivo (Observem a operação!)



(b)



(c)



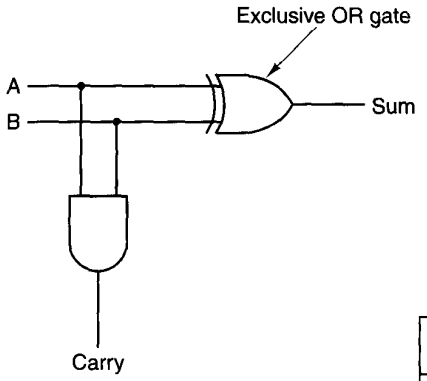
(d)

Possíveis implementações de XOR (verificar)

IMPLEMENTAÇÃO DE ALGUMAS OPERAÇÕES DA ULA

Operação Somador Binário

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

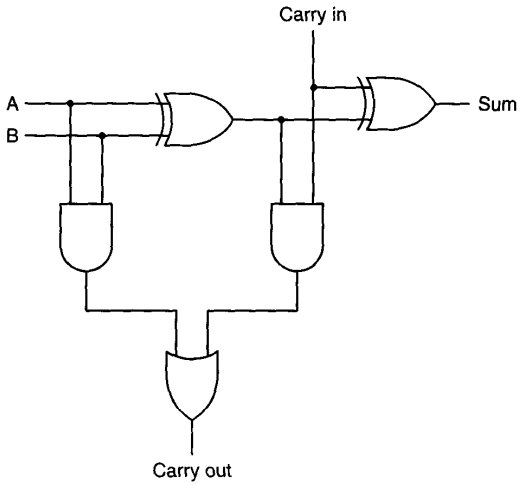


Sem Carry (vai-um)

Completo:
Com Carry (vai-um)

A	B	Carry in	Sum	Carry out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

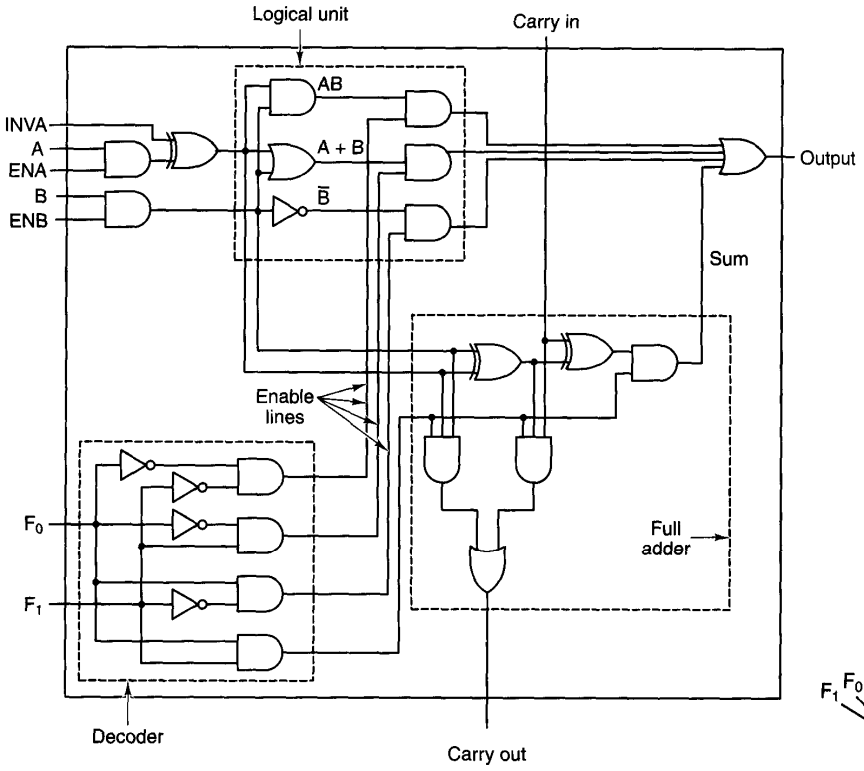
(a)



(b)

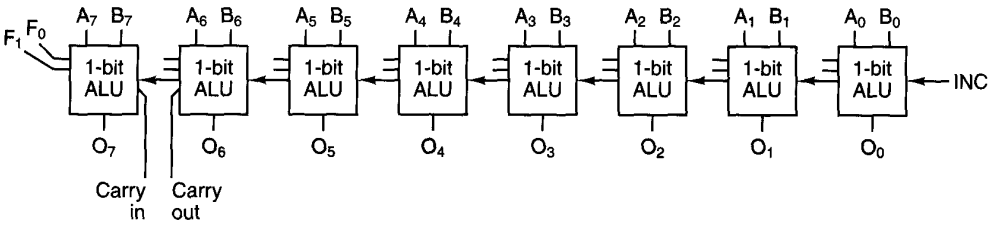
(a) Truth table for full adder. (b) Circuit for a full adder.

IMPLEMENTAÇÃO DE UM BIT DA ULA, COM ALGUMAS OPERAÇÕES



A 1-bit ALU.

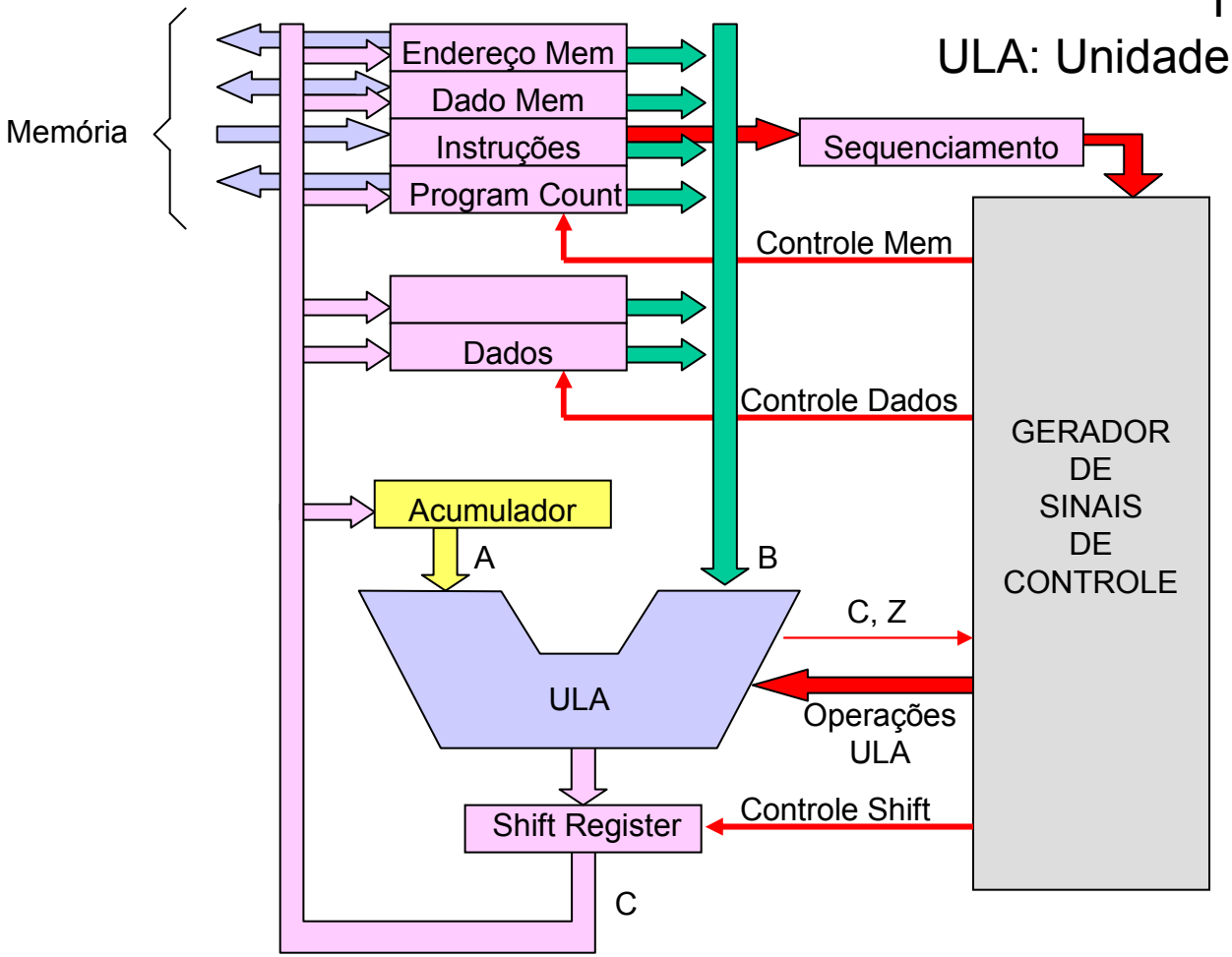
IMPLEMENTAÇÃO DE ULA DE 8 BITs



Eight 1-bit ALU slices connected to make an 8-bit ALU. The enables and invert signals are not shown for simplicity.

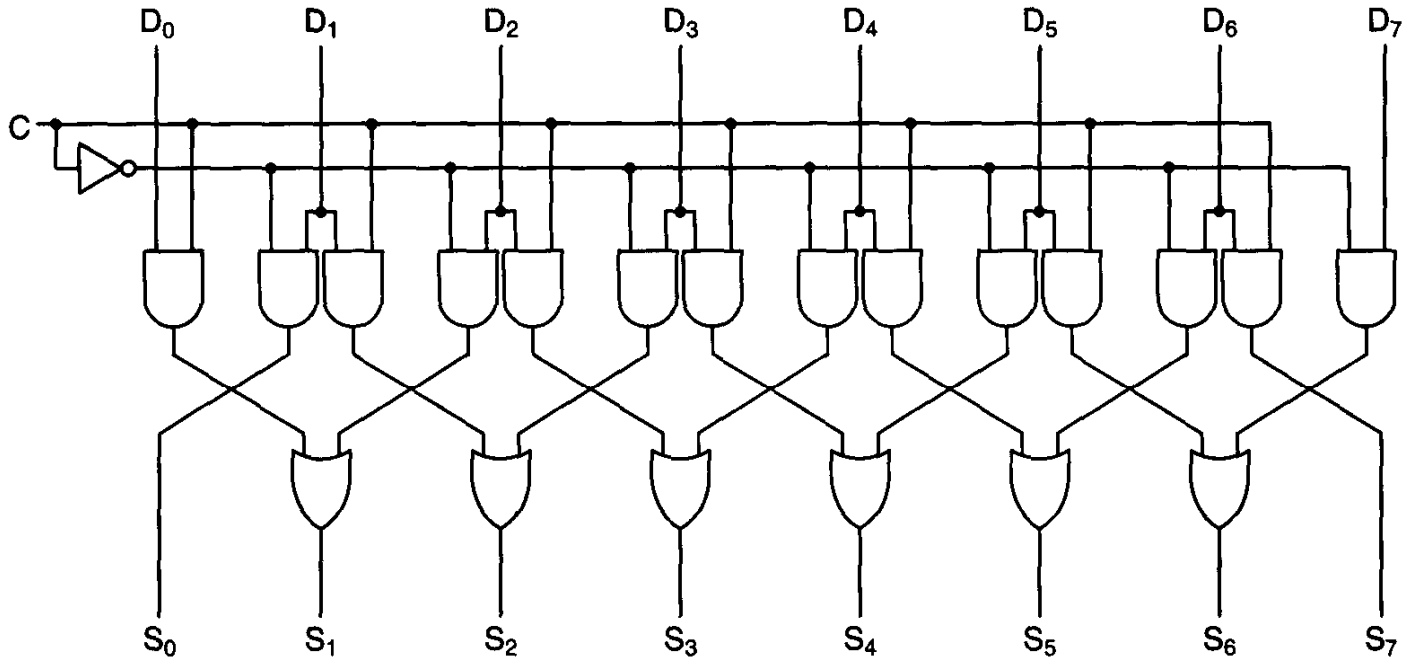
PROCESSAMENTO E A ULA

Estrutura Interna do Processador:
Típica von Neumann
ULA: Unidade Lógica Aritmética



IMPLEMENTAÇÃO DE ALGUMAS OPERAÇÕES DA ULA

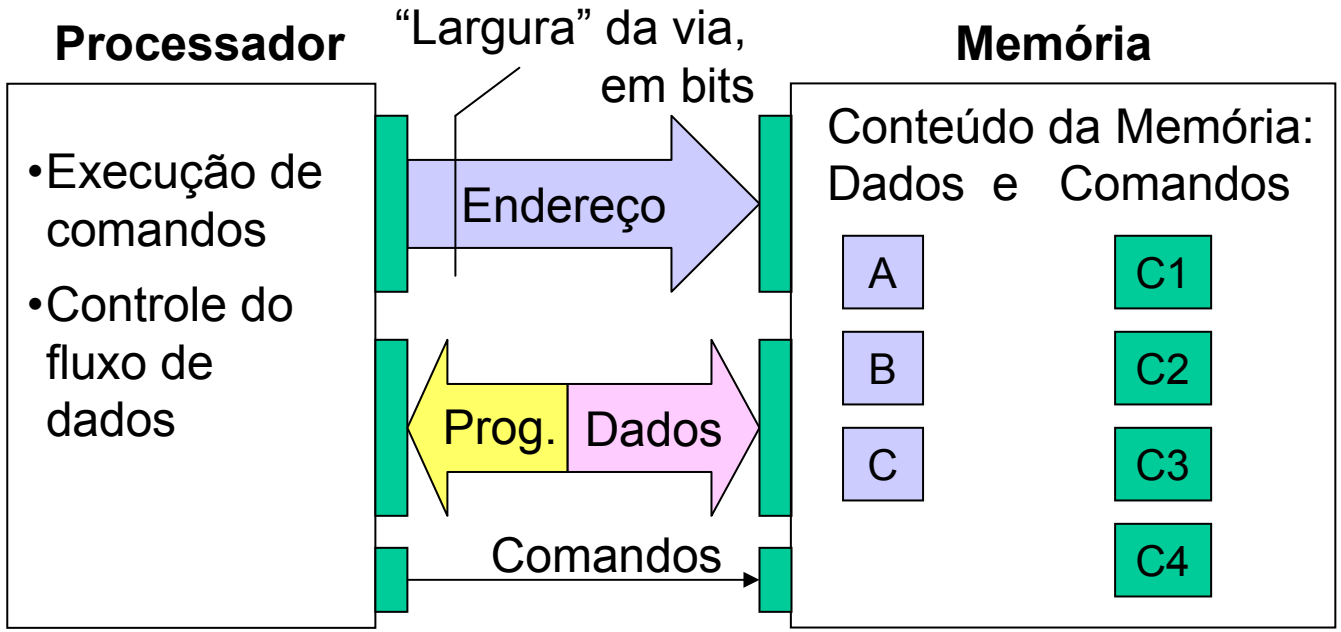
Deslocamento e Rotação (Shift) à esquerda e à direita



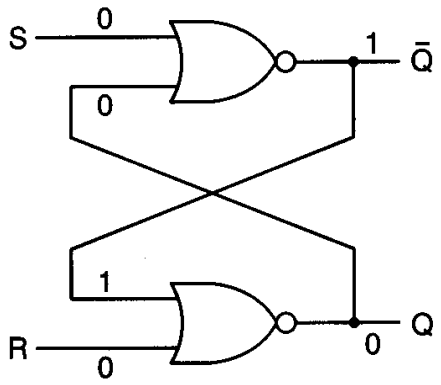
A 1-bit left/right shifter.

MEMÓRIA

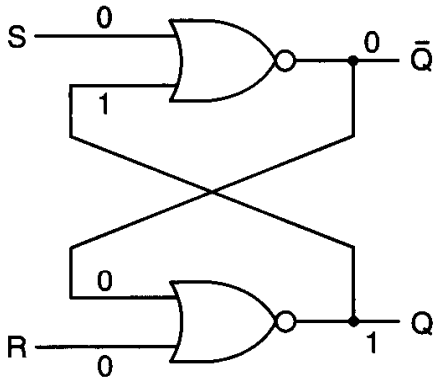
PROCESSAMENTO E A MEMÓRIA



IMPLEMENTAÇÃO DA MEMÓRIA: LATCHES



(a)

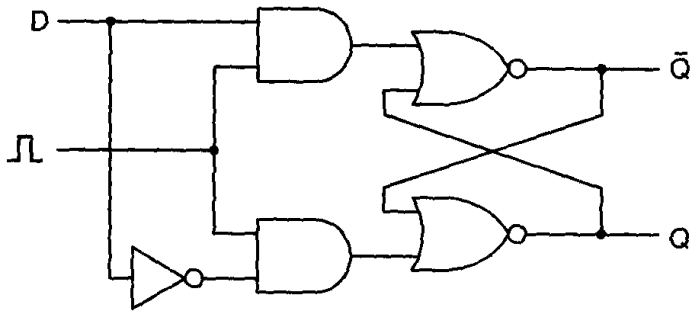


(b)

A	B	NOR
0	0	1
0	1	0
1	0	0
1	1	0

(c)

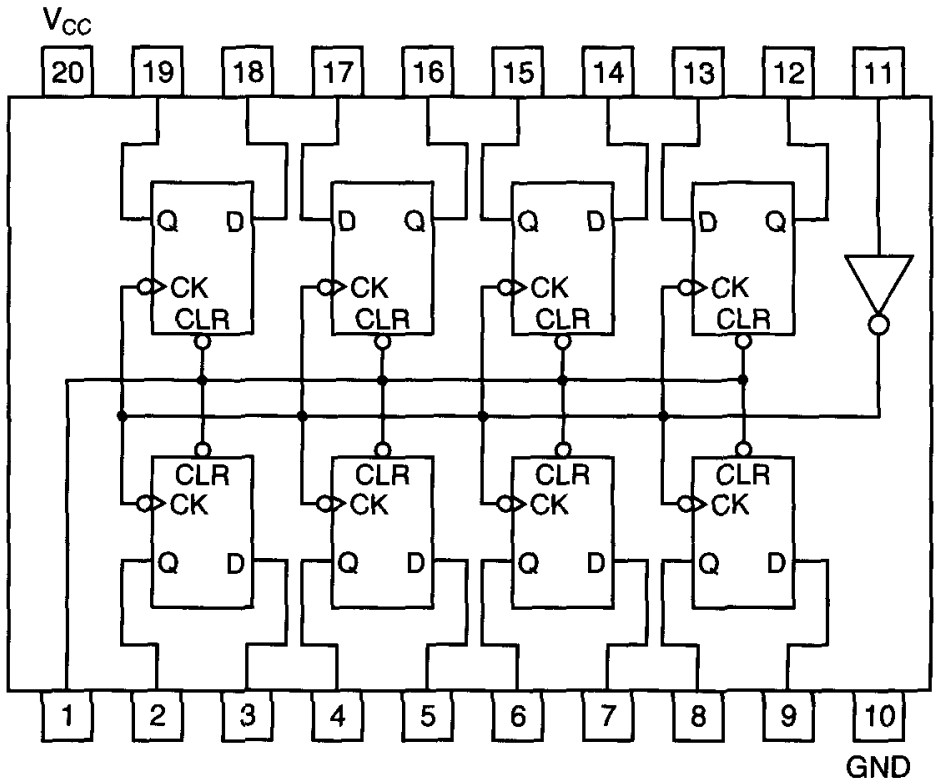
(a) NOR latch in state 0. (b) NOR latch in state 1. (c) Truth table for NOR.



A clocked D latch.

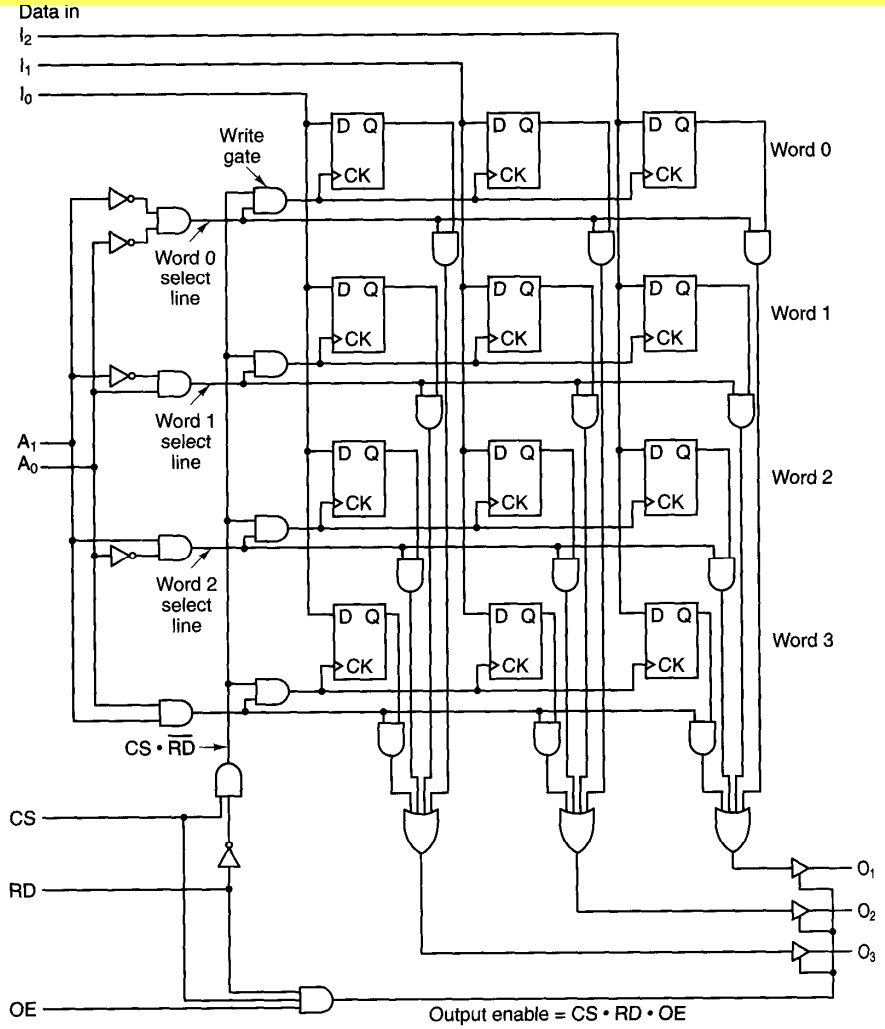
Flip-flop, com pulso de relógio (clock)

IMPLEMENTAÇÃO DA MEMÓRIA: EXEMPLO DE CI ELEMENTAR



Octal flip-flop

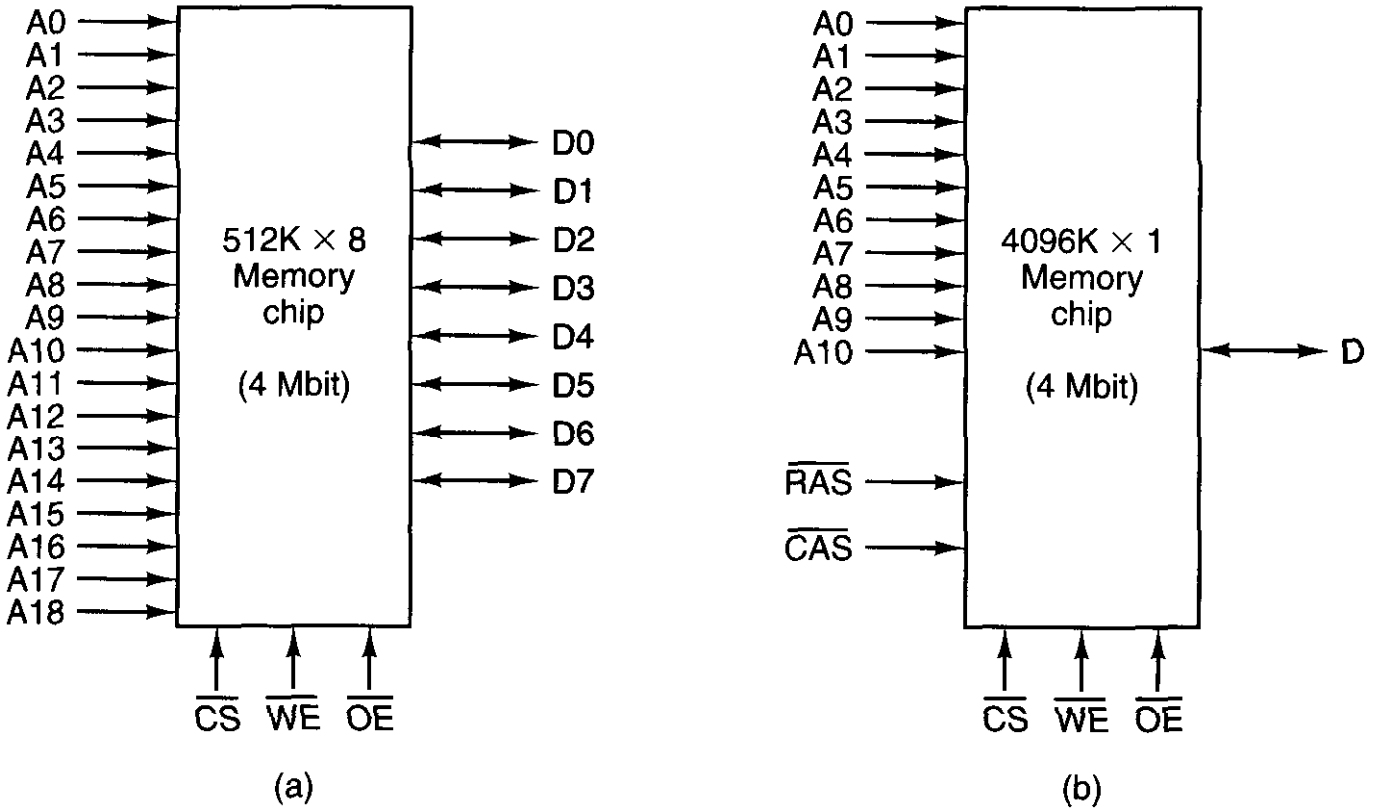
IMPLEMENTAÇÃO DA MEMÓRIA: EXEMPLO 4 X 3



Logic diagram for a 4 × 3 memory. Each row is one of the four 3-bit words. A read or write operation always reads or writes a complete word.

Memória contendo:
- 4 palavras (words)
- 3 bits por palavra
- endereços: A0 e A1
- sinais de controle

ORGANIZAÇÃO DE UM CI DE MEMÓRIA REAL DE 4 MEGA

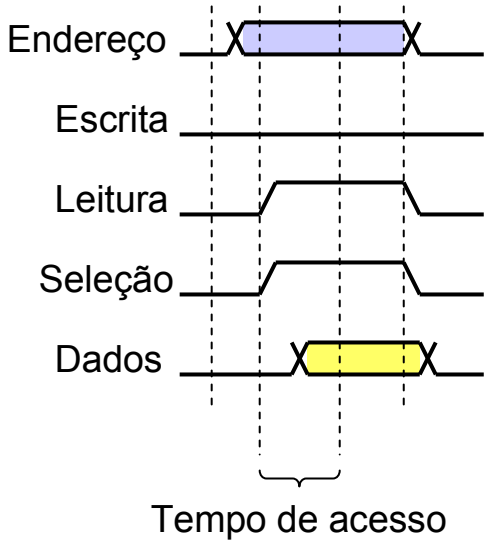


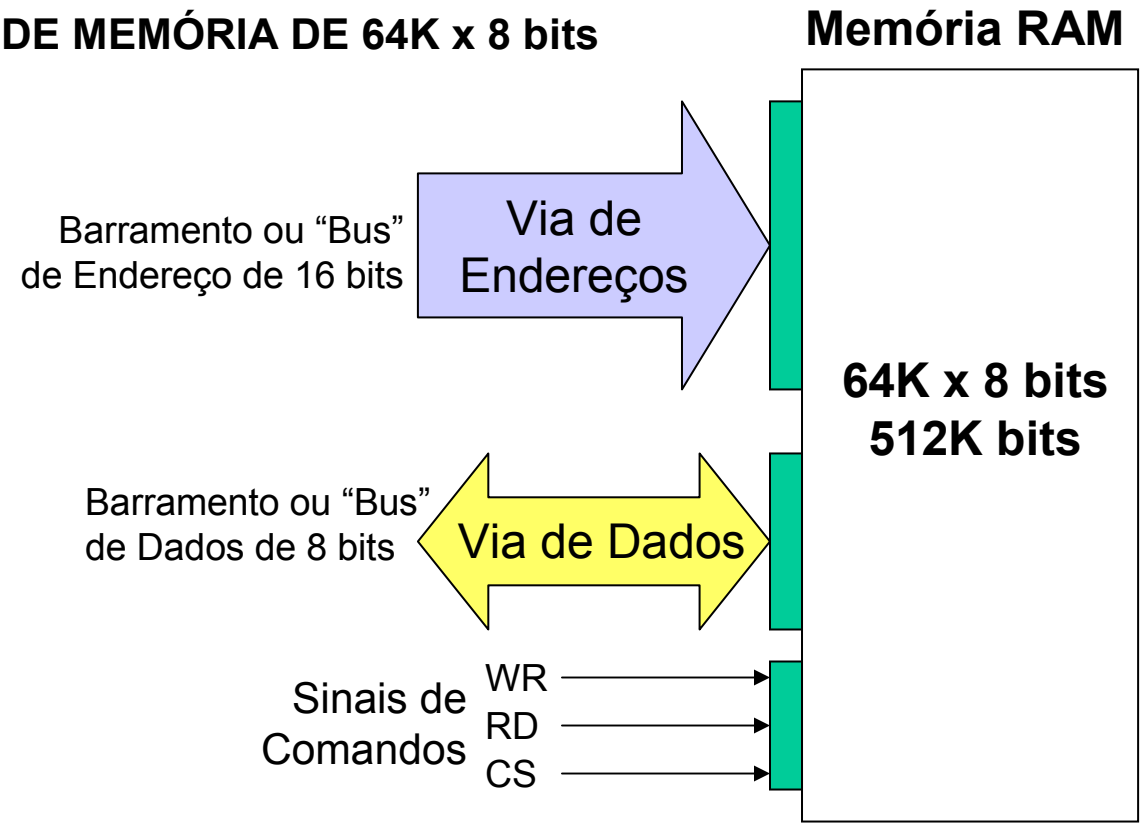
Two ways of organizing a 4-Mbit memory chip.

ACESSOS AO CI DE MEMÓRIA

EXEMPLO DE MEMÓRIA DE 64K x 8 bits

Diagrama de Tempos:
Leitura da Memória

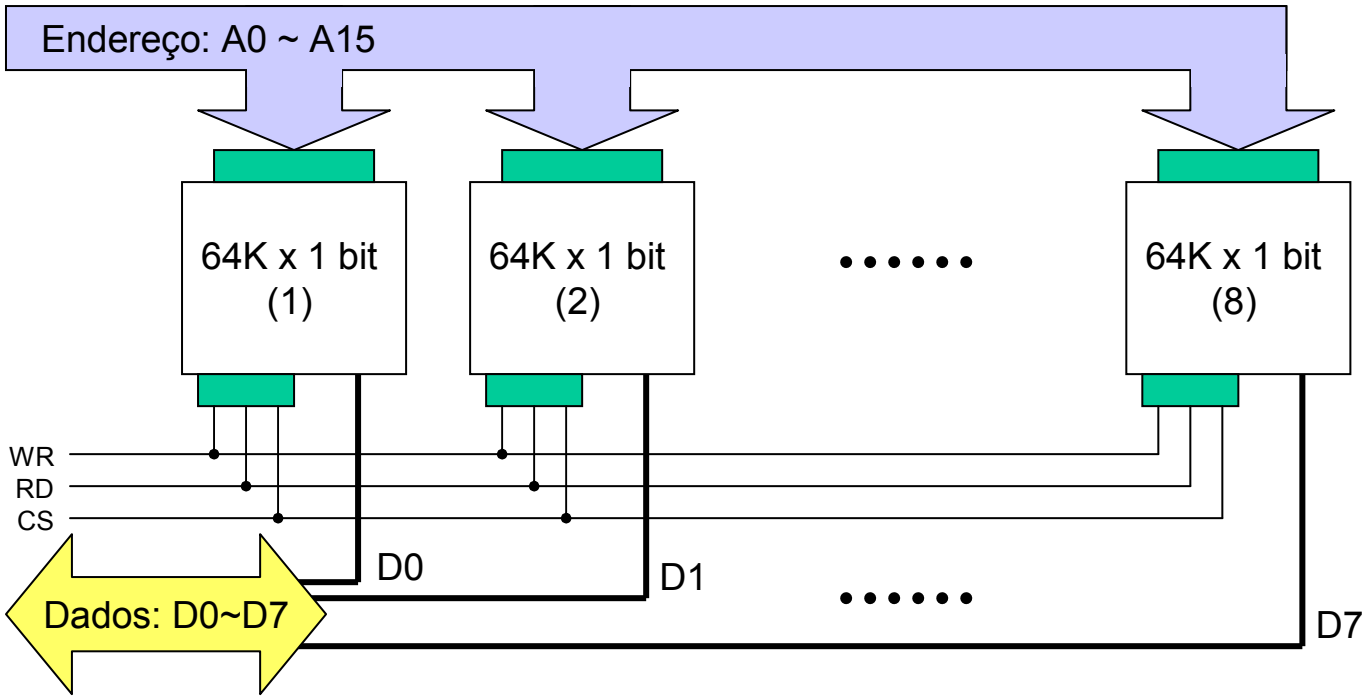




WR: Escrita (write)
RD: Leitura (read)
CS: Seleção (chip select)

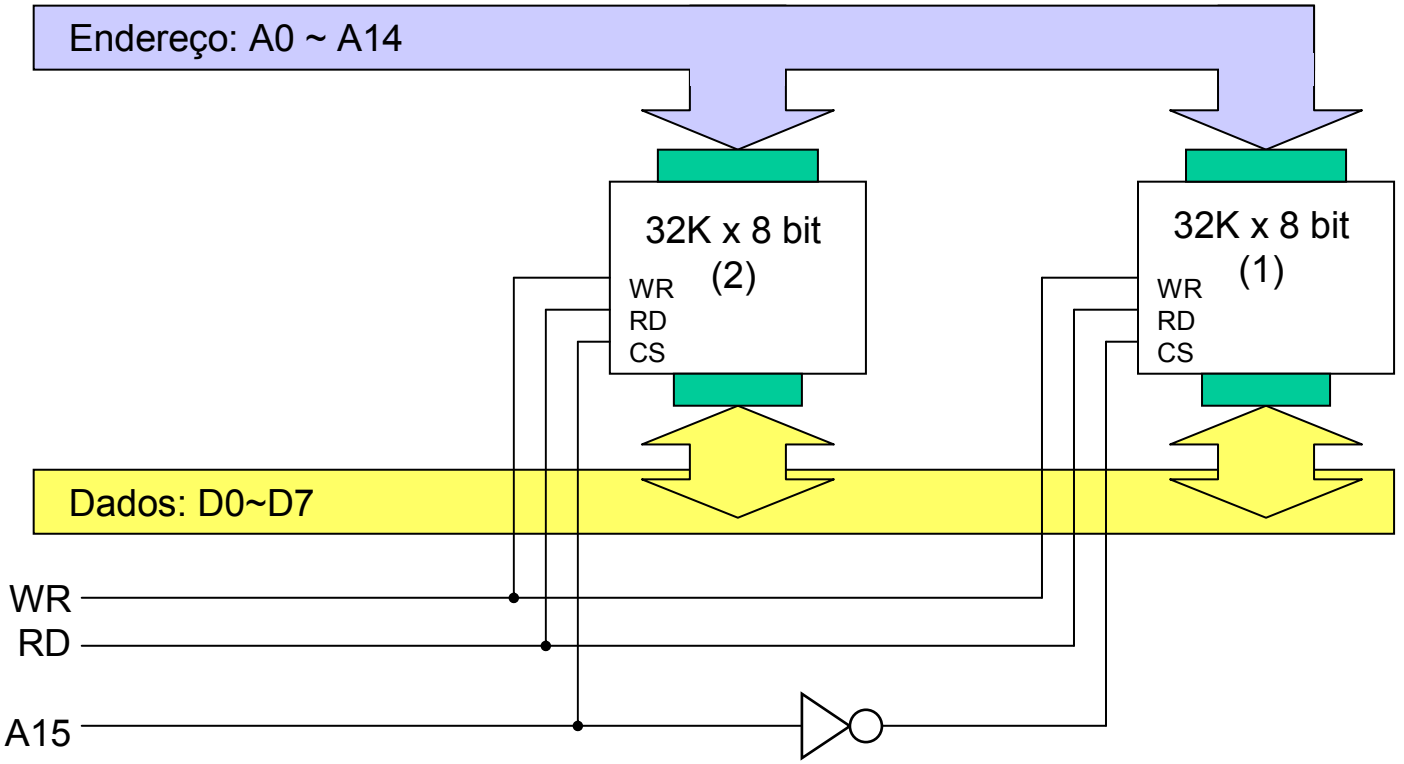
CONFIGURAÇÃO PARA MÚLTIPLOS CHIPS (1)

EXEMPLO PARA 8 CIs DE 64K x 1 bit: TOTAL 64K Bytes



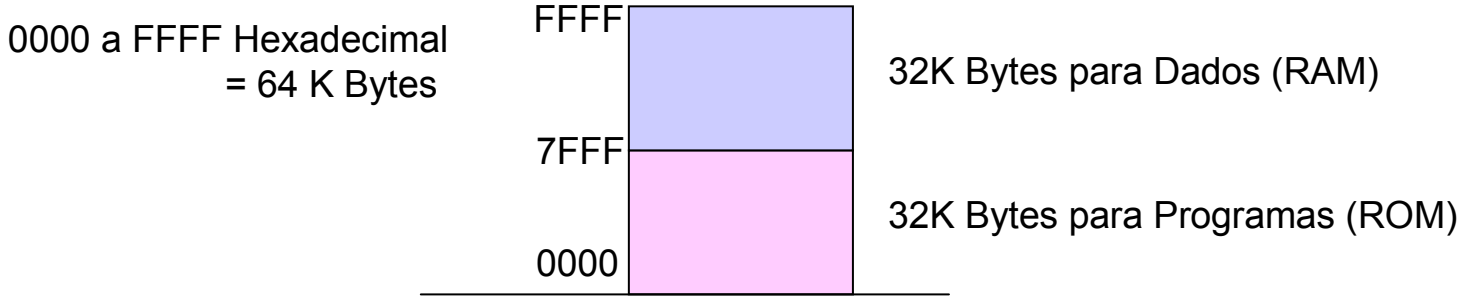
CONFIGURAÇÃO PARA MÚLTIPLOS CHIPS (2)

EXEMPLO PARA 2 CIs DE 32K x 8 bit: TOTAL 64K Bytes

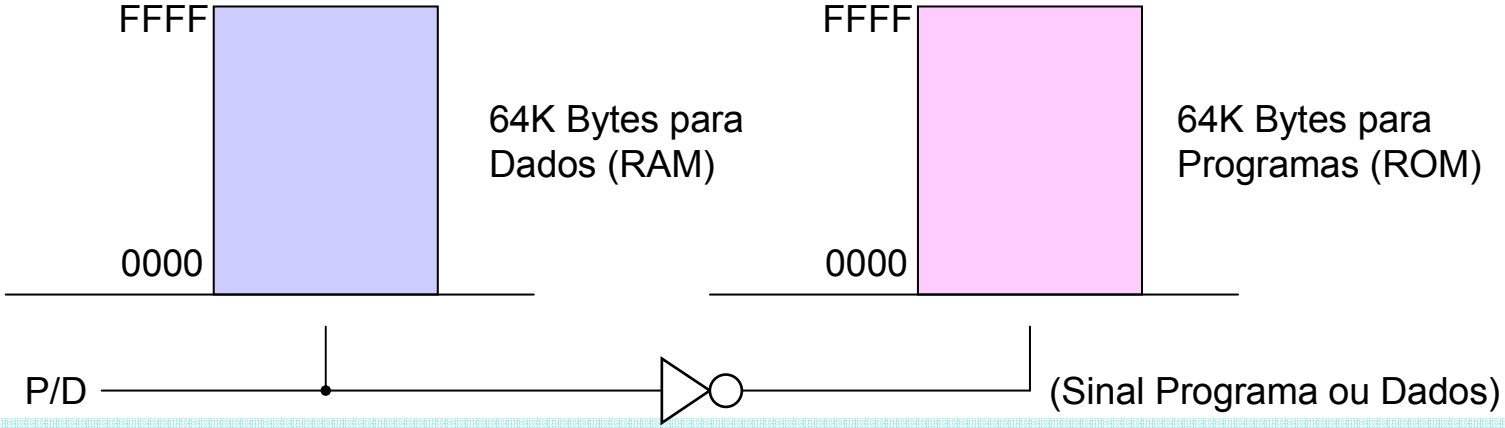


MAPA DE MEMÓRIA

EXEMPLO PARA ÁREA DE MEMÓRIA DE 64K Bytes: DIVISÃO EM PROGRAMAS E DADOS



EXEMPLO PARA ÁREA DE MEMÓRIA DE 64K Bytes: ÁREAS DE PROGRAMAS E DADOS



TIPOS DE MEMÓRIA

Type	Category	Erasure	Byte alterable	Volatile	Typical use
SRAM	Read/write	Electrical	Yes	Yes	Level 2 cache
DRAM	Read/write	Electrical	Yes	Yes	Main memory
ROM	Read-only	Not possible	No	No	Large volume appliances
PROM	Read-only	Not possible	No	No	Small volume equipment
EPROM	Read-mostly	UV light	No	No	Device prototyping
EEPROM	Read-mostly	Electrical	Yes	No	Device prototyping
Flash	Read/write	Electrical	No	No	Film for digital camera

A comparison of various memory types.

Bibliografia:

Tanenbaum, A. S. – **Organização Estruturada de Computadores**. Quinta Edição, Prentice Hall Brasil, 2007