2-) Cache Memory (Block Size)

In this problem, we will compare three direct-mapped caches with approximately the same amount of memory (128 bytes of SRAM):

i-) block size of 4 bytes ⇒ 1 block = 4 bytes = 2 words and $\frac{128}{4} = 32 = 2^5$

ii-) block size of 8 bytes ⇒ 1 block = 8 bytes = 4 words and $128/8 = 2^7/2^3 =$

iii) block size of 64 bytes ⇒ 1 block = 64 bytes = 32 words

1 word = 16-bit = 2 Bytes

Main memory is addressed by 9 bits and data bus is 16 bits.

a-) Fill in the number of bits used for each field od the address for each cache:

	tag	index	Word-0ffset	Byte-offset
i	2-bit	5-bit	1-bit	1-bit
ii	2-bit	4-bit	2-bit	1-bit
iii	2-bit	1-bit	5-bit	1-bit

$128/64 = 2$

2P 3P 3P 2P

b- Assuming a cold start, fill in the "hit" or "miss" for the following sequence of memory references for each cache (addresses are in binary)

Referenced Addresses	i	ii	iii
0 0 0 0 0 0 0 1 0	miss	miss	miss
0 0 0 0 0 0 1 0 0	miss	hit	hit
0 1 0 0 0 1 0 1 0	miss	mis	miss
0 0 0 0 0 0 1 1 1	hit	hit	miss
0 1 1 0 0 1 0 1 0	miss	miss	miss
0 1 0 1 0 1 0 1 0	miss	miss	miss

Tag | Byte offset

6P 6P 6P.

Which cache has the fewest misses for this set of references?

ii-)

00 00 00 01 0 — miss
00 00 00 10 0 — hit
01 00 01 01 0 — mis
00 00 00 11 1 — hit
01 10 01 01 0 — miss
01 01 01 01 0 — miss

Tag | index | Word | Byte

iii)

00 00 00 01 0 — miss
00 00 00 10 0 — hit
01 00 01 01 0 — miss
00 00 00 11 1 — miss
01 10 01 01 0 — miss
01 01 01 01 0 — miss

Tag | word | Byte

↓ Index

Block size of 8 bytes has the fewest misses for this set of references.

1P