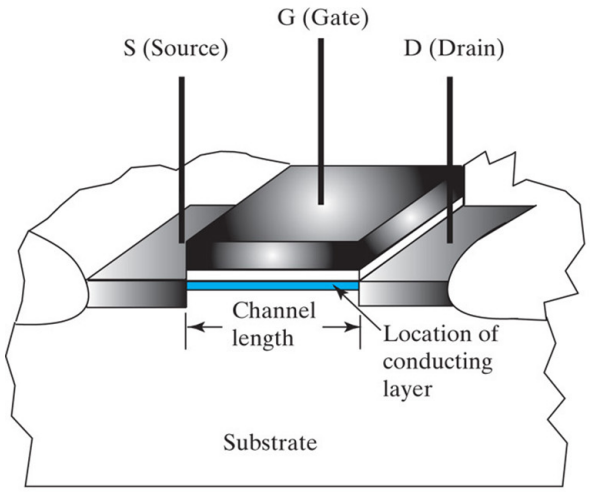
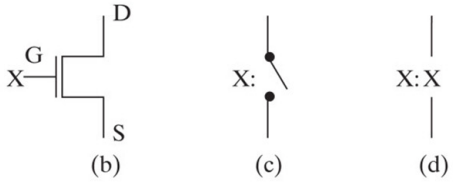
FIGURE 5-1 MOS Transistor, Symbols, and Switch Models

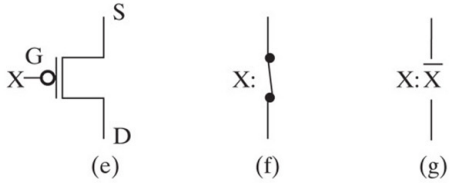


(a) Transistor geometry



(b) (c) (d)

Transistor symbols and models: n-channel



(e) (f) (g)

Transistor symbols and models: p-channel

FIGURE 5-2 Example of Switch Model Circuits

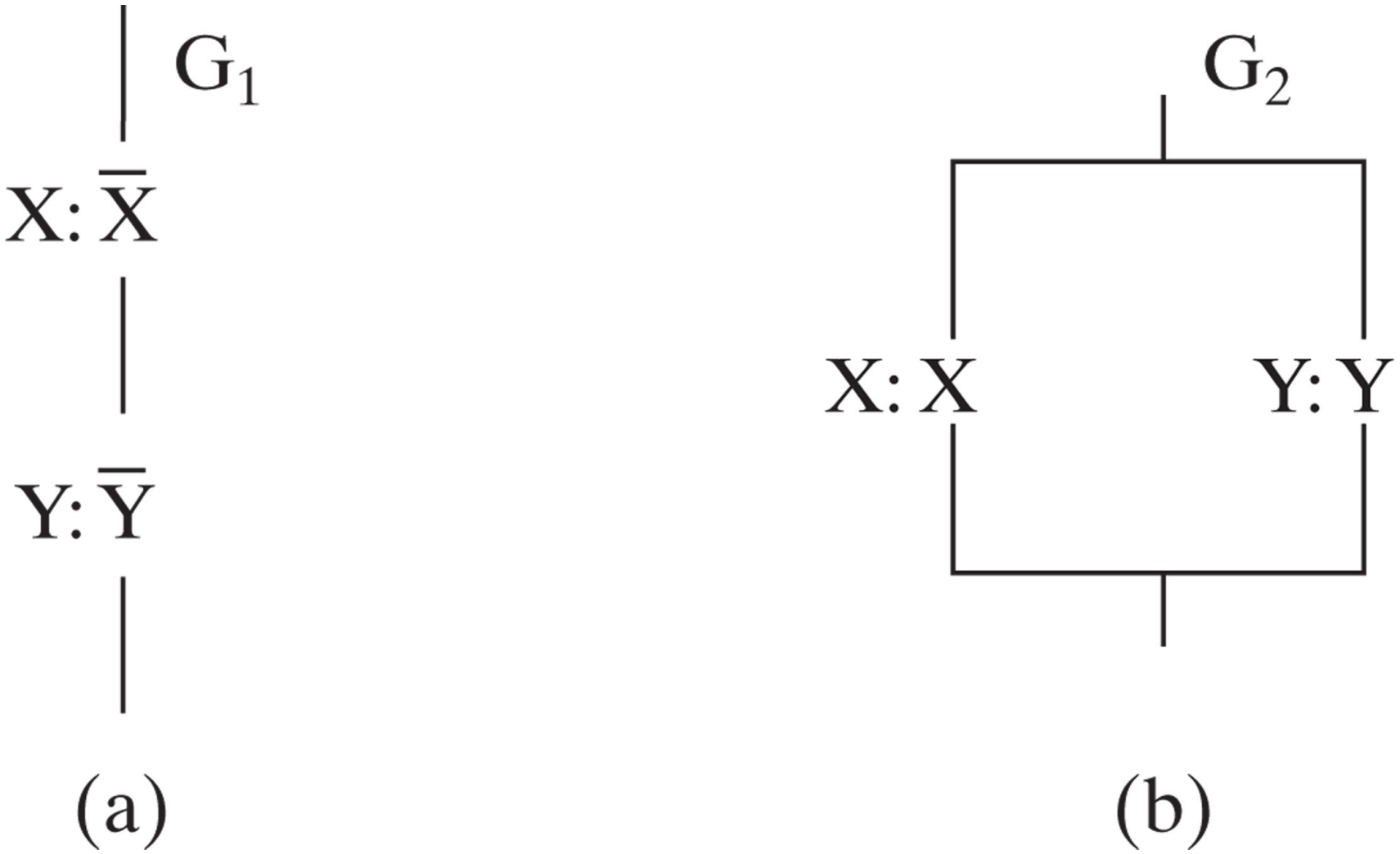


FIGURE 5-3 Fully Complementary CMOS Gate Structure and Examples

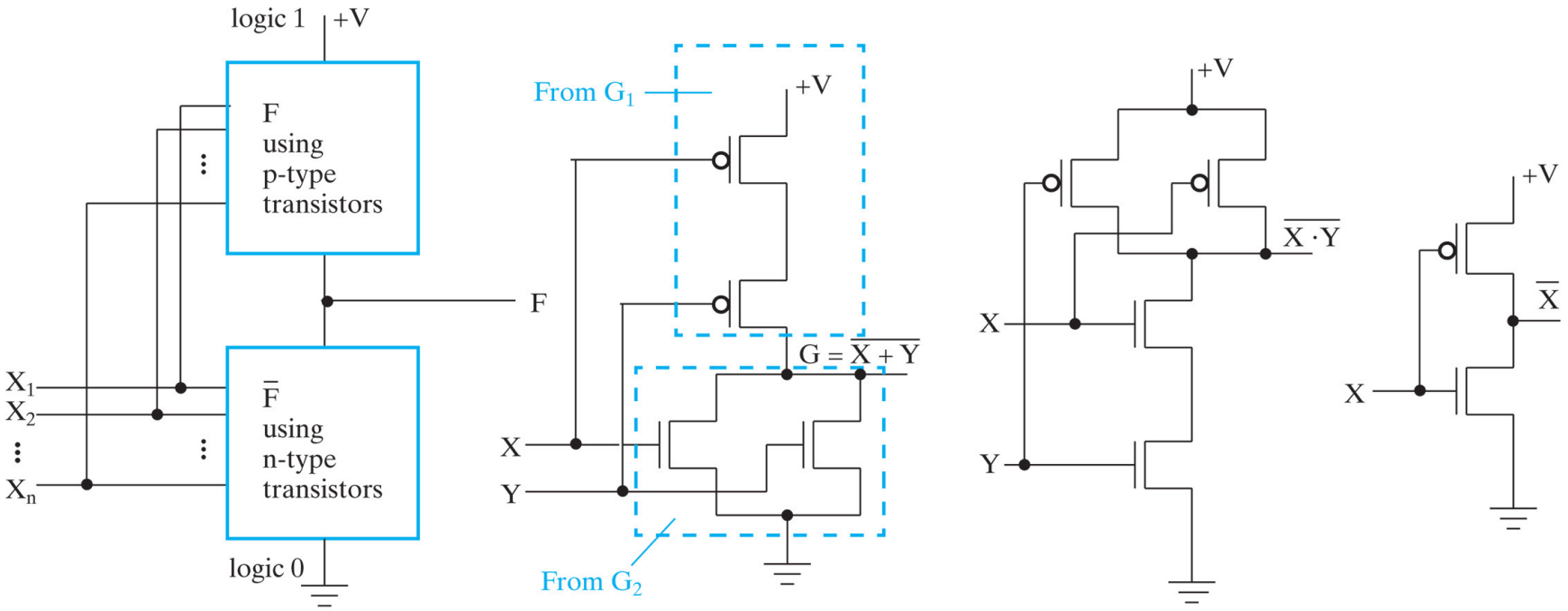


FIGURE 5-4 Implementation of a 7-Input NAND Gate Using NAND Gates with Four or Fewer Inputs

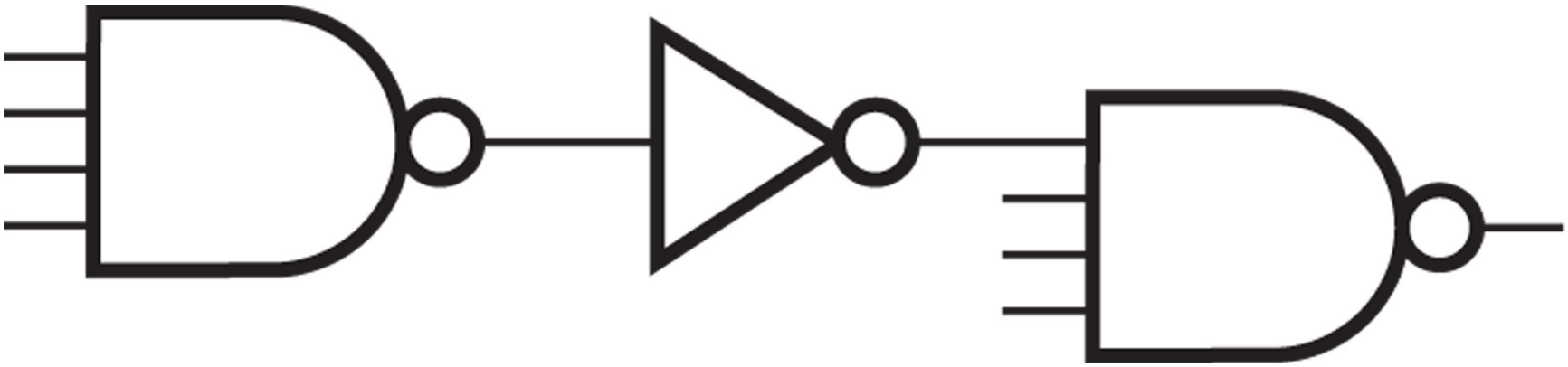
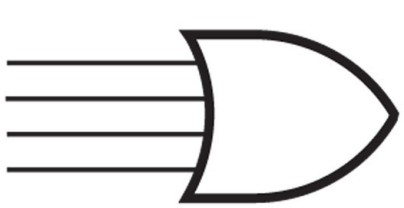
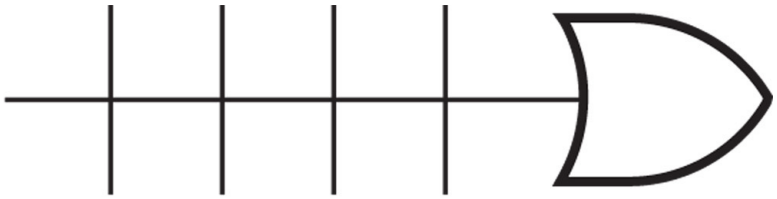


FIGURE 5-5 Conventional and Array Logic Symbols for OR Gate

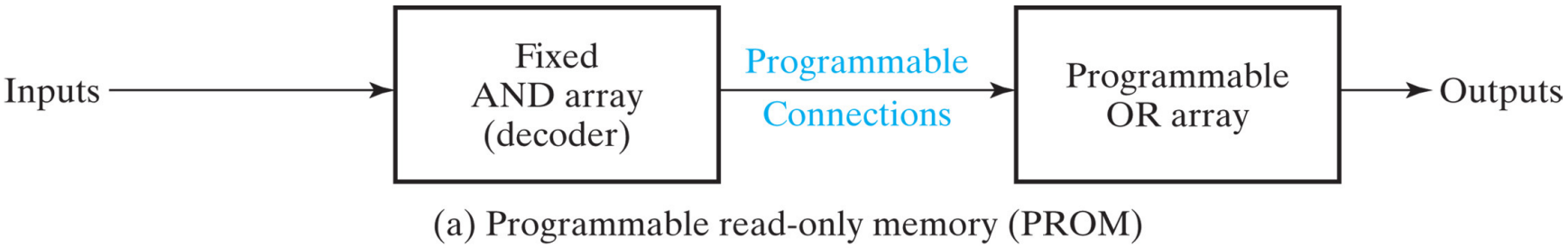


(a) Conventional symbol

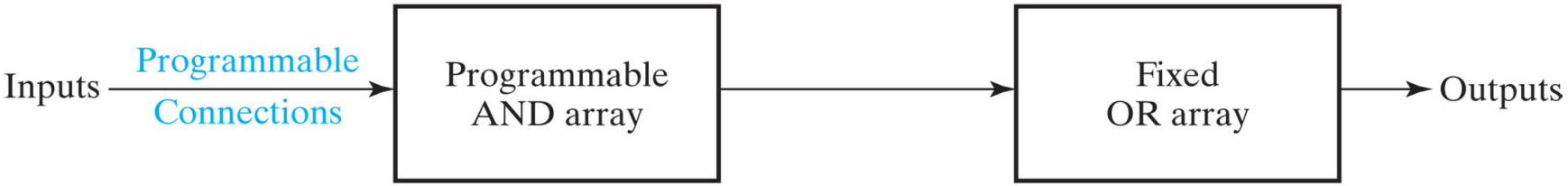


(b) Array logic symbol

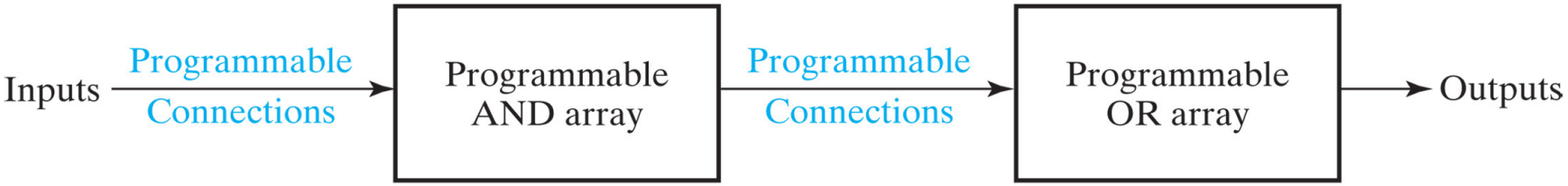
FIGURE 5-6 Basic Configuration of Three PLDs



(a) Programmable read-only memory (PROM)



(b) Programmable array logic (PAL) device



(c) Programmable logic array (PLA) device

FIGURE 5-7 Block Diagram and Internal Logic of a ROM

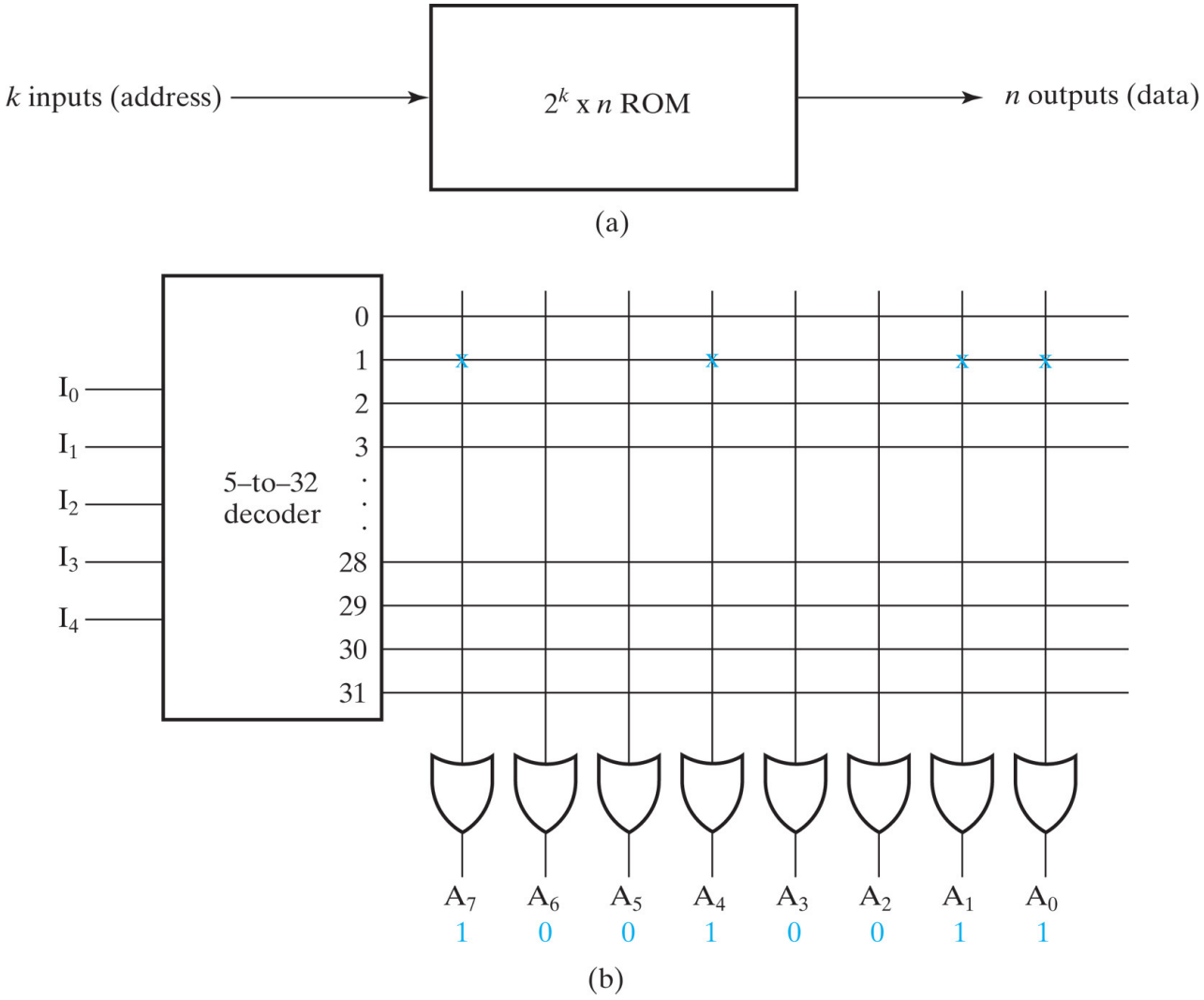


FIGURE 5-8 PLA with Three Inputs, Four Product Terms, and Two Outputs

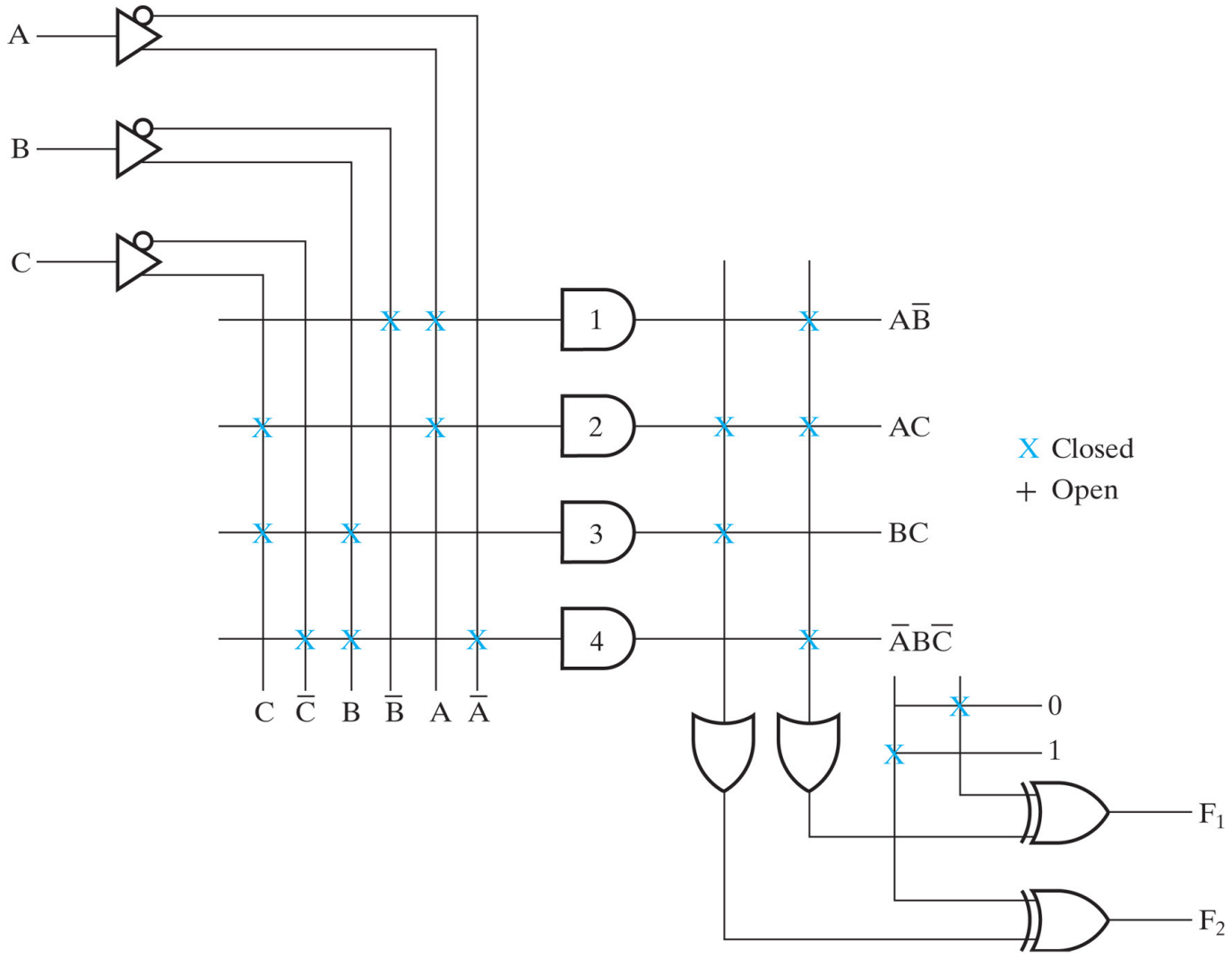
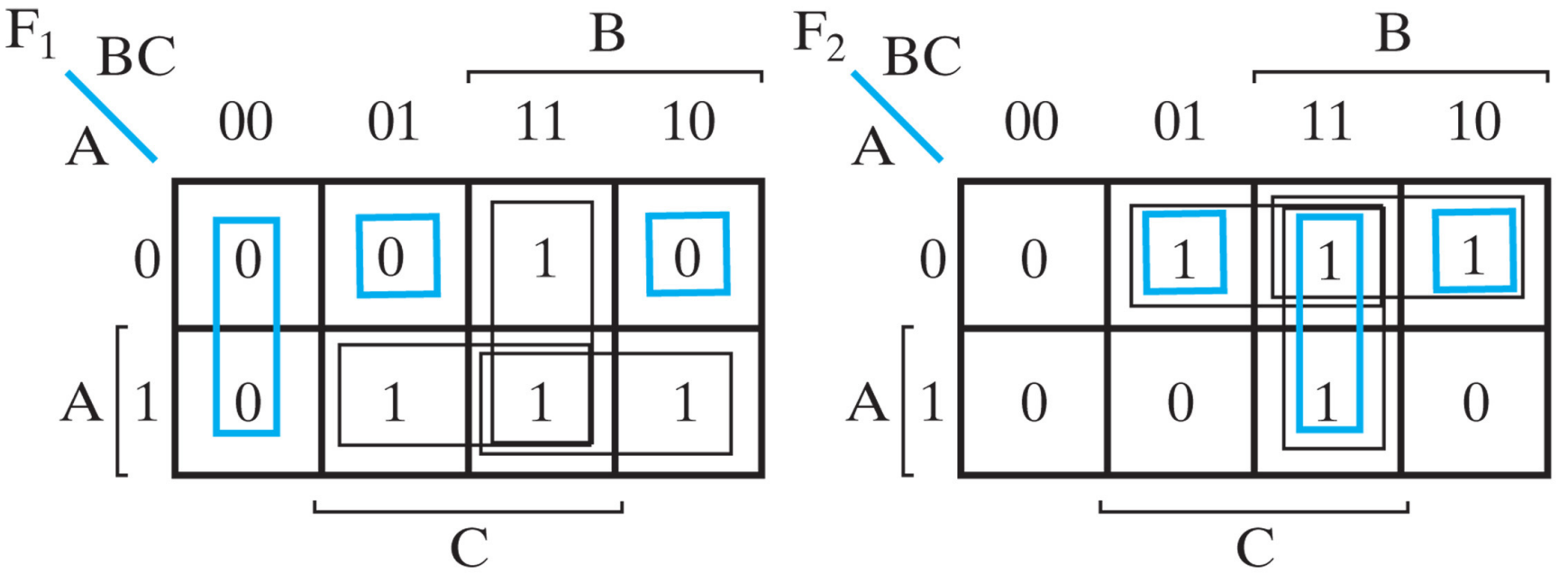


FIGURE 5-9 K-Maps and Expressions for PLA Example 5-1



$$F_1 = AB + AC + BC$$
$$\overline{F_1} = \overline{A}\,\overline{B}C + \overline{A}B\overline{C} + \overline{B}\,\overline{C}$$

$$F_2 = \overline{A}B + \overline{A}C + BC$$
$$F_2 = \overline{A}\,\overline{B}C + \overline{A}B\overline{C} + BC$$

FIGURE 5-10 PAL Device Structure with Connection Map for PAL® Device for Example 5-2

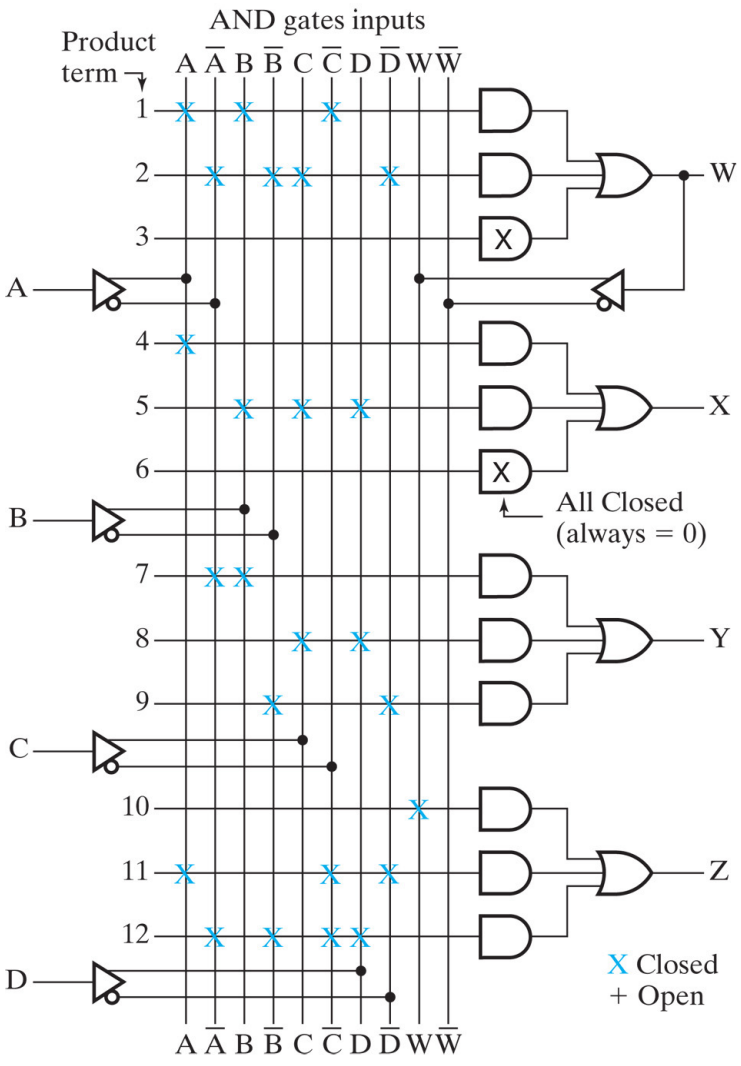


FIGURE 5-11 The Three Programmable Features of Most FPGA Devices: Logic Blocks, Interconnect, and Input/Output

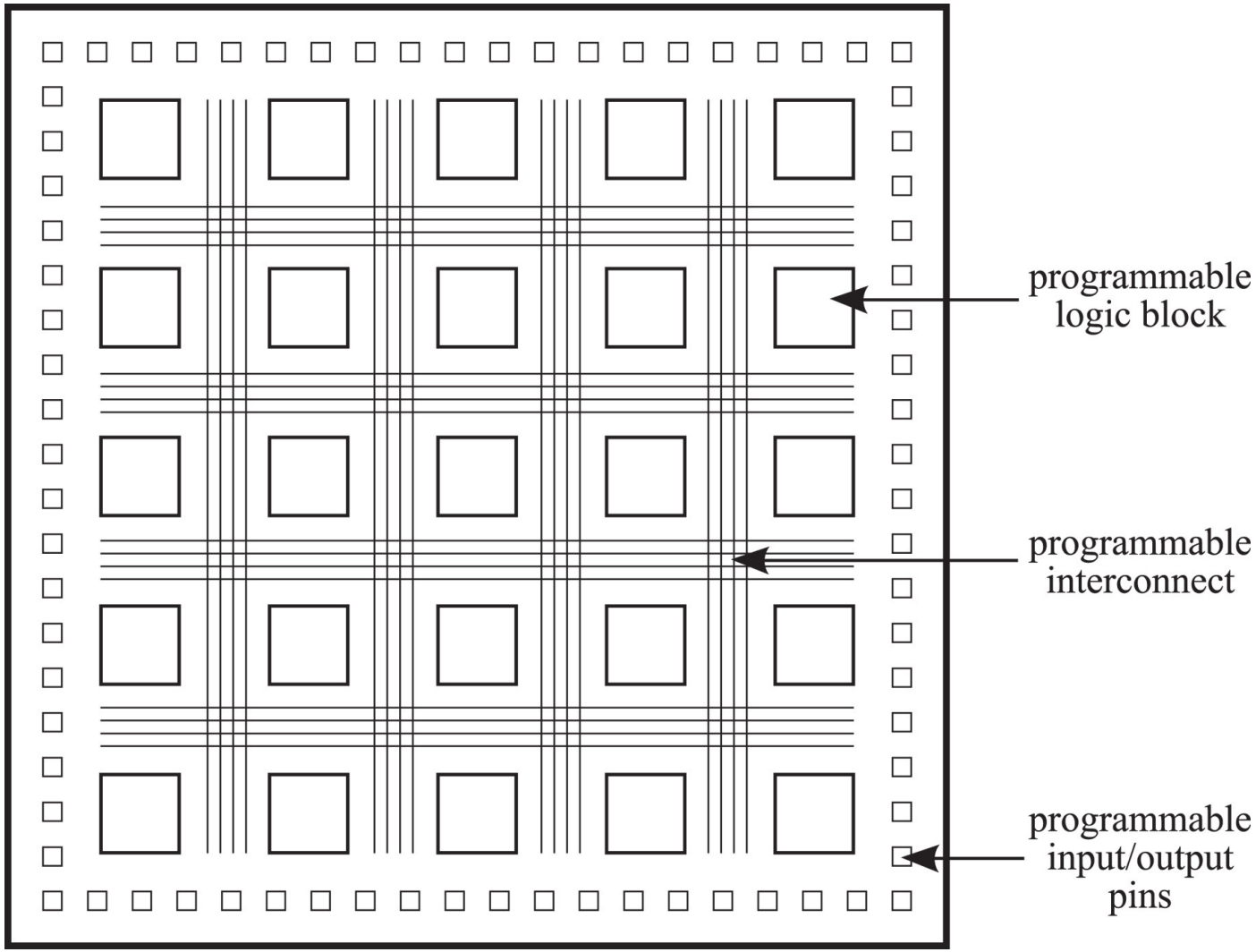


FIGURE 5-12 (a) A 2-Input Look-Up Table, (b) Implementing a 3-Input Function with Two 2-LUTs and a Multiplexer

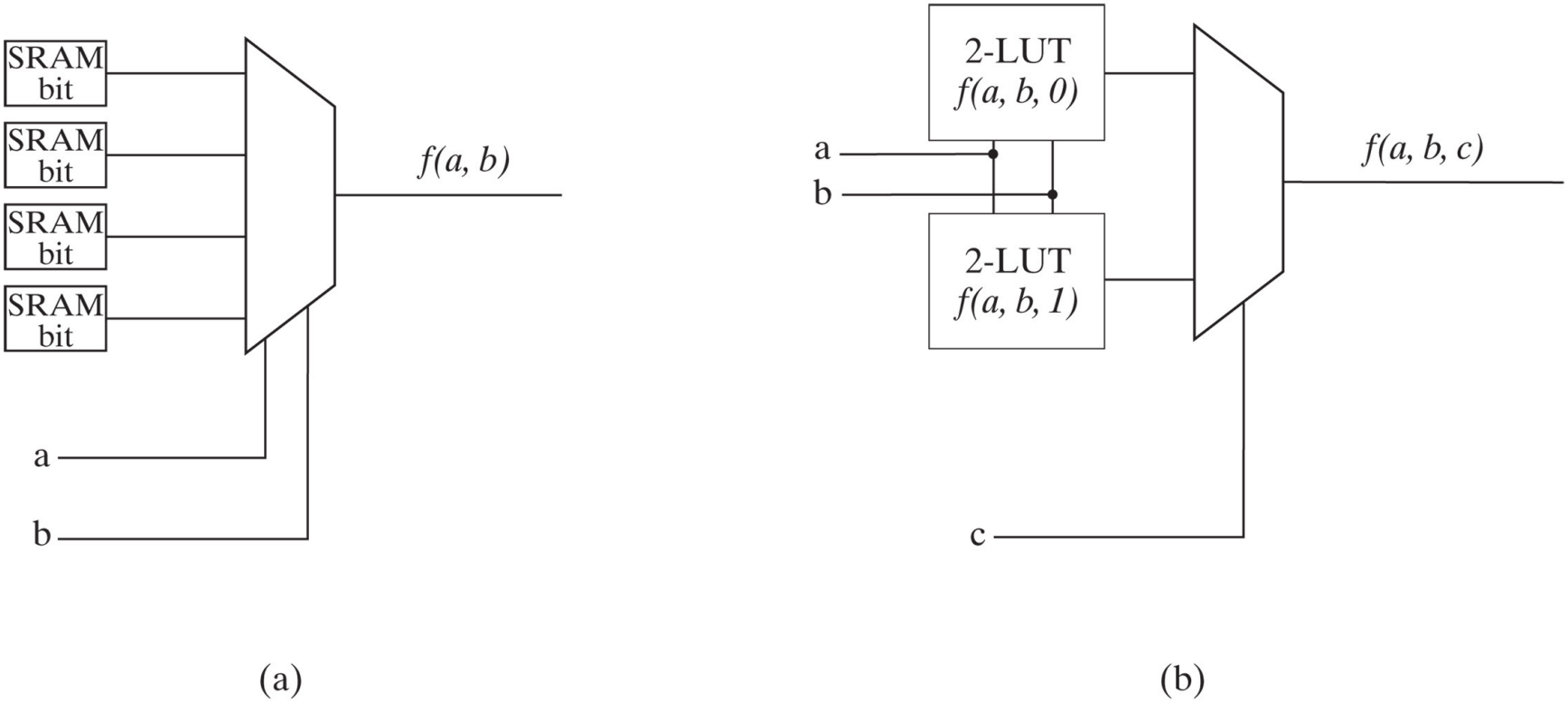


FIGURE 5-13 An Example of a Programmable Logic Block

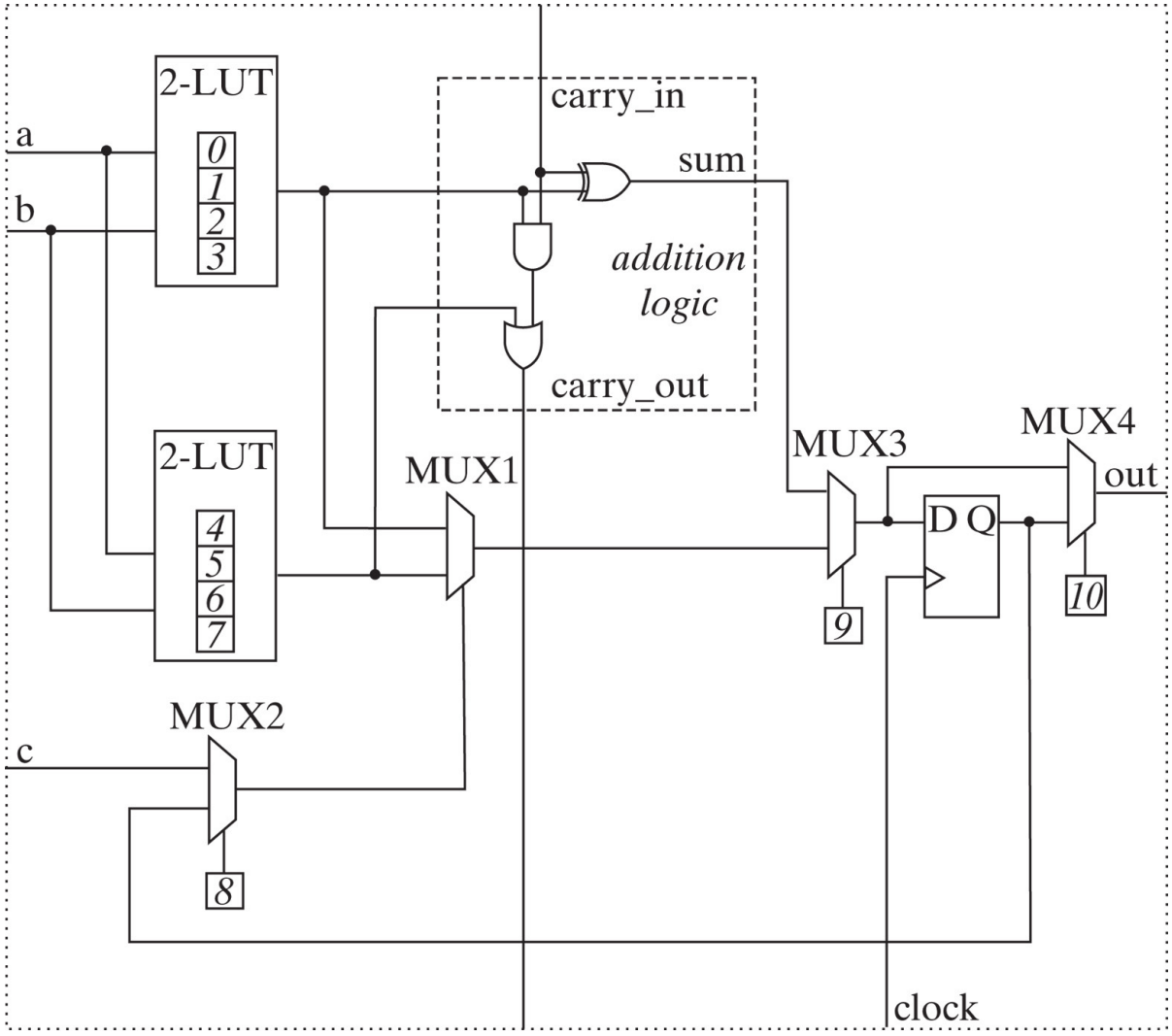


FIGURE 5-14 Switch Networks for Problem 5-1