HDMI Signal tapping and Digital Encoding for IP Monitor Surveillance

By

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Abstract

In high security surveillance scenarios there is a demand of recording the activity of the surveillance operators' computer screens. The will has risen out of the need to establish that the personnel is following protocol in certain situations or making sure that the software is working as intended. Creating a way of analyzing the behavior of both employees, software and how the hardware works together gives way to establish better protocols, find improvements in software and ultimately develop better products. Having the potential of creating a safer environment where it really matters, for instance at airports or nuclear power plants.

However given that the areas where this feature is interesting are characterized by high risk and responsibility the electronic devices used must have a very high emphasis on safety. If inserting a monitoring device between the surveillance operators' computer and screen it must under no circumstances leave the operator without a video stream. That means there must exist a passive throughput that is free from electronic components and software implementation. The device must not substantially degrade the signal integrity and in the event that it loses power it must send the signal through. A demand that prohibits the use of traditional IC based HDMI splitters since they in the event of a power loss situation does not output any signal.

Hence the birth of this project: To create a safe way of sniffing an HDMI signal without corrupting it. The solution is based on analogue operational amplifiers, something that has been proven quite difficult, given that the TMDS signaling used are very high frequency and the sheer lack of documentation on this subject.

After successfully creating a circuit that can sniff the signal, a function prototype will be created. It will be done using one of Axis Communications existing cameras and reconfiguring it to act as an encoder.

Keywords: HDMI, HDMI splitter, HDMI sniffer, fully differential, TMDS, operational amplifiers, analog signal conditioning, high frequency, digital signals.

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Preface

1. Project Introduction

Recording computer monitors can be if interest in a number of surveillance areas and scenarios. For instance it might be valuable to record the monitors in a steel-plant control room in order to verify that the control software is working properly or for establishing that the operators are following procedures. It might prove to be important data when looking for system malfunctions and testing purposes. Did the operator even receive the correct images at the correct time?

In this project we want to see if it is possible to make a device that listens on the signals on an HDMI cable and output the video stream on a separate port as depicted in the block diagram shown below in Fig. 1.

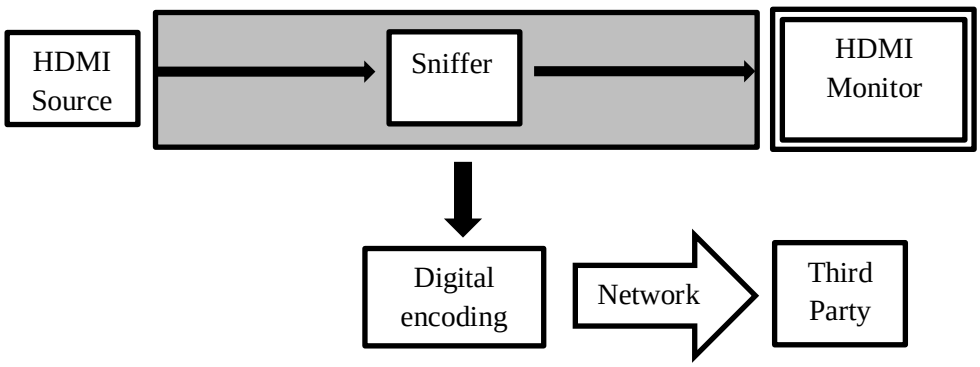

Fig. 1, shows the block diagram over the desired solution, where the grey area is the defined original path and is independent from any components.

The device must not interfere with the signals between the source and the monitor. A task that might prove tricky as the communication is done with Transition-Minimized Differential Signaling (TMDS), which have high bandwidth. The device will be inserted between the computer and the screen where the data must be sent uncorrupted, but at the same time, it also duplicates the same information to a sniffer port, which enables a second party to observe and record the stream over network.

"The source" through the project will be referring to the source of the HDMI signal, in our application case an ordinary computer. It will be kept arbitrary since the signal can come from any type of compliant source. The source point is absolutely fixated i.e., it is not possible to change the fact that the project is based on the need of a single HDMI source. The point is also the beginning of what is going to be defined as the original signal path (see the third definition and Fig.1, for graphical representation). Lastly to cover any chance of misinterpretation, if there is any mention of a; source, computer, or other device that delivers an HDMI signal they are all referring to this entry in the system.

"Monitor" is referring to the receiving end of the original signal path and is physically represented in the project as an ordinary computer monitor with HDMI input. It is thought as the representation of the computer monitor which the surveillance operator is looking at. In this project it is also a fixed point, however in the report when referring to a receiver it might be necessary for the reader to establish from context exactly which receiver that is subject.

"The original signal path" is going to be defined as the path between the source and the HDMI monitor as if no modifications has been done on the cable. It is created to underline the importance that this path cannot and shall not undergo any significant changes. It must at all times be functioning and data from the source must always be sent to the operators screen.

The other outputs of the sniffer is intended to be connected to the receiving end of an encoder unit for processing. The encoder unit will convert the original HDMI signal to the compatible color space, set up a network server and compress the video over the network. Connecting the encoder unit with the sniffer and writing new drivers to the circuitry will be covered last in the project in the productification phase. It is however apparent that the main research value of this project lies in the actual sniffing of the data signals because there is very little information available in this area. Where the biggest difficulty lies in not significantly degrading the signal integrity on

the original path. Technically that means the impedances and other parameters as seen from the source and receiver on that path must be as if it was a normal cable. What we need to keep in mind is that probably we cannot make a physical intrusion on a cable without leaving any trace, especially when we are working on very high frequencies. However the magnitude of the intrusion must be minimized and the signal on the original path must pass the HDMI standard.

The base questions that we want to answer in the project:

- Is it possible to sniff/listen to the signals on an HDMI cable?
- Is it possible to monitor the data while not significantly degrading the source signal?
- Is it possible to install the device while keeping the impedances of the wires to avoid signal reflections?

If the sniffing solution is not possible to implement:

- Provide a technical description why it doesn't work as originally intended.
- Figure out an alternative solution based on the findings.

Point of departure:

- Establish a method of quality testing the signals.
- What happens with the signal when we extend HDMI over a printed circuit board (PCB)?
- How much does the signal quality suffer when simply splitting the signal

1.1. What is HDMI?

High-Definition Multimedia Interface (HDMI) is the product of seven major corporations cooperative with the aim of standardizing transmission of High-Definition (HD) video and sound between a wide arrange of consumer products. The founders are Hitachi, Matsushita Electric Industrial, Philips, Silicon Image, Sony, Thomson, RCA and Toshiba and the interface was introduced to the market in 2003 [1]. The data protocol used is Transition-minimized Differential Signaling (which is going to be explained

in detail in 1.1.2.) and has a bit rate of up to 18 Gbit/s. Version 1.3a which is the version specification that was used in this project was first released 2006-06-22. It is specified to a single-link bandwidth of 340 MHz and a bitrate up to 10.2 Gbit/s [2]. The 1.3a HDMI specification was selected due to it is the last version before the introduced support of 4K formats and integrated Ethernet connection. The most widely adopted resolution used today on computer monitors is 1080p (Full-HD) and while in a finished product it could be wise to choose a later specification, for this project it is sufficient and working with less features, lower bitrate and lower bandwidth potentially removes complications in the initial development process.

In the future if there is any reference to an HDMI specification it is by default referring to Version 1.3a unless otherwise stated.

1.1.1. The Cable

The most commonly used type of HDMI connector that is used is the Type-A connection, this is the type of connector found in all ordinary consumer devices and therefore it is the type that is going to be featured in this project. It has 19 pins with the corresponding signals shown directly below in Fig. 3, and Table 1:

Table 1, HDMI Type-A pin and signal mapping overview [1].

Pin 1	TMDS Data2+
Pin 2	TMDS Data2 Shield
Pin 3	TMDS Data2-
Pin 4	TMDS Data1+
Pin 5	TMDS Data1 Shield
Pin 6	TMDS Data1-
Pin 7	TMDS Data0+
Pin 8	TMDS Data0 Shield
Pin 9	TMDS Data0-
Pin 10	TMDS Clock+

Pin 11	TMDS Clock Shield
Pin 12	TMDS Clock-
Pin 13	CEC
Pin 14	Reserved (HDMI 1.0-1.3c)
Pin 15	SCL (I2C Serial Clock for DDC)
Pin 16	SDA (I2C Serial Data Line for DDC)
Pin 17	DDC/CEC/ARC/HEC Ground
Pin 18	+5 V (max. 0.05 amp)
Pin 19	Hot Plug detect (all versions) and HEC/ARC (Optional, HDMI 1.4+ with HDMI Ethernet Channel and Audio Return Channel)

The pins with the most interest in this project are Pin 1 to Pin 12, as these are the signals that transfers the video data. The remaining Pins are reserved for low frequency I2C signals, such as the Consumer Electronics Control (CEC) and Extended display identification data (EDID) which travels over the Display Data Channel (DDC). To create a good solution it is important to understand the purpose of these signals. However first following is explanations about the theories that has been implemented into the technology, and which has made the standard revolutionary. To simplify the technology it can be divided into two parts:

1) The Physical Layer:
   Description of the physical transmission medium i.e. it is the specification of the actual wires. All of the electrical properties as; impedance matching and capacitances need to meet strict requirements determined in the HDMI specification.

- **Differential Signaling** – The signal is sent over two parallel lines whereas on one of the lines the signal is inverted. Upon arrival at the receiver the signals are compared to each other and merged back into one waveform. This is instead of comparing a single signal to ground and is based on the fact that noise (electromagnetic interference) typically affects the two lines in the same way making

it possible to remove the noise that both lines has in common, normally called common node noise. By doing that any presence of noise that does not have its corresponding inverted signal on the other line is removed, illustrated in Fig 2, below. However the technique to remove the noise with differential signaling encounters some problems when the noise source is close to the signal wires. In order to address that problem HDMI implements twisted wire pairs explained in the next bullet point. [4] [5]

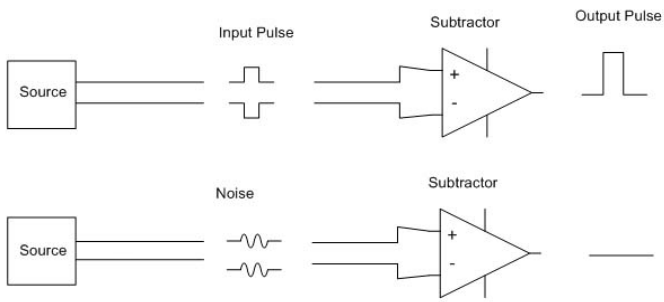

Fig. 2, conceptual picture over how differential signaling propagates signals and eliminates electromagnetic noise [4].

- **Twisted Pairs** – This term is referring to that two conductors are physically twisted around each other with the benefit of canceling out electromagnetic interference (EMI). The twisting of the wires is done to better utilize the theory of differential signaling. The technique, and why it is almost essential to differential signaling, is best explained with an example: Two wires run in parallel and a noise source is positioned close to them. The wire that is closest to the noise source will be affected more by it compared to the wire further away. Upon arrival at the receiver since the noise source did not affect the two wires in the same way it will fail to recognize it at common node noise and thus not eliminate it.

  When these two wires instead are closely twisted around themselves the noise source would affect them more evenly and the differential elimination would work more effectively. [5]

- **Low-Voltage Differential Signaling (LVDS) –** The above techniques has been implemented together with the theory of LVDS which means transmission has been made to work at low voltage levels. In LVDS the power consumption is kept low by implementing a convention where injecting one wire with a constant current of 3.5mA (typically) and the digital logic level is determined by the direction of the current. The current travels into a resistor (typ. 100Ω) that sits between the two differential wires and then back into the source. The receiver then senses the voltage polarity over the resistor and determines the logic level. Since the current is constant it greatly reduces the demand on the power supply decoupling which in turn reduces production of interference in the transmitting circuitry.

  LVDS is the technology that TMDS is built on and the advantages are plentiful; it has low power consumption; can be driven with a power supply voltage down to 2.5V or lower together with low noise generation and high noise resistance. [6]

The three above hardware solutions, in the bullet points above, creates the foundation which the HDMI standard is built on, however HDMI has been further improved with a software layer:

2) <u>The Software Layer:</u>
   Algorithms that encodes the data before sending it over the transmission lines and decodes it at sink arrival.

- **DC Balanced –** The term refers to that it is desirable to have as many ones and zeroes or the difference between the counts is no more than two and not more than five ones or five zeroes in a row in a 20-bit block of data. It is very commonly used in telecommunications to help reduce bandwidth requirements for transferring a signal. [7] [8] [9]
- **Transition Minimized –** As in most digital solutions data is usually send in chunks of 8 bits i.e. 1 byte. However when applying transition minimization to the data every 8-bits gets encoded up to 10-bits adding two control bits through a process similar to 8b/10b encoding. The reason for this is to implement the DC-balancing and

minimize the number of transmissions between high and low voltage level over the wires (transition minimized). This technique lowers the electromagnetic interference and gives a more robust signal allowing it to travel over longer lines. In this project there is no need to go deep into the technology however when calculating bandwidth requirements this needs to be remembered that there is two extra bits for each byte of data being sent. [10]

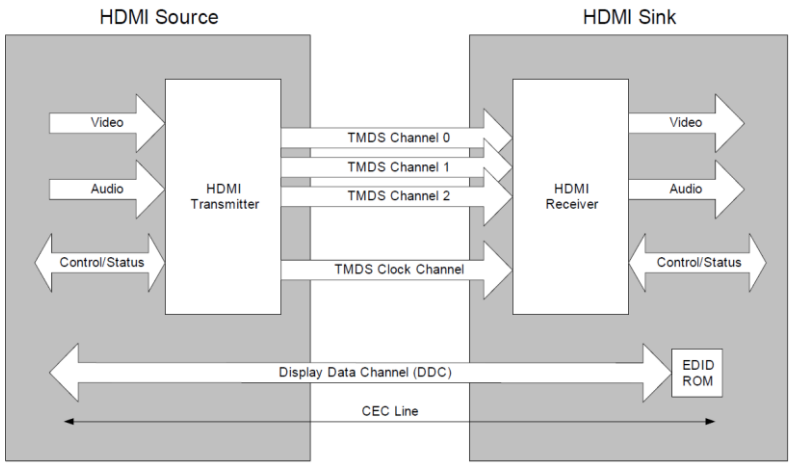

Fig. 3, block diagram of HDMI transmission [2].

1.1.2. Transition-minimized Differential Signaling

The data protocol used for sending data over HDMI used Transition-minimized Differential Signaling (TMDS). These signals are differential, sent over shielded twisted pair, have strict requirements on termination resistances and characteristic impedance on the transmission lines. A conceptual schematic for one TMDS differential pair can be seen below in Fig. 4.

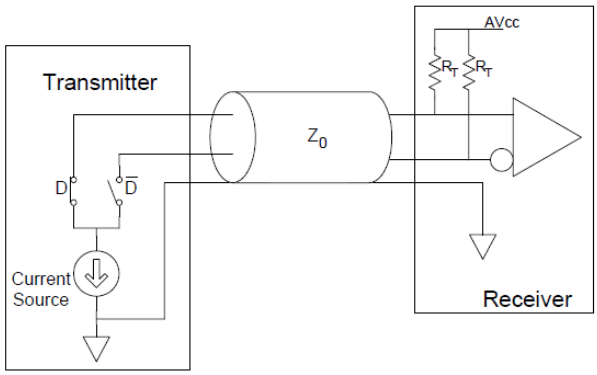

Fig. 4, conceptual Schematic for one TMDS differential pair [2].

AV_{cc} – Link Reference Voltage

R_T – Termination Resistance

Z_0 – Characteristic Impedance

As this is a differential signal the switches on the transmitter side is referring to that the two signals that are flowing over the lines are inverted to each other. Following the HDMI specification the Link Reference Voltage sets the high voltage level of the differential signal while the current source at the source together with the termination resistance sets the low voltage level. Further it is of utmost importance to avoid signal reflections and thus the characteristic impedance of the transmission lines is matched with the termination resistance. The basic electric operation conditions are presented below in Table 2 below.

Table 2, basic electric operational TMDS conditions. [2] [11]

Item:	**Value:**
Termination Supply Voltage, AV_{cc}	3.3V ± 5%
Termination Resistance, R_T	50Ω ± 10%
Nominal Transition Amplitude	500mV (+2.8V to +3.3V
Voltage Swing	150mV – 800mV

Rise Time	≤ 200ps (usually ≈ 100ps)
Data Rate Single Link	25Mpps* – 340Mpps*
Bit Times, TBIT	≥ 294ps
TMDS clock frequency Cat.1	74.25MHz
TMDS clock frequency Cat.2	340MHz

Mpps* – Mega pixel per second. Each pixel is represented by 10 bits of data (not 8 bits due to Transition-minimization, see chapter 1.1.1, point 1) which in turn makes the bit times (TBIT) a popular way of measure.

TMDS clock frequency – Cable assemblies can fall into two categories depending on how high TMDS clock frequency that they can handle. Category 1 supports frequencies up to 74.25MHz and Category 2 supports frequencies up to 340MHz. It is worth noting that when testing which category an assembly falls in they are tested with and without equalization i.e. active signal conditioning. Category 1 is tested without equalization while in Category 2 the assemblies can be tested with equalization, then required to support at least 340MHz. However they can also be tested without equalization and are then only required to support 165MHz.

2. Quality verification and Testing

2.1. How to verify the signal?

This chapter will provide a description of how to test and measure the quality of HDMI signals. It is important to understand because while there is the possibility to just plug an HDMI Device under Test (DUT) into a screen and see if it works, there is no way to determine changes in the waveform. A scientific method of evaluating the integrity of the signal was created. Thankfully there are a number of standard tests available that are

adopted throughout the HDMI industry which are based on the HDMI documentation and defined in the HDMI Compliance Test Specifications (CTS).

An HDMI system can be divided into three parts, shown in Fig. 5 below:

1) Source Device
2) Cable Assembly
3) Sink Device

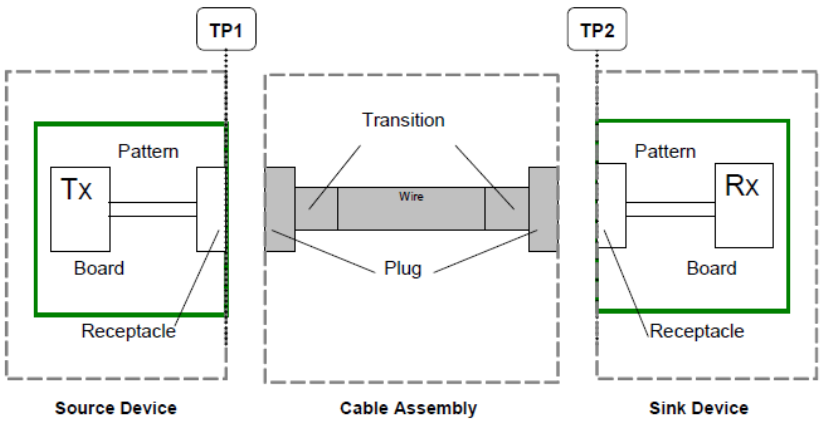

Fig. 5, TMDS Link Test Points [2].

The core tests for each part is summarized into Table 3 below:

Table 3, core HDMI CTS tests [11].

Type:	Signals	Tests	Test Point
Source	Clock and/or Data	Data Eye Diagram Clock Jitter Clock Duty Cycle Overshoot/Undershoot Rise/Fall Time	TP1 TP1 TP1 TP1 TP1
	Data-Data	Inter-pair Skew	TP1
	Single-Ended	Intra-pair Skew	TP1
	HEAC	Low Level Output Voltage Audio Transmitter Test	TP1 TP2 TP2
Sink	Differential	Jitter Tolerance Min/Max Differential Swing Tolerance Differential Impedance Deep Color Audio Clock Regeneration	TP2 TP2 TP2 TP2 TP2

		Audio Sample Packet Jitter Audio Formats One Bit Audio DVI Interoperability	TP2 TP2 TP2 TP2
	Single-Ended	Intra-pair Skew	TP2
	HEAC	Audio Transmitter Test	TP1
Cable	HEAC	Data Eye Diagram Inter-pair Skew Device Impedance Test Cable Test	TP1, TP2 TP1 & TP2 TP1 & TP2

It would be too time consuming and unnecessary this early in a development stage to perform all of these tests. The tests that is going to be heavily relied upon is the Eye Diagram and at first the Clock Jitter test. They can be conducted fairly quickly and they produce the most important information required. The tests are going to be made with the source testing point of view because the device which we are trying to build will be connected to HDMI Compliant Sinks and Cables. Source electrical characteristics presented in Table. 4 and Table 5 below.

Table 4, HDMI Source DC characteristics at TP1 [2].

Item	Value
Single-ended standby (Off) output voltage, V_{OFF}	$AV_{cc} \pm 10mV$
Single-ended output swing voltage, V_{swing}	$400mV \leq V_{swing} \leq 600mV$
Single-ended high level output voltage, V_H	Sink support only <= 165MHz: $AV_{cc} \pm 10mV$ Sink supports > 165MHz: $(AV_{cc} - 200mV) \leq V_H \leq (AV_{cc} - 400mV)$
Single-ended low level output voltage, V_L	Sink support only <= 165MHz: $(AV_{cc} - 600mV) \leq V_L \leq (AV_{cc} - 400mV)$ Sink supports > 165MHz: $(AV_{cc} - 700mV) \leq V_L \leq (AV_{cc} - 400mV)$

Table 5, HDMI Source AC characteristics at TP1 [2].

Rise/Fall Time (20% - 80%)	75ps ≤ Rise/Fall time
Clock duty cycle, min / average / max	40% / 50% / 60%
TMDS Differential Clock Jitter, max	0.25*TBIT (relative to ideal Clock Recovery).

2.1.1. The Eye Diagram Test

The digital signals sent over HDMI when visualized, form an eye pattern and by analyzing this pattern it is possible to evaluate the quality of the differential data. The eye diagram is formed by tracing the signals where the high and low logic levels together with their transitions overlap and creates the distinct pattern (see Fig. 6 below) which shows distinction between a good and a bad signal in terms of integrity.

When the quality of a signal degrades the opening in the eye will become smaller until it is completely closed. According to some [12] as long as the eye is open the signal will successfully transmit, however in order to pass the HDMI Compliance Test guidelines for a source, there has been placed a mask inside of the eye opening. If the eye collapses into the masked area either horizontally because of timing jitter or vertically because of loss in signal amplitude it does not pass the HDMI Compliance standard for a source device.

<u>The key information obtained from reading an Eye Diagram:</u>

- If the signal will transmit successfully.
- Signal amplitude.
- Signal timing jitter.

This is information that is especially valuable when trying to find the cause of data corruption, improving electrical design, evaluating signal integrity and troubleshooting HDMI systems in general.

Note: Producing Eye Diagrams is my test of choice, it is very useful in the way that it shows directly what improvements need to be done to the signal and the test itself is quick to conduct.

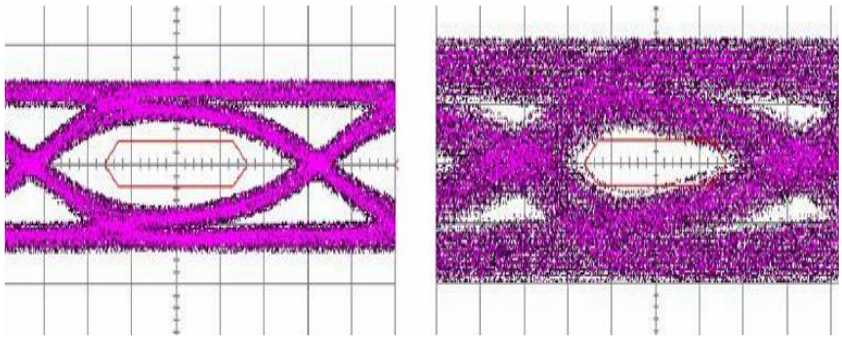

Fig. 6, shows a good HDMI signal vs. a bad HDMI signal. [13]

The Eye Diagram mask is specified according to Fig. 7 below:

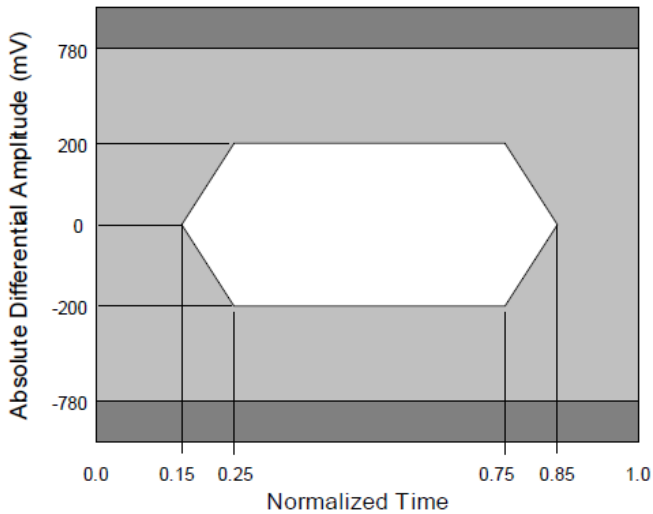

Fig. 7, Eye Diagram Mask at TP1 for testing source requirements **[2]**.

It visualizes the minimum size of the eye opening together with the maximum and minimum voltage levels. The time on the x-axis is normalized to the bit time at the operating frequency. Over- and Undershoot voltage levels are set by the maximum and minimum signal voltages at ±780mV [2]. Note that the mask is a testing measurement for a source, and not cable or receiver signals. For a signal that has traveled some distance, in

a cable or other material, it is acceptable to have mask hits and still be HDMI compliant. Thus in the testing during the project the mask will be present and I will display how many hits it gets but only in order to make comparisons in how open the eye is. During testing it also showed that the correlation between mask hits and how well the signal arrives is not strictly analogue. In one case a signal with a significantly lower hit rate didn't display very well at all on a computer screen compared to that of a signal with many more hits on the mask. But the mask serves as one type of parameter when comparing signals.

2.1.2. The Clock Jitter Test

As with all digital transmission systems the clock is conducting the orchestra. In this test the clock signal is plotted alongside a recovered clock and compared to each other using histogram boxes placed at the signal rising edges which determines the jitter present. Where the established jitter should be less than 0.25*Tbit [10].

When initially reading about this test it seemed like a great tool in the testing process but in real life no matter how bad the impedance mismatch became the signal still passed HDMI compliant testing. Even when cutting a cable in half and hand soldering a piece of common copper prototyping board in between extending the path by a few centimeters the test showed a passing grade source signal i.e. less clock jitter than 0.25*Tbit. This is due to clock recovery in the sink when upscaling the clock frequency 10x. So later for measuring signal function this test is not worth the time, as long as the PLL in the receiver maintains lock on the signal. However it shows some measureable differences in the oscilloscope while the signal needs to travel long respectively short distances. In the variable cable length measurements the results will be displayed and then further in the project the clock jitter test results will be omitted. *Note: Do not confuse this test value with the value of the data signal jitter which is very much a relevant measured value in this project.*

2.2. Technical difficulties

Since HDMI signals are very high frequency signals a few concepts stand out and become very important to explain. The three main design parameters that needs to be carefully considered are covered in this chapter; characteristic impedance, signals in part or fully reflected back and system bandwidth. The engineer designing the computer aided design (CAD) of the PCB must follow strict guidelines and the goal is to explain why.

2.2.1. Characteristic Impedance and Signal Reflections

The impedance is the resistance, capacitance and inductance lumped together for an electrical signal at a specific frequency. When using low frequency signals the capacitance and inductance play no major part in how much current can pass in the presence of an electric potential. [13] [14]

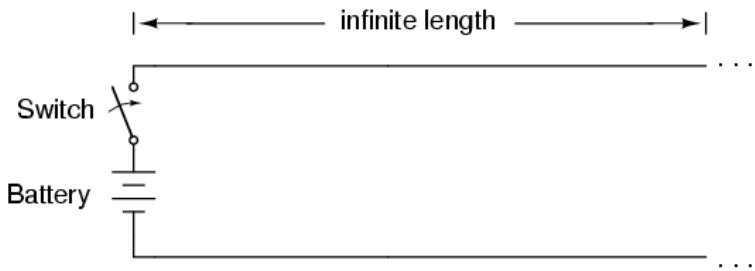

Fig. 8, showing the low frequency model of two transmission lines with infinite length running in parallel with two batteries as source **[14]**.

Normally a transmission line is depicted like above in Fig. 8 with no extra parasitics and propagating electrical signals perfectly without any delays. When dealing with short transmission lines and at low frequencies that model is a fair approximation.

However in practice a transmission line actually has parasitics and resistance which are relative to the length. That means that instead of merely considering the wires as conductors, they need to be considered as an electrical component themselves. [14]

Typical behavior of common components at high frequencies needs to be remodeled and once understood the engineer is able to handle them. Fig. 9 below shows the low frequency and high frequency (HF) behavior:

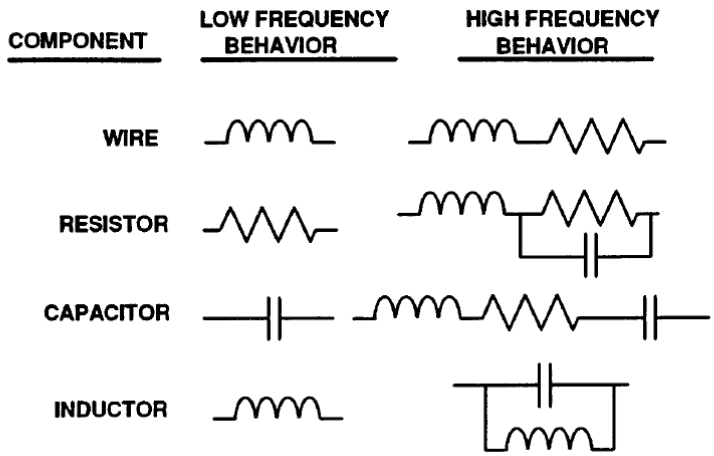

Fig. 9 Component characteristics at high frequencies **[15]**.

And if we continue with our parallel transmission lines the HF system would look like as shown below in fig. 10:

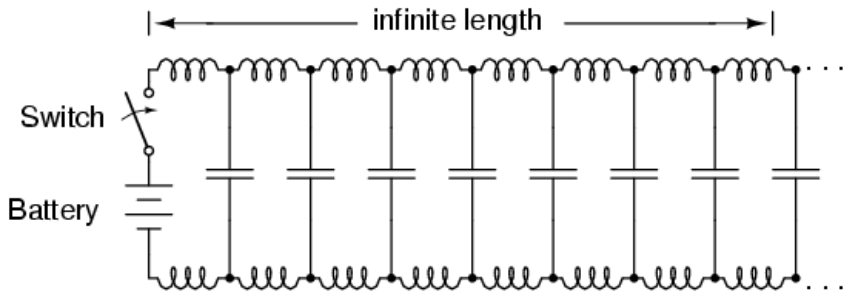

Fig. 10 shows a high frequency model of the parasitics on a transmission line **[14]**.

The capacitances and inductances will gradually charge with the propagating signal and will behave as a constant load.

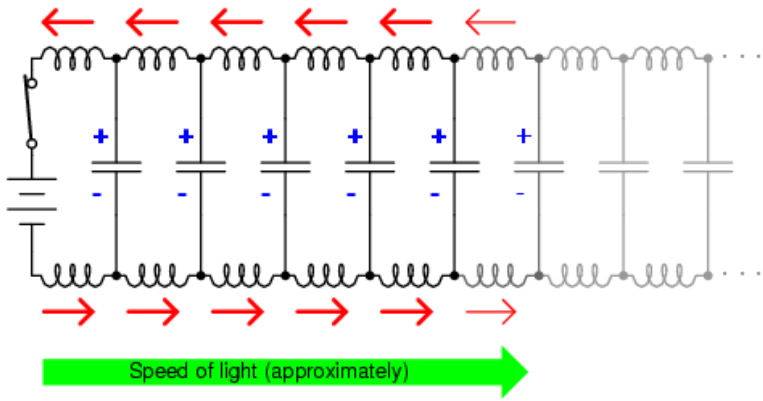

Fig. 11 shows how the high frequency behavior of a transmission line when an electric signal propagates through it [15].

The impedance of the wires which is dependent on the physical aspects of the material used needs to be considered. In high frequency a very important aspect is to determine the electric density in order to avoid reflections. This is often handled by the characteristic impedance which usually is written as Z0 and determines termination resistances. It is defined as follows:

Fig. 12 shows the components needed for calculating the characteristic impedance [14].

If the transmission lines are defined as above where a current I(x) is traveling in opposite direction and an electric potential V(x) exists between them;

- Characteristic impedance of the bottom line is: V(x) / I(x) = Z0
- Characteristic impedance of the top line is: V(x) / I(x) = -Z0

And is therefore the ratio between the voltage and current of a wave travelling along the line. [14]

Why is this important?

"When the wave reaches the end of the line, in general, there will be a reflected wave which travels back along the line in the opposite direction….. The characteristic impedance of a line is that impedance which when terminating an arbitrary length of line at its output will produce an input impedance equal to the characteristic impedance. This is so because there is no reflection on a line terminated in its own characteristic impedance" [13]

In other words; if we know the characteristic impedance of the line we also know how to terminate the line in order to avoid signal reflections.

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

Equation 1, general expression for the characteristic impedance of a transmission line [13].

Important to keep in mind is that all the components are per unit of length and therefore the characteristic impedance is not dependent of the length.

In the HDMI standard it is specified that the transmission lines all must have a characteristic impedance equal to 50Ω single ended i.e. 100Ω differential. Therefore any design that is made must follow the correct input and output termination in order to avoid reflections.

2.2.2. Bandwidth

Bandwidth is the measured value of the frequency in Hertz (Hz) of a propagating signal. In the HDMI v.1.3. Standard the pixel frequency clock is capped to 340MHz and we can come to a very important conclusion by applying the following:

The maximum throughput specified by HDMI is set to 10.2Gbit/s which means that 3.4Gbit/s is the top speed of each channel. If the clock was a bit clock this would not add up since they differ by a factor of 10 (340MHz vs. 3.4GHz). However if the pixel clock was a byte clock it comes closer to the value, but it still is 20% missing from that equation. The last 20% lies in the

TMDS encoding which encodes each 8bit byte into 10bit bytes, remembering this and applying to our calculation the numbers add up. When the clock signal arrives at the sink it uses a phase-locked loop (PLL) to rescale the clock to full frequency on chip. The data rate of the channel thus relates to the clock to a factor of 10 and the data rate over all channels relates with a factor of 30. Eg. A 100MHz pixel clock will thus have 1GHz data rate frequency on each channel or 3GHz data across all three channels. More on this later when constructing prototype circuitry, letting this act as an introduction.

2.2.3. PCB for High Speed Applications

During the project there will be conducted manufacturing of printed circuit boards for testing signal integrity and prototyping. HDMI being a very high frequency signal it is needed to take steps in order to ensure maintained signal integrity.

Without going too deep into the subject a master thesis at LTH EIT called "Signal Integrity Analysis of Package and PCB for high Speed Data link Application" by Sreejith Palleeluveedu Raghavan [17] shows that the topology (microstrip, stripline), track width/length, termination and physical structure will affect how much data jitter is present. This result further enforces the importance of choosing the right amount of routing layers, power planes, and topology for keeping signal integrity. The reason the signal integrity in our tests are well maintained (though there is room for improvement) is because the PCB designer followed high-frequency guidelines for LVDS. If there was more time in the thesis it would be possible to examine different design parameters for the PCB manufacturing for minimizing the under-/overshoot and data jitter.

Short Overview of the PCBs in this project:

- The PCBs in this project implements Microstrip topology which has less capacitive coupling and can propagate faster clock/logic signals [16], where the traces are on the outer layer. How the traces are routed and relevant parameters for impedance calculation can be shown in Fig. 13 below:

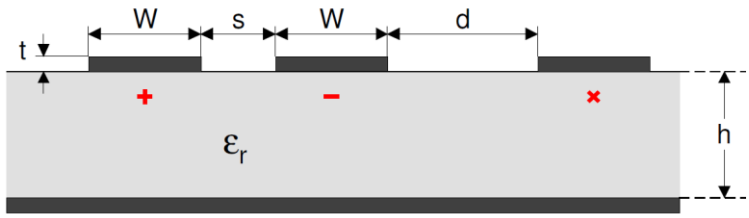

Fig. 13 Microstrip physical geometry **[17]**.

How the impedance calculations are done is for this project irrelevant, and for deeper reading I recommend reading the white paper from Texas Instrument called "HDMI Design Guide".

- Resistors are surface mounted and termination resistors is places as close as possible to the receiver.
- Differential pairs are routed with 100Ω differential impedance.
- All pairs are matched within 0.1mm, the traces are kept close together with equal spacing and equal length.
- Under all traces there is an unbroken plane (power or ground).
- They are FR-4 PCBs.

Some important data needed for making the layout [18]:

- Tbit = time duration for a single bit across a TMDS channel.
- Tcharacter = 10 x Tbit
- CLK = 340MHz
- Propagation delay for FR4 = 6.67ps/mm
- Intra-pair skew = 0.15 Tbit [2].
- Inter-pair skew = 0.20 Tcharacter [2].

Which gives us:

- Data rate = 10 x 340MHz = 3.4GHz = 385.45ps.
- Intra-pair skew in time = 0.15 x 385.45ps = 57.82ps.
- Intra-pair skew in distance = 57.82ps / 6.67ps/mm = 8.295mm.

Other layout rules [17]:

- Do not lay traces with 90° bends to avoid changing the effective width of the trace and subsequently changing the the differential impedance. Instead use 45° (chamfered corners) minimizing the discontinuity.

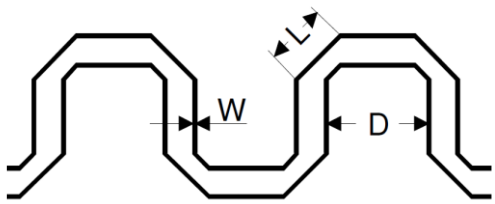

Fig. 14 Skew reduction, avoid using 90° degree bends.

- When routing around an object route both of the differential traces in parallel avoiding change in the spacing and thus keeping the differential impedance.

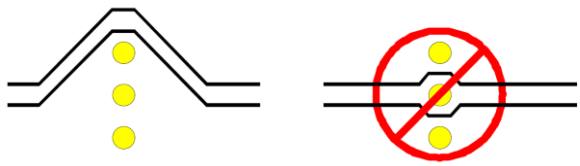

Fig. 15 Routing HDMI differential traces around an object **[17]**.

- Passive components on the signal path should be placed next to each other/parallel on the traces.

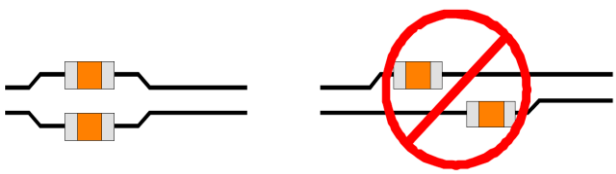

Fig. 16 trace component placement **[17]**.

- In order to avoid discontinuity in the impedance use the smallest available vias.

While some guidelines might not be implemented into the printed circuit board, it is safe to assume that there will be some signs of impedance mismatch. First there might be some parameter not implemented on the PCB and second all the components will be soldered by hand by me through a stereo microscope. Without doing any initial tests a higher rate of data jitter and signal reflections will be expected.

2.2.4. Test Equipment

All the measurements will be done on a Tektronix DSA 7125C Digital Serial Analyzer which have a bandwidth of 12.5GHz. In order to make the HDMI connection it has been used shielded coaxial cables and from Wilder Technologies HDMI test fixtures.

In this project the adapters for cable (Receptacle adapter) and source testing (Plug Adapter) were used. Included in the kit is also a low frequency control board that controls the assertion of Hot-Plug detection (HPD) and Electronic Display Identification Data (EDID) so the adapter itself is seen from the source as an ordinary screen. This is necessary since the source needs to handshake with the Sink before it starts sending data.

Key Electric Properties [20]:

- 4.95 Gb/s and 10.2 Gb/s data rated supported
- Insertion loss < -3 dB @ 9.6 GHz mated plug and receptacle fixtures
- Return loss < -20 dB @ 3.3 GHz mated plug and receptacle
- Differential Impedance 100 Ω ± 5 Ω (wo HDMI Connectors)
- Single Ended Impedance 50 Ω ± 2.5 Ω (wo HDMI Connectors)

The point in listing these characteristics is to show that the adapters themselves introduces corruption in the measurements of significant magnitude.

2.2.5. 1080p Signal Generation: Asus Laptop

In the testing it was needed to generate a test video with 1080p content running at 60Hz and 8-bit color depth. To do this an Asus U36SG Laptop is used, and to make sure that the signal quality is good enough presented below is testing results proving that it passes HDMI specifications.

Table 6, Test summary Asus U36SG Laptop (1080p @ 60Hz 8-bit).

Index	Test Name	Lanes	Spec Range	Meas Value	Result
1	7-9: Source Clock Jitter	CK	Clock Jitter < 0.25*Tbit;	0.108*Tbit	Pass
2	7-10: Source Eye Diagram	CK – D0	Data Jitter < 0.3*Tbit;	0.12*Tbit	Pass

Table 7 Asus U36SG Laptop Source Eye Diagram CK-D0, CK-D1 and CK-D2 test results.

Spec Range	Meas. Value	Tbit	Vs	Margin	Record Leng.	Mask Hits	Result
Data Jitter < 0.3*Tbit; CK – D0	0.12*Tbit	673.41ps	717.88mV	176.2m*Tbit	25.000M	0	Pass

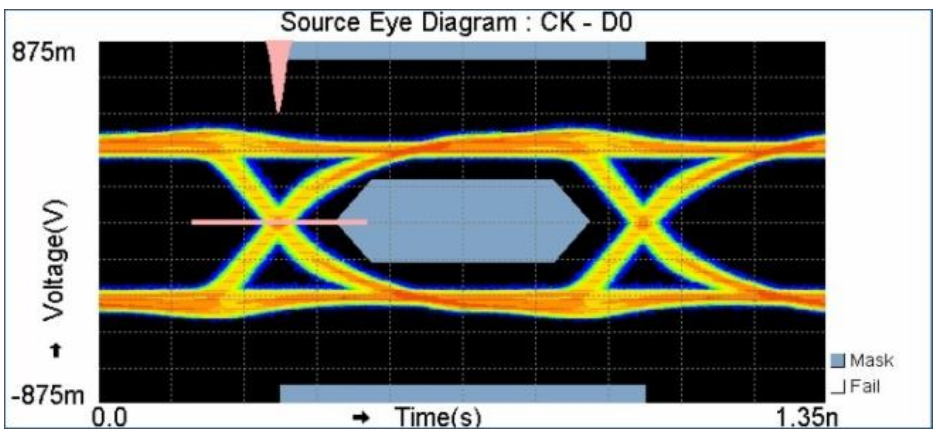

Fig. 17 Asus U36SG Laptop Source Eye Diagram: CK-D0

The eye diagrams are very clear with high and wide openings and the mask had no problem to fit inside each eye. As a source it passed the test requirements and is deemed fit to be used as a development tool in this project.

3. Case Studies: Part 1

3.1. How signal integrity changes when propagating through various lengths and is there any difference between high quality cables and low quality cables

In order to make a thorough analysis of the whole HDMI system first case study is to conduct comparable test between long, short, cheap and expensive HDMI cables. The case study serves the purpose of start using the test equipment, verify/analyze signals and test differences in signal integrity.

3.1.1. Material and method

The materials needed to exactly reproduce this test are:

- Tektronix DSA71254C Serial analyzer (See chapter 2.3.1).
- Wilder Technologies HDMI Type-A Test adapter kit (See chapter 2.3.2).
- Generic Consumer HDMI media player able to play content in 1080i at 60Hz. Here it is used an MED400X2S from Mede8r.
- HDMI Cables:

Brand:	**Type:**	**Length (m):**
Nikabe	High-End	1m 2m 3m
No Brand	Generic/Low cost	1m 2m 3m
Nikabe	High-End Ultrathin	0.5m
Luxorparts BlueConn	Generic/Low cost	0.5m

Clicktronic	High-End	15m

Table 8, list of tested cables.

The method of conducting this experiment is as follows: The laptop will send high definition content onto the cable which is connected through the test adapters into the high-speed oscilloscope. When the signals reach the scope it is possible to analyze the signal quality. All the cables will be tested accordingly to source testing on all the data channels and the tests conducted are:

- Eye Diagram Test
- Clock Jitter Test

Since the diagrams across all the channels shows little distinction it is only necessary to display the diagrams on one channel which has been chosen to be the CK-D0 channel, the choice is arbitrary and any of the other pair combinations would be fine. The device and measurement parameters are shown directly below:

Device Configurations:

- Clock Frequency(MHz): 148.499
- Resolution: 1920x1080p 8-bit
- Refresh Rate: 60Hz
- Record Length: 25.000M

3.1.2. Results

There was measureable differences between the high and low quality cables, in the high-end cables favor, but they were not significant. Therefore I will only present the eye diagrams for the high quality, unless there is for a specific set of cables with very big difference in the signal integrity.

Nikabe 0.5m High-End HDMI cable and Luxorparts BlueConn 0.5m HDMI cables Test Report:

Table 9, Nikabe 0.5m vs. generic 0.5m HDMI Cable Source Clock Jitter test results.

Spec Range	Meas. Value	Tbit	Vs	Margin
Clock Jitter < 0.25*Tbit; Nikabe 0.5m	0.134*Tbit	673.41ps	718.08mV	0.12*Tbit
Clock Jitter < 0.25*Tbit; generic 0.5m	0.115*Tbit	673.41ps	696.80mV	0.13*Tbit

Table 10, Nikabe 0.5m and BlueConn 0.5m HDMI Cable Source Eye Diagram CK-D0 test results.

Spec Range	Meas. Value	Tbit	Vs	Margin	Mask Hits	Data Jitter
Data Jitter < 0.3*Tbit; Nikabe 0.5m	0.12*Tbit	673.41ps	686.40mV	176.1m*Tbit	28	83.4ps
Data Jitter < 0.3*Tbit; BlueConn 0.5m	0.13*Tbit	673.41ps	696.60mV	170.0m*Tbit	13	89.6ps

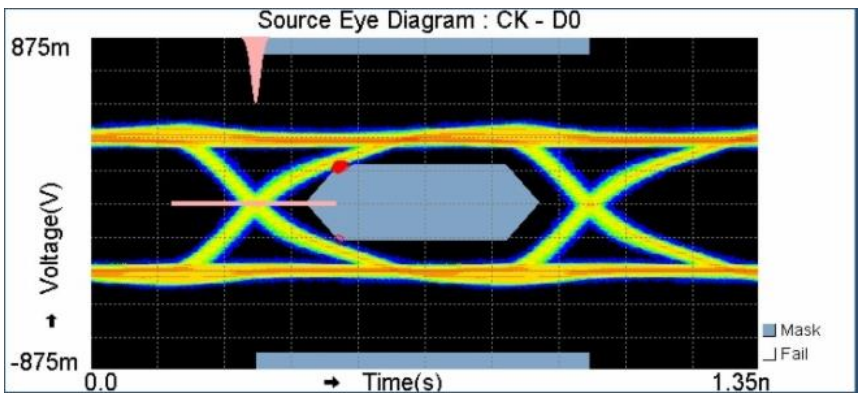

Fig. 18, Nikabe 0.5m Cable Source Eye Diagram: CK-D0 waveform.

Nikabe 1.0m High-End and generic 1.0m HDMI cable Test Report:

Table 11, Nikabe 1.0m vs. generic 1.0m HDMI Cable Source Clock Jitter test results.

Spec Range	Meas. Value	Tbit	Vs	Margin
Clock Jitter < 0.25*Tbit; Nikabe 1.0m	0.115*Tbit	673.41ps	696.96mV	0.14*Tbit
Clock Jitter < 0.25*Tbit; generic 1.0m	0.131*Tbit	673.41ps	674.56mV	0.12*Tbit

Table 12, Nikabe 1.0m vs. generic 1.0m HDMI Cable Source Eye Diagram CK-D0 test results.

Spec Range	Meas. Value	Tbit	Vs	Margin	Mask Hits	Data Jitter
Data Jitter < 0.3*Tbit; Nikabe 1.0m	0.14*Tbit	673.41ps	689.44mV	164.5m*Tbit	2.2890k	91.2ps
Data Jitter < 0.3*Tbit; generic 1.0m	0.18*Tbit	673.41ps	655.32mV	122.4m*Tbit	30.538k	120ps

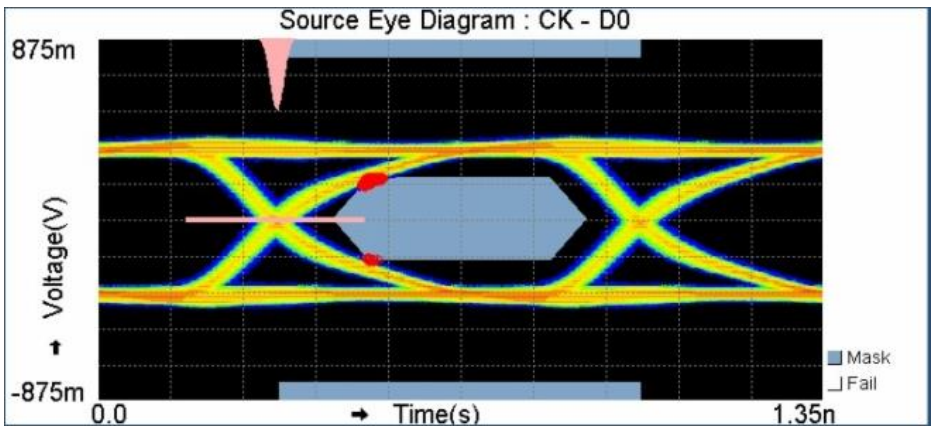

Fig. 19, Nikabe 1.0m HDMI Cable Source Eye Diagram: CK-D0 waveform.

Nikabe 2.0m High-End and generic 2.0m HDMI cable Test Report:

Unfortunately the generic 2.0m HDMI didn't work in the HDMI test fixtures that goes into the oscilloscope for some reason still unknown. Therefore only the test result for the Nikabe 2.0m HDMI cable is displayed.

Table 13, Nikabe 2.0m vs. generic 2.0m Cable Source Clock Jitter test result

Spec Range	Meas. Value	Tbit	Vs	Margin
Data Jitter < 0.3*Tbit; Nikabe 2.0m	0.131*Tbit	673.41ps	667.52mV	0.12*Tbit

Table 14, Nikabe 2.0m vs. generic 2.0m Cable Source Eye Diagram CK-D0 test results.

Spec Range	Meas. Value	Tbit	Vs	Margin	Mask Hits	Data Jitter
Data Jitter < 0.3*Tbit; Nikabe 2.0m	0.19*Tbit	673.41ps	653.20mV	112.7m*Tbit	182.12k	126ps

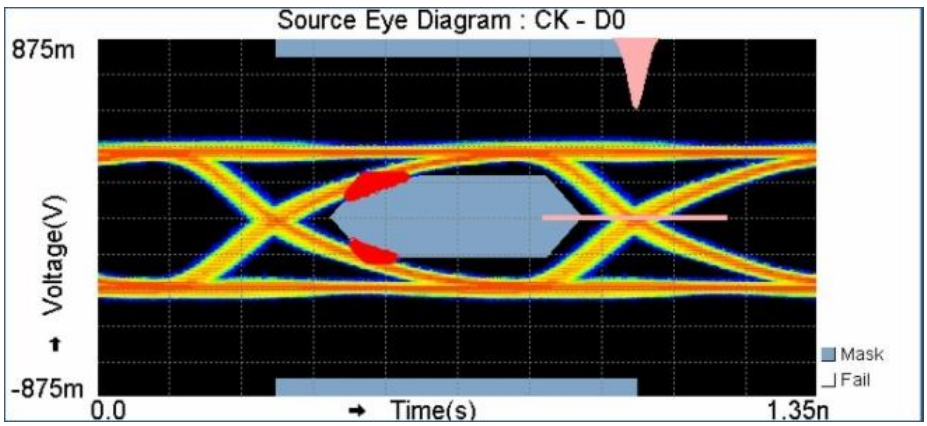

Fig. 20, Nikabe 2.0m (top) vs. generic 2.0m (bottom) Cable Source Eye Diagram: CK-D0 waveform.

Nikabe 3.0m High-End and generic 3.0m HDMI cable Test Report:

Table 15, Nikabe 3.0m vs. generic 3.0m Cable Source Clock Jitter test results.

Spec Range	Meas. Value	Tbit	Vs	Margin
Data Jitter < 0.3*Tbit; Nikabe 3.0m	0.148*Tbit	673.41ps	794.24mV	0.1*Tbit
Data Jitter < 0.3*Tbit; generic 3.0m	0.144*Tbit	673.41ps	783.36mV	0.11m*Tbit

Table 16, Nikabe 3.0m vs. generic 3.0m Cable Source Eye Diagram CK-D0 test results.

Spec Range	Meas. Value	Tbit	Vs	Margin	Mask Hits	Data Jitter
Data Jitter < 0.3*Tbit; Nikabe 3.0m	0.24*Tbit	673.41ps	793.80mV	59.59m*Tbit	353.14k	162ps
Data Jitter < 0.3*Tbit; generic 3.0m	0.24*Tbit	673.41ps	783.96mV	60.53m*Tbit	326.85k	161ps

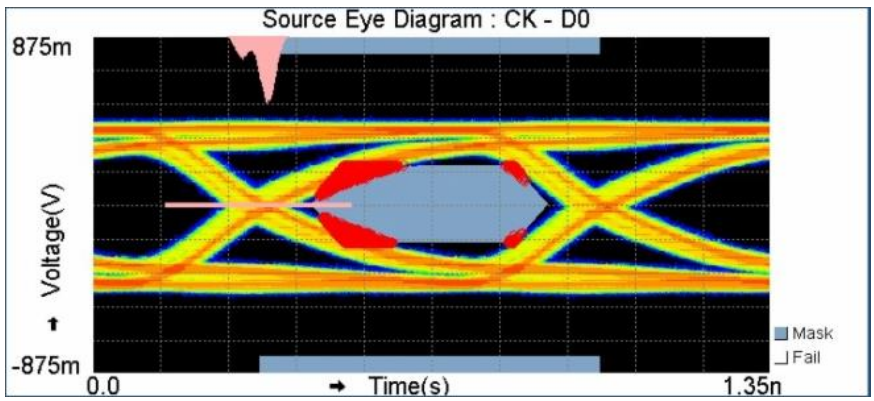

Fig. 21, Nikabe 3.0m Cable Source Eye Diagram: CK-D0 waveform.

Clicktronic 15.0m High-End HDMI cable Test Report:

Table 17, generic 3.0m Cable Source Clock Jitter test results.

Spec Range	Meas. Value	Tbit	Vs	Margin
Data Jitter < 0.3*Tbit; Clicktronic 15.0m	0.207*Tbit	673.41ps	777.60mV	69.34m*Tbit

Table 18, Clicktronic 15.0m Cable Source Eye Diagram test results.

Spec Range	Meas. Value	Tbit	Vs	Margin	Mask Hits	Data Jitter
Data Jitter < 0.3*Tbit; CK – D0	0.44*Tbit	673.41ps	661.56mV	-144.7m*Tbit	3.3770M	299ps

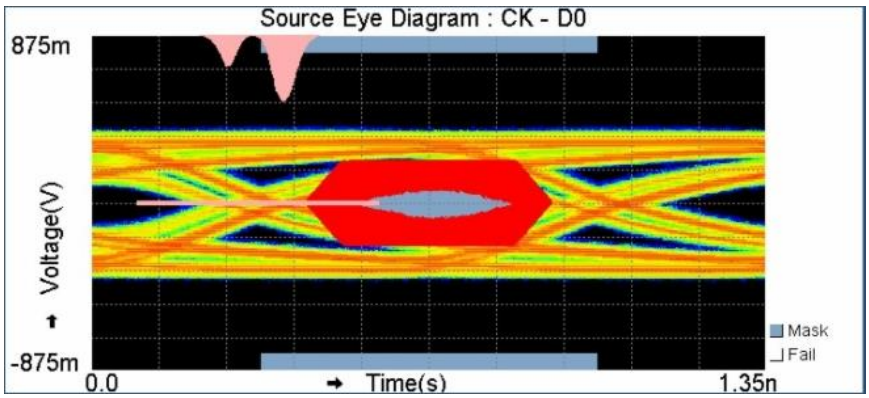

Fig. 22, Clicktronic 15.0m Cable Source Eye Diagram: CK-D0.

Conclusion and Discussion

It becomes apparent that with increasing lengths of cable the amount of corruption from parasitic capacitances is substantial. It is clearly seen in the beginning of the eye formation, taking longer and longer time to charge up to the high voltage level. 15m HDMI cables is the longest running cables recommended to use without a repeater and when looking at the eye diagrams it is easy to understand why. After a distance of 15m the jitter and measured Tbit is very corrupted and the eye is barely open, it is surprising that the image gets shown correctly on a monitor.

When it comes to comparing High-End and no-name HDMI cables the differences are small. Since there is no consistent value in the high-end cables outperforming the generic cables no real conclusion could be drawn. However in the 1m cables the measurements show that there was consistent better values of the high-end cable, in both data jitter and how open the eye was. The generic 2m cable didn't work together with the oscilloscope but still displayed an image on an HDMI monitor, which makes it not as robust as the more expensive one. With the 3m cables in some measurements the generic cables outperformed the high-end cables and showing consistently lower values of data jitter, but overall the signal integrity seemed to be on par.

The most important proof from the measurements is that the clock jitter test seems to be redundant. All of the measurements passed the specification without any problems what so ever and in order to save time in the development this test will be skipped. Another thing to notice is that all the data channels behave much the same and it is therefore only necessary to provide measured data over one channel. The channel CK-D0 was chosen as development pairs and it is safe to assume that all the other channels performs in a whole in the same manner. The tests above also gives very important information regarding how well the signal integrity is maintained over distances and would be excellent benchmark diagrams used in comparisons under development. For instance given a signal from a prototype it can be established how much equivalent distance of cable is it comparable with. For an easy comparison it could be possible to say "the prototype added corruption to the original path equivalent to x meters of cable".

3.2. Extending HDMI over PCB

Question: Is it possible to extend the signal over PCB with impedance matching without any major signal interference?

To answer this question it was designed a PCB with one HDMI input and one HDMI output and the signals are ran straight over. The characteristic impedance over the lines are 50Ω (single ended)/100Ω (differential), just as they would be in a HDMI cable. There is no need for any termination either at the input or output since both source and sink are HDMI compliant devices. The PCB design can be visualized below in Fig. 23 and the schematic can be viewed in the appendix.

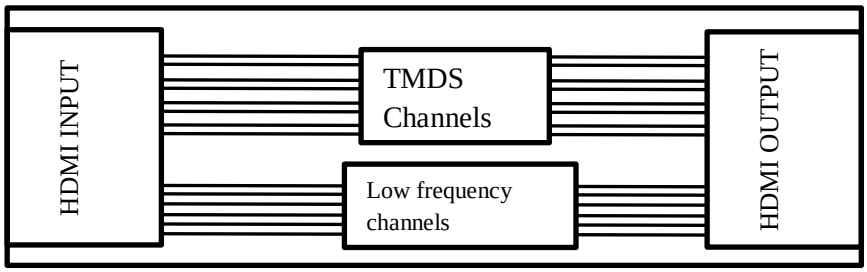

Fig. 23 block diagram over the PCB extension.

The printed circuit board was designed with HF differential signaling guidelines as described in chapter 2.2.3.

3.2.1. Material and method

Material:

- Two female HDMI type A connectors
- HDMI cable
- HDMI source
- Tektronix DSA7125C Oscilloscope
- Wilder Technologies HDMI Type-A test plug adapter

For the development in this project it is enough to relate the signal quality to a known waveform of good integrity. It is also very important to standardize comparisons between different test results; for instance how to determine superiority between two different test results. In this project it was chosen to relate the results to that of the best performing short distance HDMI cable; according to our tests the best cable on hand is the Nikabe 0.5m High-End

HDMI cable. This in practice means that the results from the device under test (DUT) is going to be compared to the signal at the end of the Nikabe 0.5m HDMI cable. The benchmark signal quality is determined to be high, since the source providing the signal passes HDMI standard test specification; it is the shortest running commercial available cable length and the cable itself is of considered high quality (24k gold plated contacts, oxide free copper wiring, triple layer shielding).

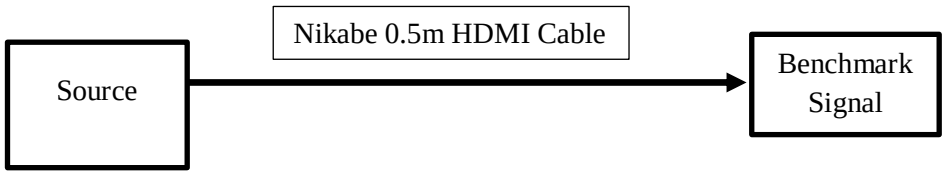

Fig. 24 diagram over how the benchmark signal was created.

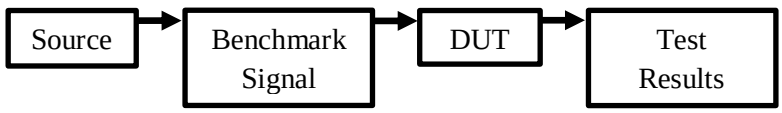

Fig. 25 The full test chain where the device under test is the extension.

With this setup it is very easy to see how much the DUT affects the signal and making comparison between signals standardized.

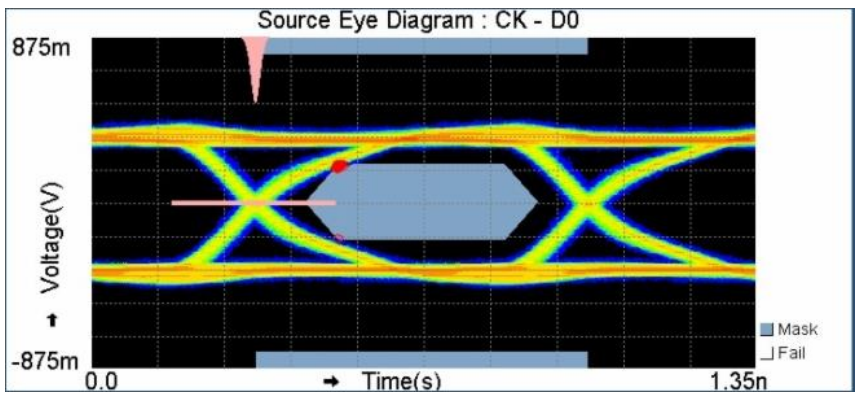

Fig. 26 Nikabe High-End 0.5m HDMI cable: 1080p 60Hz 8-bit Benchmark Signal.

Table 19 Nikabe 0.5m benchmark signal key data D0-CK

Spec Range	Meas. Value	Tbit	Vs	Data Jitter
Nikabe 0.5m	0.12*Tbit	673.41ps	686.40mV	83.4ps

The eye diagram waveform and table above shows the described benchmark signal which is going to act as comparator. For a more detailed test specification refer to the prior full test report of the 0.5m Nikabe HDMI cable. The configuration is the same as prior in the report: Clock frequency is 148.499MHz, Resolution is 1920x1080p 8-bit and the refresh rate is 60Hz.

3.2.2. Results

Table 20, HDMI-LAB-PCB: Extender Source Eye Diagram test results.

Spec Range	**Meas. Value**	**Tbit**	**Vs**	**Margin**	Data Jitter
Data Jitter < 0.3*Tbit; CK – D0	0.19*Tbit	673.41ps	841.08mV	113.3m*Tbit	126ps

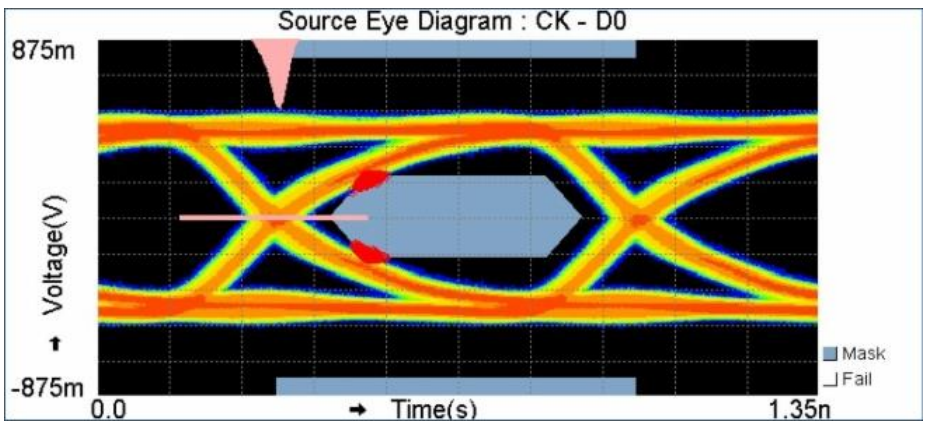

Fig. 27, HDMI-LAB-PCB: Extender Output Eye Diagram: CK-D0.

3.2.3. Conclusion and Discussion

From the eye diagrams it is possible to see that extending the signal path over the PCB does degrade the signal, most noticeable that the intensity fields are much wider. The increase in time taken to reach a high voltage level is most likely due to insertion to extra parasitic capacitances that need to be charged. According to the measurement in this given test the added corruption is not substantial but quite noticeable, and it can be seen as an initial warning that insertion of additional board components must be chosen with care. If there is noticeably added PCB parasitic capacitance without any board components inserted, it is assumable that this effect will be further increased with increased circuit complexity. According to a whitepaper made from a high frequency expert at Texas Instruments [20] designers need to be extra careful designing circuits for applications with higher than 200MHz of bandwidth due to PCB parasitics. Extracting PCB parasitics is a quite difficult process even for experienced engineers and in order to exactly account for them there is many extraction techniques that should be simulated before production. However for this project it is enough to follow common high speed PCB layout techniques to keep the capacitances and inductances low enough.

A surprising fact is that when comparing the output signal to the benchmark signal the voltage swing has increased across all channels, for instance looking at CK-D0 data pairs the swing increased from 686.40mV to 841.08mV. As said previously, looking at the intensity fields we can see that they are allot wider after the PCB extension. This effect is attributed to the introduction of signal impedance mismatch. This is known as over- and undershoot and is mostly attributed to the added capacitance, inductance and small deviations in the resistance in the PCB. This is the first proof of the effect in our measurements and since the PCB designer kept in mind that the application is high-bandwidth the effect is not catastrophically large. Looking further at the results, the jitter of the benchmark signal was 83.4ps and after the extension the jitter was 126ps which means the added data jitter introduced on the channel CK-D0 becomes: 42.6ps. Why is the added jitter so high? After talking to the PCB CAD-designer he followed high frequency guidelines but not guidelines specifically for HDMI which usually has stricter demands. In future development I recommend following new guidelines specifically for HDMI for increased signal integrity such as less data jitter.

The result of this test overall shows great promise as extending the HDMI transmission lines over PCB does not introduce major problems. As long as the guidelines are followed the parasitic capacitances from the PCB does

not pose a threat to the continuation of the research. However to further support my claim about developing new HDMI guidelines I will show how the introduction of a via with uncontrolled impedance versus the introduction of multiple impedance controlled vias affect the signal integrity. This test was done by Texas Instrument and displayed in their whitepaper: “High Speed PCB Layout Techniques” [21].

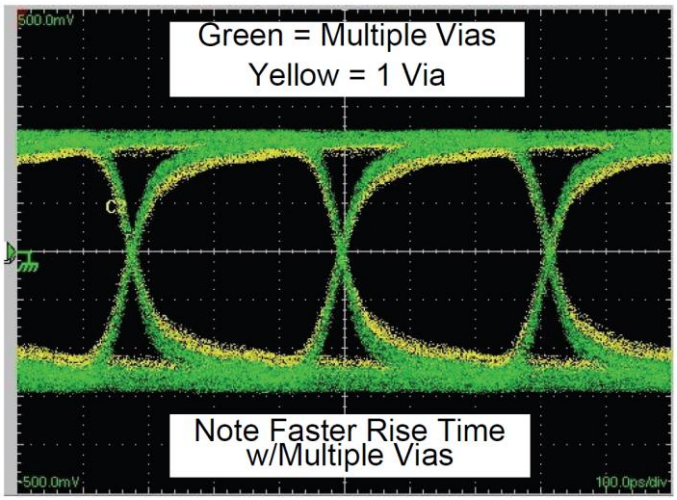

Fig. 28, multiple impedance controlled vias (green signal) vs. a single “normal” via and the effect it has on the rise and fall times in the signal. This was implemented on 7.1cm PCB traces with a 3.125GHz signal **[21]**.

In the eye diagram we can see how that even though the green signal has several vias introduced on the signal paths it has faster rise and fall times compared to that of a signal where only a single via exists. The reason is because the vias introduced on the green signal are impedance controlled and the via introduced on the yellow signal is not. This shows that even small changes in the PCB layout has large effects on the signal integrity.

Note for Axis: Make PCB Layout guidelines specifically for HDMI, it might save allot of time for the engineers trying to improve signal integrity.

3.3. Dividing the Signal

Simply dividing the HDMI signal would seem to be a convenient way to quickly achieve a copy. When monitoring network traffic over CAT5/6 cables this is the technique used and signal integrity is maintained in spite of the intrusion. This chapter tests whether or not this is possible to achieve over HDMI. There are a few splitters on the market that are passive and according to their marketing material works well. However when reading reviews of such products customers often complain for instance lack of sound, bad compatibility between devices and artifacts in the image [22].

3.3.1. Material and method

Material:

- Custom PCB (see appendix for schematic).
- Two female HDMI type-A connectors soldered to the PCB.
- HDMI cable.
- HDMI source.
- Tektronix DSA7125C Oscilloscope.
- Wilder Technologies HDMI Type-A test plug adapter.

Below in Fig. 29, is a block diagram explaining the desired test setup.

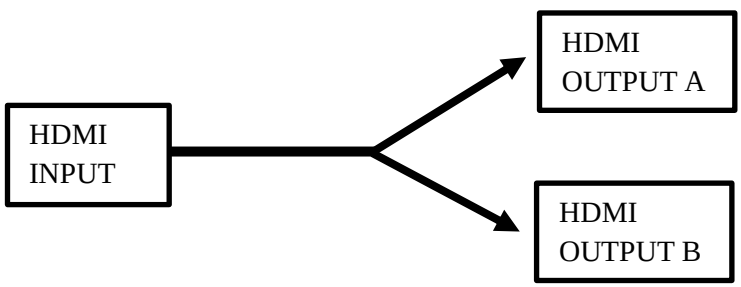

Fig. 29 block diagram over simply dividing the HDMI signal.

Also please refer to the Appendix for a computer aided design over the PCB as it was sent to be manufactured.

As before the signal sent into the HDMI input is the known benchmark signal in order to establish the amount of degradation in signal integrity imposed by the custom PCB. The signal being sent is the benchmark signal described in the before chapter. It is the signal measured from an Asus computer and ran through a 0.5m Nikabe High-End HDMI cable (thoroughly tested in chapter 3.1).

3.3.2. Results

Only presenting the results for Output A, because the waveform on both outputs was mostly identical.

Table 21, LAB-Simple-Split-PCB: Output A vs. Output B Eye Diagram CK-D0 test results.

Spec Range	Meas. Value	Tbit	Vs	Margin	Mask Hits	Data Jitter
Data Jitter < 0.3*Tbit; output A	0.16*Tbit	1.3482ns	520.00mV	135.7m*Tbit	549.06k	174ps

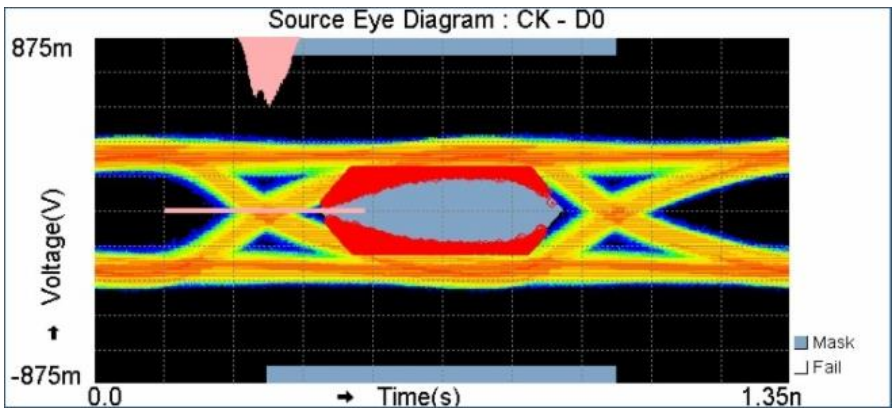

Fig. 30, LAB-Simple-Split-PCB: Output A Eye Diagram: CK-D0 waveform.

3.3.3. Conclusion and Discussion

From the eye diagrams and the measured values it can be clearly seen that simply splitting the signal, even when following HF design guidelines, introduces a vast amount of signal corruption. While using short distance cables, 0.5m – 1.0m, this type of splitter works, most of the time. Sometimes there is artifacts in the image and the sound works with some

devices and not at all with others. If running longer cables this method of splitting a HDMI signal will not work at all, because since both the receivers are sharing the same electrical signal. Is this an acceptable solution is running short distance cables? That depends, but in this project it is not since we wanted to have the original path signal as little affected as possible and the sniffed signal be a very similar copy.

The most important information from this test is in the fact that this type of solution works with short distance cables. That shows that the system is very robust and not as sensitive as previously believed. Even a very low quality signal will be delivered to the sink and displayed correctly.

4. Operational Amplifiers

After a discussion with Associate Professor, PhD Markus Törmänen at LTH EIT, an initial solution was worked out using operational amplifiers to sniff the HDMI signal. Operational is one of the most useful circuits in electronics due to its high versatility. In general IC op-amps are cheap to buy and have key characteristics that fit into data acquisition i.e. our sniffing application. Some of these key points are in an ideal situation [23]:

- Infinite input impedance
- Zero output impedance
- Zero input offset voltage
- Infinite open-loop gain
- Infinite bandwidth with no phase shift
- Zero noise

The most common OP-amps used today are single ended, which means that they amplify a signal relative to a reference ground (usually Zero). Hence the common single ended OP-amp has two inputs (signal and ground + negative feedback) and one output (amplified signal).

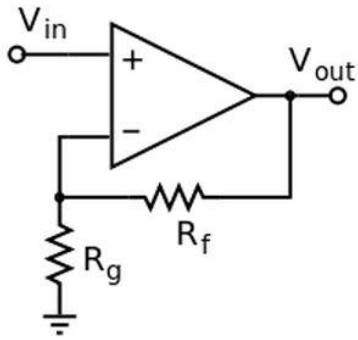

Fig. 31, non-inverting operational amplifier with negative feedback.

However since the TMDS signals used in the HDMI standard are differential it would be reasonable to use for each channel an Operational amplifier that is fully differential i.e. an OP-amp with two inputs (negative/positive) and two outputs (negative/positive). The ideally high input impedance is crucial in the sniffing application because that means that our amplifier circuit would not draw any current from the original path at the inputs.

4.1.1. The Fully Differential Operational Amplifier

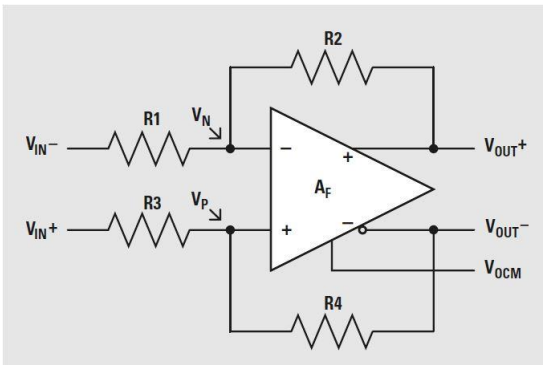

Fig. 32, schematic of a Fully Differential Operation Amplifier **[24]**.

As always when applying theory in practice it differs substantially and we need to take this into consideration when selecting suitable components.

In real world applications the ideal characteristics are translated into [25]:

- **Finite input impedance -** The input impedance of the selected amplifier needs to be high enough that we do not disturb the original path.
- **Nonzero output impedance** – In this project it is needed to match output termination with characteristic impedance equaling to 50Ω single ended or 100Ω differentially.
- **Input offset voltage** – Even if the voltage on the inputs are the same the amplifier will produce an output.
- **Finite gain** – The FDA will have an upper limit of how much it can amplify the input signal. Typically set by the ratio between the input impedance and internal or external feedback resistance.
- **Input bias current –** There will be a small amount of current flowing into the inputs.
- **Finite bandwidth -** There is a limit to how high frequency the amplifier can handle due to internal frequency compensation limitations.
- **Input capacitance –** In high frequency applications this causes a reduced open loop bandwidth.
- **Saturation –** The maximum output voltage is limited to a peak value (not a problem in this project application but worth mentioning).
- **Slewing –** The maximum rate of change in the signal at the output is limited i.e. the signal on the input might be changing faster than the amplifier can represent it at the output. Especially in high-speed situations this property might present itself clearly, so it is something that might be a problem later on.

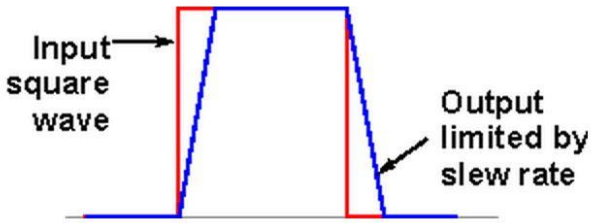

Fig. 33 Op-amp slew rate illustration **[26]**.

For a full circuit analysis of fully differential amplifiers I recommend reading the white paper from Texas Instruments: "Analysis of fully differential amplifiers" by Jim Karki [24].

The way to approach the bandwidth requirement of the OP-amps:

HDMI links have three differential data signals and a differential clock and each TMDS byte is 10 serial bits. The pixel clock frequency in the 1.3 HDMI standard is specified to have a 340MHz cap. The clock is not a bit clock, it is a byte clock (10-bit bytes), i.e clock frequency is 1/10 of the data rate, or 1/30 across all channels. So if the clock rate is 340MHz each channel is transmitting at a frequency 10x faster eg. 340MHz * 10 = 3.4GHz single channel data rate. Since the OP-amps are specified after reconstructing a sinusoidal wave we need at least twice the bandwidth of the signal speed. That means to reconstruct the signals over the full signal span the OP-amps need to have a minimum bandwidth of 3.4GHz * 2 = 6.8GHz.

Following this reasoning the LMH3401 and LMH5401 is good choices and if a compromise is needed to be made we need to look at the actual data rate for 1080p@60Hz.

From the HDMI specification we can gather information and calculate the data rate for 1080p video:

$$(Hsync + Hor\ blank\ pixels) * (Vsync + Ver\ blank\ pixels) * colorspace * refreshrate = Total\ Gbps\ bandwidth$$

Equation 2, calculation to determine the total bandwidth for HDMI per channel. Note: that the Audio is multiplexed into the channels and do not add to the bitrate.

We need to keep in mind that the TMDS encoding makes an 8 bit byte into a 10 bit byte, normally used is 8bit color for each pixel on each channel (red, green, blue) but in TMDS it would be 10bit color depth per channel totaling to 30 TMDS-bits or 24bit in normal encoding. Number of horizontal blanking lines at 1080p is 280pixels and vertical blanking lines are 45pixels. Keeping this in mind we get the following expression for the channel bandwidth:

$$(1920 + 280) * (1080 + 45) * 10 * 60 = 1.485Gbps$$

Equation 3 number populated equation for TMDS channel bandwidth.

Since the clock frequency is 1/10 of the channel data rate the clock frequency would total to 148.8MHz. These calculations were confirmed by looking at the measured clock frequency in the oscilloscope.

Now that the data bandwidth for 1080p@60Hz with 24-bit color depth has been established we can re-specify the demands on out OP-amps: 1.486GHz times two is 2.972GHz.
Final conclusion: 340MHz is the maximum system clock in the 1.3 HMDI specification, the data on one channel will be maximum 3.4GHz and the OP-amp needs to handle twice of that totaling to a minimum specified bandwidth of 3.4GHz * 2 = 6.8GHz.

Minimum slew rate:
Since the bandwidth has been identified it is useful to also specify the minimum slew rate.

$$Slew\ Rate = 2\pi fV$$

Equation 4, determines the minimum required slew rate for an amplifier, where f = max signal frequency (Hz) and V = max peak voltage of the signal **[26]**.

Equation 2 above, with the values f = 3.4GHz and V = 875mV, gives the Slew Rate = 18 694.9 V/µs. This is the number to cover the whole HDMI 1.3. Specification, the actual slew rate needed to construct the sniffer is allot lower.

5. Case Studies: Part 2

The proposed sniffing solution was using fully differential operational amplifiers and two schematics featuring two different amplifiers from Texas Instruments was developed. Both have a very high specified bandwidth 7GHz for the LMH3401 and 8GHz for the LMH5401 and they fulfill our requirement of 6.8GHz. The reason for choosing two different amplifiers with similar specified bandwidth is that we want to research the impact of the amplifiers input resistance. They both fulfill our bandwidth requirements but they differ at the inputs regarding their impedances.

Table 22, key characteristics comparison of the implemented amplifiers **[27] [28]**.

	Bandwidth	Slew Rate	Supply Voltage	Max Input Impedance (Differential)
LMH3401	7GHz	18000V/µs	±2.5V	Min: 22Ω Typ: 25Ω Max: 29Ω
LMH5401	8GHz	17500V/µs	±2.5V	4600Ω (open loop)

The reason for choosing amplifiers with such high bandwidths is to cover the whole specification with a pixel clock frequency set at 340MHz. From Table 22 above the most important difference between is the difference in input impedance. In one aspect it is desired to have as high input impedance as possible to minimize the intrusion (leak current) on the original path. However due to the high frequencies the high resistance might create signal reflections that might corrupt the circuit. Hence choosing one amplifier with low input resistance and one amplifier with higher input resistance has relevant research value. Because the amplifiers otherwise have the same specification we have the ability to compare the results, high versus low input resistance and the effect it has on the circuit.

5.1. FDM – LMH3401

Please refer to the appendix to view the schematic design over the circuit.

Throughout this chapter, pictures and equations are, unless stated, taken from the LMH3401 datasheet [27].

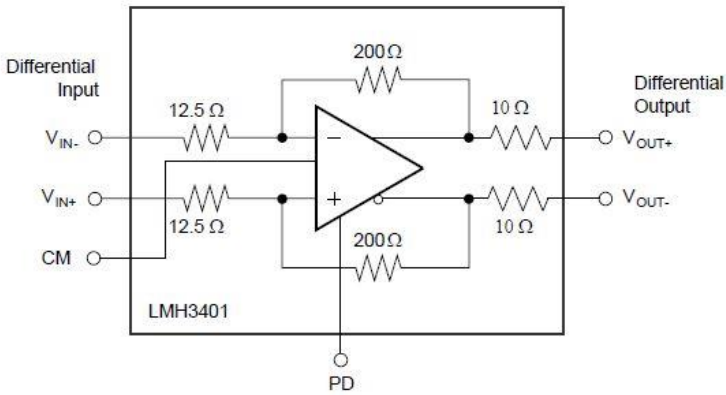

Fig. 34, functional diagram over the LMH3401 op-amp.

The TI LMH3401 is a very high-performance fully differential operational amplifier specially developed for high-speed applications. It has an on-chip 200Ω feedback resistor (R_F) which cannot change. While this simplifies the implementation on the printed circuit board (PCB) it removes the freedom to manually set R_F, which might prove to be troublesome while setting the gain. In the event that a higher input resistance is needed, this particular point (fixed R_F) is going to be the biggest disadvantage of this amplifier. Since the gain is determined by:

$$A_v = \frac{200\Omega}{R_{In} + 12.5\Omega}$$

Equation 5, the gain equation for the LMH3401.

A_v – Gain factor, the amplification factor at the output.
R_{In} – The impedance value of the input resistor to the amplifier.

It is clearly shown by the equation 5 above that if we want to increase the resistance on the input the gain will decrease.

However since the purpose of choosing this amplifier is to look at a low input impedance amplifier and its effects, this is not going to present itself as a big issue. Because if it is needed to increase the resistance on the input, for any reason, it follows that this amplifier is not suitable in this specific application.

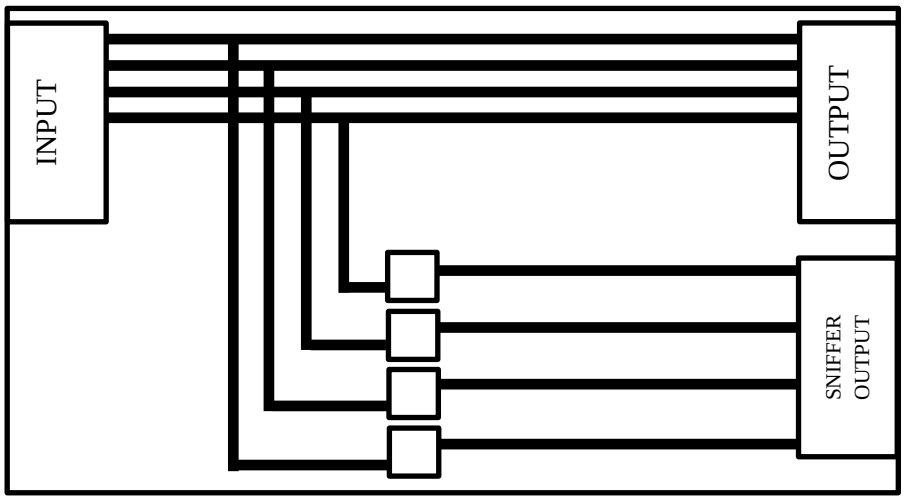

Fig. 35 block diagram over the circuit where the small squared are Fully Differential Amplifiers and the signals are differential, low frequency lines omitted.

5.1.1. Material and Theory

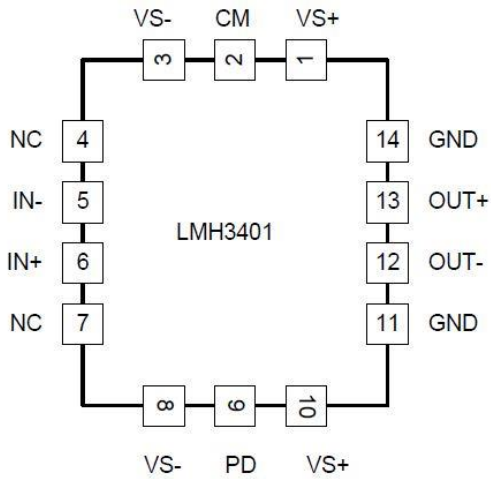

Fig. 36. Pin configuration of the LMH3401 OP-amp.

PIN 1, 3, 8 and 10 – Power to the amplifier.
PIN 5(IN-) and 6(IN+) – Differential input signal.
PIN 13(OUT+) and 12(OUT-) – Differential output signal.
PIN 2(CM) – Output common-mode voltage control input.
PIN 9(PD) – Power down: High = sleep, Low = active.

Before going into the schematic it could be of importance to first shortly go through what we want to achieve with the design. The most important requirement on the project is that the device is merely going to listen to the signals on the original path. Therefore on the PCB the HDMI signal is going to travel from an input to an output without any electronics in between, this is the original path.

On the TMDS signal paths we want insert the amplifiers as gently as possible. It has been solved on the PCB in a way that the signal will travel from input on one side of the board and then through vias down onto the other side of the board and continue to the output. As close as possible to the via holes the amplifiers are connected.

For the schematic see the attached appendix, below in Fig. 37 is presented a close-up of the Computer Aided Design (CAD) model over the amplifier and its surrounding components on one channel. The CAD modeling was done by Ola Welin, Engineer at the PCB CAD department at Axis while following HDMI design guidelines. The most important is that all the TMDS data channels need to be the same length so that the signals arrive at the same times and all the transmission lines need to be impedance matched to the characteristic impedance for HDMI.

Please refer to the appendix for the full schematic and CAD over the circuit.

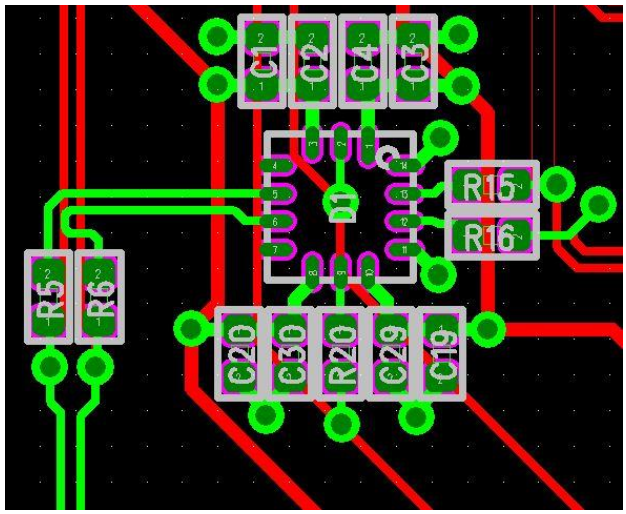

Fig. 37 close-up of the PCB implementation of the LMH3401 on one TMDS data channel.

In the close-up (Fig. 37) above we can see how the amplifier is implemented on the one of the TMDS differential signal channels (They are identically implemented on all of the four channels). The two green signal lines running from the left bottom corner in the picture is the HDMI data signal coming from the input. The round holes before the input resistors (R5 and R6 in the picture) is the via which allows the signal to travel to the other side of the PCB and continue to the original path output. From the input resistors the signal travels into the differential input on the amplifier. The decoupling capacitances on the top and bottom of the amplifier is chosen from the recommended values from the datasheet. They are present to remove noise on from the power supply lines. Since the amplifiers are

symmetric around the inputs it is usually easier and faster to talk about each side separately i.e. the single ended properties.

The starting point values of the components are (single ended):

Table 23, starting values on the components for the LMH3401 op-amp.

Component	**Value**
R_{IN}	39Ω
C_{VCC1}	10nF
C_{VCC2}	2nF
R_{OUT}	39Ω

The resistors were chosen to first initially match the characteristic impedance specified for HDMI (50Ω single ended). R_{IN} together with the internal impedance of 12.5Ω gives us the total input resistance of 51.5Ω (single ended), which is close enough. The same reasoning is applied to the output with the difference that the internal output resistance is 10Ω which totals the output resistance to 49Ω (single ended).

The component values used in this project are all standard and while it would be possible to use more specified values e.g. R_{IN}/R_{OUT} = 37.5Ω/40Ω totaling the input/output resistance to exactly 50Ω, it is not prioritized. The reason for this is because of productification process. In the event that this would be implemented into a real product the cost would greatly increase due to the need of special ordering custom made resistors.

Throughout the PCB there has also been implemented a few 0Ω resistors to be able to connect and disconnect features on the same PCB:

- On the PD-pin of the amplifier there is the possibility to connect an external power and or other components. This could be of interest if there for any reason is a desire to power down the amplifier without cutting the source power supply.
- Between the original path and the low frequency channels: CEC, Utility, SCL, SDA, and HPD. In this project these channels are not interesting and most of them will be left unplugged. But for instance

of we want to test the signals on consumer devices such as a normal HDMI screen we might need to use these channels. Most notably is the Hot Plug Detect (HPD) which needs to be asserted high.

- +5V channel where it is possible to switch between using the 5V from the original path and connecting an external 5V in the event that the sniffer output draws too much power.

Other notable design characteristics is that all the resistors and capacitors have the same form factor (0402), which means that we can switch all the values and optimize the circuit to get the best performance out of the amplifiers.

The only hard requirement on the circuit is that the output of the original path must pass the HDMI test specification for source devices. With that point of view the chosen method for testing the circuit is going to be as follows:

1) Test the initial values shown in Table 23 above.
2) Test if the original path pass HDMI source tests
3) If passed, test the monitor port quality. If not increase the values of the input resistors until it passes the test specification.
4) When the original path passes HDMI test specification for source devices, try to optimize the circuit.

5.1.2. Results and Discussion

The Results was produced by iterating through a number of input resistances and then for each measuring the signal integrity. For each input impedance the results has been collected in Table 24 below. The Eye diagram from the amplifier output and original path is shown first in Fig. 38 below.

Table 24, HDMI-LAB-PCB: LMH3401; Rout = 39Ω, Source Eye Diagram CK-D0 test results ordered after increasing Ri impedance.

Rin	Spec Range	Meas. Value	Tbit	Vs	Margin	Mask Hits
39Ω	Data Jitter < 0.3*Tbit; Original Path	0.22*Tbit	673.41ps	763.68mV	78.65m*Tbit	101.79k

	Data Jitter < 0.3*Tbit; Sniffer Port	NA	456.64ps	33.300mv	NA	6.5652M
120Ω	Data Jitter < 0.3*Tbit; Original Path	0.15*Tbit	673.41ps	573.52mV	151.3m*Tbit	228.12k
	Data Jitter < 0.3*Tbit; Sniffer Port	0.16*Tbit	673.41ps	423.36mV	0.14*Tbit	3.0334M
150Ω	Data Jitter < 0.3*Tbit; Original Path	0.18*Tbit	673.41ps	609.12mV	0.12*Tbit	234.26k
	Data Jitter < 0.3*Tbit; Sniffer Port	0.19*Tbit	673.41ps	396.80mV	0.11*Tbit	5.0698M

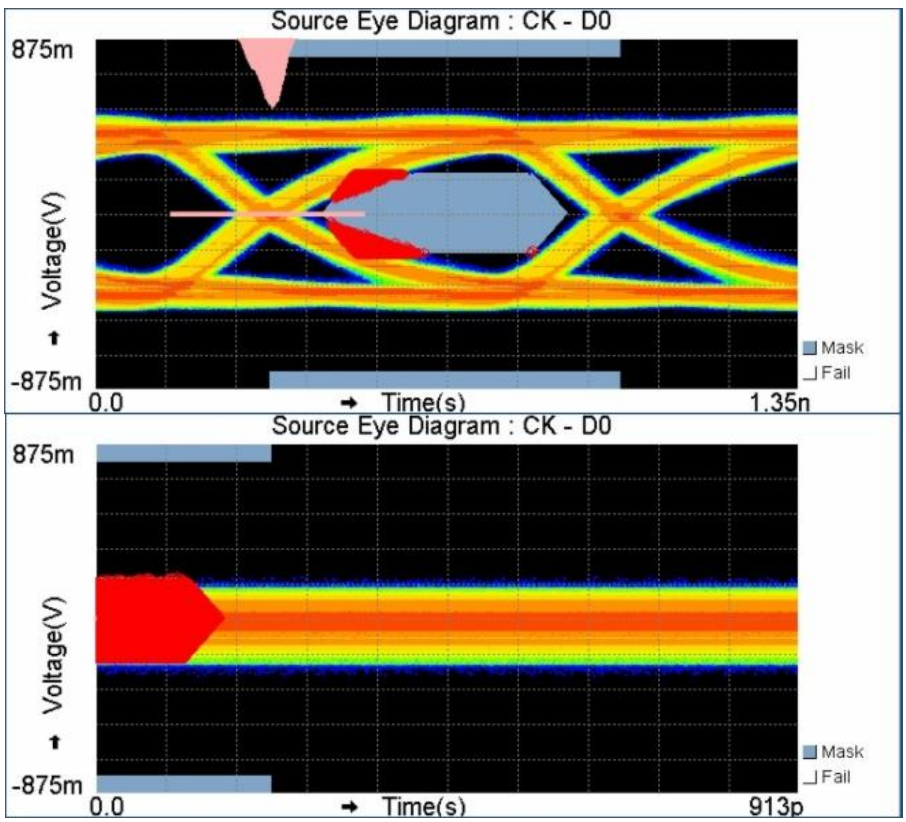

Fig. 38 HDMI-LAB-PCB: LMH3401 when Ri=39Ω; Original Path (top) and sniffer port (bottom) Source Eye Diagram: CK-D0 waveform.

For each test the signal was tested on an HDMI compliant computer monitor and for all input impedances lower than 120Ω there were pixel artifacts on the screen. Only when increasing the input resistor to 150Ω the picture became free from artifacts.

Trying to further increase the gain of the output there was some experimentation with modulation of the termination resistance Rout. For Rout=0Ω → 10Ω there was a substantial amount of signal reflections corrupting the signal. I have captured this behavior shown below in Fig. 39.

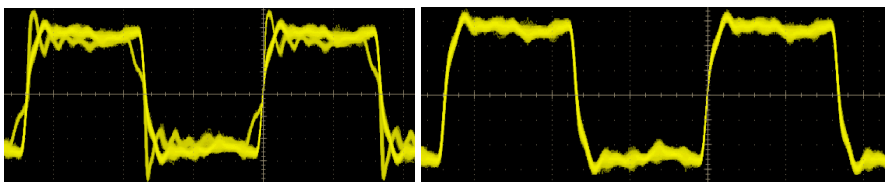

Fig. 39 Signal reflection present at the amplifier output when changing the termination resistor. The left picture is when Rout = 10Ω and the right waveform was captured when Rout = 15Ω.

Finally using Rout = 15Ω gave insignificant reflections and opened the eye with around 100mV. Following the theory it is quite strange that the output when Rout=15Ω did not show any reflections. According to the theory behind the characteristic impedance Rout needs to be around 40Ω together with the internal 10Ω adding up to 50Ω as to avoid reflections. The most probable explanation is that there was large impedance mismatch and in this particular case a 15Ω resistor worked totaling the termination resistance to 25Ω. It is not very likely that this result would be reproduced on another set of PCB and component combination. However in the end those settings gave the best working compromise laying weight to the voltage swing, robustness of the signal on the original path and picture quality when displaying the signal on a monitor.

Final ratings: Rin = 150Ω and Rout = 15Ω.

Table 25 HDMI-LAB-PCB: LMH3401; Rin = 150Ω, Rout = 15Ω, Source Eye Diagram CK-D0 final test results.

Spec Range	Meas. Value	Tbit	Vs	Margin	Mask Hits

Data Jitter < 0.3*Tbit; Original Path	0.19*Tbit	673.41ps	717.24mV	0.11*Tbit	84.982k
Data Jitter < 0.3*Tbit; Sniffer port	0.2*Tbit	673.41ps	442.88mV	0.1m*Tbit	2.6803M

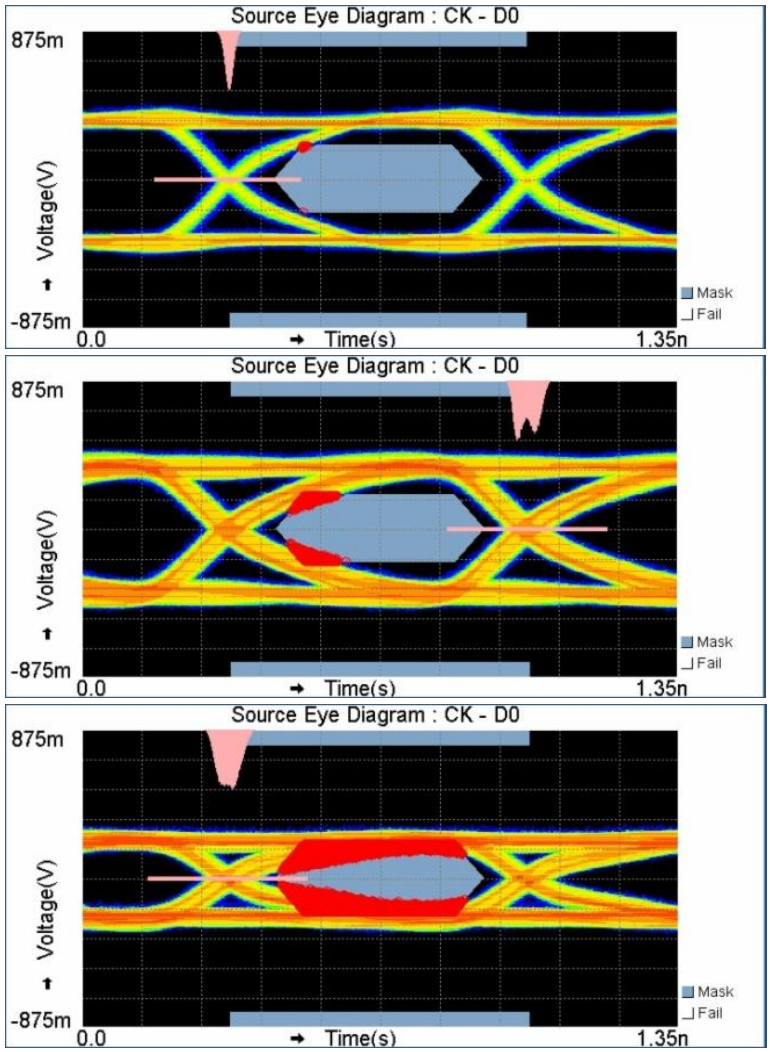

Fig. 40 LMH3401 Final Eye Diagram Test results after optimization, Benchmark (top), Original Path output (Middle), Sniffer Output (bottom).

5.1.3. Possible Improvements

The tests showed that for any input resistance to the amplifiers under 150Ω gave a significant amount of artifacts in the image outputted on the original path. Following that observation the best improvement is to have as high input impedance to the sniffer circuit as possible. Since the gain cannot be set externally with the LMH3401 further increasing the resistance is not possible due to the voltage swing on the sniffer port getting too low. It shows great promise in the development conducted in the next chapter using the LMH5401 amplifier where the input resistor and feedback resistor can be set externally and thus having the ability to increase the gain.

5.2. FDM – LMH5401

The Texas Instrument Fully Differential Operational Amplifier LMH5401 is a high bandwidth amplifier with external feedback resistor. This feature gives a significant improvement over the LMH3401 amplifier covered in Chapter 5.1.

5.2.1. Material and Theory

Please refer to the appendix to view the schematic design over the circuit.

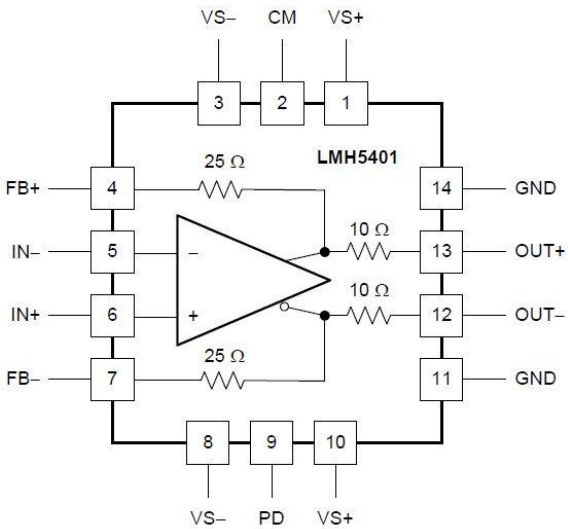

Fig. 41, TI LMH5401 FDA pin configuration with visible integrated feedback and output resistances.

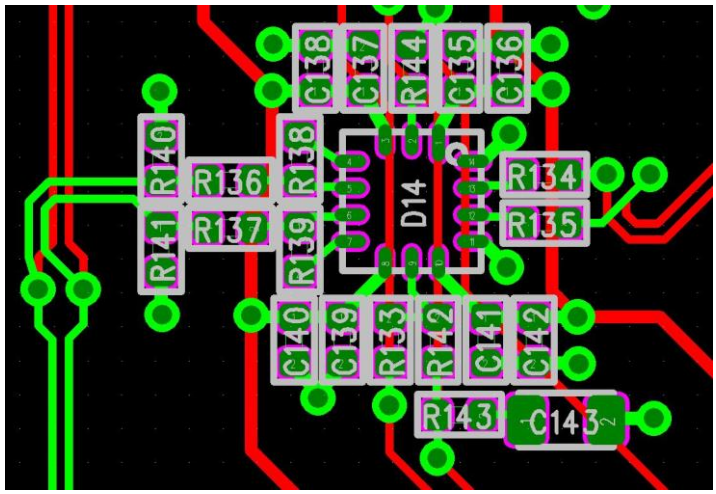

Fig. 42, CAD close-up over the LMH5401 electrical implementation on one TMDS data channel.

Rf - feedback resistor.
Ri - input resistor.
Rt - output termination resistor.
C_{VCCa} - power decoupling capacitance.
C_{VCCb} – power decoupling capacitance.

Table 26, starting values on the components for the LMH5401 op-amp (single ended).

Component	**Value**
Ri	50Ω
Rf	75Ω
C_{VCCa}	10nF
C_{VCCb}	2nF

Rt	39Ω

Using the information from using the LMH3401, that input impedances (single ended) under 150Ω yields artifacts in the image, after testing the initial values it is reasonable to immediately increase Rin to 150Ω. Further it is redundant to test the quality of the monitor port until the signal quality of the original path is satisfactory.

The output termination resistance is fixed to 39Ω to minimize reflections, if needed at the end it will be tested if changing it gives any significant increase in performance.

5.2.2. Results and Discussion

The test results are ordered after rising input impedance, as stated before the starting input resistor has the value 0f 47Ω and the feedback resistor has the starting value of 75Ω. It is included to show the process of how the gain and input impedance was optimized.

Device Configuration:

- Device Details: HDMI-LAB-PCB: FDA-LMH5401
- Clock Frequency(MHz): 148.499
- Resolution: 1920x1080p 8-bit
- Refresh Rate: 60Hz
- Record Length: 25.000M
- Termination impedance: 39Ω

Table 27, HDMI-LAB-PCB: LMH5401 Test results.

Rin	Spec Range	Meas. Value	Tbit	Vs	Margin	Mask Hits
47Ω	Data Jitter < 0.3*Tbit; Original Path; Rf=75Ω	0.18*Tbit	673.41ps	442.88mV	124.4m*Tbit	2.1865M
	Data Jitter < 0.3*Tbit; Sniffer Port; Rf=75Ω	NA	673.41ps	2.000mv	NA	6.4646M

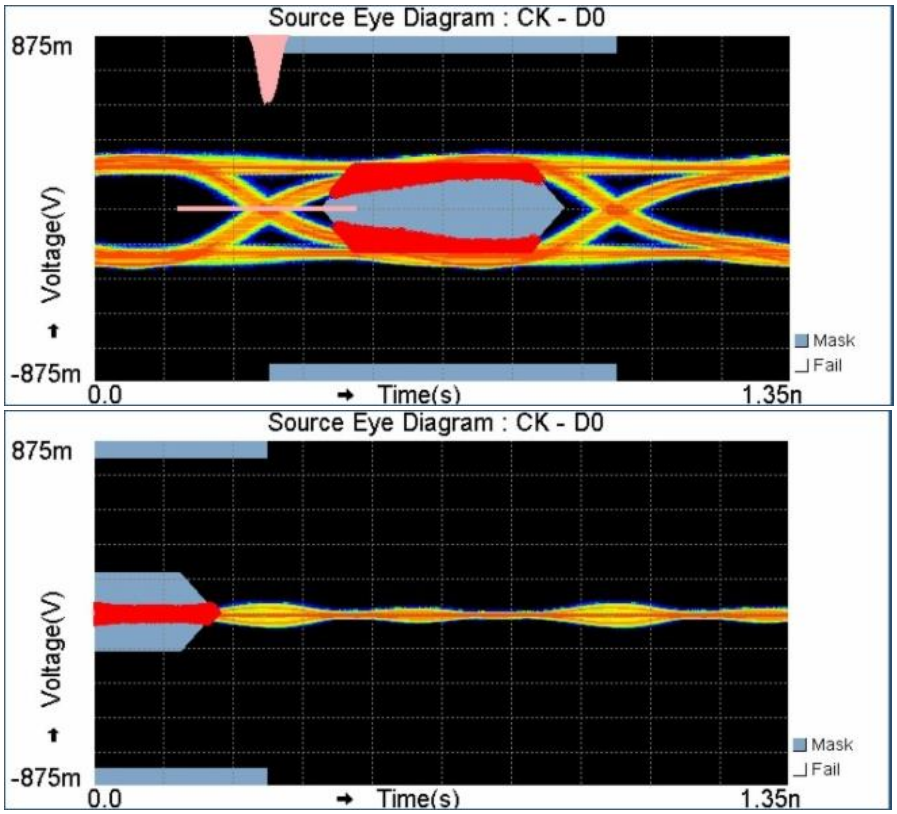

Fig. 43 LMH5401 Starting value Eye Diagram test results. Original Path output (top), Sniffer Output (bottom).

After testing Rin=220Ω there was a significant amount of ringing in the signal due to a very low feedback impedance. Even though the feedback resistor in theory should not have any impact in the original path (Ideally there is no current flowing into the feedback input) this shows that there is an amount of leakage in practice. It was fixed by increasing the value of Rf to 270Ω, this value was chosen to make no attempt in this stage to amplify the signal; before and after the increase shown below in Fig. 44:

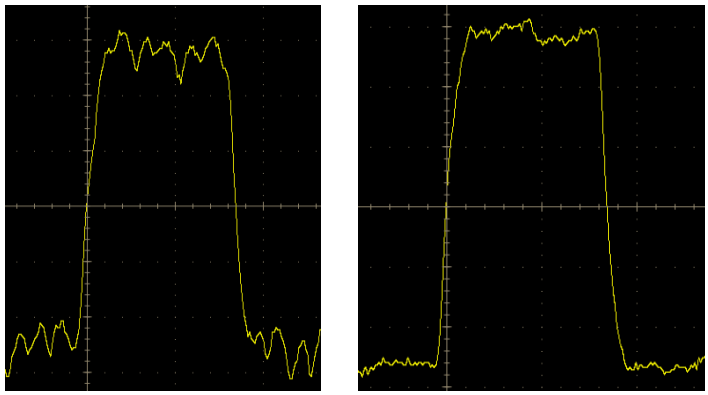

Fig. 44 Ringing response due to too low feedback resistor.

It also gave a significant increase in performance on the original path yielding an extra 100mV in voltage swing. It was also decided at this time that is was worth to start testing the quality of the sniffer port and increase the gain:

Table 28 HDMI-LAB-PCB: LMH5401 Test results.

Rin	Spec Range	Meas. Value	Tbit	Vs	Margin	Mask Hits
220 Ω	Data Jitter < 0.3*Tbit; Original Path; Rf=390Ω	0.18*Tbit	673.41ps	748.20	0.12*Tbit	33.275k
	Data Jitter < 0.3*Tbit; Sniffer Port; Rf=390Ω	0.24*Tbit	673.41ps	620mV	0.06*Tbit	768.00k
	Data Jitter < 0.3*Tbit; Original Path; Rf=470Ω	0.17*Tbit	673.41ps	677.44mV	128.0m*Tbit	108.27k
	Data Jitter < 0.3*Tbit; Sniffer Port; Rf=470Ω	NA	673.41ps	220.16mV	NA	4.7037M

When increasing the feedback impedance from 390Ω to 470Ω there is a complete loss of signal on the sniffer port and it can be concluded that due to limitations in the amplifier before the change it was operating at peak performance. After testing, further increase of the input resistance did not show any significant benefit and the best compromise was chosen with the values; Rin = 220Ω and Rf = 390Ω.

Finally modulation of the termination resistance gave an increased

performance. The amount of reflections while using the LMH5401 on the output was more sensitive than when using the LMH3401. Termination impedances between 0Ω → 27Ω had huge problems reflected signals corrupting the output signal as captured in Fig. 45 below:

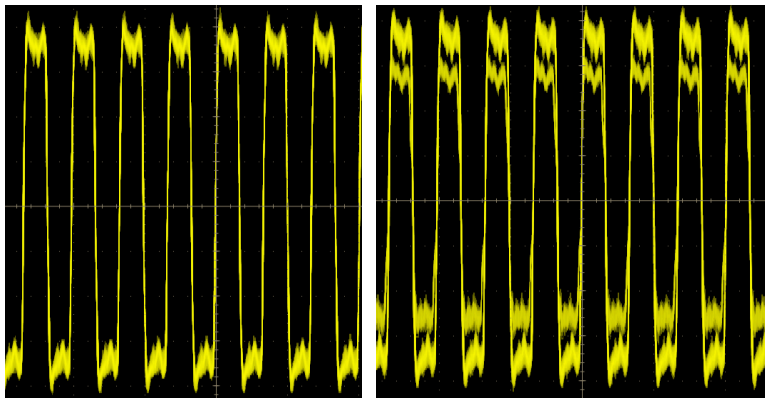

Fig. 45 Showing the output clock waveform of the sniffed signal. Left waveform did not show any reflections when Rt = 39Ω (49Ω total together with the internal resistance) compared to when Rt = 15Ω.

As shown the reflection difficulties decreases when getting closer to the termination resistance of a total of 50Ω (single ended) however it was no longer visible when reaching Rt = 33Ω (43Ω total). It also ties in with the theory that termination impedance equal to that of the characteristic impedance eliminates signal reflections but it is worth checking if there is any room for modulation.

Table 29 Final resistor values for the LMH5401 amplifier; Rin = 220, Rf = 390, Rt=33.

Rin	Spec Range	Meas. Value	Tbit	Vs	Margin	Mask Hits
220Ω	Data Jitter < 0.3*Tbit; Original Path;	0.17*Tbit	673.41ps	745.04mV	0.13*Tbit	11.769k
	Data Jitter < 0.3*Tbit; Sniffer Port;	0.27*Tbit	673.41ps	829.28mv	0.03*Tbit	108.94k

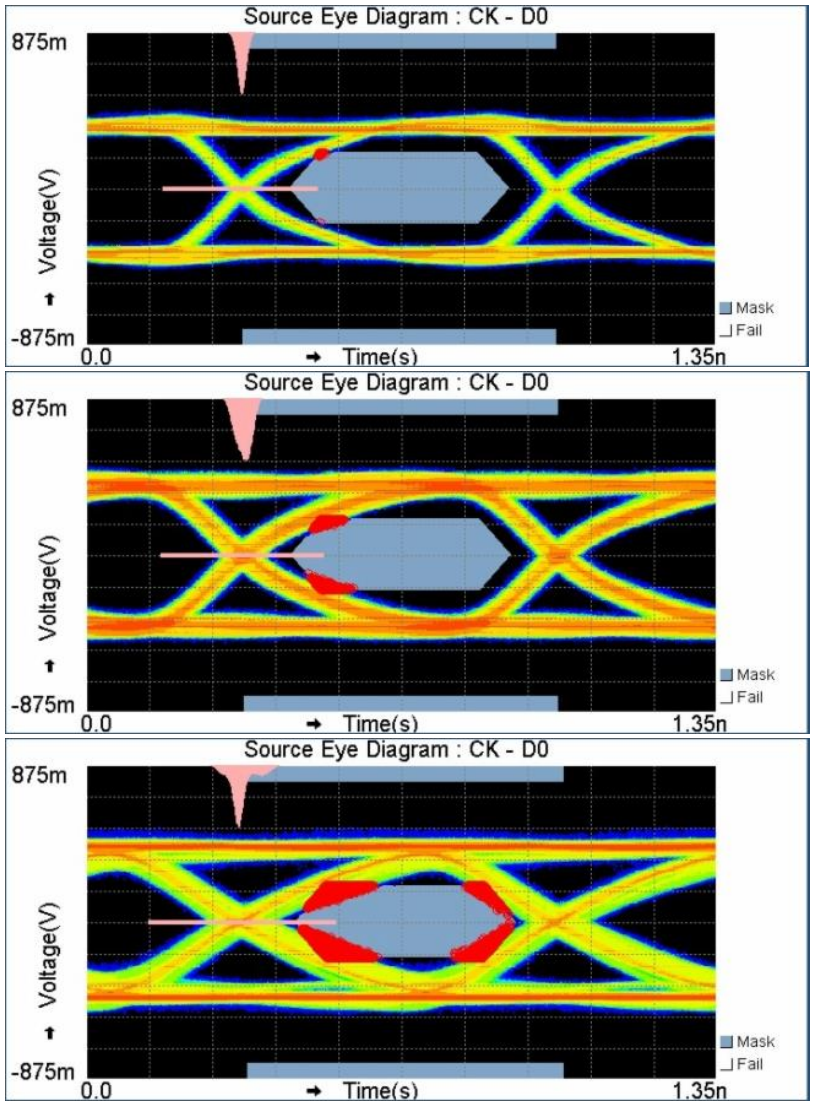

Fig. 46, comparable view over how the signal changes when sniffing with the LMH5401. Benchmark signal (top) i.e. the signal going into the PCB, Original Path output waveform (middle) and the sniffer output waveform (bottom).

After testing both the original path and sniffer output they were both were both good enough to drive 15m HDMI cables to an HDMI monitor. Since a 15m cable is the longest running cable length recommended to be used without a repeater that is considered good enough and further development improving the signal integrity is not needed.

5.2.3. Possible Improvements

The following problems with the solution stood out if this ever would be produced as a real product:

- Too expensive.
- Draws too much current.

The amplifier circuits featuring the TI LMH3401 FDA and TI LMH5401 FDA both produced good results with an undistorted original path and a sniffed signal good enough to send video to a normal screen. The signal quality of the output from the LMH5401 was better and thus is better in this specific application. However if this is going to become a real product one day it also has its' faults.

1) At nearly 8$ per OP-amp totaling 32$ for the four needed to make the circuit they are too expensive to be used.
2) Drawing at 0.49A at -2.5V and 0.14A at +2.5V the total power consumption is around 1.6W (V * A = W) which is too high.

Since the bandwidth of the used Op-amps highly exceeds the bandwidth requirement of the application, the price can be pushed down by using Hi-Speed FDAs with lower bandwidth.

6. Productification and Sniffer Integration

The next step in the project is to productify and use the sniffer and make an early functioning prototype. The first step is to make the connection electrically and the second step is to program/configure the drivers to the HDMI receivers and CPU. On a given Ethernet network a network camera has its own dedicated IP-address, FTP server, FTP client, E-mail client, alarm management and built-in Web server. It operates as an independent server on the network and can be accessed without installation of extra software remotely from any computer with access to the network [30]. That means if able to replace the video stream normally coming from the camera lens/sensor with the sniffer, convert the computers outputted RGB signal into a CPU compatible format and configure the CPU correctly a functioning prototype would be finished. The prototype would then have all the benefits of a network camera as remote access, dedicated IP-address and so on. A block diagram over the prototype is presented below in Fig. 47: The image conversion from 1080p@60Hz 8-bit RGB to a format compatible with the Axis Artpec-5 is executed and outputted from the HDMI receiver (ADV7611). Inside the Artpec-5 the data stream is then compressed into a format better suitable to be sent over Ethernet, such as H.264, in order to meet bandwidth requirements.

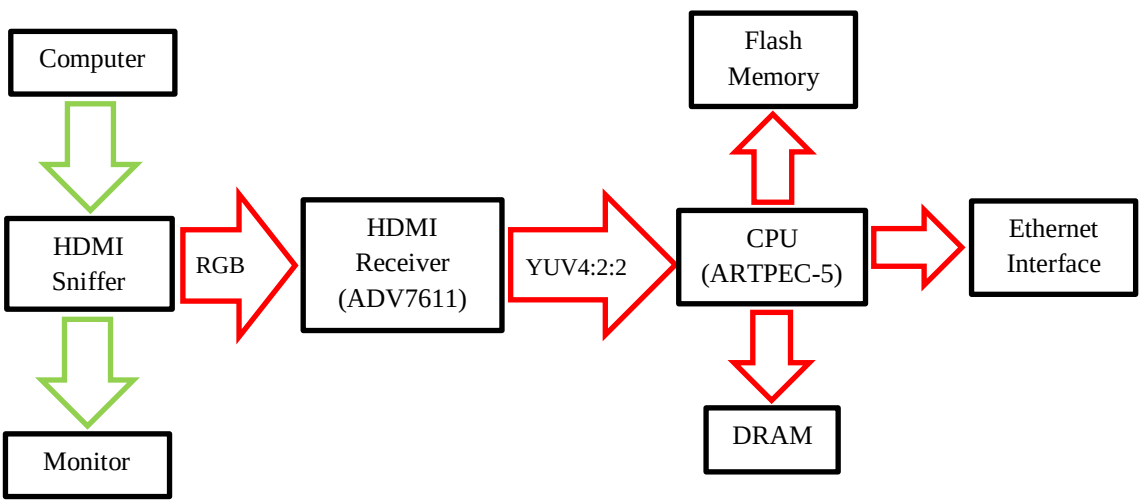

Fig. 47 block diagram over the HDMI Encoder prototype.

The reason we need to encode the video is because when it is uncompressed it takes up an enormous amount of space and it is not recommended to send it over Ethernet.

In RGB each pixel has three equally important values proportional to the amount of red, green and blue color it contains.

The changes also gives a change in definition of the camera unit which is switched from a network camera into a HDMI network encoder.

6.1. Making the Electrical Connection

The idea is to connect the sniffer with an existing Axis camera that already has an HDMI receiver integrated and make it act as an encoder. In this particular case that means removing the HDMI type-A connector at the sniffer output and replacing it with a flexible band cable. In a real product the sniffer would be fully integrated onto the PCB to maintain a better signal integrity. From the first phase of the project we determined that the best amplifier for the job was the LMH5401 and thus the original schematic has been modified and the PCB has been designed with the same guidelines established for HF (microstrip, four layers etc.). If there was more time a new power supply would also be designed so the HDMI sniffer could be driven by the camera units Power over Ethernet (PoE).

6.2. Configuring the Drivers

The following integrated circuits (IC) need to be configured with new drivers:

- Analog Devices ADV7611
    - Low Power
    - 165Mhz Maximum TMDS clock frequency

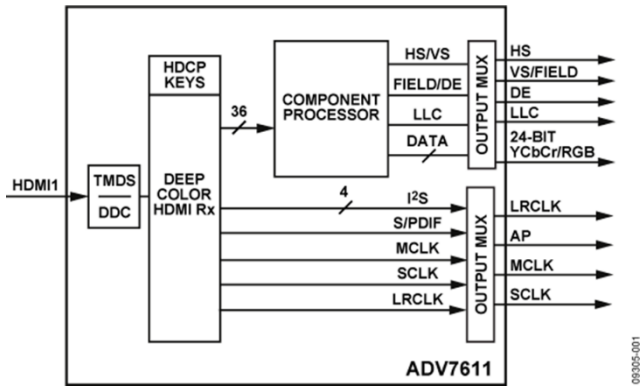

Fig. 48 Functional block diagram over the ADV7611 **[30]**.

For deeper reading please refer to the ADV7611 Datasheet for a full description of features and characteristics.

- Axis Artpec-5 CPU.
    - Embedded CPU running Linux
    - Ethernet Controller
    - 1080p 60 frames per second video processing

In the report I will not go further into how the actual drivers was configured. Development was done programming in C, on an open-source Linux distribution, normal text editor. Communication to the ICs are done over I2C protocol making it possible to set and read register values in real time. As a complement there was also an ADV7611 evaluation board to assist configuring the circuit.

From the HDMI sniffer it is transmitted a 1080p 60 frames per second RGB video stream. This stream is inputted into the ADV7611 and there it is converted into Single Data Rate (SDR) 16-bit YCbCr/YUV 4:2:2 which is compatible with the CPU.

Note: There is not enough time in this project to implement multi resolution support into the firmware.

6.3. Productification Results

The productification phase was a success yielding a functioning prototype which has the capability to capture a video stream between a computer and a HDMI screen and display it over the network.

The following tests are performed to see that the functionality works as intended:

1) Capture the video stream and display it over the network and make sure that the HDMI monitor works properly; if the video stream is shown correctly remotely over the network and the HDMI monitor displays the video stream the test passes; if there is apparent problems with either the encoder or the picture of the HDMI monitor the test is a failure.
2) Turn the power off to the encoder prototype; if the HDMI monitor still works the test is a success; if the HDMI monitor does not display the data properly the test is a failure.
3) Turn the power on to the encoder; if the picture is still present on the HDMI monitor and the encoder starts working the test is given a passing grade; otherwise the test is a failure.

First test: **Pass,** video displays correctly on the screen and remotely over the network.

Second test: **Pass,** when the power to the prototype is turned off to mimic a malfunction the HDMI monitor does not lose any functionality and shows no sign of signal integrity related problems.

Third test: **Pass,** when the prototype encoder is turned on again, it displays the video signal over the network properly and the HDMI monitor shows no sign of the event.

7. Conclusions

In this report successful construction of a semi-passive HDMI splitter and HDMI network encoder was documented. The fundamental questions that we wanted to answer as stated in the beginning of the report:

- **Is it possible to sniff/listen to the signals on an HDMI cable?**
  Yes, following PCB layout guidelines, keeping traces short, keeping strict impedance matching and using high impedance fully differential operational amplifiers it was possible to sniff/listen to an HDMI signal.
- **Is it possible to monitor the data while not significantly degrading the source signal?**
  While making the intrusion and extending HDMI signal over PCB introduced some corruption to the signal integrity, it was not significant. It was still possible to use long running cables while monitoring the data and the end user would not notice any difference in image quality.
- **Is it possible to install the device while keeping the impedances of the wires to avoid signal reflections?**
  Yes, following the PCB layout guidelines closely and keeping the impedance mismatch to a minimum there was no problems with signal reflections and signal integrity.

After answering the fundamental questions asked in the beginning in the project using the documented events and conclusions in the report as support the development in this master thesis comes to a halt.

8. Future work

While the encoder prototype is very much in an early development stage the main functionality works as intended in a finished product. There is however future development that should be considered:

- Create a double sided power supply that runs over Power over Ethernet (PoE), eliminating the need for and external power supply **(high priority)**.
- The prototype converts one of Axis cameras into functioning as an encoder, thus there is allot of extra electronics not needed. The creation of a new schematic tailor made for encoder purposes should be done **(high priority)**.
- Create better software with multi resolution support that senses automatically what resolution is being sent **(high priority)**.
- Experiment with lower cost amplifiers and lower bandwidth amplifiers in order to cut down component cost and hopefully power consumption **(medium priority)**.
- Extend functionality of the encoder, such as the possibility to restart computers remotely in the event of a frozen terminal **(low priority)**.

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List of figures

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Appendix A: Extended material

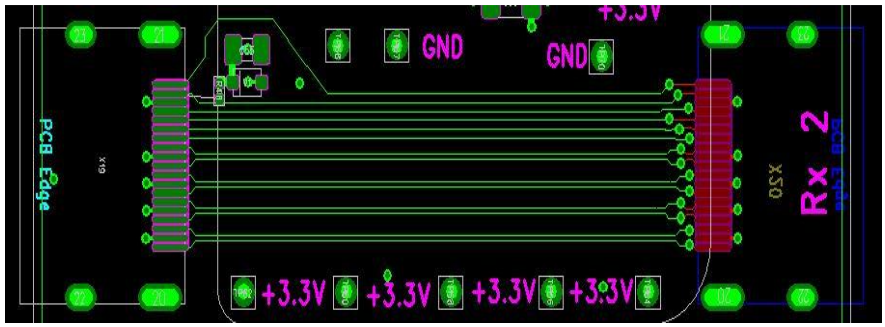

Fig. 49 Shows the PCB extension used in Chapter 3.2

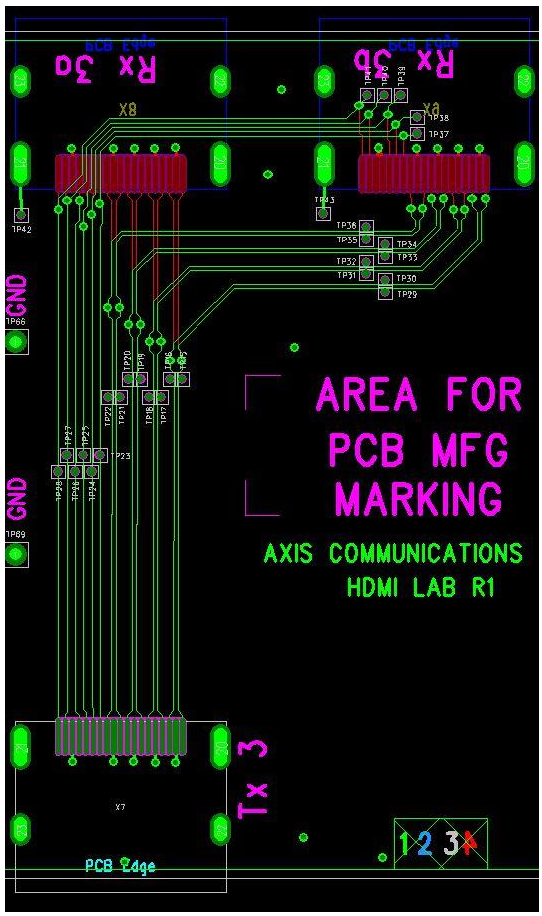

Fig. 50 show the CAD over the passive splitting solution found in Chapter 3.3

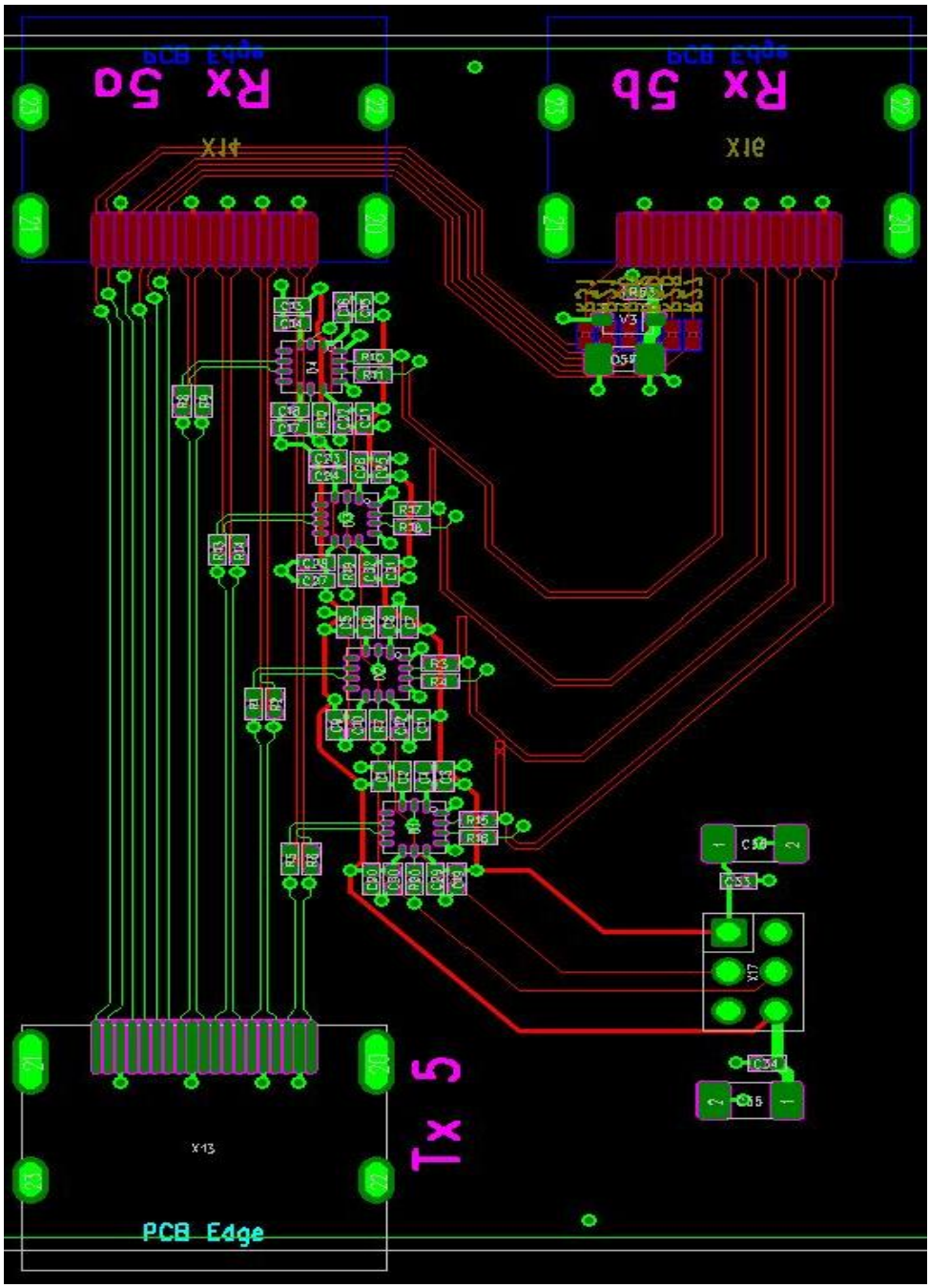

Fig. 51 Shows the full CAD over the solution implementing the TI FDA LMH3401

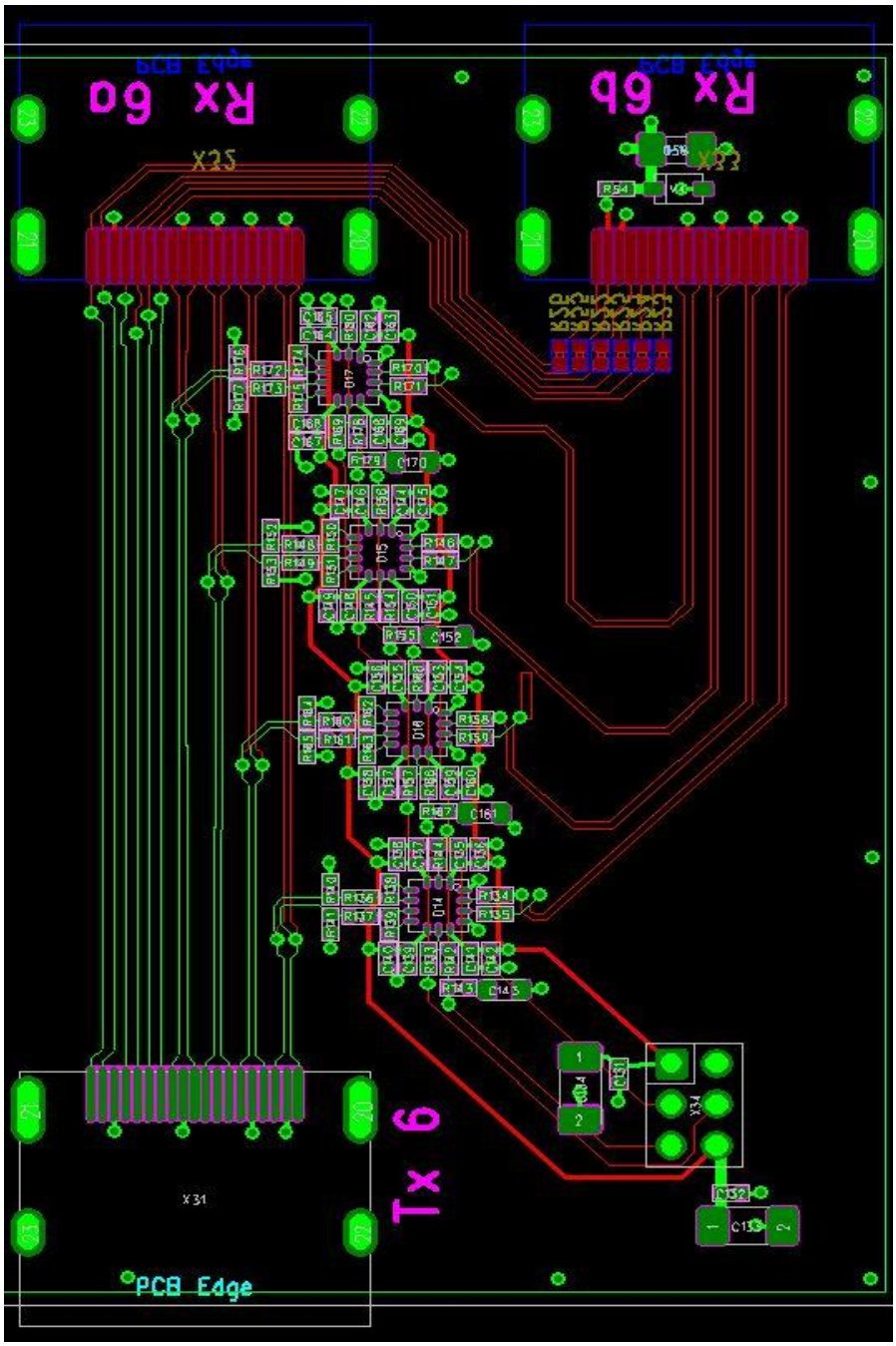

Fig. 52 Shows the full CAD over the solution implementing the TI FDA LMH5401