CS433 – Embedded Systems

Project 2 - LED / Switch game based on CYCLONE III DE0 Board - Uğurkan Ateş 151044012

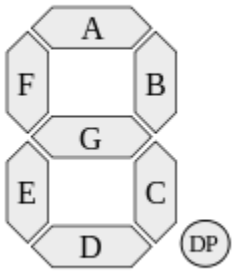
For this project I have implemented 6 level Verilog game using Quartus II 13.0 Web Edition and used Visual Studio Code for prototyping Verilog files.

I have used 4 BCD 7 segment display.
Used 9 switch - used 9 LEDS.
Used Clock 50 Mhz
Reset Pin
Button Input as module inputs/outputs.

 # 7 Segment Display

https://en.wikichip.org/wiki/seven-segment_display

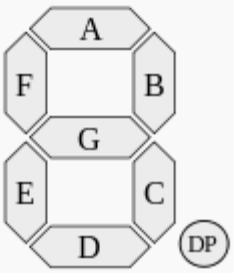
I have used this as guide.



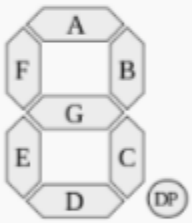
All 7 parts have different assigments in my project.

Digit	BCD				7-Segments							abcdefg	gfedcba	Display	Reference
	D	C	B	A	a	b	c	d	e	f	g				
0	0	0	0	0	1	1	1	1	1	1	0	0x7E	0x3F	0	

1	0	0	0	1	0	1	1	0	0	0	0	0x30	0x06	
2	0	0	1	0	1	1	0	1	1	0	1	0x6D	0x5B	
3	0	0	1	1	1	1	1	1	0	0	1	0x79	0x4F	
4	0	1	0	0	0	1	1	0	0	1	1	0x33	0x66	
5	0	1	0	1	1	0	1	1	0	1	1	0x5B	0x6D	
6	0	1	1	0	1	0	1	1	1	1	1	0x5F	0x7D	
7	0	1	1	1	1	1	1	0	0	0	0	0x70	0x07	
8	1	0	0	0	1	1	1	1	1	1	1	0x7F	0x7F	
9	1	0	0	1	1	1	1	1	0	1	1	0x7B	0x6F	
A	X	X	X	X	1	1	1	0	1	1	1	0x77	0x77	
b	X	X	X	X	0	0	1	1	1	1	1	0x1F	0x7C	
C	X	X	X	X	1	0	0	1	1	1	0	0x4E	0x39	
d	X	X	X	X	0	1	1	1	1	0	1	0x3D	0x5E	
E	X	X	X	X	1	0	0	1	1	1	1	0x4F	0x79	
F	X	X	X	X	1	0	0	0	1	1	1	0x47	0x71	



I have used words like STR,END,GO,FALS,ERRR,true for instructing the user.

Digit	7-Segments							abcdefg	gfedcba	Display	Reference
	a	b	c	d	e	f	g				
A	1	1	1	0	1	1	1	0x77	0x77	A	
b	0	0	1	1	1	1	1	0x1F	0x7C	b	
C	1	0	0	1	1	1	0	0x4E	0x39	C	
c	0	0	0	1	1	0	1	0x0D	0x58	c	
d	0	1	1	1	1	0	1	0x3D	0x5E	d	
E	1	0	0	1	1	1	1	0x4F	0x79	E	
F	1	0	0	0	1	1	1	0x47	0x71	F	
G	1	0	1	1	1	1	0	0x5E	0x3D	G	
H	0	1	1	0	1	1	1	0x37	0x76	H	
h	0	0	1	0	1	1	1	0x17	0x74	h	
I	0	0	0	0	1	1	0	0x06	0x30	I	
J	0	1	1	1	1	0	0	0x3C	0x1E	J	
L	0	0	0	1	1	1	0	0x0E	0x38	L	
n	0	0	1	0	1	0	1	0x15	0x54	n	
O	1	1	1	1	1	1	0	0x7E	0x3F	O	
o	0	0	1	1	1	0	1	0x1D	0x5C	o	
P	1	1	0	0	1	1	1	0x67	0x73	P	
q	1	1	1	0	0	1	1	0x73	0x67	q	
r	0	0	0	0	1	0	1	0x05	0x50	r	
S	1	0	1	1	0	1	1	0x5B	0x6D	S	
t	0	0	0	1	1	1	1	0x0F	0x78	t	
U	0	1	1	1	1	1	0	0x3E	0x3E	U	
u	0	0	1	1	1	0	0	0x1C	0x1C	u	

9 LED Array

I have used [9:0] led array for assigning different lights for them. Here is their pin assigments from pin planner / Quartus

led[9]	Output	PIN_B1	1	B1_N0	2.5 V (default)		8mA (default)	2 (default)
led[8]	Output	PIN_B2	1	B1_N0	2.5 V (default)		8mA (default)	2 (default)
led[7]	Output	PIN_C2	1	B1_N0	2.5 V (default)		8mA (default)	2 (default)
led[6]	Output	PIN_C1	1	B1_N0	2.5 V (default)		8mA (default)	2 (default)
led[5]	Output	PIN_E1	1	B1_N0	2.5 V (default)		8mA (default)	2 (default)
led[4]	Output	PIN_F2	1	B1_N0	2.5 V (default)		8mA (default)	2 (default)
led[3]	Output	PIN_H1	1	B1_N1	2.5 V (default)		8mA (default)	2 (default)
led[2]	Output	PIN_J3	1	B1_N1	2.5 V (default)		8mA (default)	2 (default)
led[1]	Output	PIN_J2	1	B1_N1	2.5 V (default)		8mA (default)	2 (default)
led[0]	Output	PIN_J1	1	B1_N1	2.5 V (default)		8mA (default)	2 (default)

LED’s constantly changing according to states and state changes if user press same buttons as led inputs.

9 Switch Array

switch[9]	Input	PIN_D2	1	B1_N0	2.5 V (default)		8mA (default)	
switch[8]	Input	PIN_E4	1	B1_N0	2.5 V (default)		8mA (default)	
switch[7]	Input	PIN_E3	1	B1_N0	2.5 V (default)		8mA (default)	
switch[6]	Input	PIN_H7	1	B1_N0	2.5 V (default)		8mA (default)	
switch[5]	Input	PIN_J7	1	B1_N1	2.5 V (default)		8mA (default)	
switch[4]	Input	PIN_G5	1	B1_N0	2.5 V (default)		8mA (default)	
switch[3]	Input	PIN_G4	1	B1_N0	2.5 V (default)		8mA (default)	
switch[2]	Input	PIN_H6	1	B1_N0	2.5 V (default)		8mA (default)	
switch[1]	Input	PIN_H5	1	B1_N0	2.5 V (default)		8mA (default)	
switch[0]	Input	PIN_J6	1	B1_N0	2.5 V (default)		8mA (default)	

Switch input assigments.

Reset , Button and Clock

I have used G21 pin of DE0 Development board 50 MHz Ossicalator. I am changing Clock rate inside Verilog code. Button Is used for answering arithmetic questions in level ends.

How game works :

I have 2 FSM inside the system.

First FSM starts with State_Start which initialize the data , outputs STR to BCD then in next assignment we are going on

STATE LEVEL 1 = In loop if anyone not breaks the loop, Loop breaks with out signal

STATE_LEVEL_1_SORU = Its only triggered when out is 1 and question shows up

When user answers the question with Switch inputs(its arithmetic question) then he needs to press START button for checking.

state_LEVEL1_Out_TruWait = Answer for level is correct, We need user to turn off all switches, and BCD says TRU letters.

state_LEVEL1_Out_FalWait = Answer is false , we need user to turn off all switches and BCD says FALS letters.

We have 6 LEVEL for this system.

Other FSM state is for loop of LED's. 9:0 LEDS are in loop. They go their level routes accordingly.

I have Counter module implemented

```
always @ (posedge Clock, posedge reset) begin
   if (reset) count <= 26'b0;
         else if (pulse) count <= 26'b0;
         else count <= count + 26'b1;
  end
```

List of end-Level Questions

LEVEL1 = 1 2 3 4 = 12+34 = 46

LEVEL2 = 4 2 1 5 = 42 -15 = 27

LEVEL3 = 1 2 1 1 = 12*11 = 132

LEVEL4 = 9 8 ‘ 7 = 98/7 = 14

LEVEL5 = Series of leds turn of in range and user must count number of them

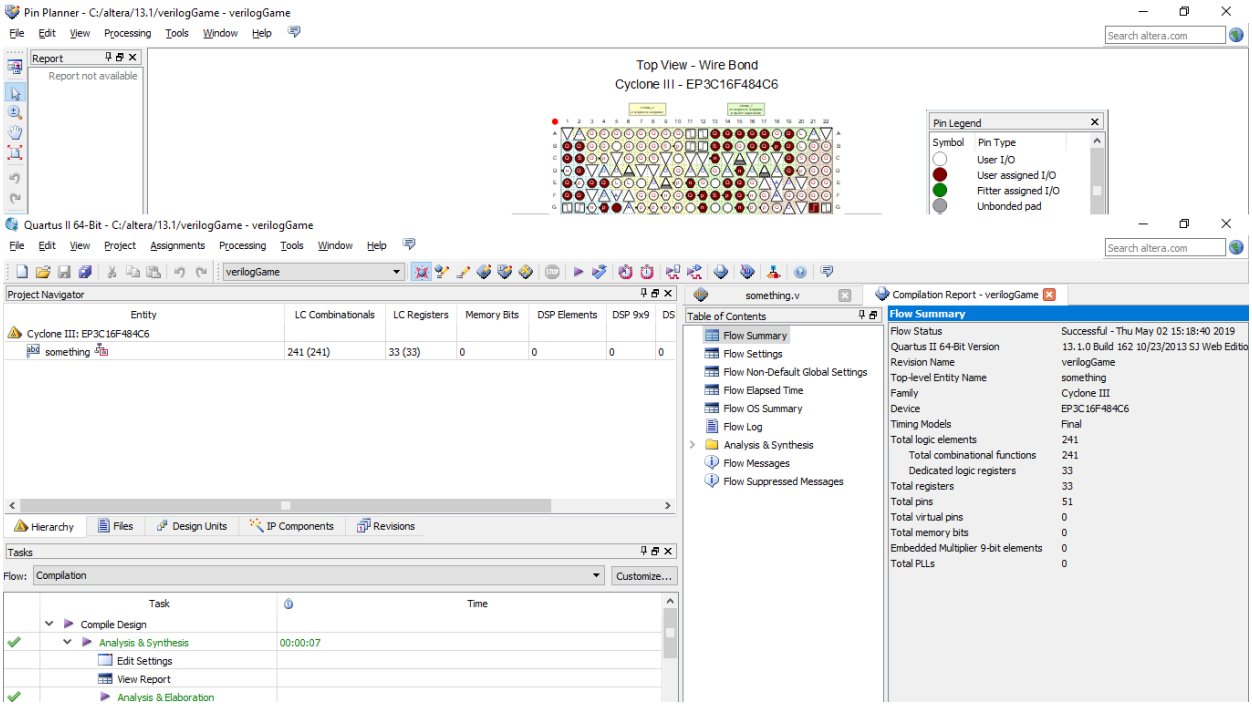
LEVEL6 = Series of leds turn of in range and user must count number of them(faster)

LEVEL 1 and LEVEL 2 works on slowClock 50mhz

LEVEL3 and LEVEL 4 works on midClock 50 mhz / 2

LEVEL5 and LEVEL6 50 mhz / 4

Flow Status	Successful - Thu May 02 15:18:40 2019
Quartus II 64-Bit Version	13.1.0 Build 162 10/23/2013 SJ Web Editio
Revision Name	verilogGame
Top-level Entity Name	something
Family	Cyclone III
Device	EP3C16F484C6
Timing Models	Final
Total logic elements	241
Total combinational functions	241
Dedicated logic registers	33
Total registers	33
Total pins	51
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0


Pin Planner - C:/altera/13.1/verilogGame - verilogGame
File Edit View Processing Tools Window Help
Search altera.com
Report
Report not available
Top View - Wire Bond
Cyclone III - EP3C16F484C6
Pin Legend
Symbol Pin Type
User I/O
User assigned I/O
Fitter assigned I/O
Unbonded pad
Quartus II 64-Bit - C:/altera/13.1/verilogGame - verilogGame
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
verilogGame
Project Navigator
Entity
LC Combinationals
LC Registers
Memory Bits
DSP Elements
DSP 9x9
Cyclone III: EP3C16F484C6
something
241 (241)
33 (33)
0
0
0
0
Hierarchy
Files
Design Units
IP Components
Revisions
Tasks
Flow: Compilation
Customize...
Task
Time
Compile Design
Analysis & Synthesis
00:00:07
Edit Settings
View Report
Analysis & Elaboration
something.v
Compilation Report - verilogGame
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Total PLLs
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