Laboratory Exercise
Introduction to Verilog HDL

Objectives:

At the end of the exercise, the students should be able to:

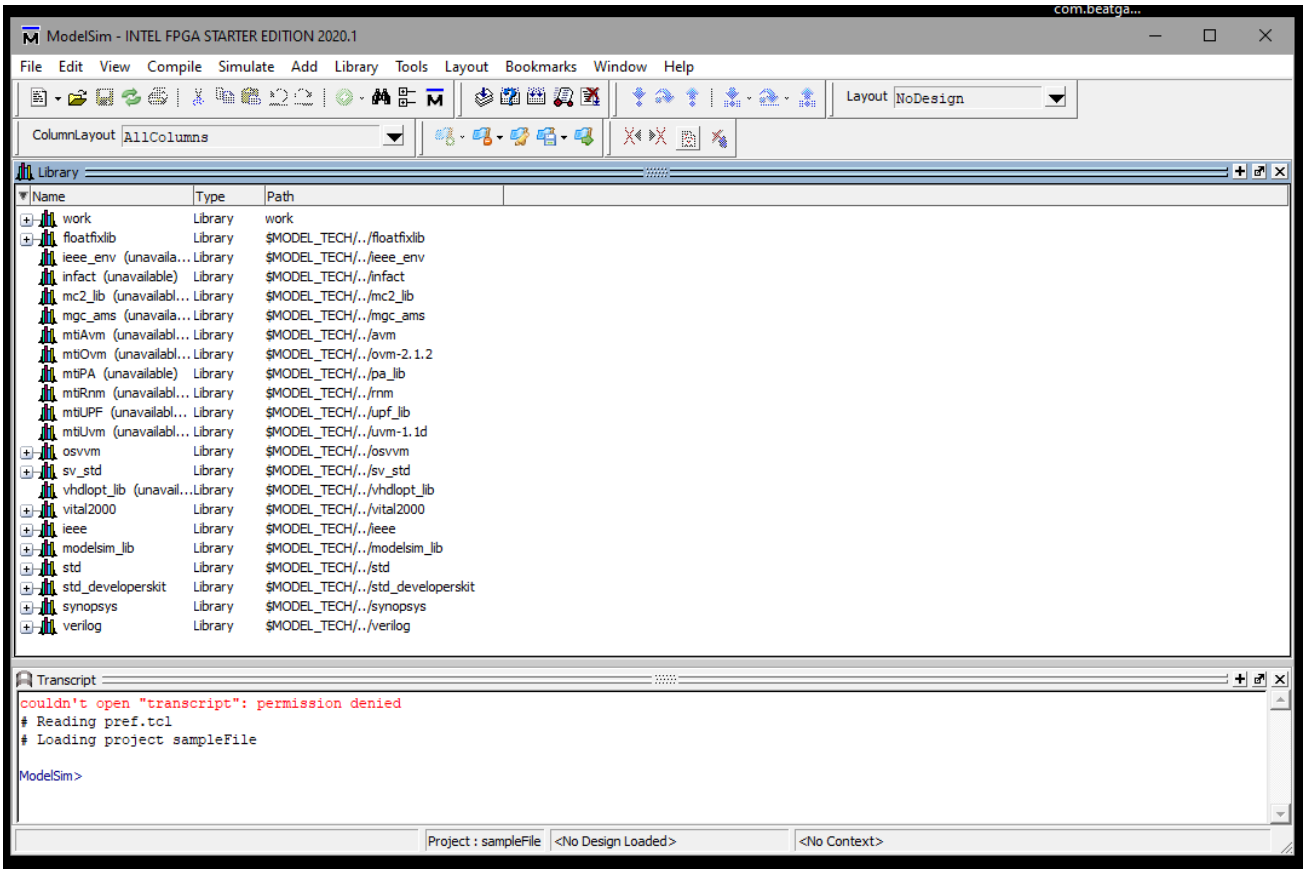
- Implement working knowledge in Verilog modules; and
- Create modules with logic gates of 3-input XOR Gate.

Materials:

- Computer with ModelSim Intel FPGA Starter Edition installed

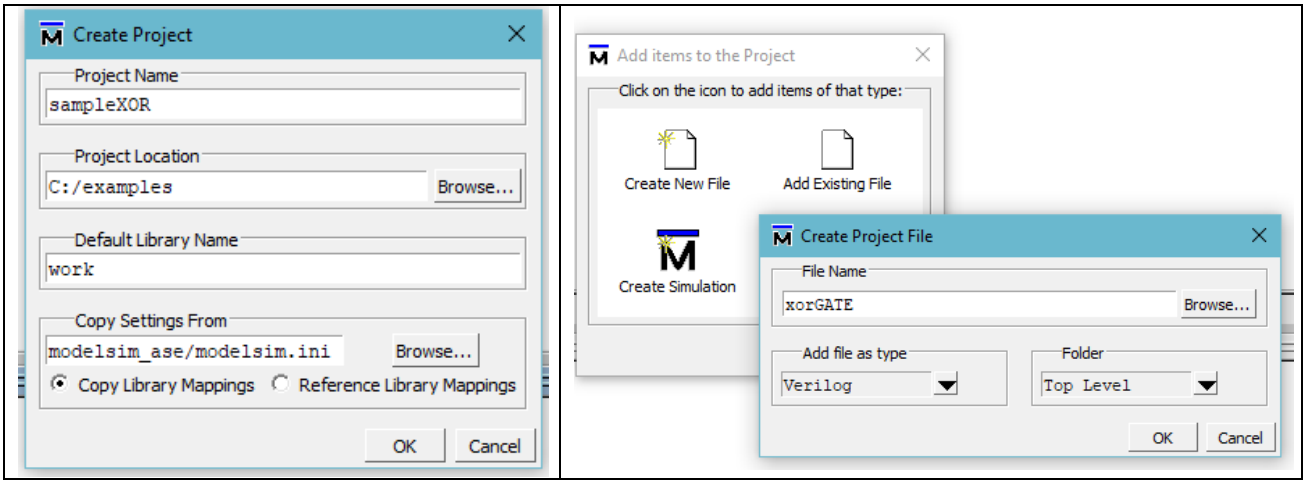
Basic Principles:

ModelSim simulates behavioral, RTL, and gate-level code, delivering increased design quality, debugging efficiency, and platform-independent compile with outstanding performance. Single Kernel Simulator technology enables transparent mixing of VHDL and Verilog in one design.



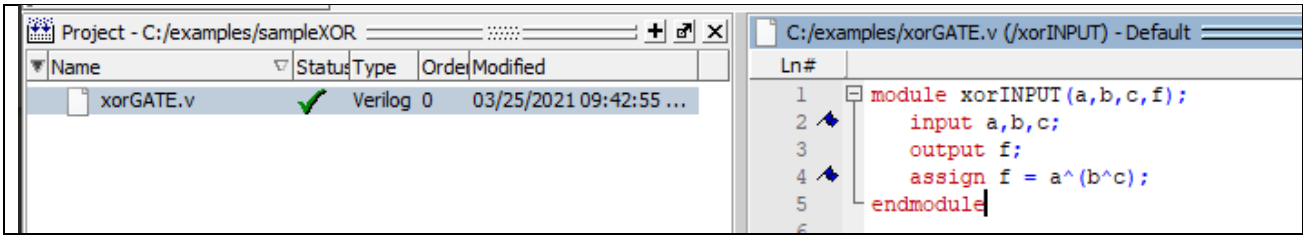
Procedure:

1. To create a new project from scratch, click **FILE > NEW > PROJECT**. A new window will pop up.
2. Type in the **Project Name**: "**sampleXOR**" and click **OK**. Set the **Project Location** in "**C:/examples**".
3. Click on **Create New File** and type in the **File Name** as "**xorGate**". Select **Verilog** as the file type and press **OK**. Click close/

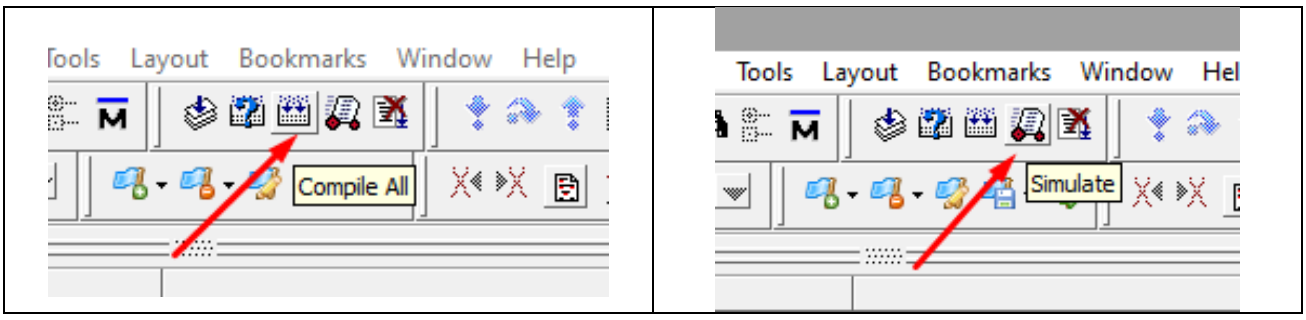


4. Double-click the Verilog file "**xorGATE.v**" and type in the following code:

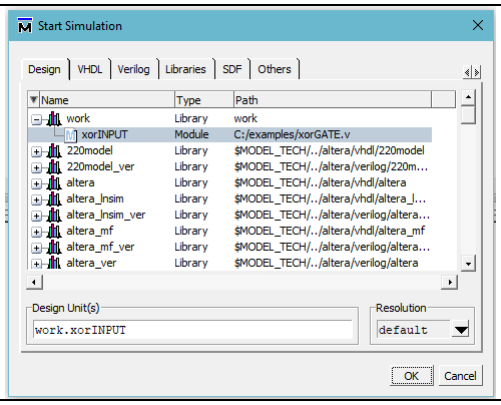
```
module xorINPUT(a,b,c,f);
   input a,b,c;
   output f;
   assign f = a^(b^c);
endmodule
```

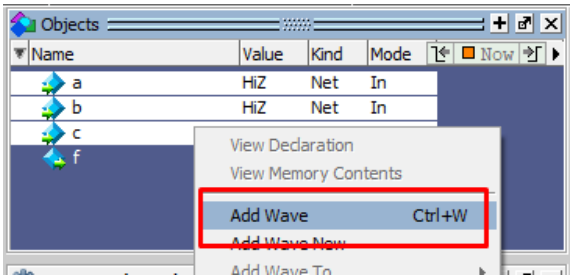


5. Click the **Compile All** button. Click the **Simulate** button to execute all the modules. ***Note: Check for errors and warnings. Syntax errors and logic errors will appear, if any.***

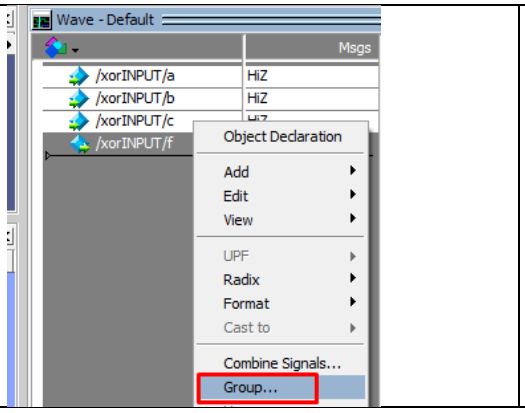


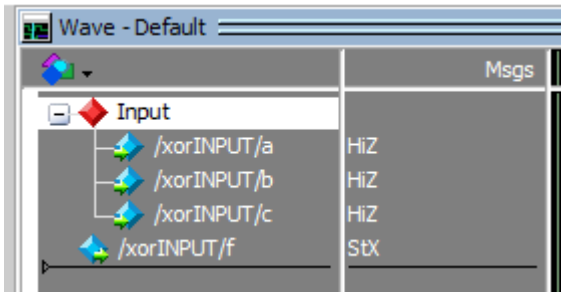
6. Select **work** > **xorINPUT** and click **OK** and it will display the object window. Select and right click all objects, then select **Add Wave**. The **Wave** window will appear. Make sure that the Design Unit(s) is set to **work.xorINPUT**.



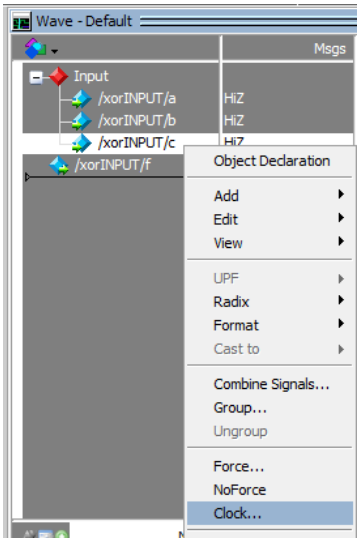


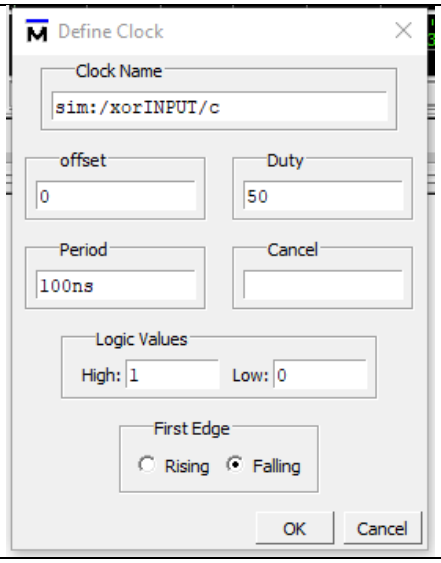
7. In the **Wave** window, segregate the input and the output by selecting **inputs A and B**, right-click and Click **Group**. Type in the **Group Name** as "**Input**". Do the same for the output.





8. In order for the timings to be displayed in each signal. Select **/xorINPUT/c**, right-click on it and select **Clock**. Set the parameter **Period** to "**100ns**". Select **First Edge** to **Falling** option and click **OK**.

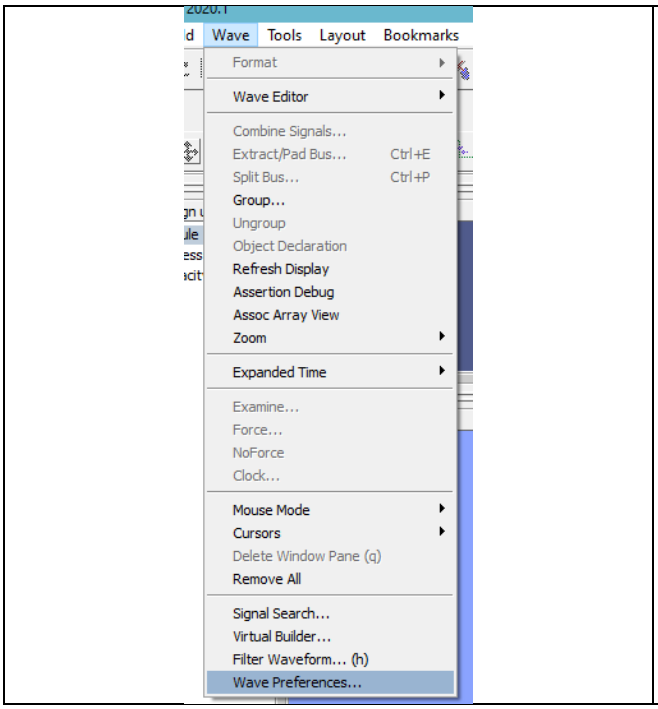


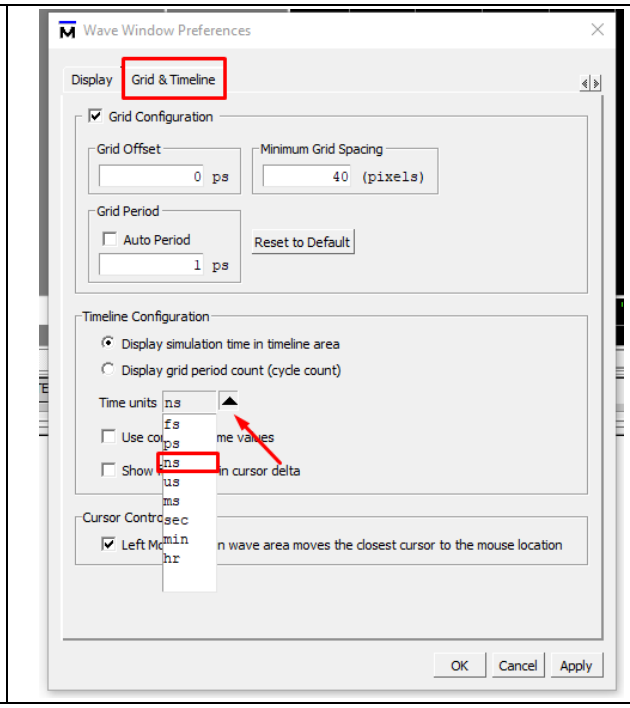


9. Do the same for the other objects with the following values:
   - **/xorINPUT/b**
     - Period to **200ns**
     - First Edge to **Falling option**
   - **/xorINPUT/a**
     - Period to **400ns**
     - First Edge to **Falling option**

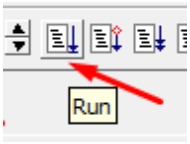
10. On the top middle of the screen, adjust the **Run Length** from **100 ps** to **400 ns**.

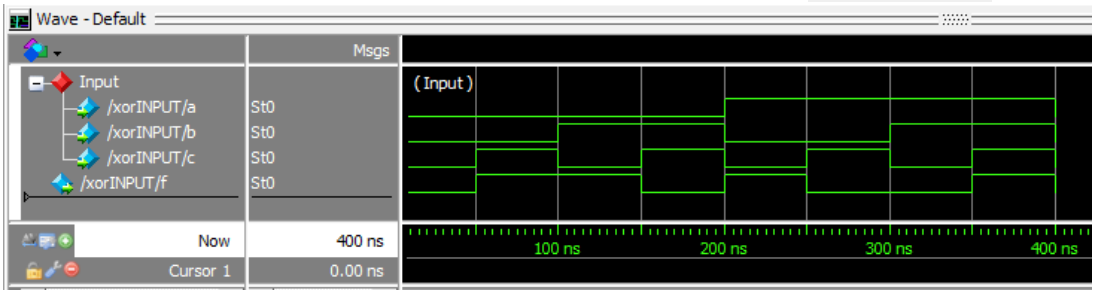
11. Maneuver to the dropdown menu and access **Wave > Wave Preferences…** Afterwards, in the **Wave Window Preferences**, click the **Grid & Timeline** tab and set the **Time units** from **ps** to **ns**. Click **Apply** and **OK**.





12. Click **Run** button near the **Run Length** to see the result. The result should look like this.





13. Show/submit your output to your instructor.

Conclusion:

Guide question:

1. What have you learned in this activity? Do you think it is helpful in HDL analysis?

GRADING RUBRIC:

- Activity 1 **(20 points)**

Criteria	Indicator	Score
Simulation	Organized and clean implementation of signals and logic.	10
Programming	Correct usage of code and syntaxes. No errors found.	10
	Total	**20**

- Conclusion **(10 points)**

Criteria	Indicator	Score
Content	Provided supporting details and factual scenarios	5
Organization of Ideas	Expressed clear points and arranged ideas	5
	Total	**10**