國立高雄科技大學

電子工程系(第一校區)

硬體描述語言

Lab 3

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Lab 3.

1. A *full subtractor* has three 1-bit inputs *x*, *y*, and *z* (previous borrow) and two 1-bit outputs *D* (difference) and *B* (borrow). The logic equations for D and B are as follows:

$D = x'y'z + x'yz' + xy'z' + xyz$

$B = x'y + x'z + yz$

Write the full Verilog description **(dataflow modeling)** for the full subtractor module, including I/O ports (Remember that + in logic equations corresponds to a logical or operator (||) in dataflow). Instantiate the subtractor inside a stimulus block and test all eight possible combinations of *x*, *y*, and *z* given in the following truth table. (Hint: Each test pattern has a delay of 10 ns, and the simulation is finished at 200 ns.)

x	y	z	B	D
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

----------第一題作答區----------

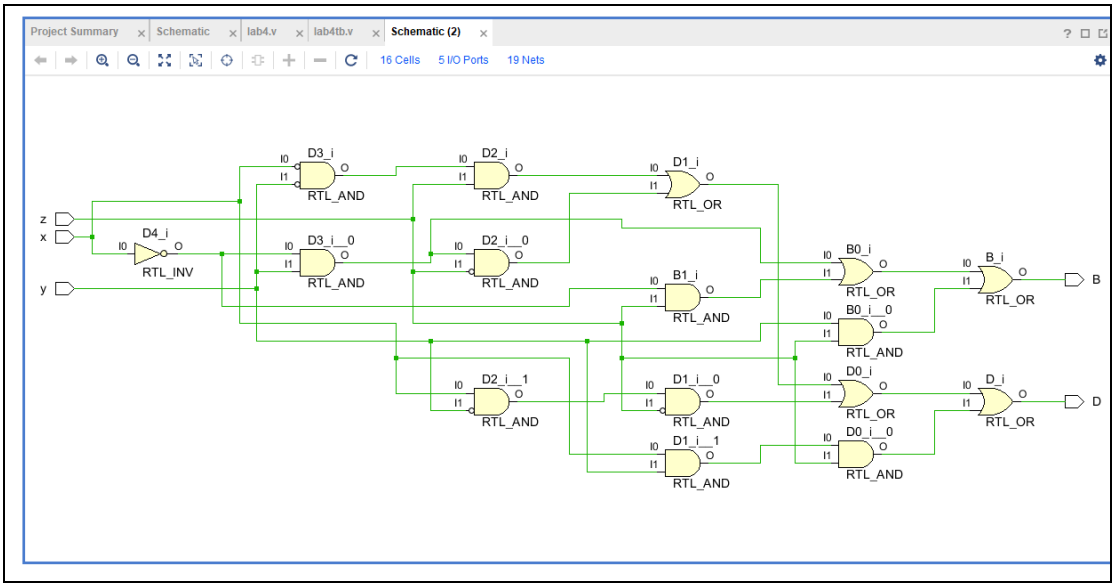
主(電路)程式

```
‘timescale 1ns / 1ps

module lab4(D,B,x,y,z);
output D,B;
input x,y,z;
wire D,B;
assign D=((~x)&(~y)&z)|((~x)&y&(~z))|(x&(~y)&(~z))|(x&y&z);
assign B= ((~x)&y)|((~x)&z)|(y&z);
endmodule
```

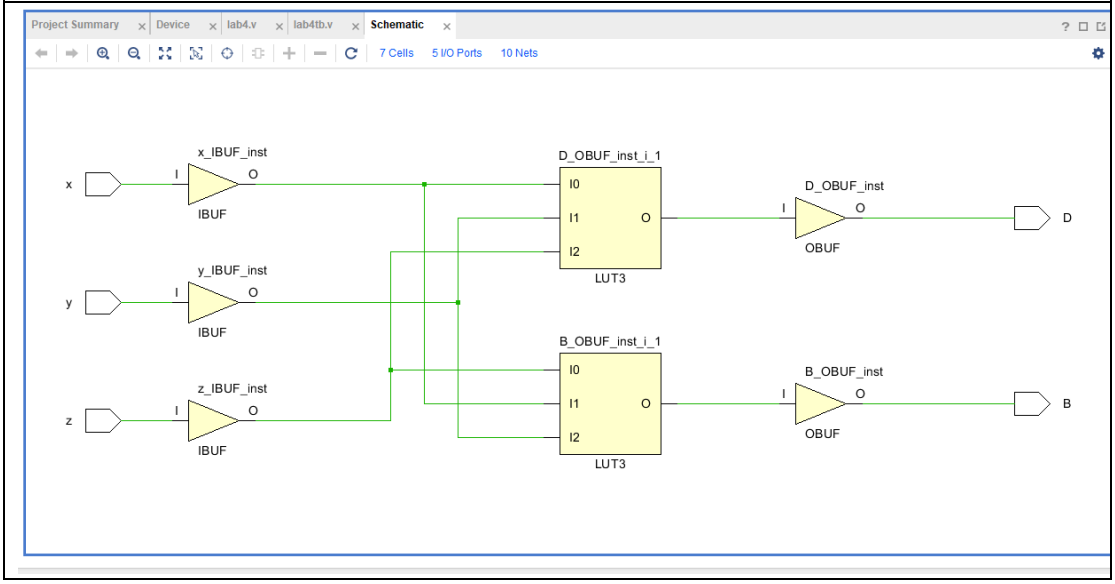
測試程式(testbench)

```
‘timescale 1ns / 1ps
module  lab4tb();
reg x,y,z;
wire D,B;

// Instantiate the 4-bit full adder. call it FA1_4
lab4 UU1(D,B,x,y,z);
initial
begin

$monitor($time," x= %b, y=%b, z= %b, --- D= %b, B= %b\n",
x, y, z,D, B);
end
// Stimulate inputs
initial
begin
x = 1'b0 ; y =1'b0; z=1'b0;
#10 x = 1'b0 ; y =1'b0; z=1'b1;
#10 x = 1'b0 ; y =1'b1; z=1'b0;
#10 x = 1'b0 ; y =1'b1; z=1'b1;
#10 x = 1'b1 ; y =1'b0; z=1'b0;
#10 x = 1'b1 ; y =1'b0; z=1'b1;
#10 x = 1'b1 ; y =1'b1; z=1'b0;
#10 x = 1'b1 ; y =1'b1; z=1'b1;
end
initial #200 $finish;

endmodule
```

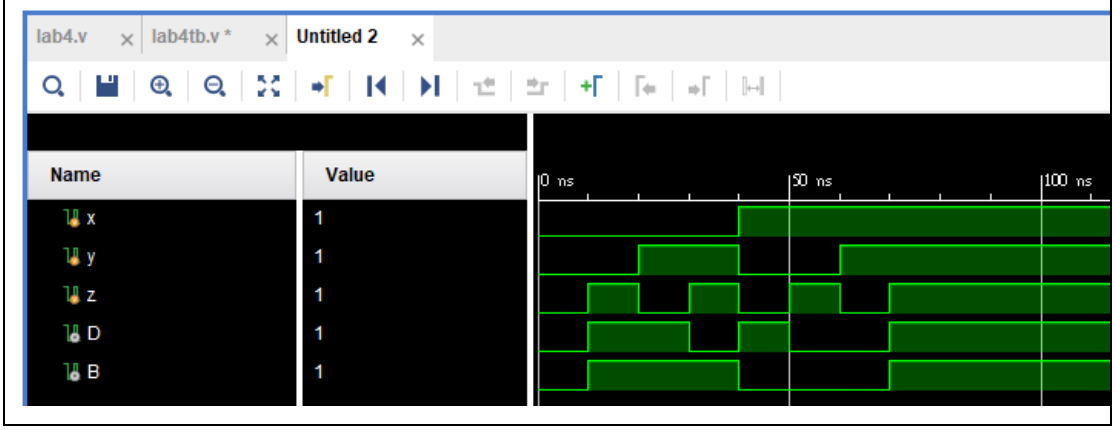
RTL schematic

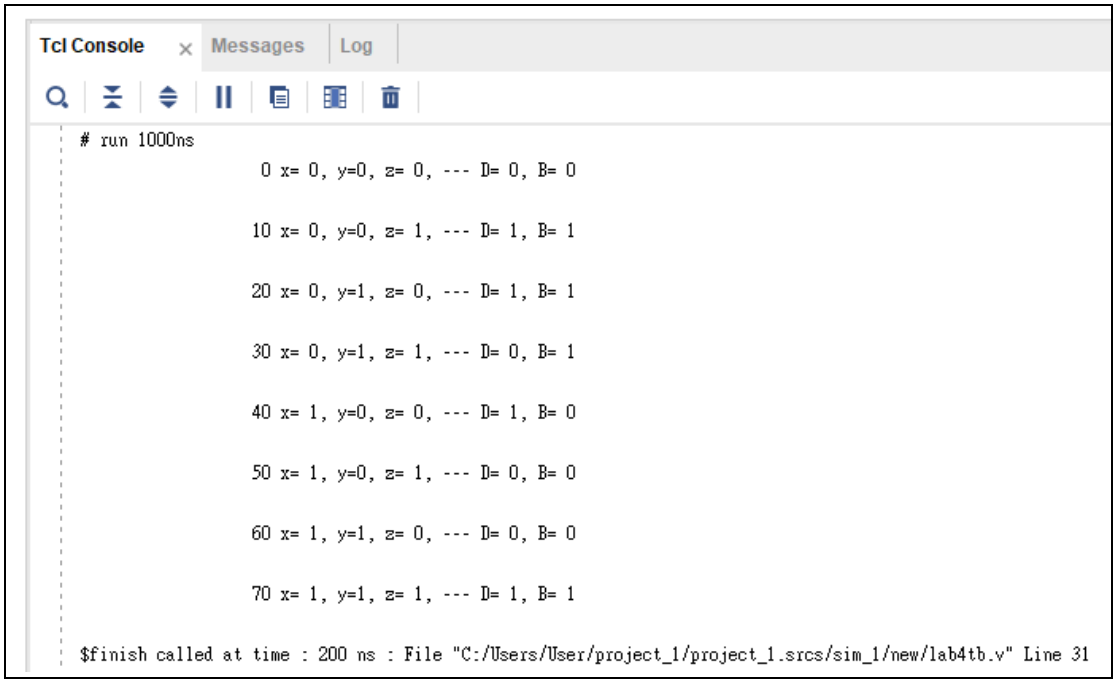


Technology Schematic



Behavioral Simulation Waveform(含 $monitor)




Tcl Console
Messages
Log
run 1000ns
0 x= 0, y=0, z= 0, --- D= 0, B= 0
10 x= 0, y=0, z= 1, --- D= 1, B= 1
20 x= 0, y=1, z= 0, --- D= 1, B= 1
30 x= 0, y=1, z= 1, --- D= 0, B= 1
40 x= 1, y=0, z= 0, --- D= 1, B= 0
50 x= 1, y=0, z= 1, --- D= 0, B= 0
60 x= 1, y=1, z= 0, --- D= 0, B= 0
70 x= 1, y=1, z= 1, --- D= 1, B= 1
$finish called at time : 200 ns : File "C:/Users/User/project_1/project_1.srcs/sim_1/new/lab4tb.v" Line 31

----------作答區結束----------

2. If the equations D, B have regular delays of 「10」 and 「20」 ns respectively, please use the same truth table as above to simulate the operation results. Please show the correct results of D, and B after the simulation. (Hint: Each test pattern has a delay of 10 ns, and the simulation is finished at 200 ns.)

----------第一題作答區----------

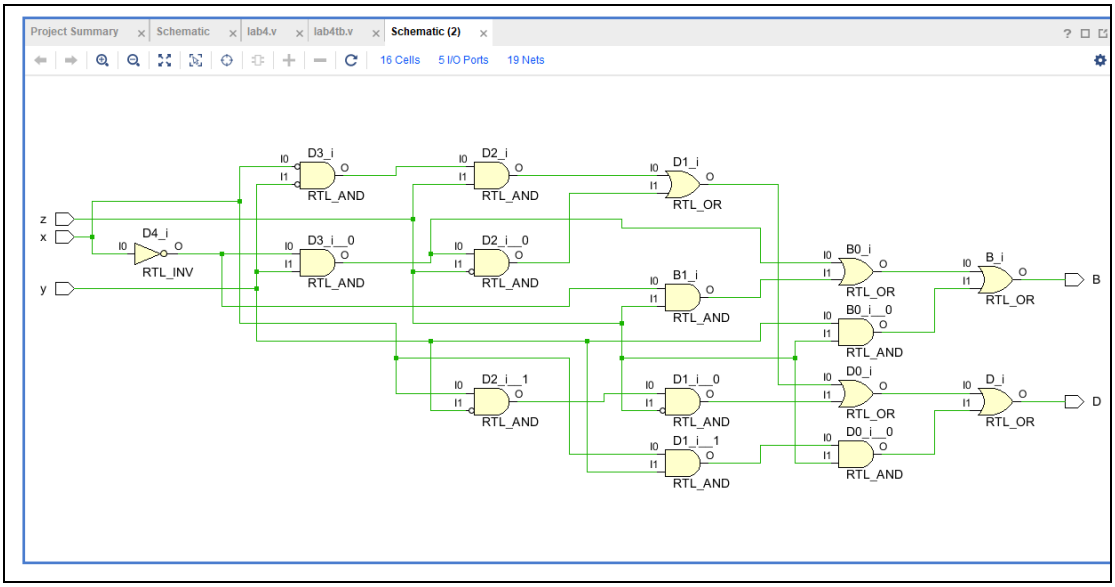
主(電路)程式

```
‘timescale 1ns / 1ps

module lab4(D,B,x,y,z);
output D,B;
input x,y,z;
wire D,B;
assign  D = ((~x)&(~y)&z) | ((~x)&y&(~z)) | (x&(~y)&(~z)) | (x&y&z);
assign  B = ((~x)&y) | ((~x)&z) | (y&z);
endmodule
```

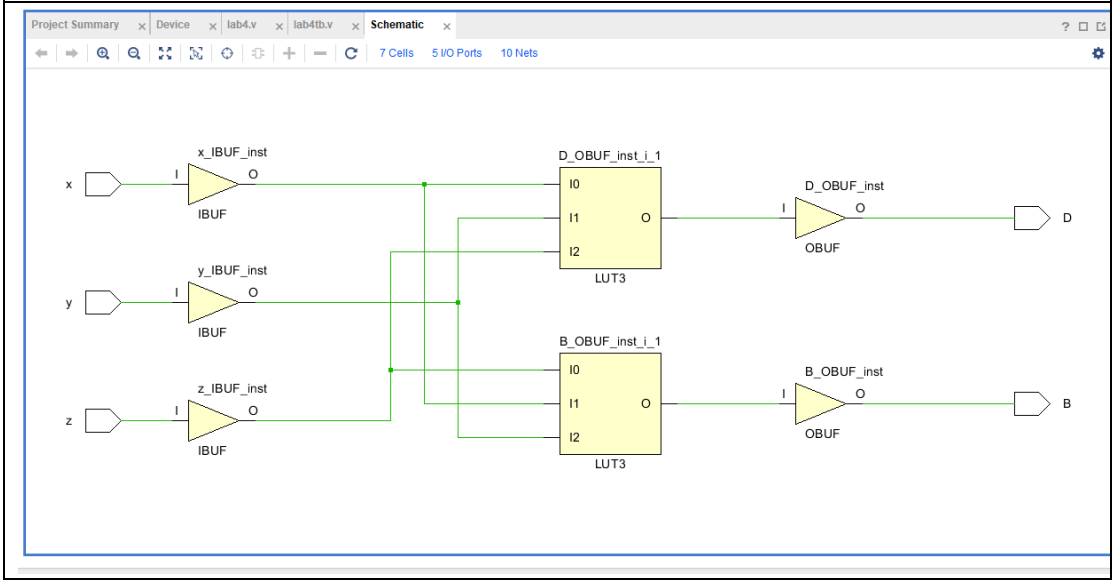
測試程式(testbench)

```
‘timescale 1ns / 1ps
module  lab4tb();
reg x,y,z;
wire #10 D;
wire #20 B;

lab4 UU1(D,B,x,y,z);
initial
begin

$monitor($time," x= %b, y=%b, z= %b, --- D= %b, B= %b\n",
x, y, z,D, B);
end
// Stimulate inputs
initial
begin
x = 1'b0 ; y =1'b0; z=1'b0;
#10 x = 1'b0 ; y =1'b0; z=1'b1;
#10 x = 1'b0 ; y =1'b1; z=1'b0;
#10 x = 1'b0 ; y =1'b1; z=1'b1;
#10 x = 1'b1 ; y =1'b0; z=1'b0;
#10 x = 1'b1 ; y =1'b0; z=1'b1;
#10 x = 1'b1 ; y =1'b1; z=1'b0;
#10 x = 1'b1 ; y =1'b1; z=1'b1;
end
initial #200 $finish;

endmodule
```

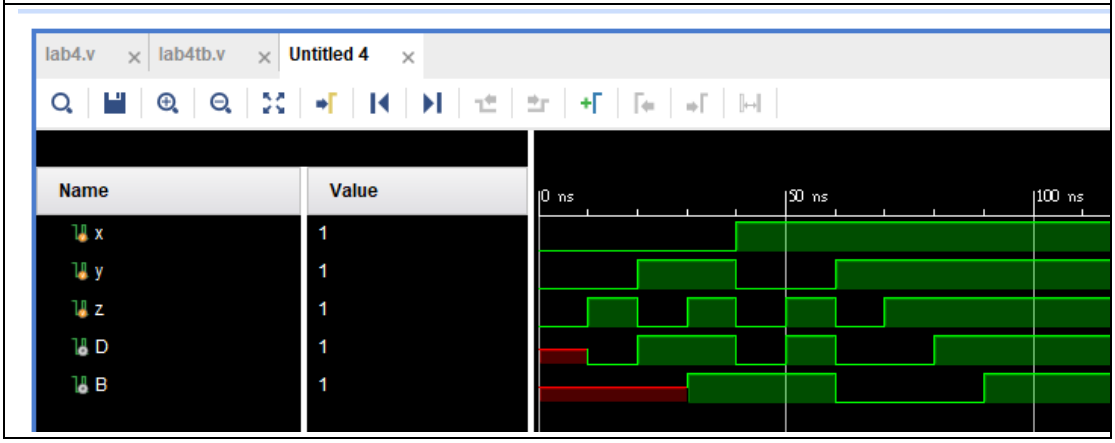
RTL schematic

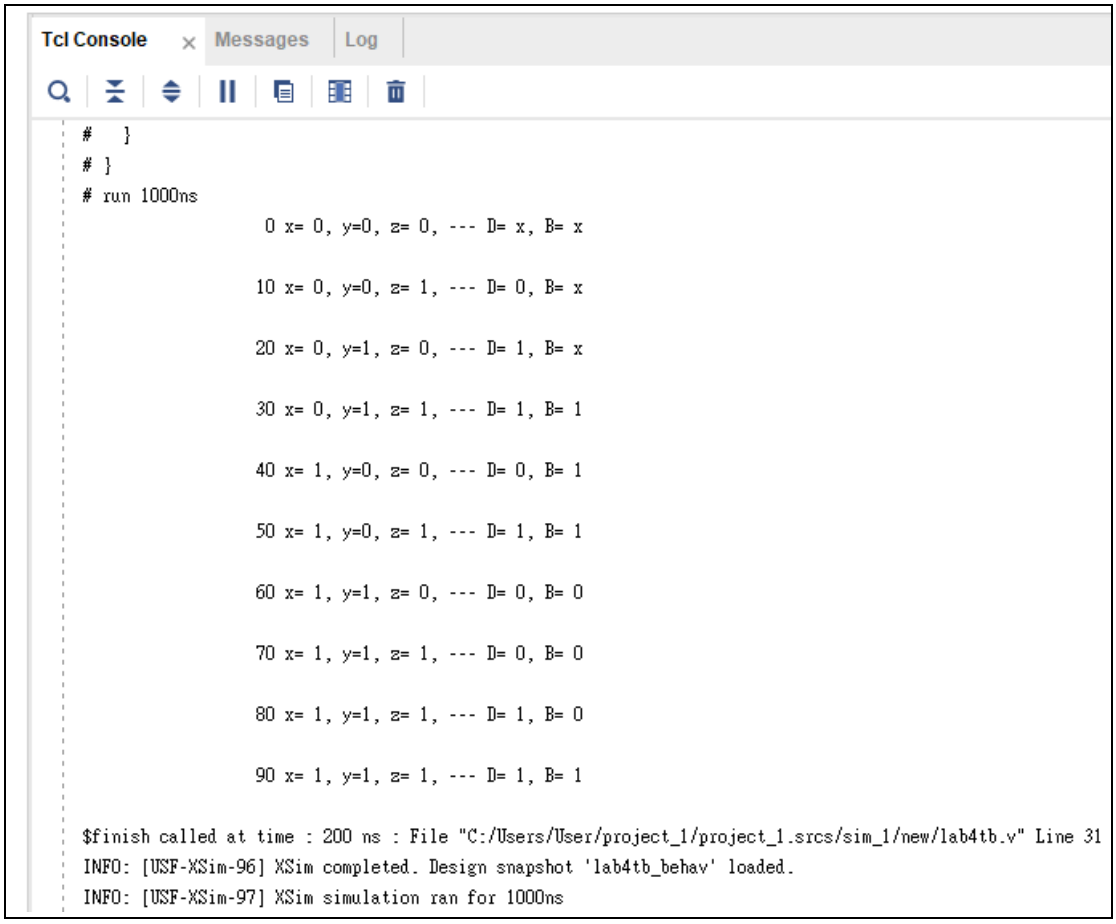


Technology Schematic



Behavioral Simulation Waveform(含 $monitor)




Tcl Console
Messages
Log
}
}
run 1000ns
0 x= 0, y=0, z= 0, --- D= x, B= x
10 x= 0, y=0, z= 1, --- D= 0, B= x
20 x= 0, y=1, z= 0, --- D= 1, B= x
30 x= 0, y=1, z= 1, --- D= 1, B= 1
40 x= 1, y=0, z= 0, --- D= 0, B= 1
50 x= 1, y=0, z= 1, --- D= 1, B= 1
60 x= 1, y=1, z= 0, --- D= 0, B= 0
70 x= 1, y=1, z= 1, --- D= 0, B= 0
80 x= 1, y=1, z= 1, --- D= 1, B= 0
90 x= 1, y=1, z= 1, --- D= 1, B= 1
$finish called at time : 200 ns : File "C:/Users/User/project_1/project_1.srcs/sim_1/new/lab4tb.v" Line 31
INFO: [USF-XSim-96] XSim completed. Design snapshot 'lab4tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns

----------作答區結束----------