國立高雄科技大學

電子工程系(第一校區)

硬體描述語言

Lab. 6: ALU

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Lab. 6: ALU (Chap.7-B)

本周學習目標：活用 case 語法，以及模擬程式迴圈語法。

題目說明：

1. **Define a function to design an 8-function ALU that takes two 4-bit numbers *a* and *b* and computes a 5-bit result *out* based on a 3-bit *select* signal.**
   - **Ignore overflow or underflow bits.**
   - **Utilize the Vivado to simulate your design.**

Select Signal	Function Output
3'b000	a
3'b001	a + b
3'b010	a - b
3'b011	a * b
3'b100	a % 1 (remainder)
3'b101	a << 1
3'b110	a >> 1
3'b111	(a > b) (magnitude compare)

----------第一題作答區----------

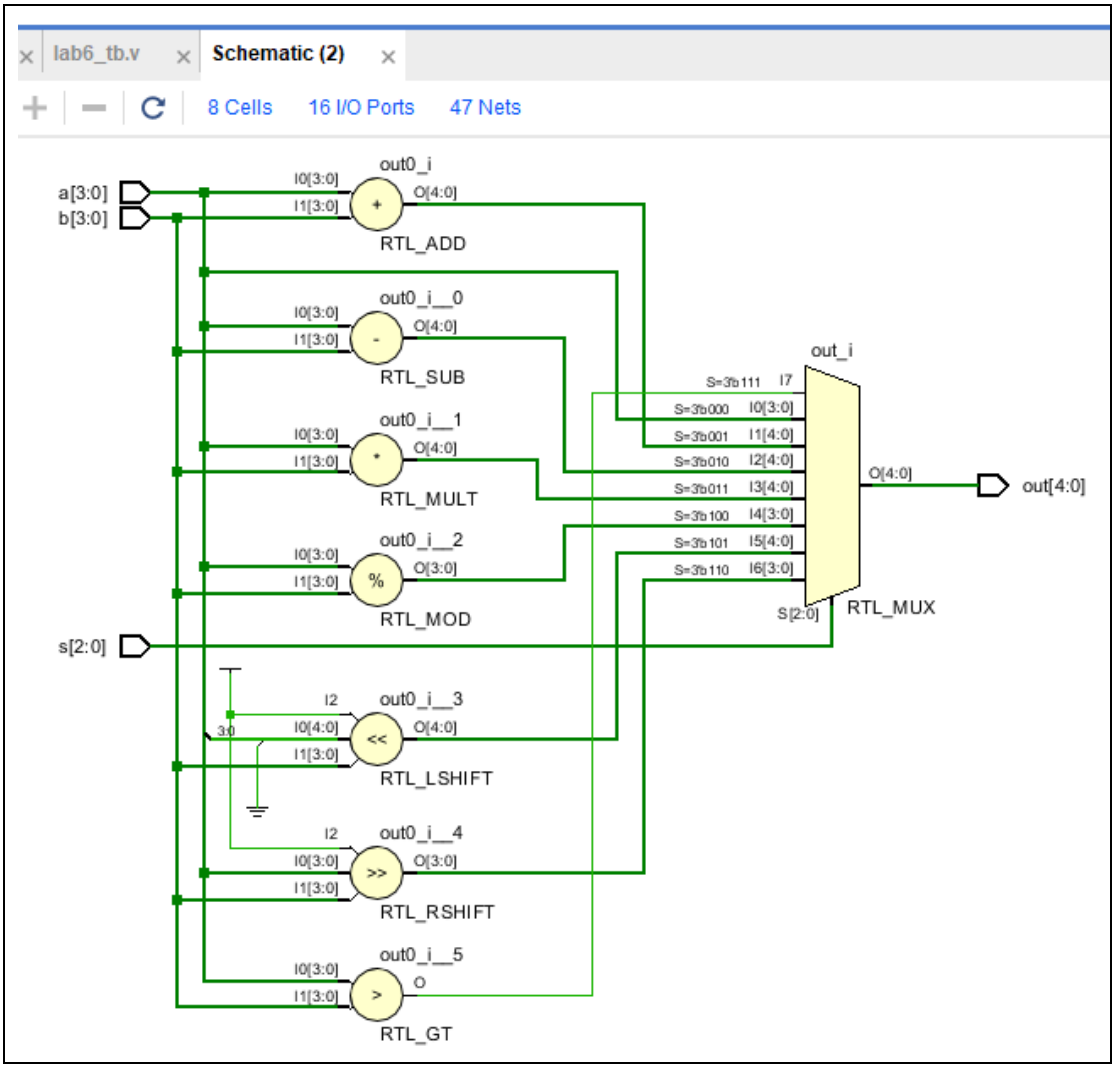
主(電路)程式

```
module alu (a, b, s, out);
output [4:0]out;
input [3:0]a,b;
input [2:0]s;
reg [4:0]out;
always @(a or b or s )
begin
    case (s)
        3'b000 : out = a;
        3'b001 : out = a+b;
        3'b010 : out = a-b;
        3'b011 : out = a*b;
        3'b100 : out = a%b;
        3'b101 : out = a<<b;
        3'b110 : out = a>>b;
        3'b111 : out = a>b;
        default: out = out;
    endcase
end
endmodule
```

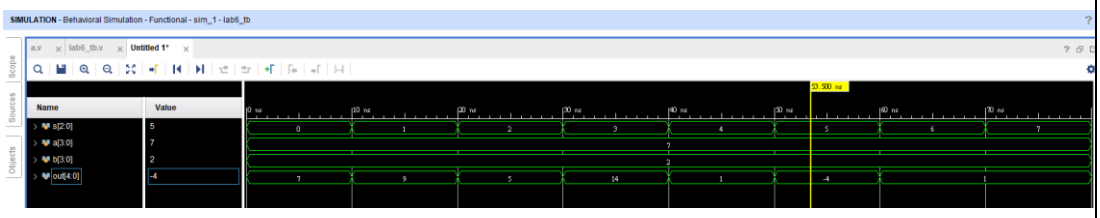
測試程式(testbench)

```
‘timescale 1ns / 1ps
module lab6_tb();
reg [2:0] s;
reg [3:0]a,b ;
wire [4:0]out;
alu UU1(a, b, s, out);
initial
begin
    $monitor($time," a = %b, b=%b, s= %b, out= %b\n",a,b,s,out);
end
initial
begin
    a=4'b0111;b=4'b0010;s=3'b000;
    #10 s = 3'b001;
    #10 s = 3'b010;
    #10 s = 3'b011;
    #10 s = 3'b100;
    #10 s = 3'b101;
    #10 s = 3'b110;
    #10 s = 3'b111;
end
initial #80 $finish;
endmodule
```

RTL schematic



Behavioral Simulation Waveform(含 $monitor)



```
# run 1000ns
                 0 a = 0111, b=0010, s= 000, out= 00111
                10 a = 0111, b=0010, s= 001, out= 01001
                20 a = 0111, b=0010, s= 010, out= 00101
                30 a = 0111, b=0010, s= 011, out= 01110
                40 a = 0111, b=0010, s= 100, out= 00001
                50 a = 0111, b=0010, s= 101, out= 11100
                60 a = 0111, b=0010, s= 110, out= 00001
                70 a = 0111, b=0010, s= 111, out= 00001

$finish called at time : 80 ns : File "C:/Users/User/project_1/project_1.srcs/sim_1/new/lab6_tb.v" Line 23
INFO: [USF-XSim-96] XSim completed. Design snapshot 'lab6_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
```

----------作答區結束----------

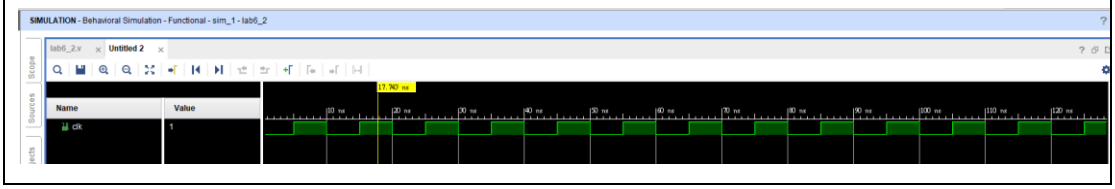
2. **Using a while loop, design a clock generator.**
   - **Initial value of clock is 0 and time period for the clock is 10.**

----------第一題作答區----------

測試程式(testbench)

```
module lab6_2(clk);
output clk;
reg clk;
initial
begin
    clk = 0 ;
    while (1'b1)
        begin #5 clk= ~clk;
    end
end
endmodule
```

Behavioral Simulation Waveform(含 $monitor)



----------作答區結束----------

（本題繳交作業內容請依照附表填入應有項目）

第一題 ： 主程式、測試程式、RTL Schematic、Behavioral waveform (include $monitor) 一共四項 (Hint : 波型輸出進制請選擇無號數形式顯示。)

第二題 ： 主程式(無)、測試程式、RTL Schematic(無)、Behavioral waveform (include $monitor) 一共兩項