國立高雄科技大學

電子工程系(第一校區)

硬體描述語言

Lab. 5: Blocking/Nonblocking

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Lab. 5: Blocking/Nonblocking (Chap. 7-A)

本次作業目標：了解 blocking & nonblocking 的動作方式。

(共四題，每題 25%，詳細配分級作答格式列於作業最後方)

1. Give below is an initial block with *blocking* procedural assignments.

- At what simulation time is each statement executed ?

  ANS：

      時間 0　時執行 0 丟給 a (Line1)

      時間 15 時執行 1 丟給 b (Line2)

      時間 25 時執行 1 丟給 c (Line3)

      時間 50 時將 a,b,c 丟給 d (Line4)

- What are the final values of *a, b, c, d* ?

  ANS： a=0 , b=1 , c=0 , d=010

```
initial
begin
    a = 1'b0;
    b = #15 1'b1;
    c = #10 1'b0;
    d = #25 {a,b,c};
end
```
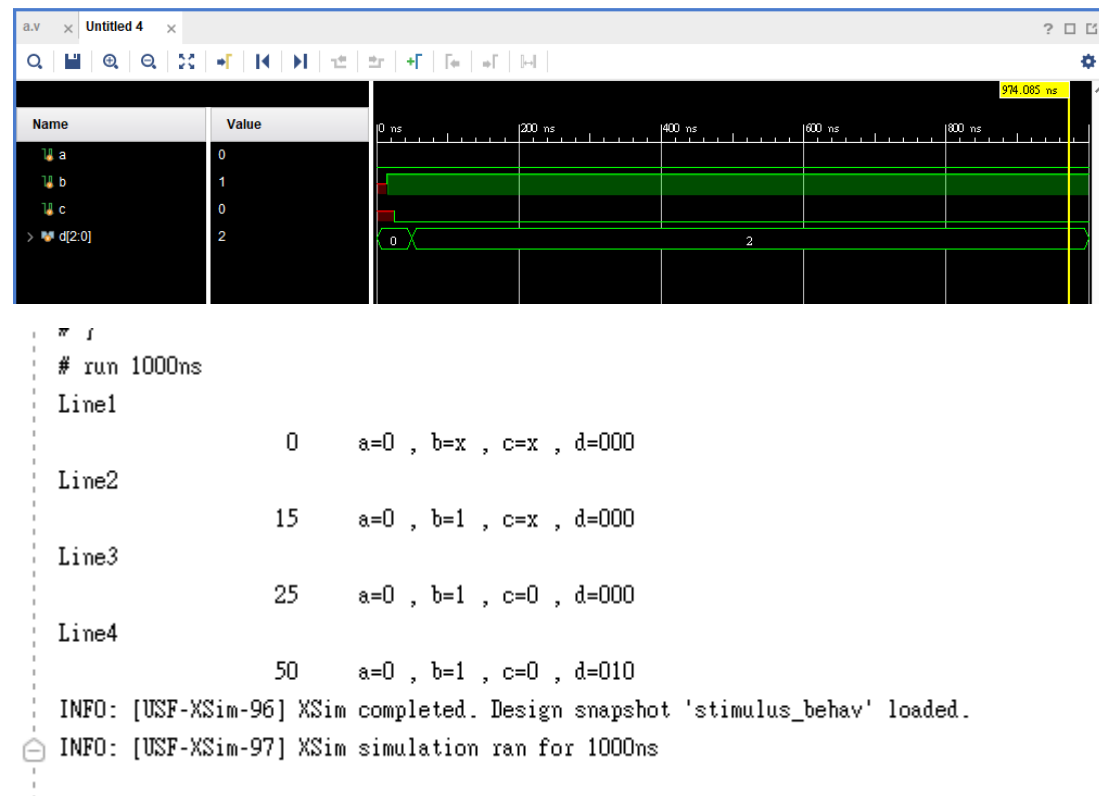

--第一題作答區--

測試程式(testbench)

```
C111112132 蕭詠釗 Lab5
module stimulus;
reg a, b, c;
reg[2:0] d=3'b000;
initial
begin
    a =1'b0 ;           $display("Line1");
    b =#15 1'b1;        $display("Line2");
    c =#10 1'b0;        $display("Line3");
    d =#25 {a, b, c};   $display("Line4");
end
initial
begin
    $monitor($time,"\t a=%b , b=%b , c=%b , d=%3b",a,b,c,d);
end
initial
```

```
begin
    #200 $finish;
end
endmodule
```

<table>
<tr><td colspan="1">Behavioral Simulation Waveform(含 $monitor)</td></tr>
</table>


```
# run 1000ns
Line1
                0       a=0 , b=x , c=x , d=000
Line2
                15      a=0 , b=1 , c=x , d=000
Line3
                25      a=0 , b=1 , c=0 , d=000
Line4
                50      a=0 , b=1 , c=0 , d=010
INFO: [USF-XSim-96] XSim completed. Design snapshot 'stimulus_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
```

---作答區結束---

2. Repeat exercise 1 if *nonblocking* procedural assignments were used.
   ● At what simulation time is each statement executed ?
     ANS：
          時間 0　時執行 0 丟給 a (Line1)
          時間 10 時準備將 0 丟給 c (Line2)
          時間 15 時準備將 1 丟給 b (Line3)
          時間 25 時準備將 a,b,c 丟給 d (Line4)
   ● What are the final values of *a, b, c, d* ?
     ANS：a=0 , b=1 , c=0 , d=xxx

---------------------------------------第一題作答區---

<table>
<tr><td>測試程式(testbench)</td></tr>
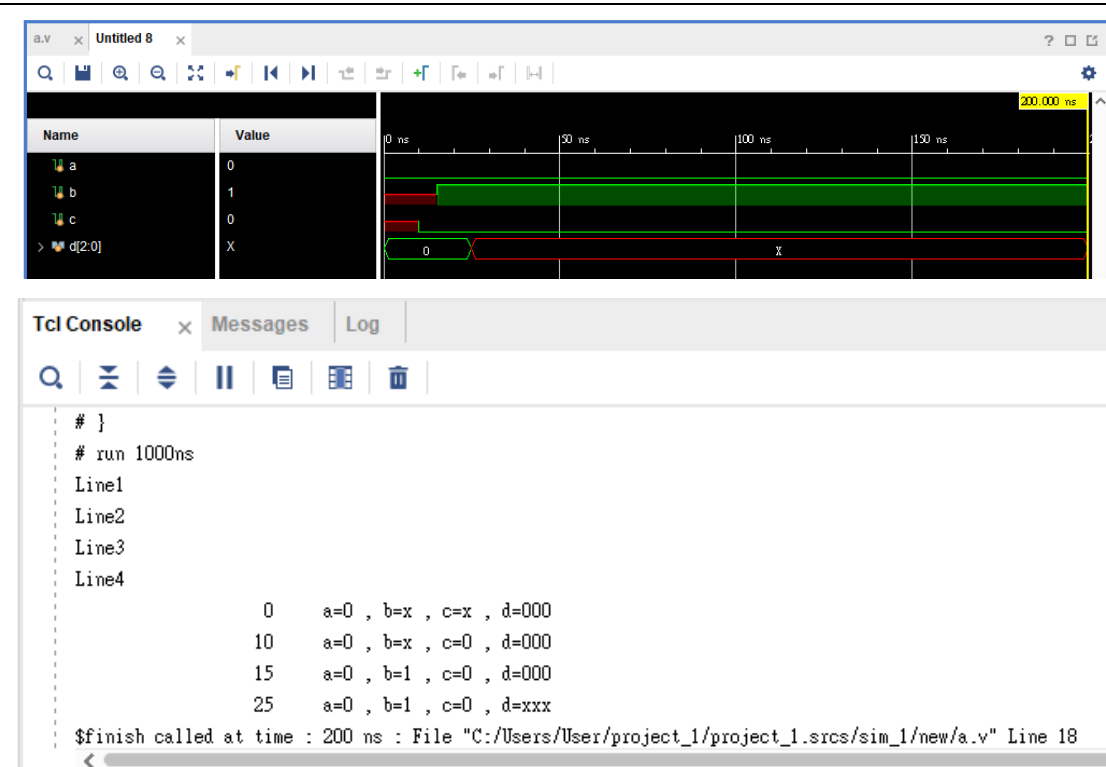</table>

```
C111112132 蕭詠釗 Lab5
module stimulus;
reg a, b, c;
reg[2:0] d=3' b000;
```

```
initial
begin
    a <=1'b0 ;          $display("Line1");
    b <=#15 1'b1;       $display("Line2");
    c <=#10 1'b0;       $display("Line3");
    d <=#25 {a, b, c};  $display("Line4");
end
initial
begin
    $monitor($time,"\t a=%b , b=%b , c=%b , d=%3b",a,b,c,d);
end
initial
begin
    #200 $finish;
end
endmodule
```

Behavioral Simulation Waveform(含 $monitor)

--作答區結束--

3. What is the order of execution of statements in the following Verilog code?
    ANS：Line1 => Line3 => Line2 => Line4
        Line1 = a = 1'b0;
        Line2 = #0 b = c;
        Line3 = c = 1'b1;

Line4 = #0 d = a;

Is there any ambiguity in the order of execution ?
ANS：no
What are the final values of *a, b, c, d* ?
ANS：a=0 b=1 c=1 d=000

```
initial
begin
        a = 1'b0;
        #0 b = c;
end


initial
begin
        c = 1'b1;
        #0 d = a;
end
```

--第一題作答區--

<table>
<tr><td>測試程式(testbench)</td></tr>
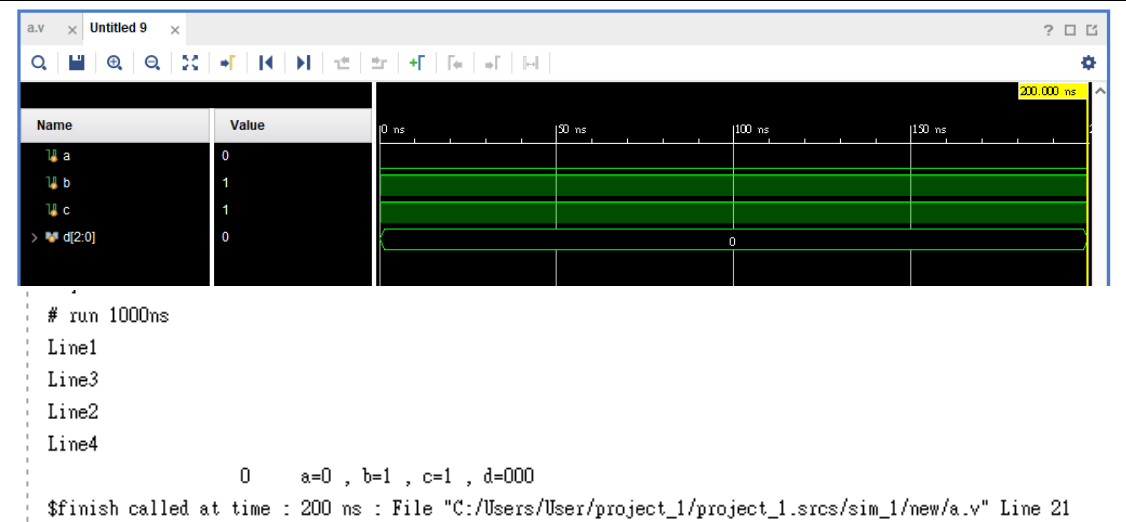</table>

```
C111112132 蕭詠釗 Lab5
module stimulus;
reg a, b, c;
reg[2:0] d=3'b000;
initial
begin
     a = 1'b0; $display("Line1");
     #0 b = c;$display("Line2");
end
initial
begin
     c = 1'b1;$display("Line3");
     #0 d = a;$display("Line4");
end
initial
begin
   $monitor($time,"\t a=%b , b=%b , c=%b , d=%3b",a, b, c, d);
end
initial
begin
```

```
    #200 $finish;
end
endmodule
```

Behavioral Simulation Waveform(含 $monitor)


```
# run 1000ns
Line1
Line3
Line2
Line4
               0    a=0 , b=1 , c=1 , d=000
$finish called at time : 200 ns : File "C:/Users/User/project_1/project_1.srcs/sim_1/new/a.v" Line 21
```

--作答區結束--

4. What is the final value of *d* in the following example?

ANS：d=0

(Hint: See intra-assignment delays.)

```
initial
begin
        b = 1'b0; c = 1'b1;
        #10 b = 1'b1;
end
initial
begin
        d = #20 (b & c);
end
```

--第一題作答區--

測試程式(testbench)
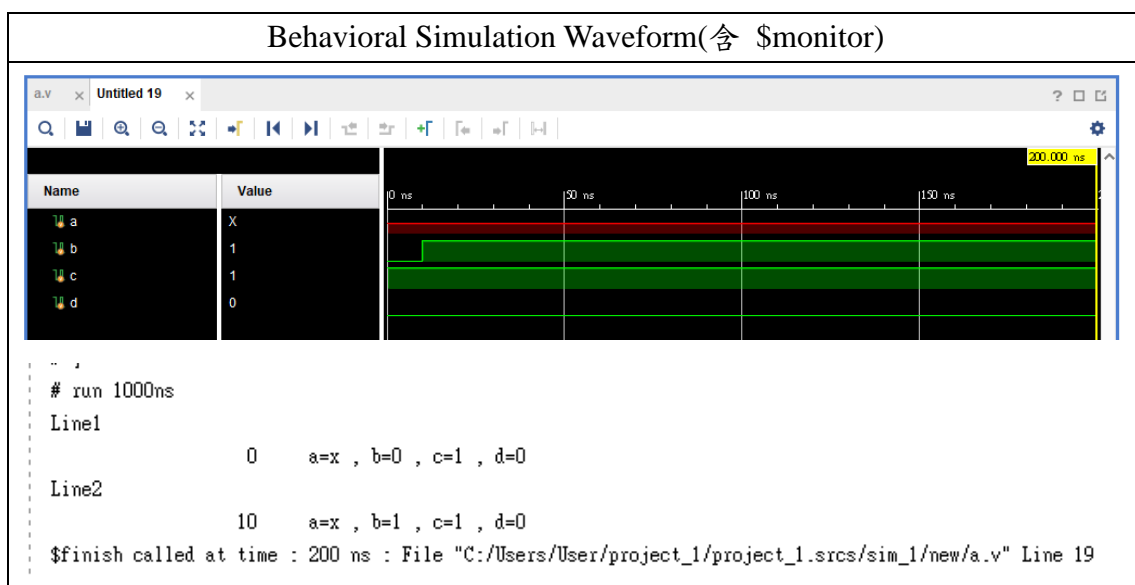
```
C111112132 蕭詠釗 Lab5
module stimulus;
reg a, b, c;
reg d=1'b0;
initial
begin
```

```
        b = 1'b0; c = 1'b1;$display("Line1");
        #10 b = 1'b1;$display("Line2");
end
initial
begin
        d = #20 (b & c);
end
initial
begin
    $monitor($time,"\t a=%b , b=%b , c=%b , d=%b",a,b,c,d);
end
initial
begin
    #200 $finish;
end
endmodule
```

Behavioral Simulation Waveform(含 $monitor)


```
# run 1000ns
Line1
                0       a=x , b=0 , c=1 , d=0
Line2
                10      a=x , b=1 , c=1 , d=0
$finish called at time : 200 ns : File "C:/Users/User/project_1/project_1.srcs/sim_1/new/a.v" Line 19
```

---作答區結束---

作答方式

　　本次作業全部都是寫測試程式來模擬電路的動作順序，故於建立檔案時要記得是在 View = Simulation 的欄位下右鍵點選 xc3c200a-4dt256 之後建立一個 Verilog Test Fixture 再開始撰寫程式，題目給的為程式片段請自行將其填入。

本次作業作答格式

每題的黏貼順序請按照下列順序
[1]　測試程式(註解記得加上學號姓名以及 Lab 說明)。

★ 程式碼一樣是使用 notepad++匯出成 PDF 檔再插入。

★ 程式轉檔後有橘或綠的顏色標示，請關閉 notpad++重啟程式即可解決。

[2]　　Simulation Waveform (含 $monitor 結果)。

[3]　　依照題目回答問題。

作業評分方式

　每題三個項目內容各 8 分排版 1 分，本次評分細項如下。

[1]　　程式若有橘或綠標示遮擋程式，程式項以 0 分計算。

[2]　　程式無適當縮排扣 2 分。

[3]　　波型模擬若無檢附 $monitor 扣 4 分。

[4]　　根據答題內容一個錯誤扣 2 分