國立高雄科技大學

電子工程系(第一校區)

硬體描述語言

Lab 9

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Lab. 9

1. Define a **function** to **multiply** two 4-bit numbers a and b.
   - The output is an 8-bit value.
   - Invoke the function by using stimulus and check results.
   - Multiply List :
     - (1) #25 2*3
     - (2) #25 9*4
     - (3) #25 8*7
     - (4) #25 6*9

   作業作答格式

   檢附項目 : 主(電路)程式、測試程式、RTL schematic、Technology Schematic、Behavioral Simulation Waveform(含 $monitor)。

   ----------第一題作答區----------

主(電路)程式

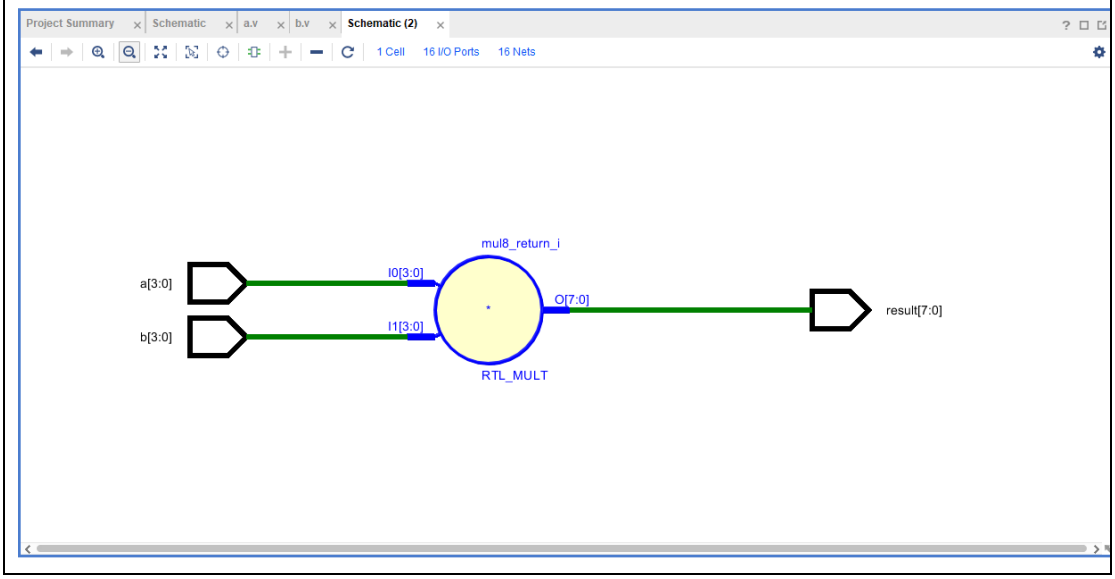
```
`timescale 1ns / 1ps
module mult(result,a,b);
output [7:0] result;
input  [3:0] a,b;
reg [7:0] result;

function [7:0] mul8;
input [3:0] a,b;
begin
    mul8 = a * b ;
end
endfunction

always @(a or b)
    result = mul8(a,b);
endmodule
```

測試程式(testbench)

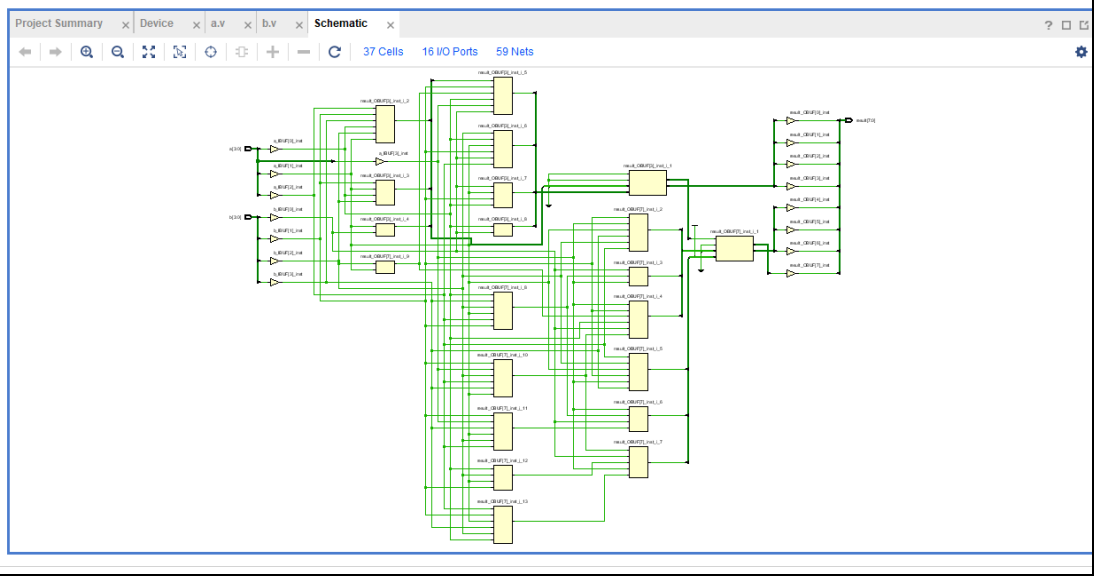
```
`timescale 1ns / 1ps
module stimulus;
    reg [3:0] a,b;
    wire [7:0] result;
mult uut(result,a,b);

initial begin
    a=0;b=0;
    #25 a=4'b0010 ;b=4'b0011;
```

```
        #25 a=4'b1001 ;b=4'b0100;
        #25 a=4'b1000 ;b=4'b0111;
        #25 a=4'b0110 ;b=4'b1001;
end
initial begin
        #150 $finish;
end
initial $monitor($time,"a=%d , b=%d, result=%d",a , b, result);
endmodule
```

RTL schematic



Technology Schematic



Behavioral Simulation Waveform(含 $monitor)


```
# run 1000ns
                    0a= 0 , b= 0, result=  0
                   25a= 2 , b= 3, result=  6
                   50a= 9 , b= 4, result= 36
                   75a= 8 , b= 7, result= 56
                  100a= 6 , b= 9, result= 54
$finish called at time : 150 ns : File "C:/Users/User/project_1/project_1.srcs/sim_1/new/b.v" Line 15
INFO: [USF-XSim-96] XSim completed. Design snapshot 'stimulus_behav' loaded
```

2. Define a **task** to compute **even parity** of a 16-bit number.
   - The result is a 1-bit value that is assigned to the output after three positive edges of clock.
     (Hint: use a **repeat** loop in the task)

作業說明

Even parity :
在一串(N-1)個資料上加上一個同位元檢查位元，成為N個位元資料串。
依照最後資料中高電位(1)的個數結果有以下兩種 :

1. 奇同位元 (odd parity) (表示N個位元裡總共有奇數的1)
2. 偶同位元 (even parity) (表示N個位元裡總共有偶數的1)

EXAMPLE :

parity check	data	parity bit
even parity	0110111	1 (6 個 1)
odd parity	0110111	0 (5 個 1)

作業作答格式
檢附項目 : 主(電路)程式、測試程式、RTL schematic、Technology Schematic、Behavioral Simulation Waveform(含 $monitor)，。

----------第二題作答區----------

主(電路)程式

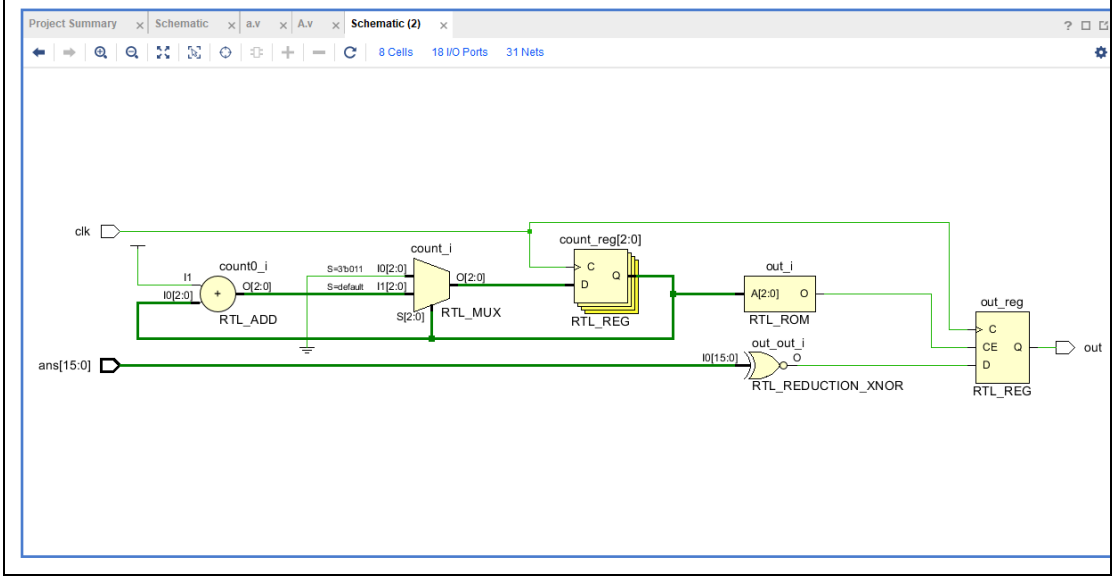
```
`timescale 1ns / 1ps
module a(out, ans, clk);
input [15:0] ans;
output out;
input clk;
reg out;
reg [2:0] count;
always @(posedge clk)
begin
    if (count == 3)
    begin
        compute_parity(out, ans);
        count <= 0;
     end
     else
         count <= count + 1;
    end
    initial
    begin
        count <= 0;
```

```
        repeat (3) @(posedge clk);
    end
     task compute_parity;
          output out;
          input [15:0] ans;
        begin
              out = ~^ans;
        end
    endtask
endmodule
```

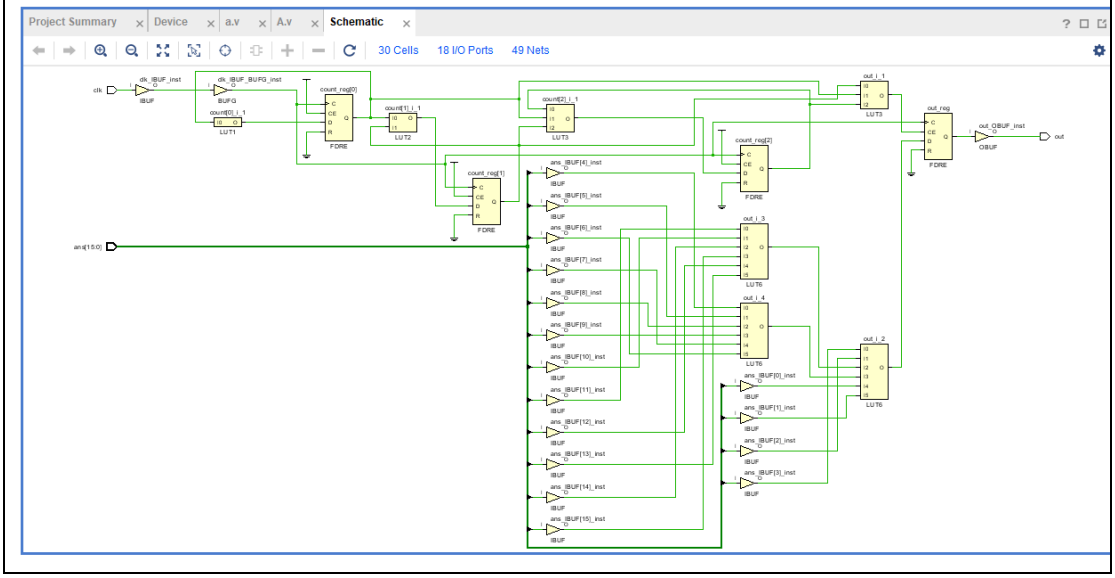
測試程式(testbench)

```
`timescale 1ns / 1ps
module b;
reg[15:0] ans;
reg clk=1'b0;
wire out;
a uut (out,ans,clk);
initial begin
      forever #5 clk=~clk;
end
initial begin
      #15    ans=16'b0000000000000001;
      #115 ans=16'b0000000000000011;
      #300 $finish;
end
initial $monitor($time,"ans=%b, out=%b", ans, out);
endmodule
```

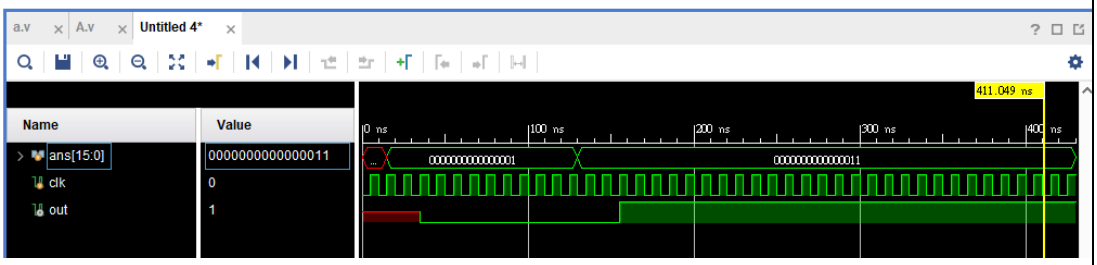
RTL schematic



Technology Schematic



Behavioral Simulation Waveform(含 $monitor)




```
# run 1000ns
                   0ans=xxxxxxxxxxxxxxxx, out=x
                  15ans=0000000000000001, out=x
                  35ans=0000000000000001, out=0
                 130ans=0000000000000011, out=0
                 155ans=0000000000000011, out=1
$finish called at time : 430 ns : File "C:/Users/User/project_2/project_2.srcs/sim_1/new/A.v" Line 13
```

----------作答區結束----------