國立高雄科技大學

電子工程系(第一校區)

硬體描述語言

Lab 4

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Lab 4.

1. A master-slave D-type flipflops is designed with a negative edge clk. Circuit diagram for the D-type flipflop is given below. Write the dataflow description for the D-type flipflops. And write a stimulus file for testing the function.

TestBench Hint:

(TestBench Hint: The input signal D toggles every 15 ns, while the clock signal CLK toggles every 5 ns. The simulation terminates at 200 ns.)

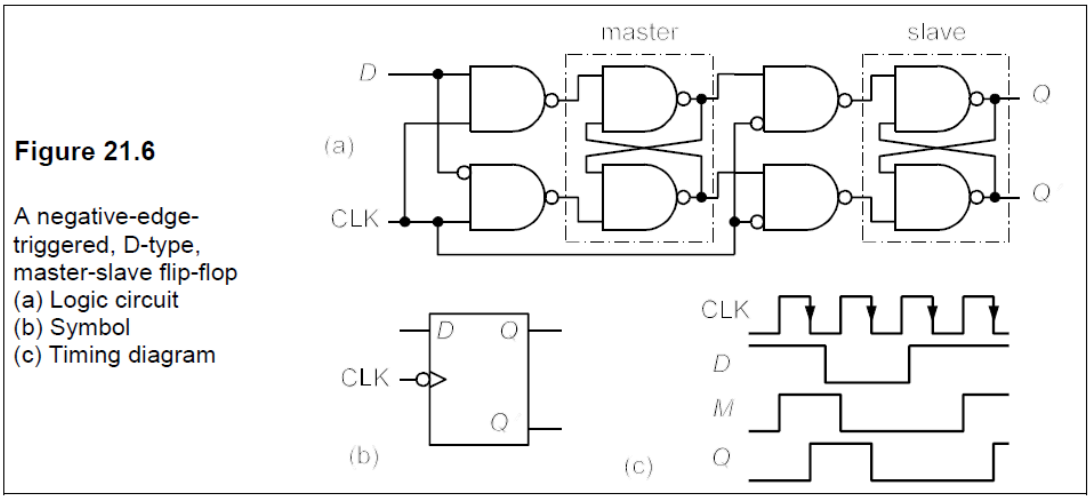


Figure 21.6

A negative-edge-triggered, D-type, master-slave flip-flop
(a) Logic circuit
(b) Symbol
(c) Timing diagram

資料來源: https://link.springer.com/content/pdf/10.1007%2F978-0-230-21633-4_21.pdf

----------第一題作答區----------

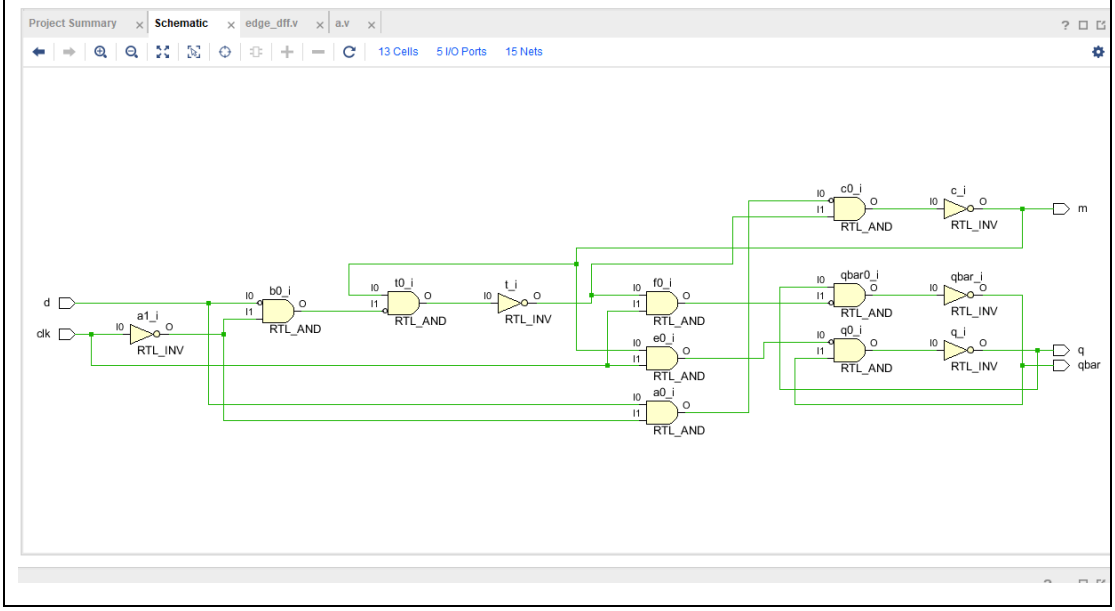
主(電路)程式

```
module edge_dff(d,clk, q,qbar,m);
output q,qbar,m;
input d, clk;

wire a,b,c,t,e,f;

assign a = ~(d & ~clk),
b = ~(~d & ~clk),
c = ~( a & t),
t = ~( c & b),
e = ~( c & clk),
f = ~( t & clk);

assign q =~(e & qbar);
assign qbar =~(q & f);
assign m =c;
endmodule
```

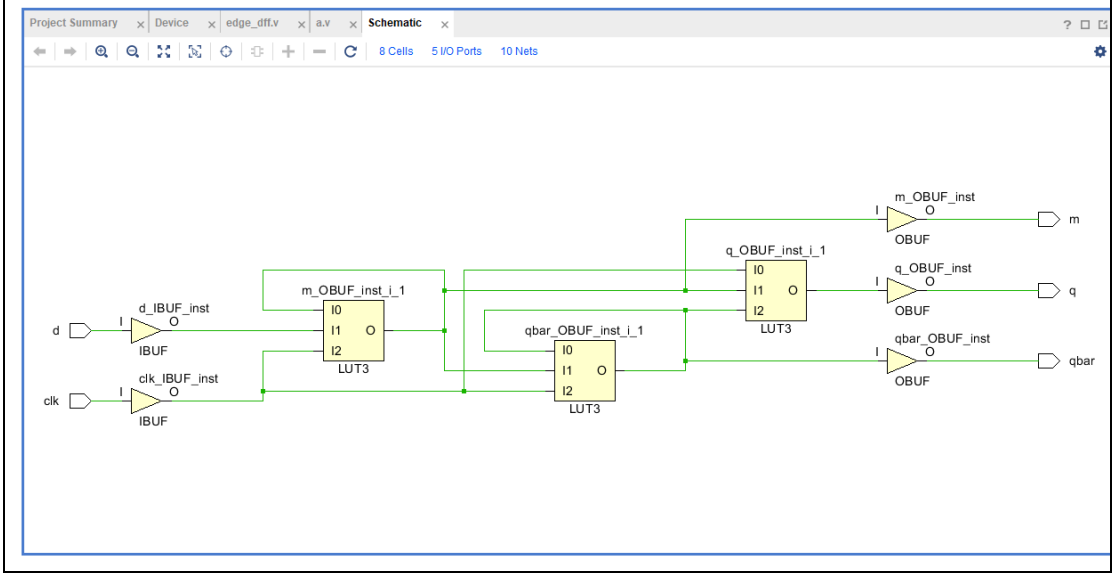
測試程式(testbench)

```
module stimulus;
reg d, clk;
wire q,qbar;

edge_dff UUT(d,clk, q,qbar,m);

initial
begin
    clk = 1'b0;
    forever #5 clk = ~clk;
end
initial
begin
    $monitor($time, " \t d = %b clk= %b q= %b m= %b ",d,clk,q,m);
    d = 1'b0;
    forever #15 d = ~d;
end
initial
begin
    #200 $finish;
end
endmodule
```

RTL schematic



Technology Schematic



Behavioral Simulation Waveform(含 $monitor)

```
# run 1000ns
                   0     d = 0 clk= 0 q= x m= 0
                   5     d = 0 clk= 1 q= 0 m= 0
                  10     d = 0 clk= 0 q= 0 m= 0
                  15     d = 1 clk= 1 q= 0 m= 0
                  20     d = 1 clk= 0 q= 0 m= 1
                  25     d = 1 clk= 1 q= 1 m= 1
                  30     d = 0 clk= 0 q= 1 m= 0
                  35     d = 0 clk= 1 q= 0 m= 0
                  40     d = 0 clk= 0 q= 0 m= 0
                  45     d = 1 clk= 1 q= 0 m= 0
                  50     d = 1 clk= 0 q= 0 m= 1
                  55     d = 1 clk= 1 q= 1 m= 1
                  60     d = 0 clk= 0 q= 1 m= 0
                  65     d = 0 clk= 1 q= 0 m= 0
                  70     d = 0 clk= 0 q= 0 m= 0
                  75     d = 1 clk= 1 q= 0 m= 0
                  80     d = 1 clk= 0 q= 0 m= 1
                  85     d = 1 clk= 1 q= 1 m= 1
                  90     d = 0 clk= 0 q= 1 m= 0
                  95     d = 0 clk= 1 q= 0 m= 0
                 100     d = 0 clk= 0 q= 0 m= 0
                 105     d = 1 clk= 1 q= 0 m= 0
                 110     d = 1 clk= 0 q= 0 m= 1
                 115     d = 1 clk= 1 q= 1 m= 1
                 120     d = 0 clk= 0 q= 1 m= 0
                 125     d = 0 clk= 1 q= 0 m= 0
                 130     d = 0 clk= 0 q= 0 m= 0
                 135     d = 1 clk= 1 q= 0 m= 0
                 140     d = 1 clk= 0 q= 0 m= 1
                 145     d = 1 clk= 1 q= 1 m= 1
                 150     d = 0 clk= 0 q= 1 m= 0
                 155     d = 0 clk= 1 q= 0 m= 0
                 160     d = 0 clk= 0 q= 0 m= 0
                 165     d = 1 clk= 1 q= 0 m= 0
                 170     d = 1 clk= 0 q= 0 m= 1
                 175     d = 1 clk= 1 q= 1 m= 1
                 180     d = 0 clk= 0 q= 1 m= 0
                 185     d = 0 clk= 1 q= 0 m= 0
                 190     d = 0 clk= 0 q= 0 m= 0
                 195     d = 1 clk= 1 q= 0 m= 0
                 195     d = 1 clk= 1 q= 0 m= 0
$finish called at time : 200 ns : File "C:/Users/User/project_1/project_1.srcs/sim_1/new/a.v" Line 20
INFO: [USF-XSim-96] XSim completed. Design snapshot 'stimulus_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
```

----------作答區結束----------