REVISION HISTORY

4

3

2

Schematics Index:

P01: REVISION HISTORY

P02: BLOCK

P03: POWER TREE

P04: GPIO ASSIGNMENT

P05: SOC1

P06: SOC2

P07: DDR3 16X2

P08: POWER

P09: NAND-eMMC

P10: CARD-USB-IR-SPDIF

P11: KEY-LED-ETH-DEBUG

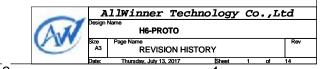
P12: AV-HDMI

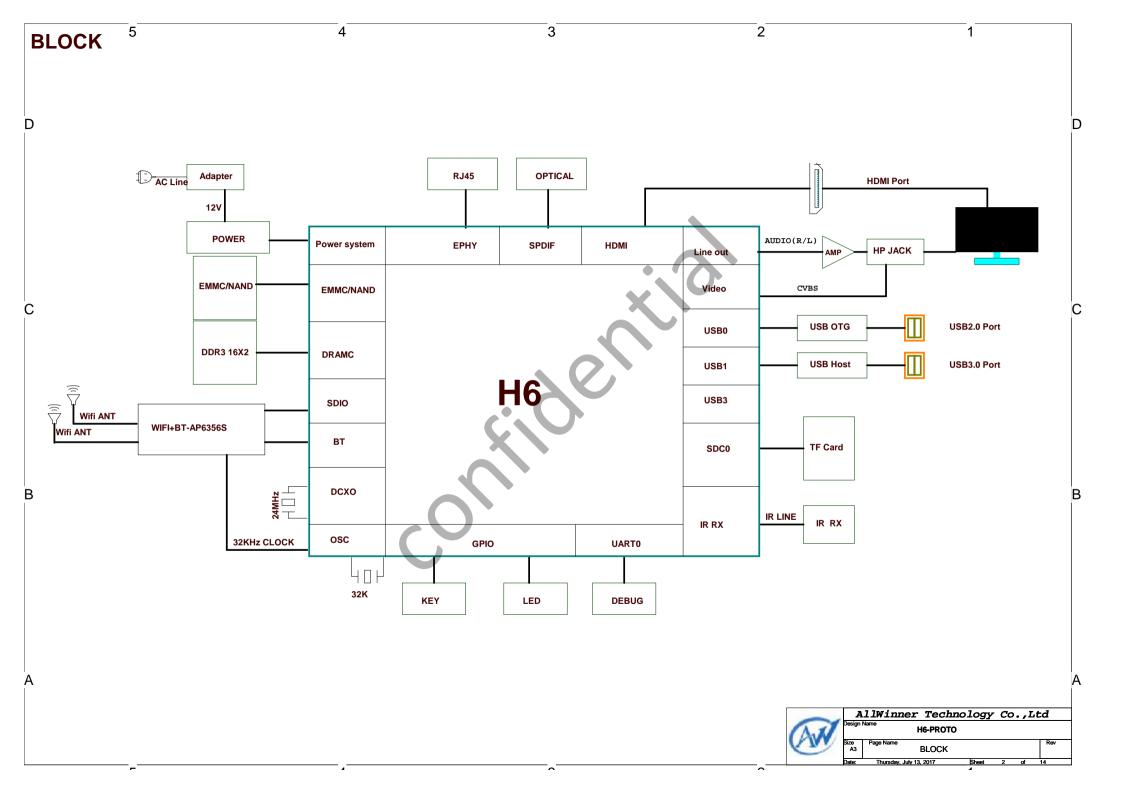
P13: WIFI-BT 2T2R P14: WIFI-BT 1T1R

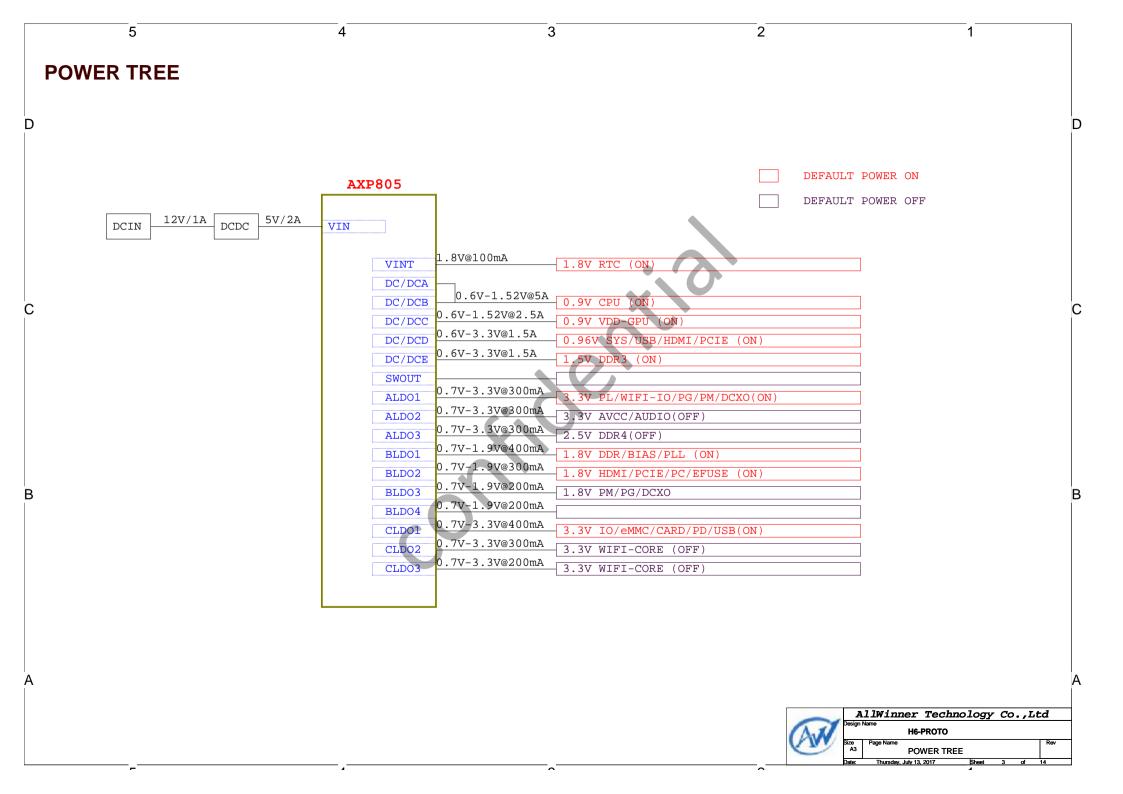
P15: GMAC

Revision	Description	Date	Drawn	Checked
Ver 0.5	Initial Version	2016-12-26	HJ	
Ver 0.9		2017-04-10	HJ	
Ver 1.0		2017-07-06	НЈ	









PIN Define

PC0 NAND WE

PC2 NAND_CLE

PC3 NAND_CE0

PC1 NAND_ALE/SDC2_DS

PC4 NAND_RE/SDC2_CLK

PC6 NAND_DQ0/SDC2_D0

PC7 NAND_DQ1/SDC2_D1

PC8 NAND_DQ2/SDC2_D2

PC9 NAND_DQ3/SDC2_D3

PC10NAND_DQ4/SDC2_D4

PC11NAND_DQ5/SDC2_D5

PC12NAND_DQ6/SDC2_D6

PC13NAND_DQ7/SDC2_D7

PC14NAND_DQS/SDC2_RST

PC15NAND_CE1

PC16 NAND_RB1

PC5 NAND_RB0/SDC2_CMD

4

CFG Function

2/3 NAND/eMMC

2/3

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2/3

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PIN	Define	CFG	Funct
PD0			
PD1			
PD2			
PD3			
PD4			
PD5			
PD6			
PD7			
PD8			
PD9			
PD10			
PD11			
PD12			l .
PD13			1
PD14			

PIN	Define	CFG	Function
PD15			
PD16			
PD17			
PD18			
PD19			
PD20			
PD21			
PD22			
PD23			
PD24			
PD25			
PD26			

PIN	Define	CFG	Function
PG0	SDC1_CLK	2	
PG1	SDC1_CMD	2	
PG2	SDC1_D0	2	
PG3	SDC1_D1	2	
PG4	SDC1_D2	2	
PG5	SDC1_D3	2	
PG6	UART1_TX	2	WIFI+BT
PG7	UART1_RX	2	MILITEI
PG8	UART1_RTS	2	
PG9	UART1_CTS	2	
PG10	PCM2_SYNC	2	
PG11	PCM2_CLK	2	
PG12	PCM2_DOUT	2	
PG13	PCM2_DIN	2	
PG14	!		

PIN	Define	CFG	Function
PF0	SDC0_D1	2	
PF1	SDC0_D0	2	
PF2	SDC0_CLK/UART0_TX	2/3	
PF3	SDC0_CMD	2	CARD0
PF4	SDC0_D3/UART0_RX	2/3	
PF5	SDC0_D2	2	
PF6	SDC0-DET	2	

PIN	Define	CFG	Function
PH0	CPUX-UTX	2	
PH1	CPUX-URX	2	
PH2	DDC_CEC_EN	6	1
PH3			
PH4			
PH5]
РНб			
PH7	SPDIF_OUT	3	
PH8	HSCL	2	
PH9	HSDA	2	HDMI
PH10	HCEC	2	

PIN	Define	CFG	Function
PL0	PMU-SCK	3	
PL1	PMU-SDA	3	
PL2	RECOVERY	6	
PL3	LINK-LED	1	
PL4	PWR-LED	1	
PL5	USB0-DRVVBUS	1	
PL6	MUTE	1	
PL7	STATUS-LED	1	
PL8	BT-WIFI-ON	1	
PL9	IR-RX	2	
PL10			
PM0	WL-WAKE-AP	6	
PM1	BT-WAKE-AP	6	
PM2	AP-WAKE-BT	1	WIFI+BT
PM3	WL-REG-ON	1	MILILDI
PM4	BT-REG-ON	1	

AllWinner Technology Co.,Ltd

Design Name
H6-PROTO
Size Page Name
GPIO ASSIGNMENT
Deter Thursday July 20 2017 Sheet 4 of 14

