

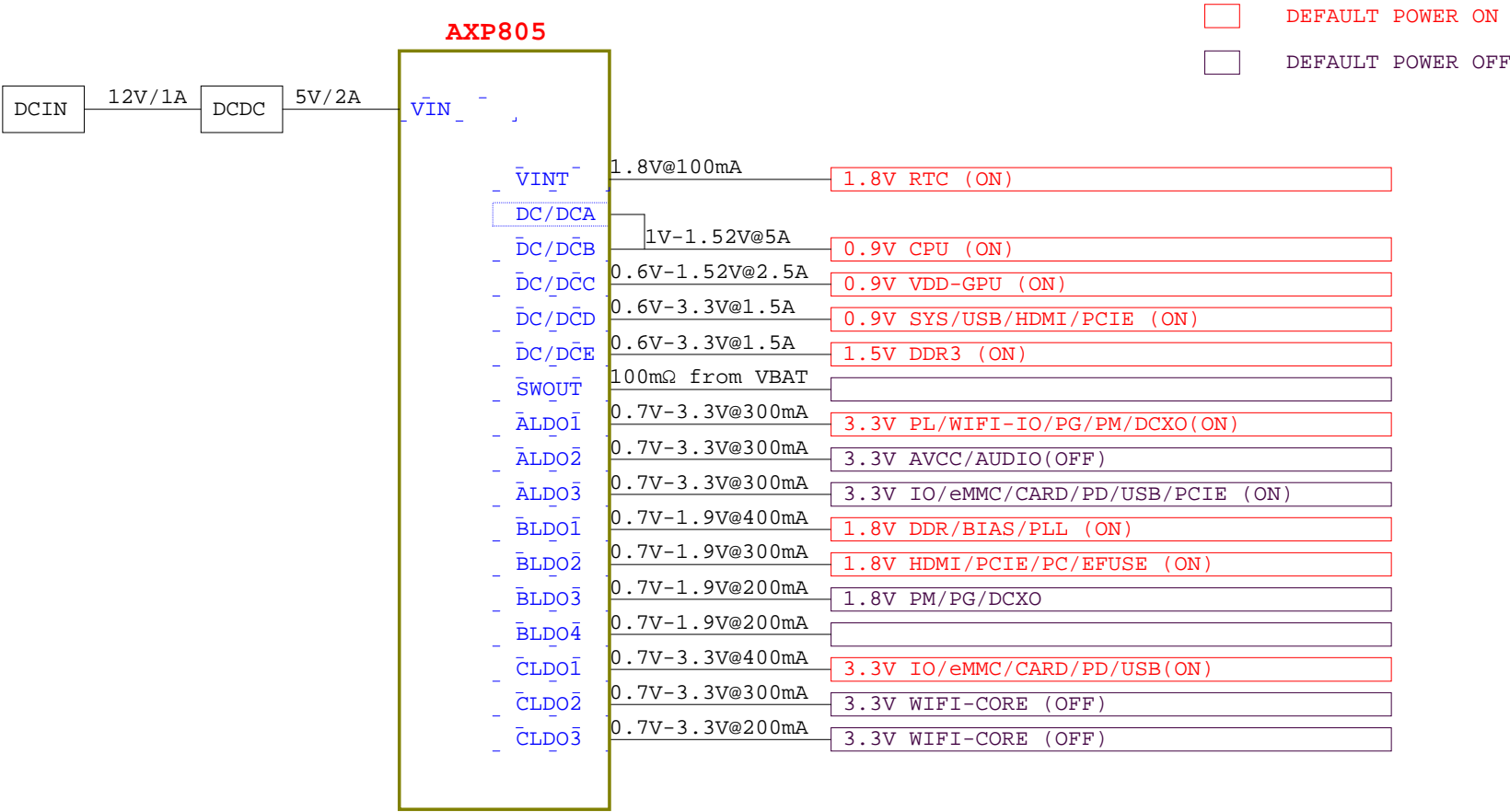
5  
REVISION HISTORY

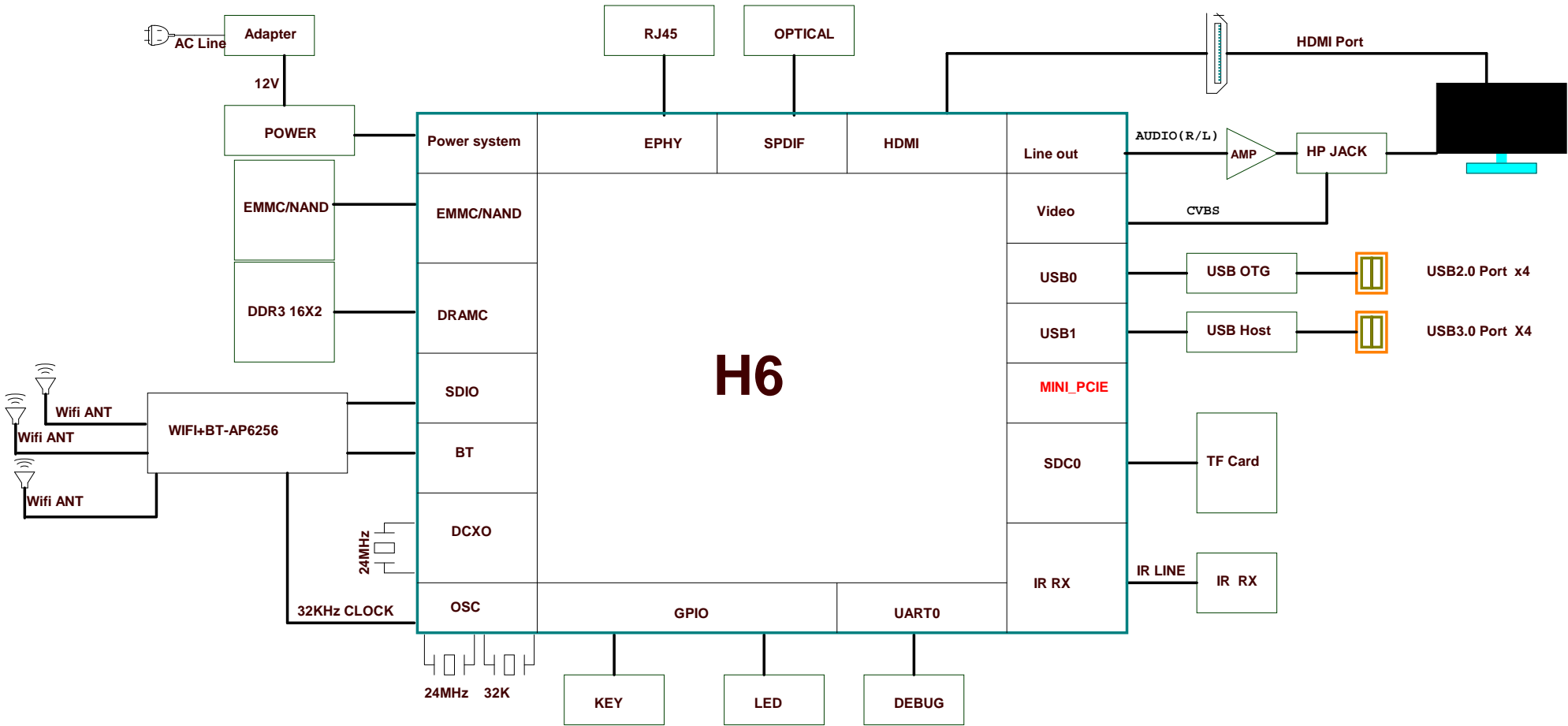
Revision	Description	Date	Drawn	Checked
Ver 0.5	Initial Version	2016-12-26	HJ	
Ver 0.8		2017-02-23	HJ	
Ver 0.9		2017-03-22	HJ	
Ver 1.0	1.增加电阻，连通VCC18-RTC 和 VDD18-LPDDR 2.将HDMI和CAMERA处的SDA SCK网络进行调整，H6分两组来控制HDMI和CAMERA。 3.将H6 的PG14脚悬空。 4.主控处的电压改接成BLD01,之前是与DDR3共用。 5.将CAMERA与HDMI IN处复用的网络用0R电阻分开接出，PCB中绕线更短。 6.将之前40PIN座子修改成26PIN 7.新增USB3.0_HUB功能 8.新增千兆网口模块	2018-03-20		
	9. 12页去掉AUDIO部分的放大电路模块，左右声道各加一个电阻和电容 10.13页 USB3.0去掉EEPOM模块			
Ver 1.1	11.13页 USB3.0接口处的0R电阻去掉，修改TX->RX网络，ESD器件预留0402的封装，VCC18-RTC与VDD18-LPDDR网络通过0R电阻连接			
Ver 1.6	从AP6255更换到AP6256型号	2024-04-17		

Schematics Index:

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P14: MINI PCIe  
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POWER TREE





GPIO ASSIGNMENT

PIN	Define	CFG	Function
PC0	NAND_WE	2	NAND/eMMC
PC1	NAND_ALE/SDC2_DS	2/3	
PC2	NAND_CLE	2	
PC3	NAND_CE0	2	
PC4	NAND_RE/SDC2_CLK	2/3	
PC5	NAND_RB0/SDC2_CMD	2/3	
PC6	NAND_DQ0/SDC2_D0	2/3	
PC7	NAND_DQ1/SDC2_D1	2/3	
PC8	NAND_DQ2/SDC2_D2	2/3	
PC9	NAND_DQ3/SDC2_D3	2/3	
PC10	NAND_DQ4/SDC2_D4	2/3	
PC11	NAND_DQ5/SDC2_D5	2/3	
PC12	NAND_DQ6/SDC2_D6	2/3	
PC13	NAND_DQ7/SDC2_D7	2/3	
PC14	NAND_DQS/SDC2_RST	2/3	
PC15	NAND_CE1	2	
PC16	NAND_RB1	2	

PIN	Define	CFG	Function
PD0			
PD1			
PD2			
PD3			
PD4			
PD5			
PD6			
PD7			
PD8			
PD9			
PD10			
PD11			
PD12			
PD13			
PD14			

PIN	Define	CFG	Function
PD15			
PD16			
PD17			
PD18			
PD19			
PD20			
PD21			
PD22			
PD23			
PD24			
PD25			
PD26			

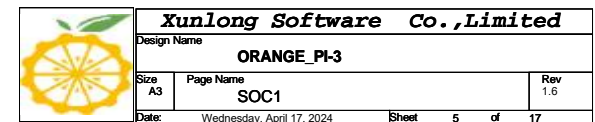
PIN	Define	CFG	Function
PG0	SDC1_CLK	2	WIFI+BT
PG1	SDC1_CMD	2	
PG2	SDC1_D0	2	
PG3	SDC1_D1	2	
PG4	SDC1_D2	2	
PG5	SDC1_D3	2	
PG6	UART1_TX	2	
PG7	UART1_RX	2	
PG8	UART1_RTS	2	
PG9	UART1_CTS	2	
PG10	PCM2_SYNC	2	
PG11	PCM2_CLK	2	
PG12	PCM2_DOUT	2	
PG13	PCM2_DIN	2	
PG14			

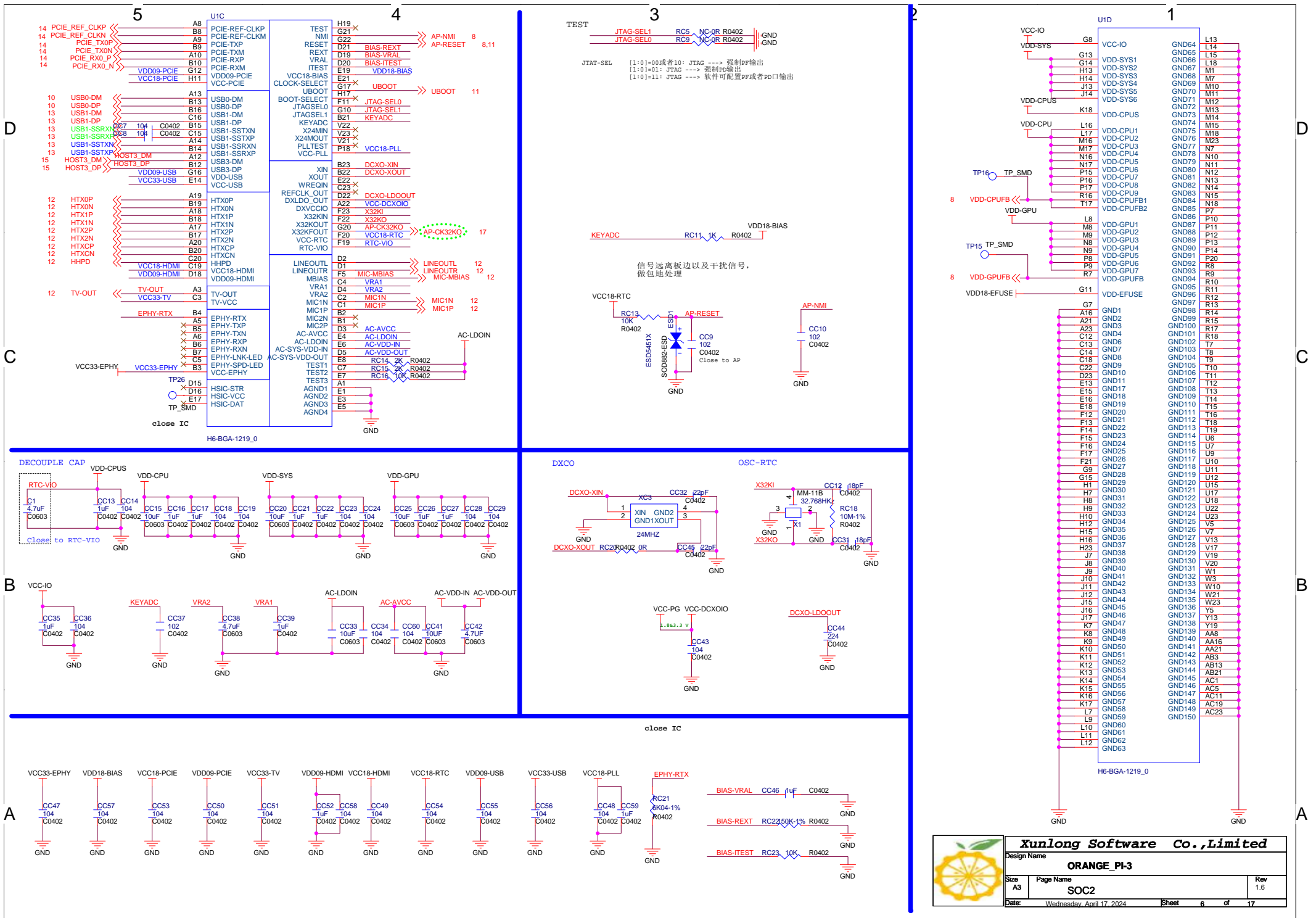
PIN	Define	CFG	Function
PF0	SDC0_D1	2	CARD0
PF1	SDC0_D0	2	
PF2	SDC0_CLK/UART0_TX	2/3	
PF3	SDC0_CMD	2	
PF4	SDC0_D3/UART0_RX	2/3	
PF5	SDC0_D2	2	
PF6	SDC0-DET	2	

PIN	Define	CFG	Function
PH0	CPUX-UTX	2	
PH1	CPUX-URX	2	
PH2			
PH3			
PH4			
PH5			
PH6			
PH7	SPDIF_OUT	3	
PH8	HSCL	2	
PH9	HSDA	2	
PH10	HCEC	2	HDMI

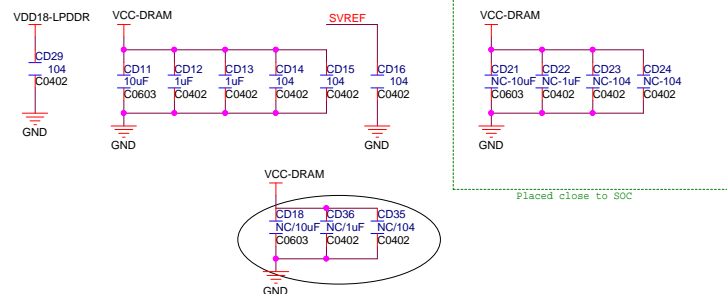
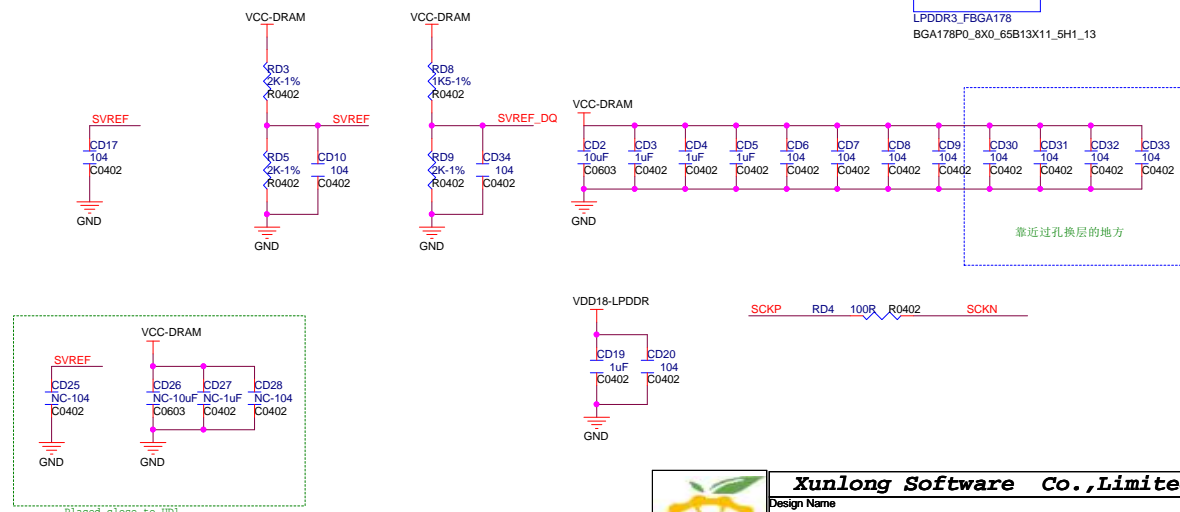
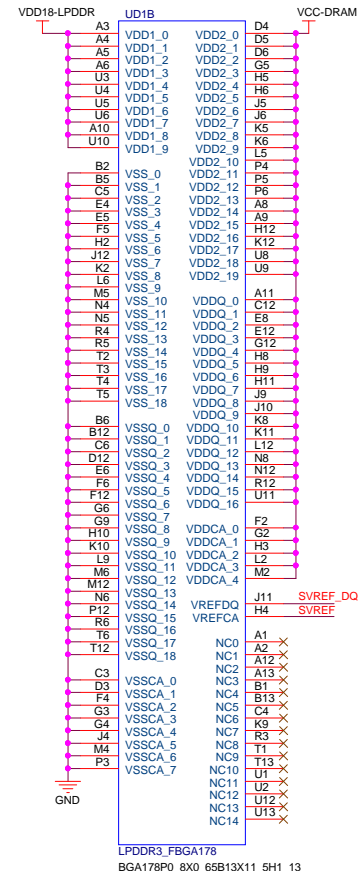
PIN	Define	CFG	Function
PL0	PMU-SCK	3	WIFI+BT
PL1	PMU-SDA	3	
PL2	RECOVERY	2	
PL3	LINK-LED	1	
PL4	PWR-LED	1	
PL5	USB0-DRVVBUS	1	
PL6	MUTE	1	
PL7	STATUS-LED	1	
PL8			
PL9	IR-RX	2	
PL10	BT-WIFI-ON	1	
PM0	WL-WAKE-AP	0	
PM1	BT-WAKE-AP	0	
PM2	AP-WAKE-BT	1	
PM3	WL-REG-ON	1	
PM4	BT-REG-ON	1	





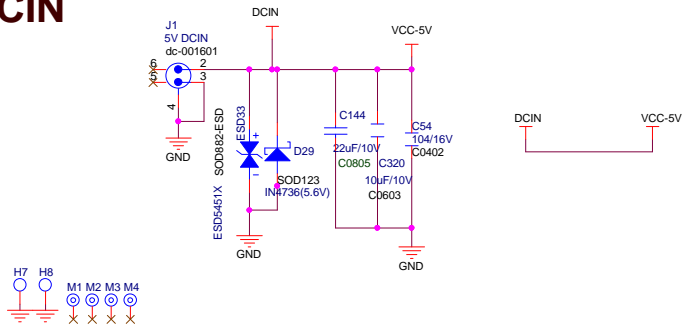


## 1



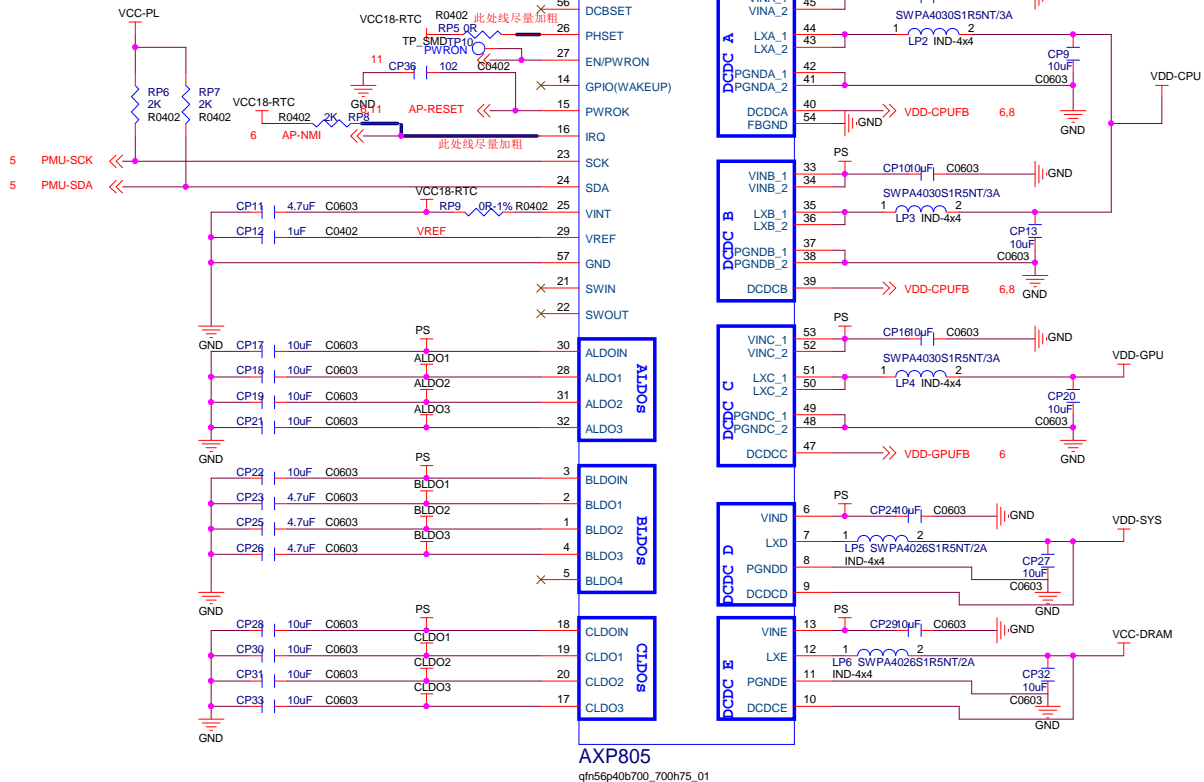
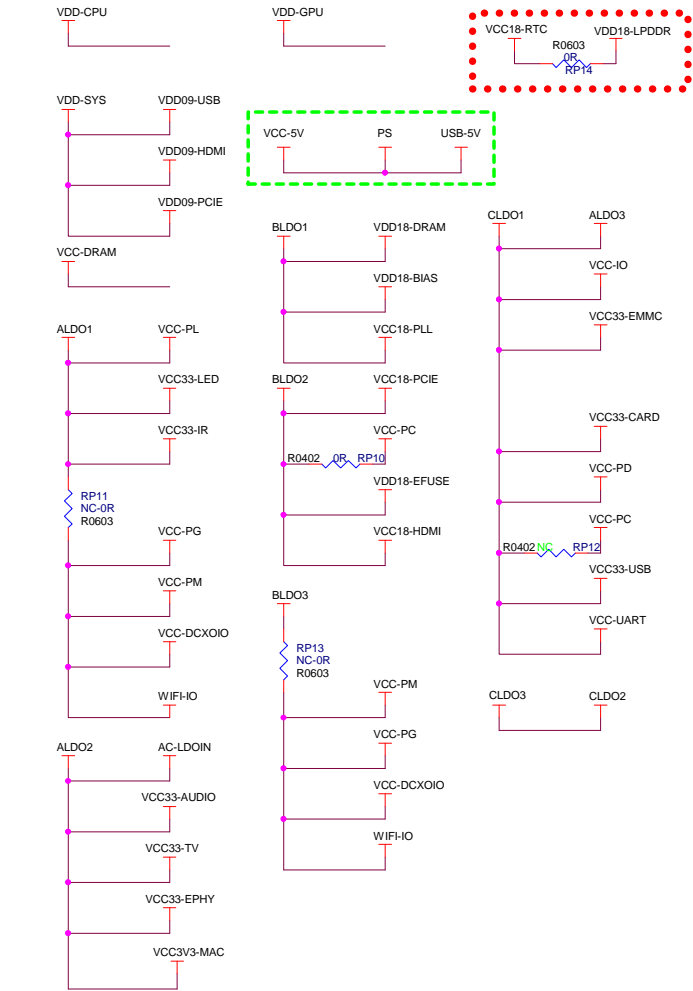
A3	LPDDR3	1.6
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# DCIN



# PMIC

## AXP805

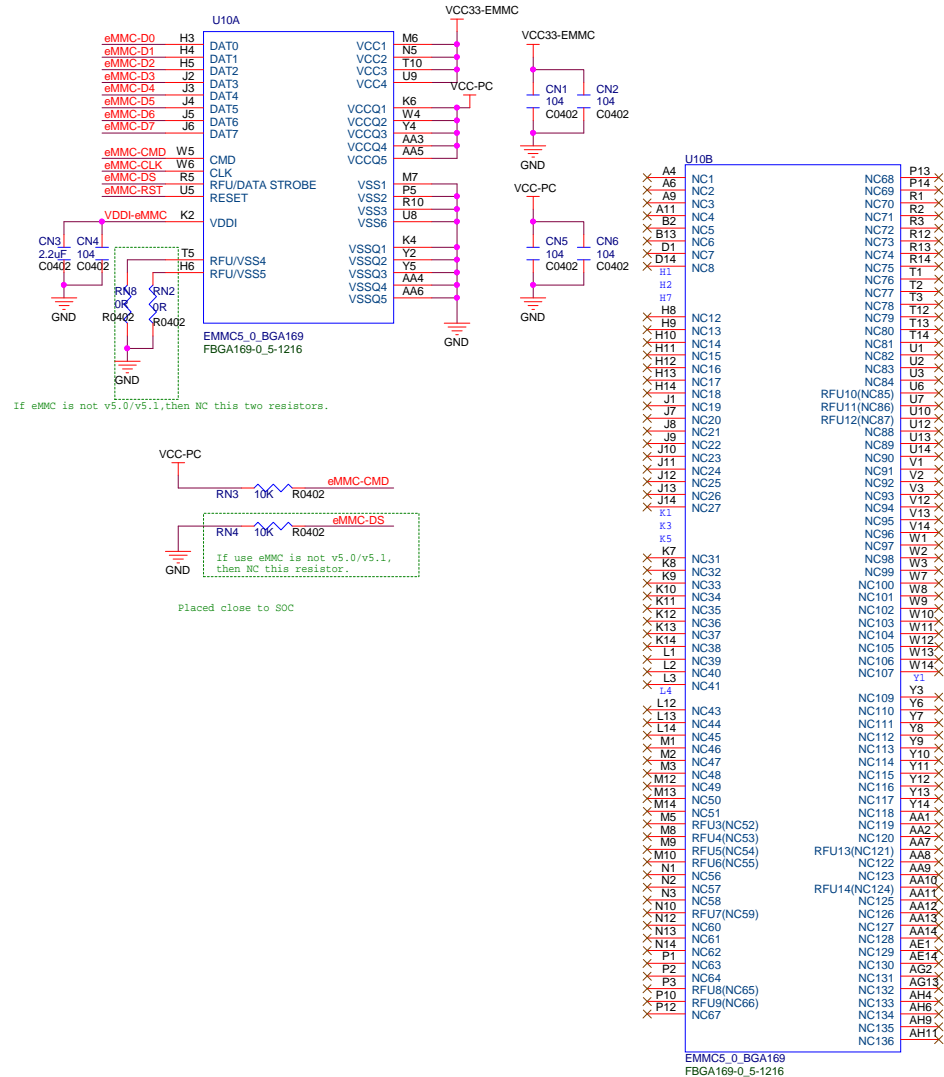


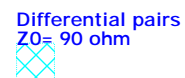
Xunlong Software Co., Limited			
Design Name			
ORANGE_PI-3			
Size	Page Name	Rev	
A3	POWER	1.6	
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# eMMC

eMMC-DS 5  
 eMMC-CLK 5  
 eMMC-CMD 5  
 eMMC-RST 5  
 eMMC-D[7..0] 5

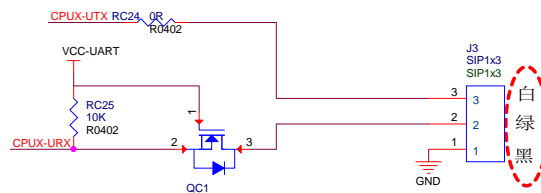




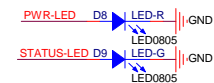
5 CPUX-UTX  
5 CPUX-URX  
5 PWR-LED  
5 STATUS-LED

6 UBOOT  
5 RECOVERY  
8 PWRON

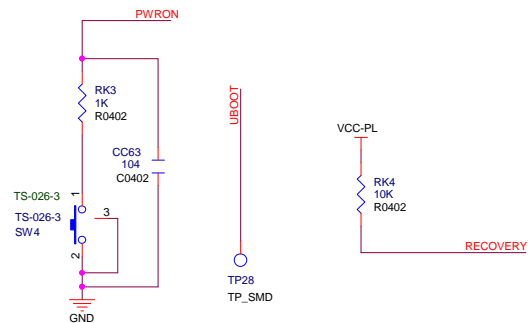
## DEBUG



## LED

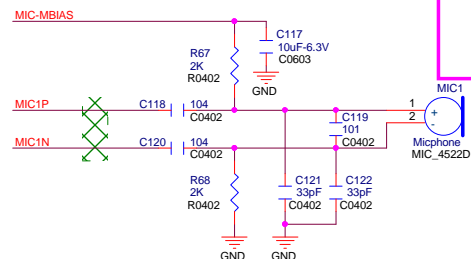


## KEY

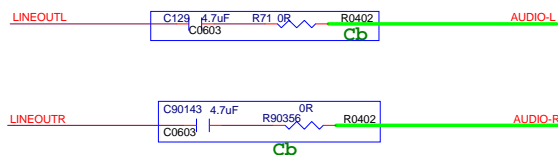


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Design Name			
ORANGE PI-3			
Size	Page Name	Rev	
A3	KEY-LED-DEBUG	1.6	
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## Mic

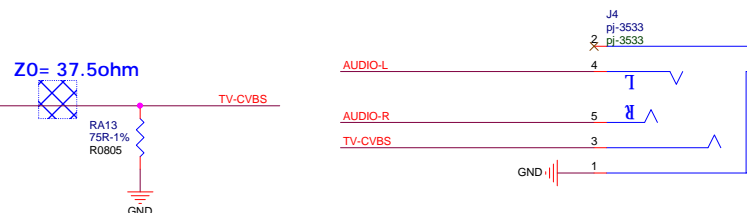


## Audio

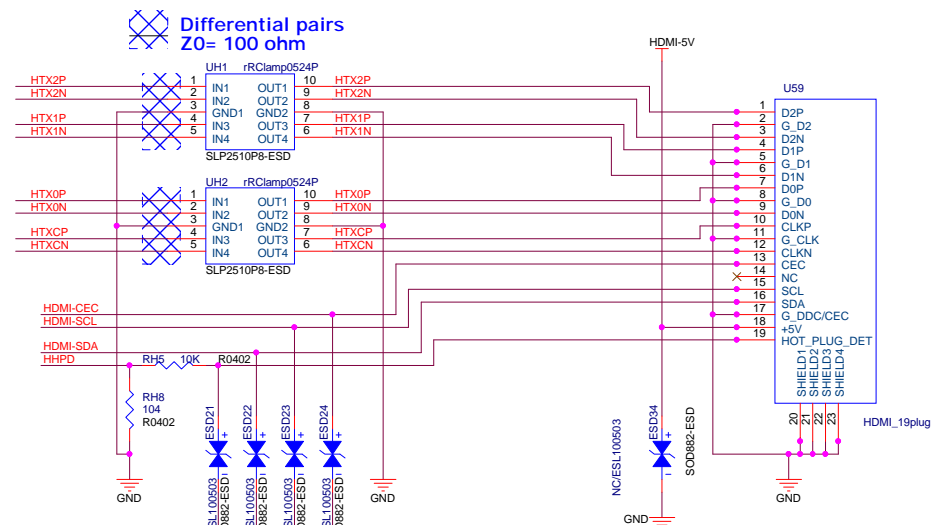
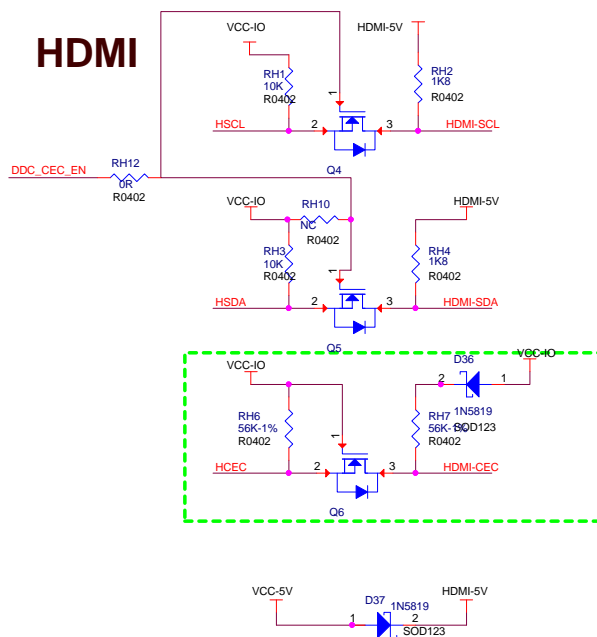
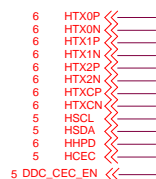


## Video

走线请包地处理



## HDMI

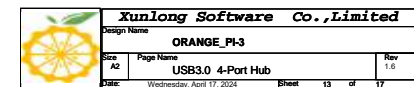


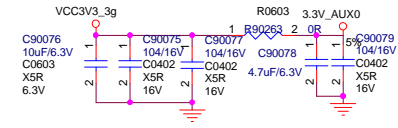
**Xunlong Software Co., Limited**

Design Name	ORANGE PI-3
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Size A3	Page Name AV-HDMI	Rev 1.6
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5

4

3

2

1

D

D

C

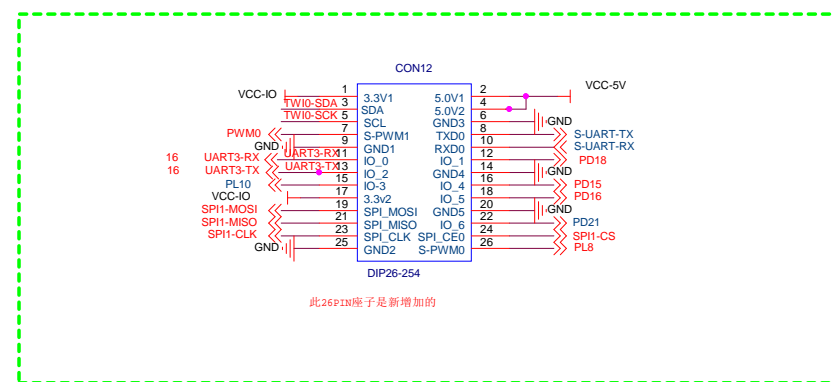
C

B

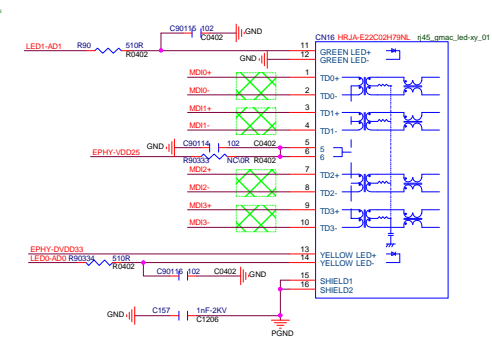
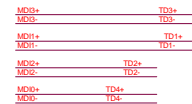
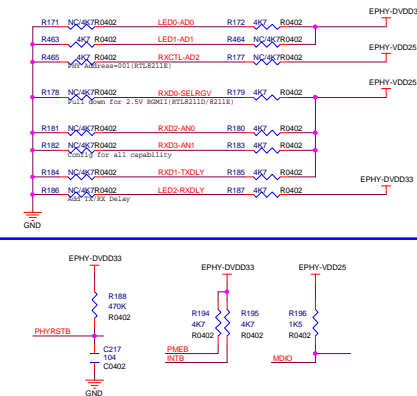
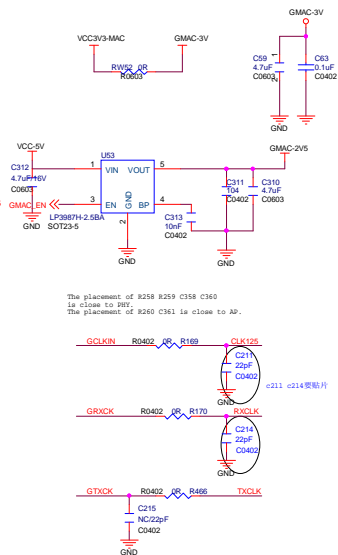
B

A

A



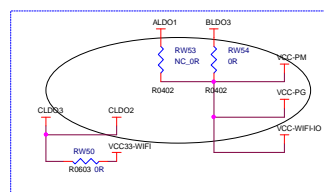
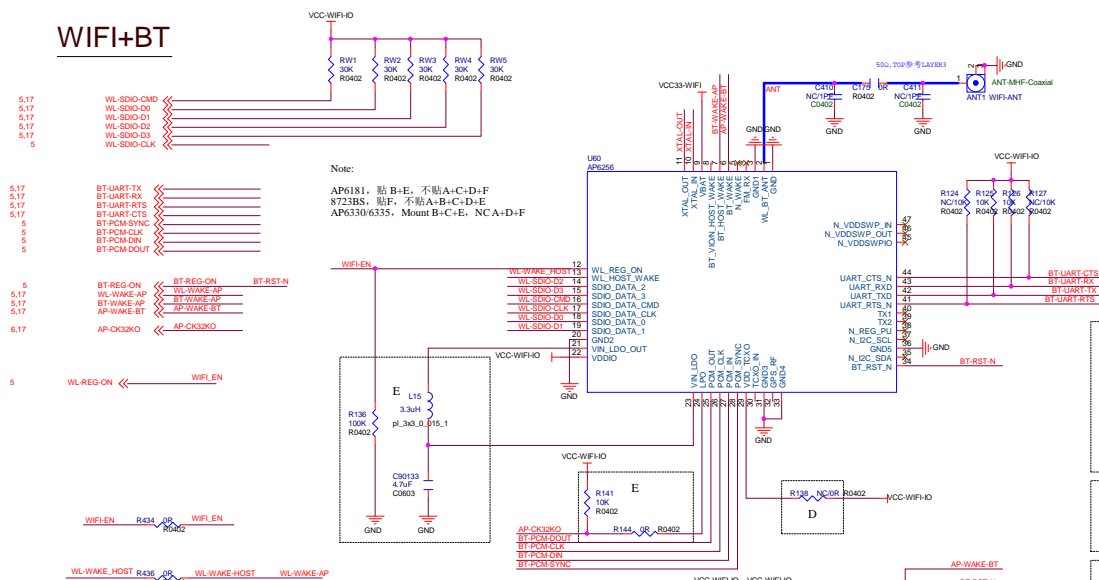
**10/100/1000 MII Ethernet PHY**  
EMAC-MII



LED0:Blinking=Transmitting or Receiving.  
LED1:Link Up/Down



## WIFI+BT



RW51 RW45 RW46 RW50 RW52 RW53

不带蓝牙遥控	IO为1.8V	NC	NC	NC	0R	NC	0R
	IO为3.3V	NC	NC	NC	0R	0R	NC
带蓝牙遥控	IO为1.8V	0R	NC	NC	NC	NC	NC
	IO为3.3V	0R	0R	0R	NC	NC	NC

