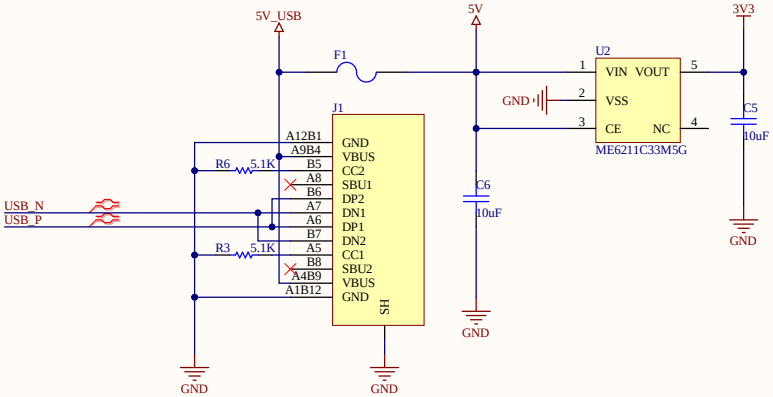
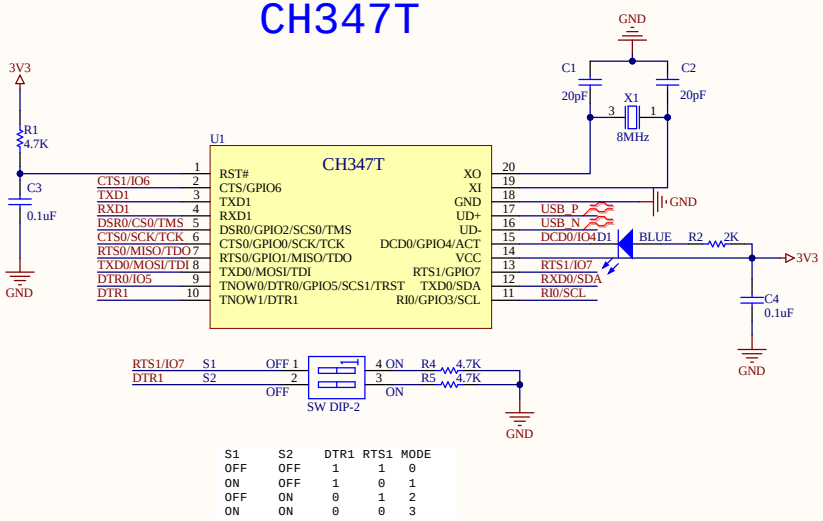
USB-HS-Bridge v1.0

POWER



CH347T



S1	S2	DTR1	RTS1	MODE
OFF	OFF	1	1	0
ON	OFF	1	0	1
OFF	ON	0	1	2
ON	ON	0	0	3

UART0

CTS0/SCK/TCK	U0_CTS
TXD0/MOSI/TDI	U0_TXD
RXD0/SDA	U0_RXD
RTS0/MISO/TDO	U0_RTS
DTR0/IO5	U0_DTR
DSR0/CS0/TMS	U0_DSR
RI0/SCL	U0_RI
DCD0/IO4	U0_DCD

I2C

RI0/SCL	I2C_SCL
RXD0/SDA	I2C_SDA

SPI

DSR0/CS0/TMS	SPI_CS0
DTR0/IO5	SPI_CS1
CTS0/SCK/TCK	SPI_CLK
RTS0/MISO/TDO	SPI_MISO
TXD0/MOSI/TDI	SPI_MOSI

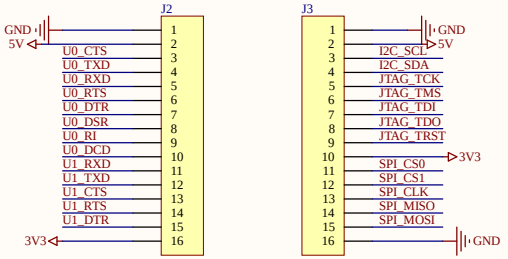
UART1

CTS1/IO6	U1_CTS
TXD1	U1_TXD
RXD1	U1_RXD
RTS1/IO7	U1_RTS
DTR1	U1_DTR

JTAG

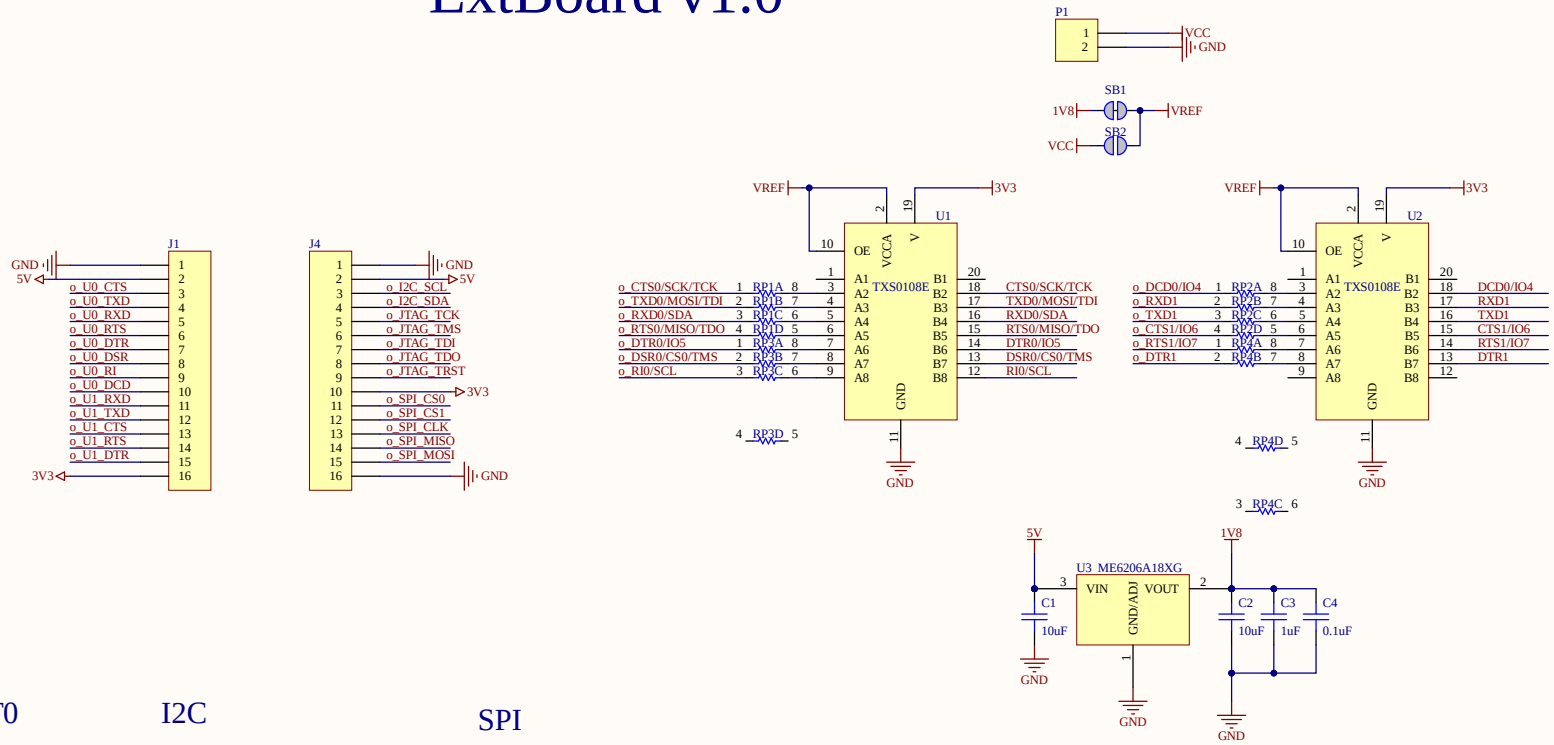
CTS0/SCK/TCK	JTAG_TCK
DSR0/CS0/TMS	JTAG_TMS
TXD0/MOSI/TDI	JTAG_TDI
RTS0/MISO/TDO	JTAG_TDO
DTR0/IO5	JTAG_TRST

HEADER



Title		
Size A3	Number	Revision
Date: 8/29/2022		Sheet of
File: F:\private\..\ch347.SchDoc		Drawn By:

ExtBoard v1.0



UART0

o_CTS0/SCK/TCK	o_U0_CTS
o_TXD0/MOSI/TDI	o_U0_TXD
o_RXD0/SDA	o_U0_RXD
o_RTS0/MISO/TDO	o_U0_RTS
o_DTR0/IO5	o_U0_DTR
o_DSR0/CS0/TMS	o_U0_DSR
o_RI0/SCL	o_U0_RI
o_DCD0/IO4	o_U0_DCD

I2C

o_RI0/SCL	o_I2C_SCL
o_RXD0/SDA	o_I2C_SDA

SPI

o_DSR0/CS0/TMS	o_SPI_CS0
o_DTR0/IO5	o_SPI_CS1
o_CTS0/SCK/TCK	o_SPI_CLK
o_RTS0/MISO/TDO	o_SPI_MISO
o_TXD0/MOSI/TDI	o_SPI_MOSI

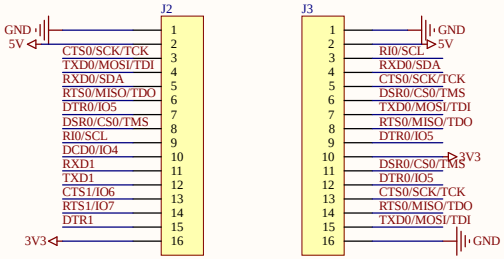
UART1

o_CTS1/IO6	o_U1_CTS
o_TXD1	o_U1_TXD
o_RXD1	o_U1_RXD
o_RTS1/IO7	o_U1_RTS
o_DTR1	o_U1_DTR

JTAG

o_CTS0/SCK/TCK	o_JTAG_TCK
o_DSR0/CS0/TMS	o_JTAG_TMS
o_TXD0/MOSI/TDI	o_JTAG_TDI
o_RTS0/MISO/TDO	o_JTAG_TDO
o_DTR0/IO5	o_JTAG_TRST

HEADER



Title		
Size: A3	Number	Revision
Date: 11/18/2023		Sheet of
File: F:\private\..\ch347-extboard.SchDoc		Drawn By: