Von Neumann-modellen

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INF-0103
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Datamaskiners virkemåte og programmering

Plan for forelesninga

- 5 komponenter i modellen
- Instruksjonssyklusen
- Historisk kontekst
- Dagens situasjon
- Veien videre

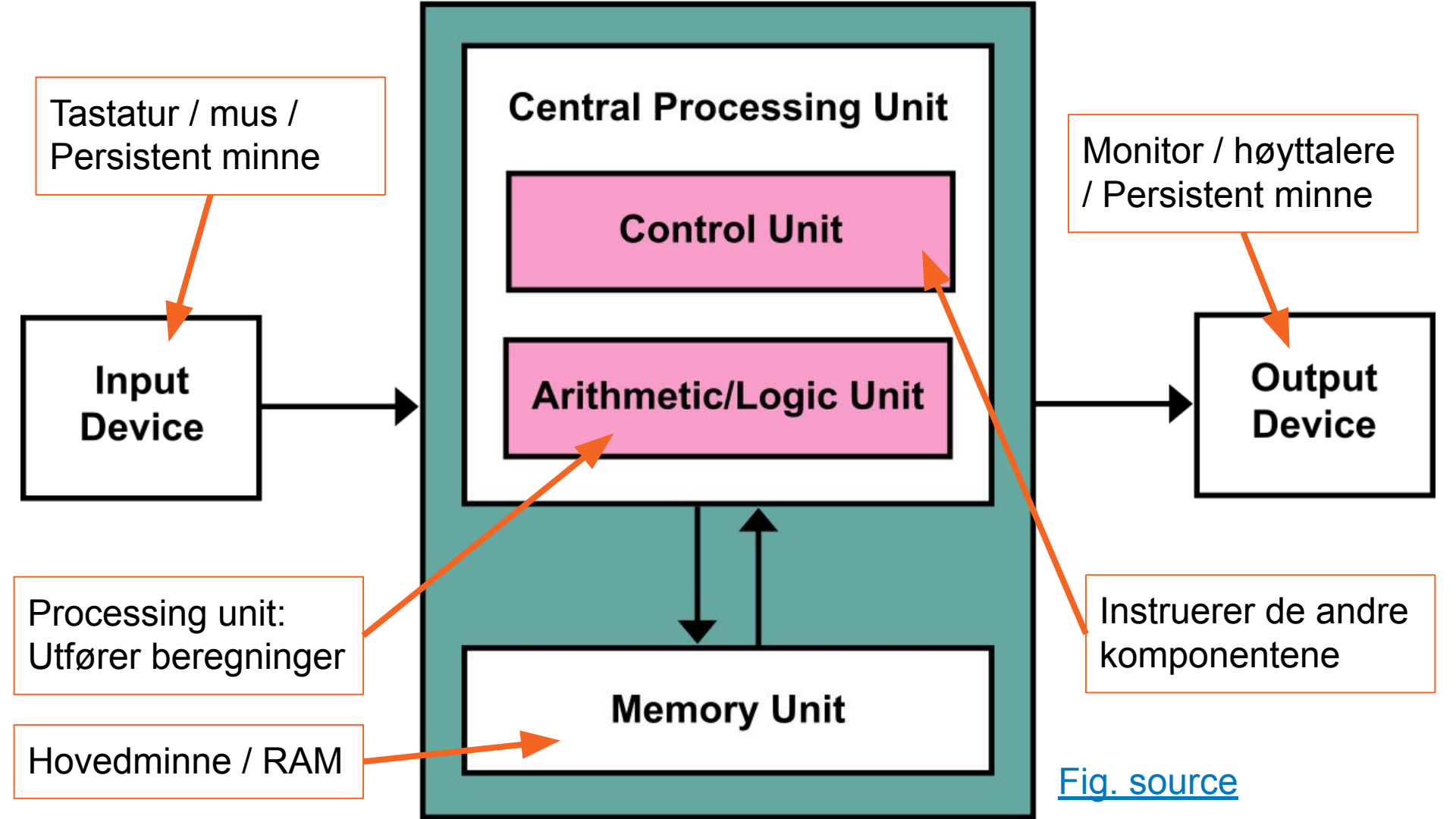
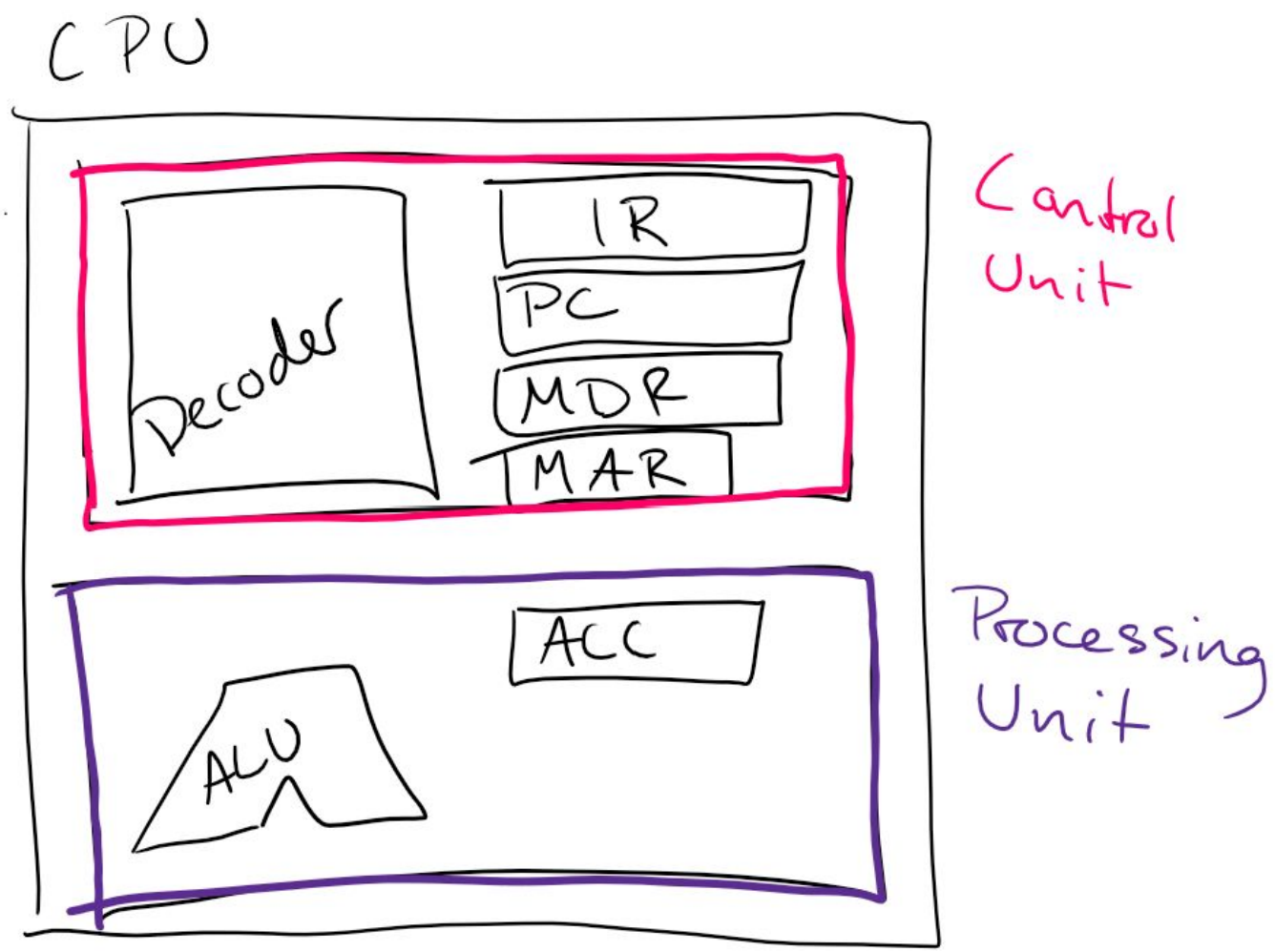
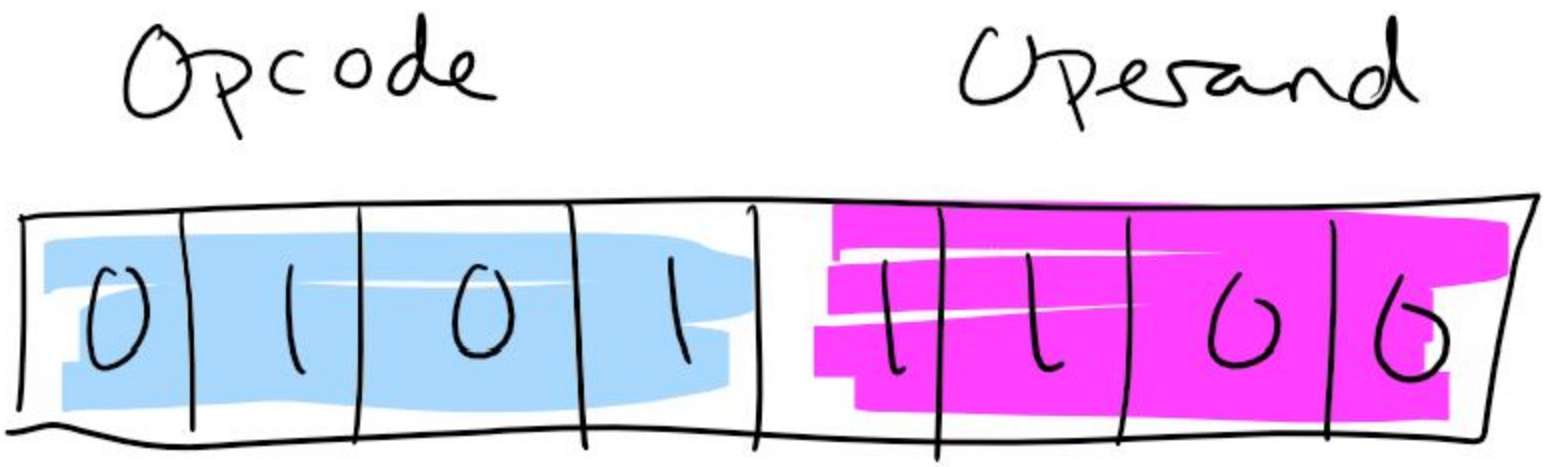
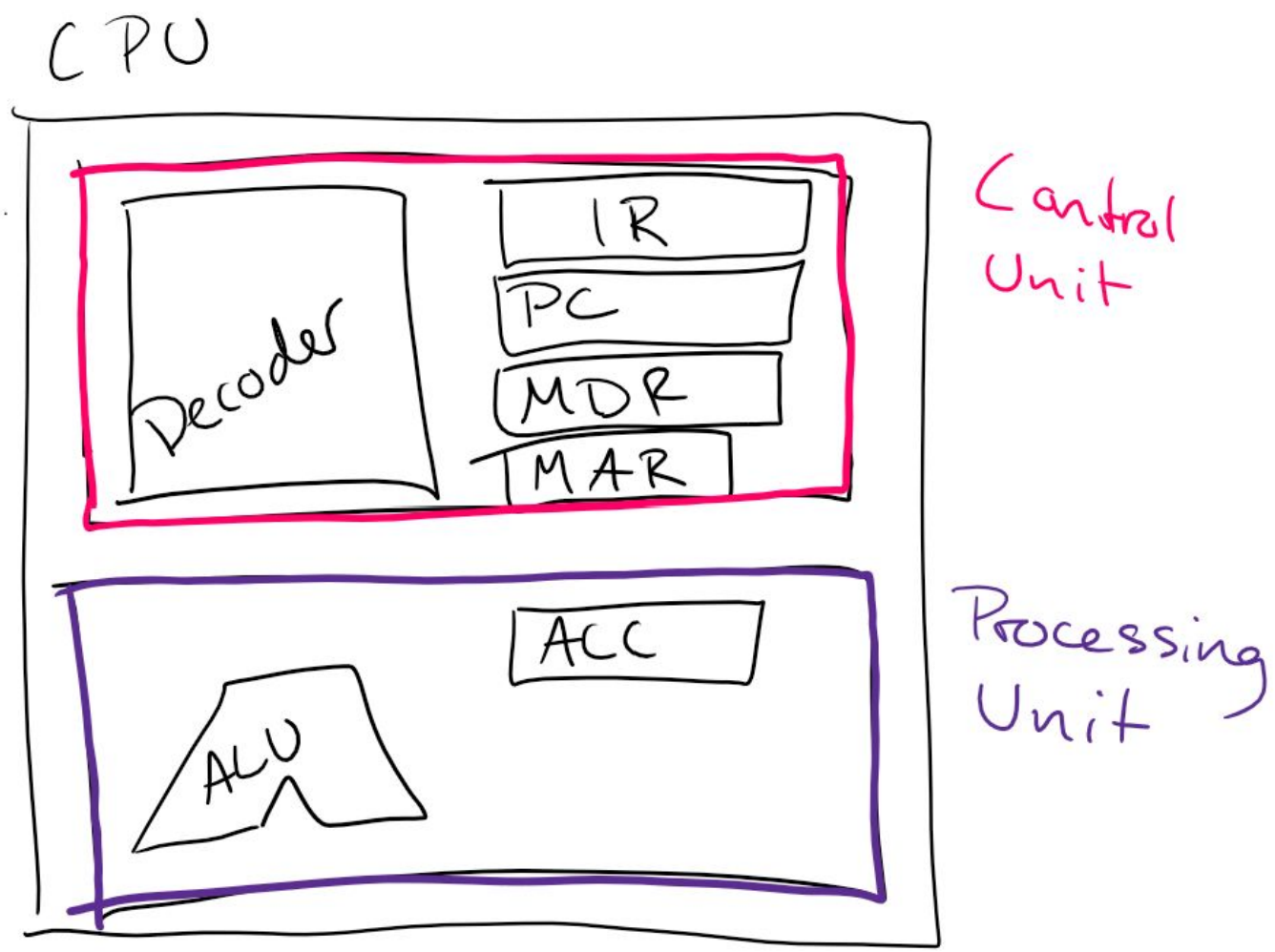

Tastatur / mus /
Persistent minne
Central Processing Unit
Control Unit
Arithmetic/Logic Unit
Monitor / høyttalere
/ Persistent minne
Input
Device
Output
Device
Processing unit:
Utfører beregninger
Instruerer de andre
komponentene
Memory Unit
Hovedminne / RAM

Fig. source


CPU
Decoder
IR
PC
MDR
MAR
Control Unit
ACC
ALU
Processing Unit


Opcode
Operand
0 1 0 1 1 1 0 0
LOAD
Addr.


CPU
Decoder
IR
PC
MDR
MAR
Control Unit
ACC
ALU
Processing Unit

5 hovedkomponenter

- Minne
- Kontrollenhet
- Prosesseringsenhet (ALU)
- Input-enheter
- Output-enheter

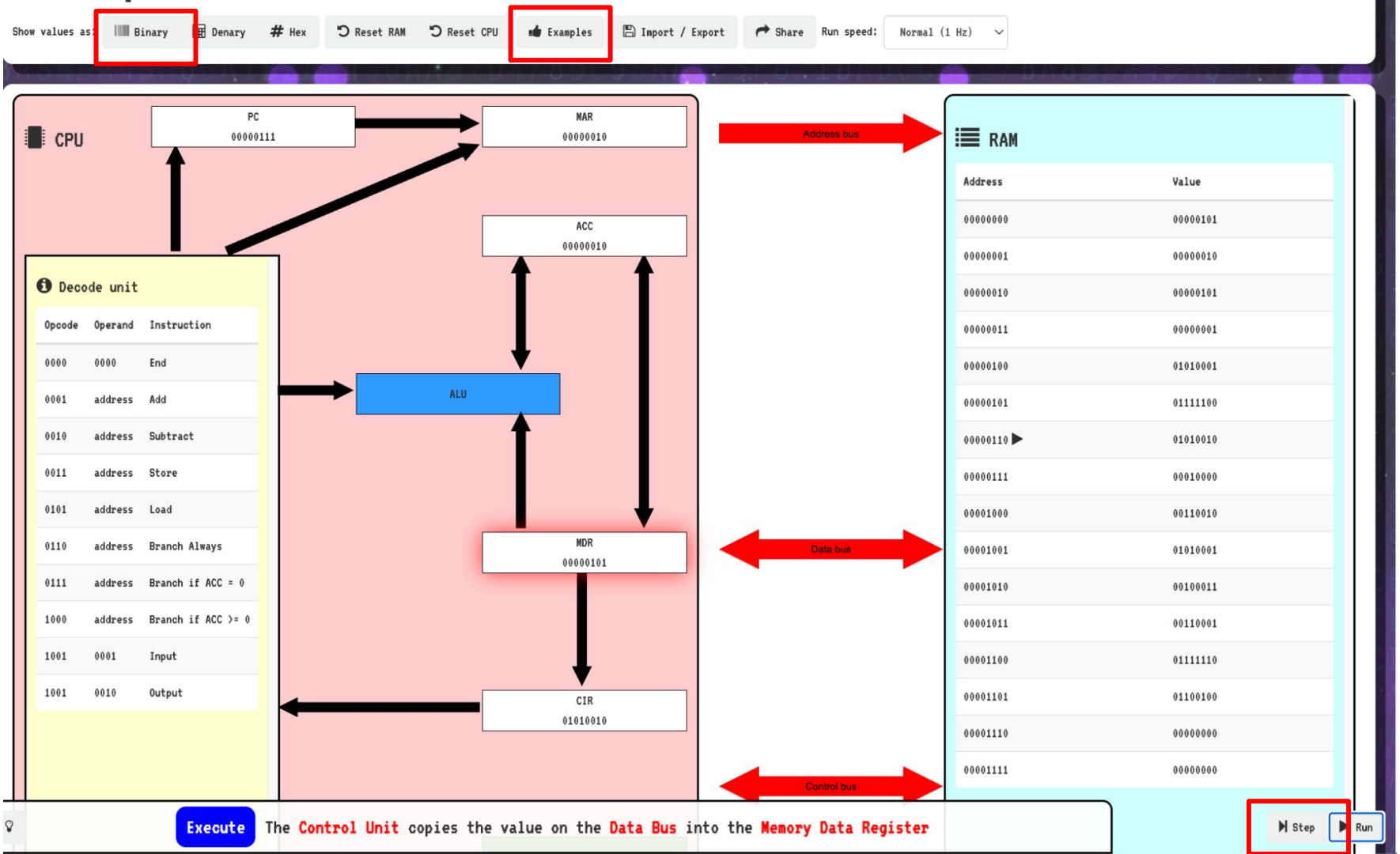
Instruksjonssyklusen

Simulering

Fetch - Decode - Execute

Vi bruker simulatoren

1. Gå til https://tools.withcode.uk/cpu/
2. Velg eksempelet hvor to tall legges sammen
3. Velg binærrepresentasjon
4. Gå gjennom programmet med Fetch-Decode-Execute steg for steg (Step-knappen)
5. Prøv å modifisere programmet til å lese fra minnet i stedet for input


Show values as:
Binary
Denary
Hex
Reset RAM
Reset CPU
Examples
Import / Export
Share
Run speed:
Normal (1 Hz)
CPU
PC
00000111
MAR
00000010
ACC
00000010
Decode unit
Opcode Operand Instruction
0000 0000 End
0001 address Add
0010 address Subtract
0011 address Store
0101 address Load
0110 address Branch Always
0111 address Branch if ACC = 0
1000 address Branch if ACC >= 0
1001 0001 Input
1001 0010 Output
ALU
MDR
00000101
CIR
01010010
Address bus
Data bus
Control bus
RAM
Address Value
00000000 00000101
00000001 00000010
00000010 00000101
00000011 00000001
00000100 01010001
00000101 01111100
00000110 01010010
00000111 00010000
00001000 00110010
00001001 01010001
00001010 00100011
00001011 00110001
00001100 01111110
00001101 01100100
00001110 00000000
00001111 00000000
Execute
The Control Unit copies the value on the Data Bus into the Memory Data Register
Step
Run

Spørsmål?

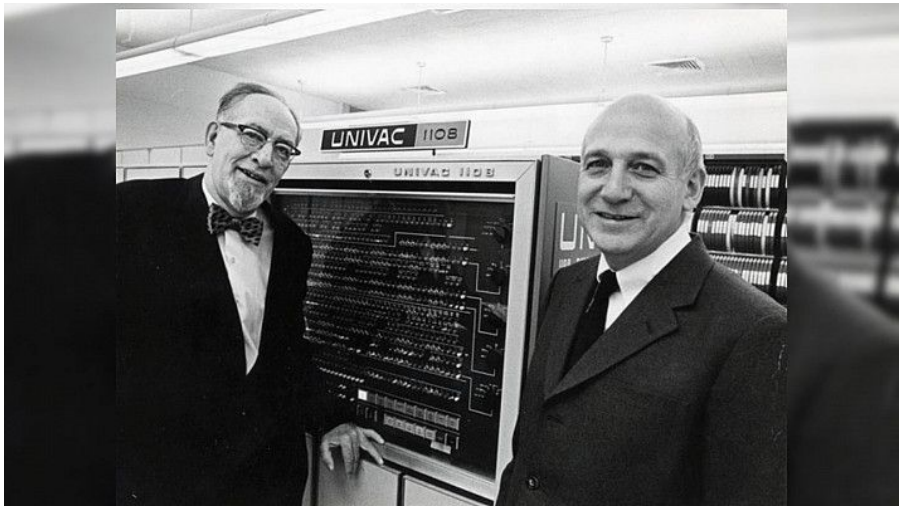
- De fem komponentene i modellen
- Instruksjonssyklusen

Historisk tilbakeblikk

- Stored program
- Felles minne
- Binær
- Elektronisk
- General purpose

Mauchly

Eckert



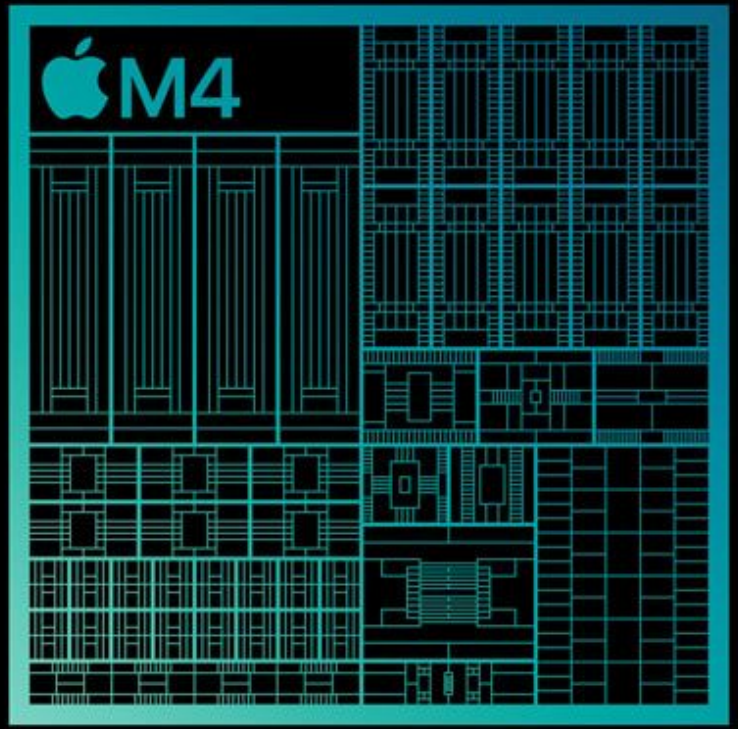
Img. source

Img. source

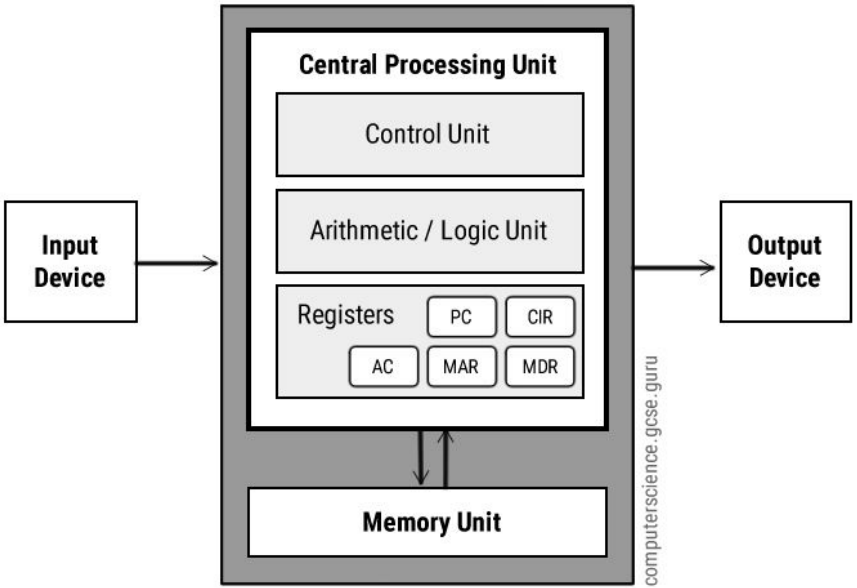
10-core CPU

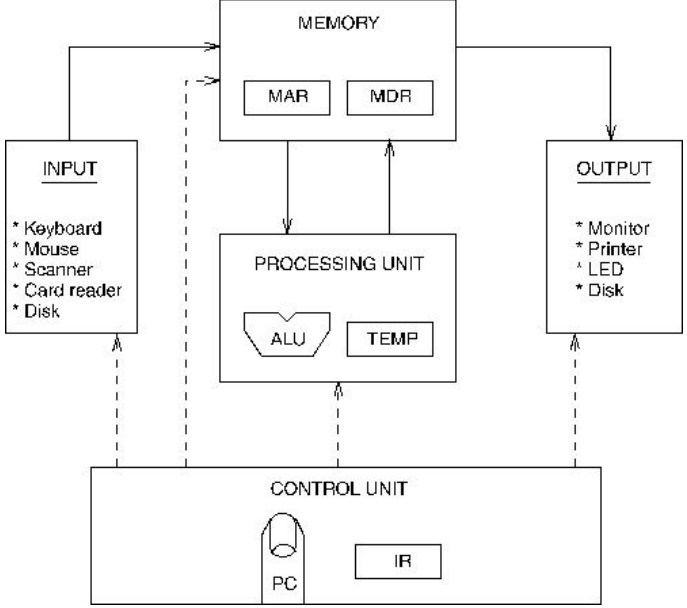
4 performance cores
Improved branch prediction
10-wide instruction decode
40% larger reorder buffer
Next-generation ML accelerators

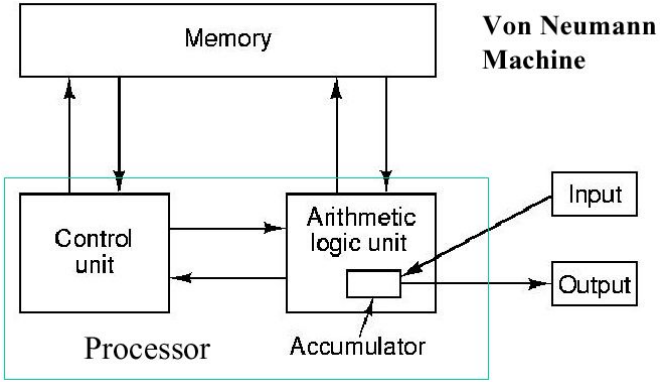
6 efficiency cores
Improved branch prediction
Double front-end fetch width
Wider and lower-latency vector FP
Next-generation ML accelerators

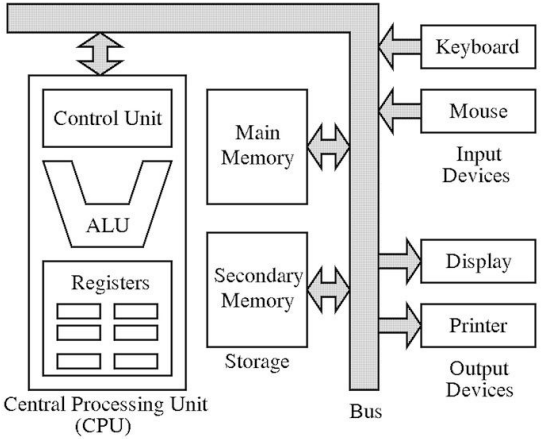


- Flere kjerner
- Cache-lag
- Mod. Harvard
- GPU
- Klokkesykluser
- Pipelining
- Ulike ALUer
- …


Central Processing Unit
Control Unit
Arithmetic / Logic Unit
Registers
PC
CIR
AC
MAR
MDR
Input Device
Output Device
Memory Unit
computerscience.gcse.guru


MEMORY
MAR
MDR
INPUT
* Keyboard
* Mouse
* Scanner
* Card reader
* Disk
PROCESSING UNIT
ALU
TEMP
OUTPUT
* Monitor
* Printer
* LED
* Disk
CONTROL UNIT
PC
IR


Memory
Von Neumann Machine
Control unit
Arithmetic logic unit
Input
Output
Processor
Accumulator


Control Unit
ALU
Registers
Central Processing Unit (CPU)
Main Memory
Secondary Memory
Storage
Keyboard
Mouse
Input Devices
Display
Printer
Output Devices
Bus

Viktige begreper

MDR	ALU
MAR	CPU
IR / CIR	Opcode
ACC / TEMP	Operand
PC	

Videre arbeid

- Gamle eksamensoppgaver fra INF-1100
- Oppgaver fra boka kap. 4
- Teste simulatoren:
  - https://tools.withcode.uk/cpu/?ram=00000000000000000000000000000000
  - Bonus: Preloadet med et annet program:
    - https://tools.withcode.uk/cpu/?ram=05030001517c5210325123317e645200 (NB! Programtelleren må initialiseres med verdien 00000100)
- Om Harvard vs. von Neumann-arkitektur:
  - https://www.youtube.com/watch?v=4nY7mNHLrLk
- Historie fra computerphile om von Neumann:
  - https://www.youtube.com/watch?v=Ml3-kVYLNr8
- The Fetch-Execute Cycle:
  - https://www.youtube.com/watch?v=Z5JC9Ve1sfI

- INF-2200 Computer Architecture