Meeting 6 SP23

Intro to Pipelining

@crawfish

Outline

Section 1

Motivation

Goals of Processor Design

- Low latency
- High throughput
- Small size
- Low energy requirements
- etc.

Latency vs. Throughput

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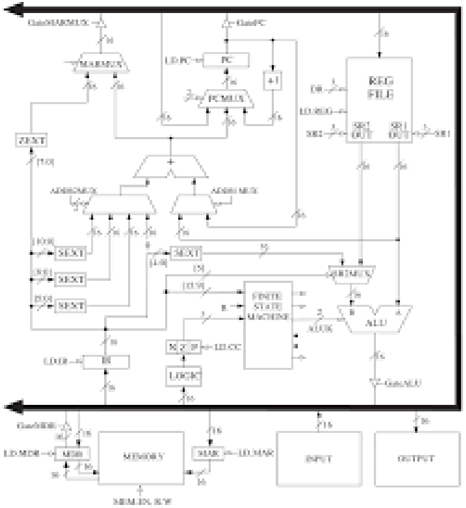
- **Throughput** refers to the average number of tasks we can complete per unit time
  - Most relevant for program run-time
- Pipelined processor designs optimize for throughput
  - Extra logic required actually causes a slight *increase* in latency

Single Cycle Processors

A **single cycle processor** is one in which an individual instruction takes one clock cycle to execute*.

LC3 Single-Cycle Datapath



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- Clock cycles are long

Section 2

Pipelining

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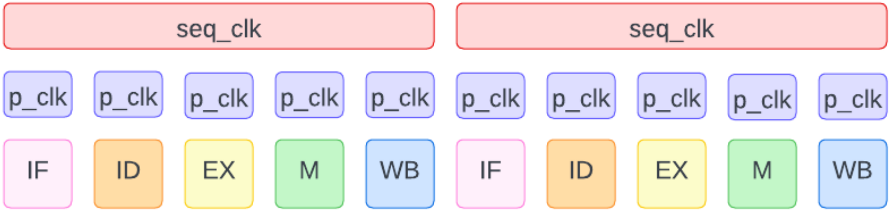
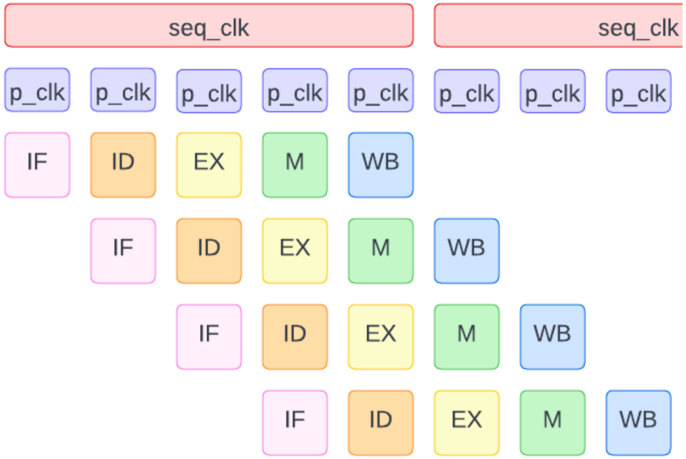
- Instruction dispatch is staggered such that each unit is always working on exactly 1 instruction

Sequential Execution



Pipelining


seq_clk
seq_clk
p_clk
p_clk
p_clk
p_clk
p_clk
p_clk
p_clk
p_clk
IF
ID
EX
M
WB
IF
ID
EX
M
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IF
ID
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IF
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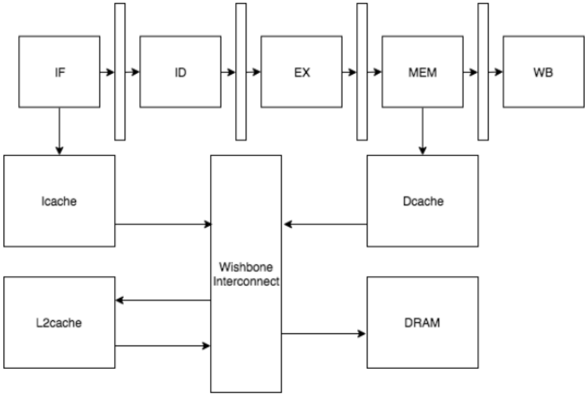
LC3 Pipelined Architecture



Instruction Fetch

```
module InstructionFetch(
    input clk,
    input [15:0] pc,
    input stall,
    output [15:0] instr_out,

    // One way read-only memory itf
    mem_itf.read_only_o mem_itf
);
```

Instruction Decode

```
module InstructionDecode(
    input [15:0] instr,

    // From instr 'microcode', produce ctrl signals
    control_signals_itf.control_signals cs_itf
);
```

Execution

```
module ExecutionUnit(
    // reg_a, reg_b are read from register file
    input logic [15:0] reg_a,
    input logic [15:0] reg_b,
    input logic[1:0] opcode,

    // c is forwarded for later writeback
    output logic [15:0] c
);
```

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- How do we deal w/ long memory operations in our pipeline?
  - Stall :(

Write Back

- Instruction results are 'committed' to register file
- Input comes from either execution stage or register file depending on control signals

What are some problems with this design?

```
; R4 = 0x1, R5 = 0x2
ADD R4, R5, R0
ADD R4, R4, R4
NOP
NOP
NOP ; R4 = 0x6?
```

Hazards

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- How do we fix this?
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  - Instruction forwarding
- Other hazard types exist in more complicated pipeline structures

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- Branch / Jump instructions modify the program counter in an unexpected* way
- These changes take effect during the ’write-back’ phase
  - Implemented as an addition or replacement of the program counter register
- What about instructions that populate the pipeline in the meantime?
  - Not useful instructions
  - If they modify state (registers, memory) they will cause incorrect future results upon completion

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- Stall the pipeline (Wait)
- Branch prediction (Guess)
  - If we guessed wrong, don't commit anything
  - Lots of research has been done to optimize branch prediction
  - Code is very repetitive
  - If we guess, we can be right fairly often

Golden Rule of CPU Design: Hide Latency to Increase Throughput

The end. (Now go do some 233 practice problems)