NC State University

Department of Electrical and Computer Engineering

ECE 463/521: Fall 2015 (Rotenberg)

Project #1: Cache Design, Memory Hierarchy Design

By

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NCSU Honor Pledge: "I have neither given nor received unauthorized aid on this test or assignment."

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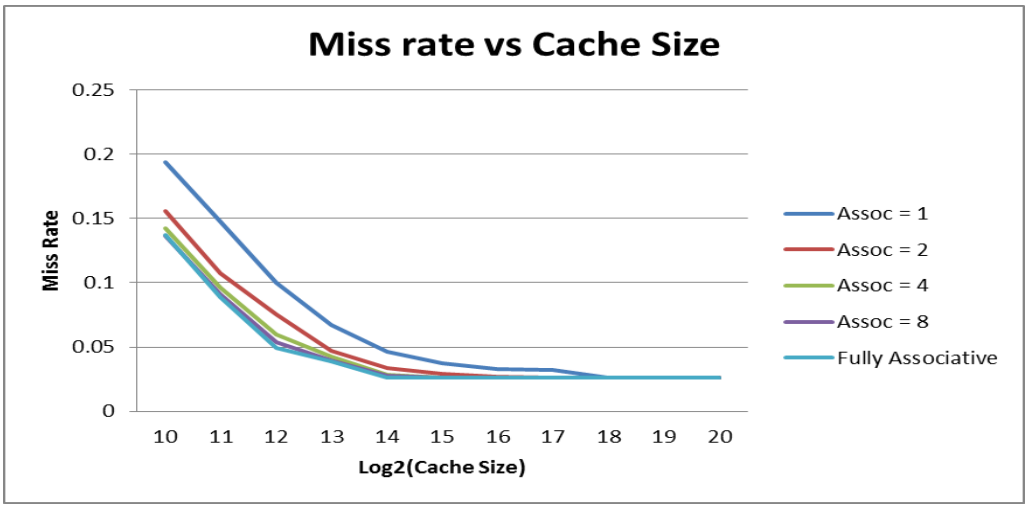
Course number: 521

9.1. L1 Cache exploration: SIZE and ASSOC

Graph #1:



Discussions

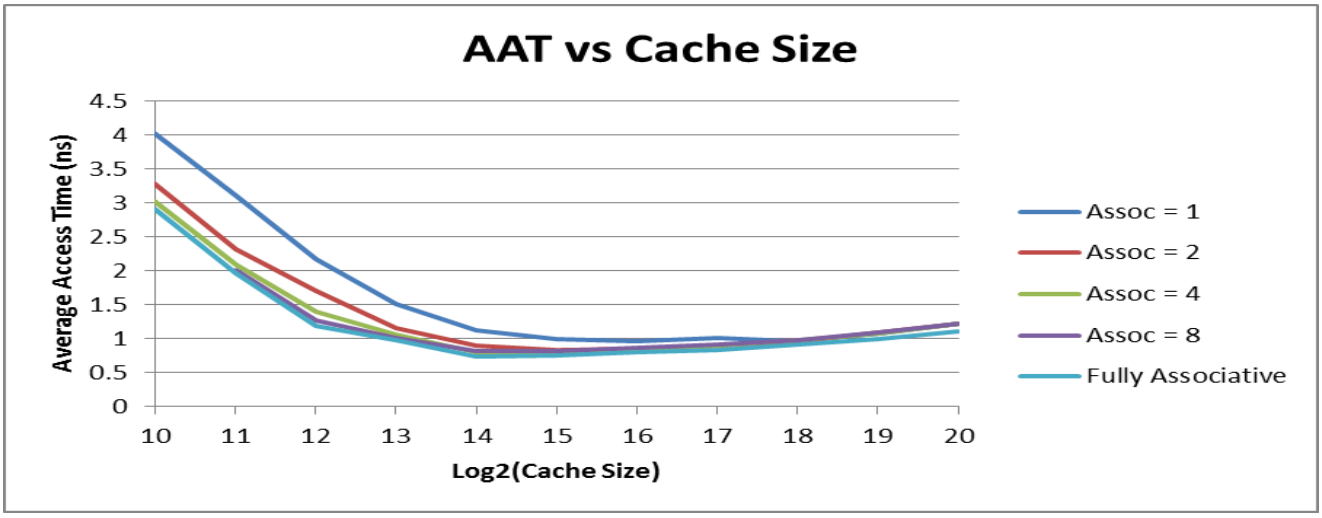
1) As we can see from the graph, for a particular associativity, increasing the cache size reduces the miss rate exponentially. This is because, as the cache size increases, more blocks can be acoomodated in more sets, resulting in lesser misses.
   Also, for a given cache size, increasing the associativity generally reduces the miss rate. However, with for large caches, increasing the associativity does not have much effect on the miss rate.

2) Estimated Compulsory Miss Rate: 0.0258
   We can estimate the *compulsory miss rate* by looking at 1Mb cache at full associativity. The only kind of misses this cache will have are compulsory ones.

3) Estimated Conflict Miss Rate:
   a. Associativity = 1 : 0.0565
   b. Associativity = 2 : 0.019
   c. Associativity = 4 : $5.7 * 10^{-3}$
   d. Associativity = 8 : Negligible (~0.000003)

   We can estimate the *conflict miss rate* by subtracting from the miss rate for a certain assoc, the miss rate of the fully associative cache for the same cache size.

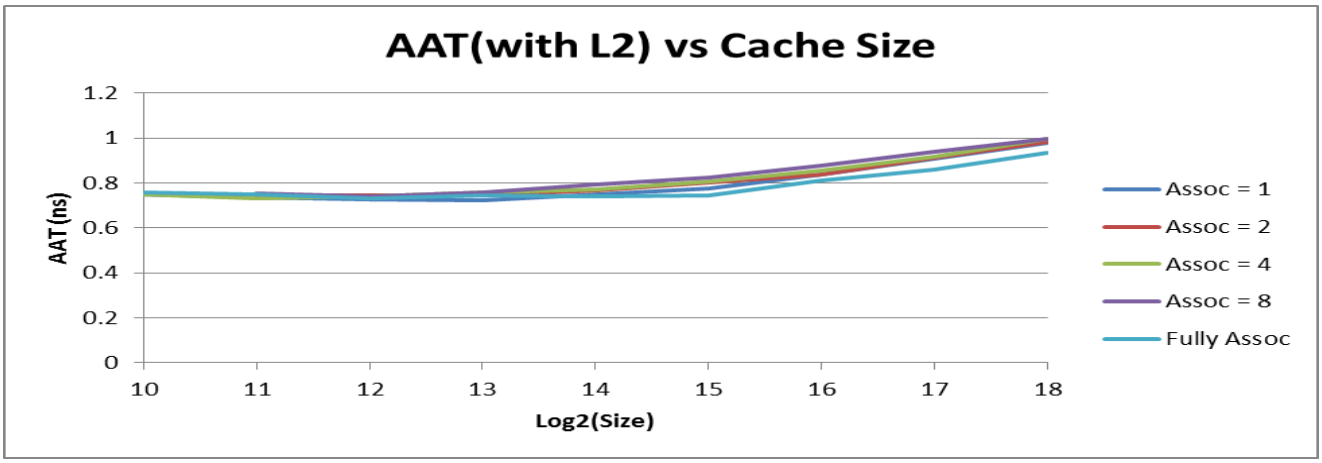
Graph #2:



Discussions

As we can see from the graph, for an L1 cache with a blocksize of 32 bytes, the lowest AAT is yielded by a 16Kb, fully associative cache.

Graph #3:

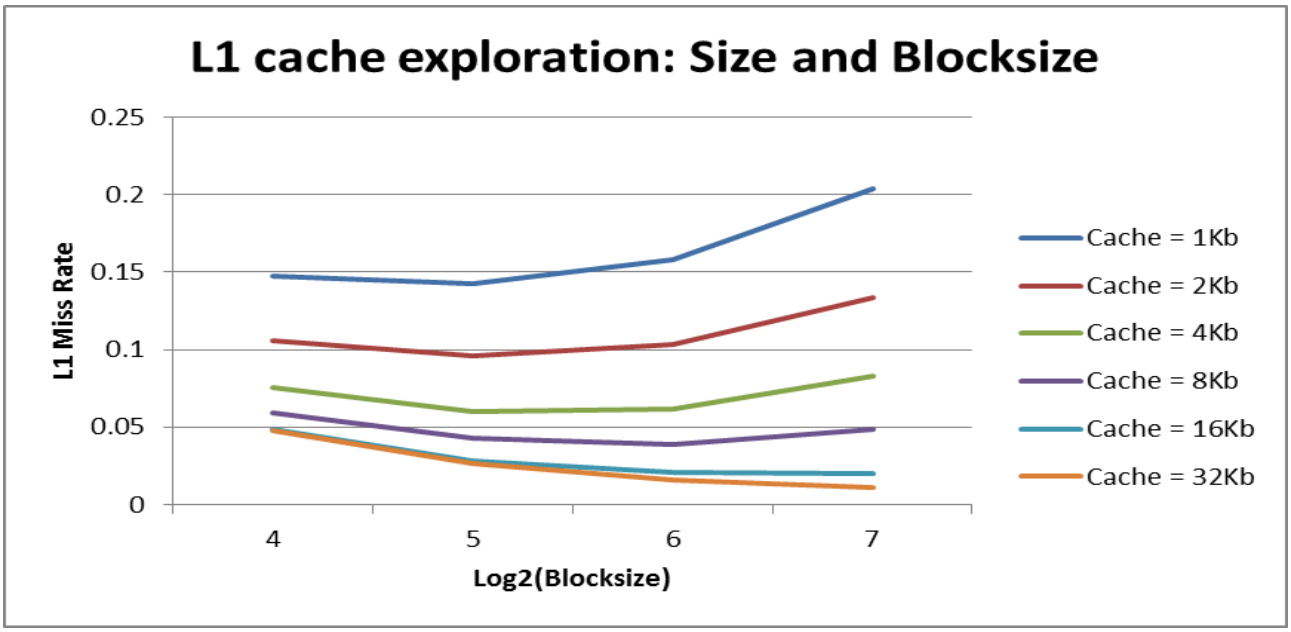


Discussions

1) As we can see from the above graph, although most of the L1 cache configurations are result in AATs close to the best AAT in the previous graph, the direct mapped L1 cache with a size of 8 Kb comes closest.
2) With an L2 cache added, the best AAT is yielded by a direct-mapped L1 cache of size 8 Kb. This optimal AAT is 0.012 nanoseconds less than the optimal AAT in the previous graph.
3) Total area required for the optimal AAT in Graph 3 = 0.0532 + 2.64 = 2.6932 mm^2.
   Total area required for the optimal AAT in Graph 2 = 0.0634 mm^2.

9.2. L1 cache exploration: SIZE and BLOCKSIZE

Graph #4:

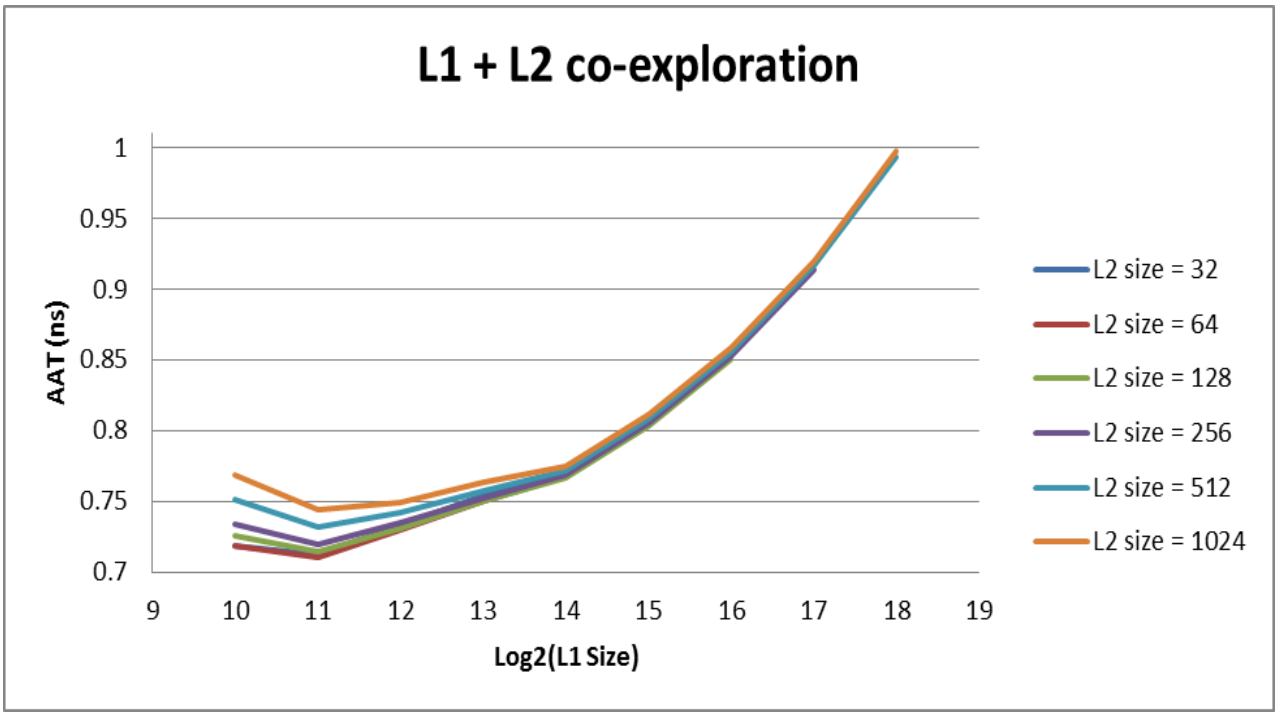


Discussions

1) As we can see from the above graph, smaller caches prefer smaller blocksizes as the miss rates for caches with size <= 8Kb increase with an increase in the blocksize.
   However, bigger caches (size > 8Kb) prefer bigger blocksizes as the miss rates for these caches decrease with an increase in the blocksize.
   This is due to the fact that the blocksize has a direct effect on the number of blocks that a cache can accommodate. For small caches, if the blocksize is too large, the number of blocks that can be stored becomes very limited, leading to a lot of misses. For bigger caches, to compensate for the large size of the cache, blocksizes should be larger as this would reduce the time required to search the cache for a small block.
2) Yes, the trade-off between exploiting more spatial locality vs an increasing cache pollution is quite evident from the graph. The balance between the two factors does shift with different cache sizes since for smaller caches, exploiting spatial locailtiy is limited due to the size of the caches.

9.3. L1 + L2 co-exploration

Graph #5:

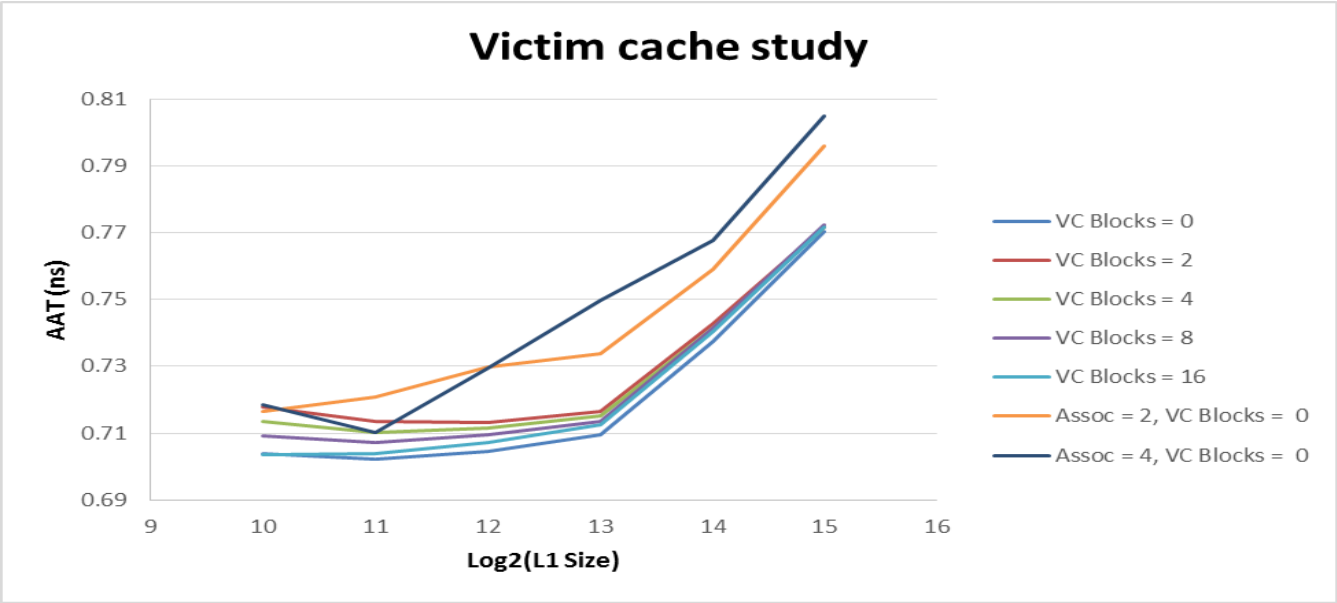


Discussions

1) As we can see from the above graph, the best AAT is yielded when we have an L2 cache of 64Kb and an L1 cache of 2048Kb.
2) The memory hierarchy configuration of a 32Kb L2 cache with a 1Kb L1 cache has the smallest Total Area (0.2572 mm^2) out of the ones which yield an AAT within 5% of the best AAT.

9.4. Victim cache study

Graph #6:



Discussions

1) On adding a victim cache to a direct-mapped L1 cache, we almost always get better results as compared to making the L1 cache two -way set-associative. The exception to this is for an L1 cache of 2048Kb, increasing the associativity to 4 yields a better AAT than adding a VC of 2 blocks to a direct mapped cache of the same size.
2) The memory hierarchy configuration of a 64Kb L2 cache with a 2Kb, direct-mapped L1 cache with 0 VC blocks yields the best AAT.
3) The above memory hierarchy configuration has the smallest total area (0.38 mm^2).