NC State University

Department of Electrical and Computer Engineering

ECE 463/521: Fall 2015 (Rotenberg)

Project #3: Dynamic Instruction Scheduling

by

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NCSU Honor Pledge: "I have neither given nor received unauthorized aid on this test or assignment."

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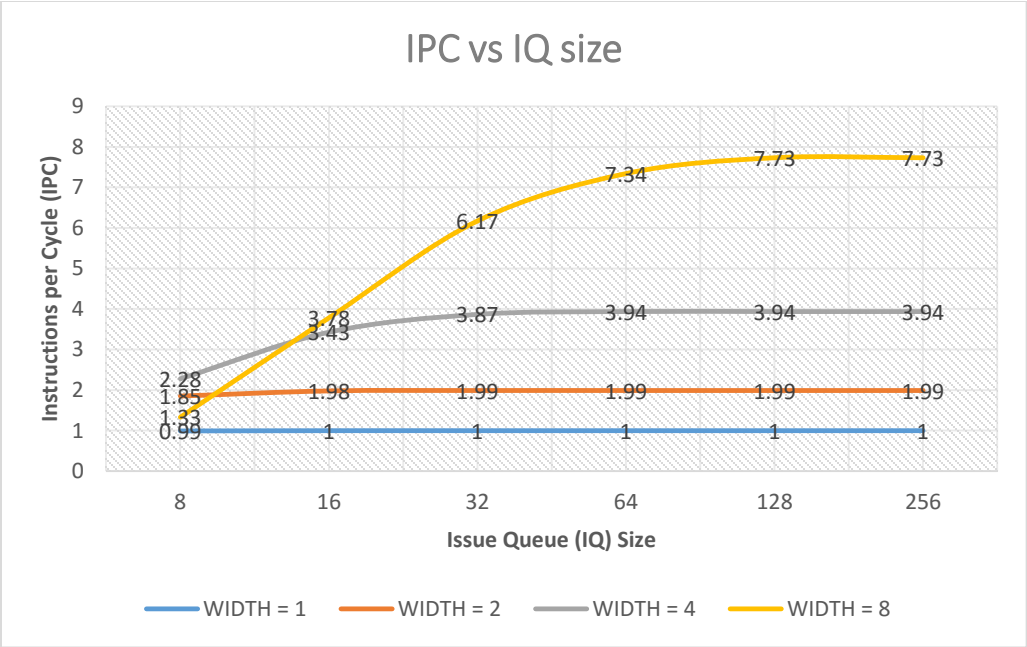
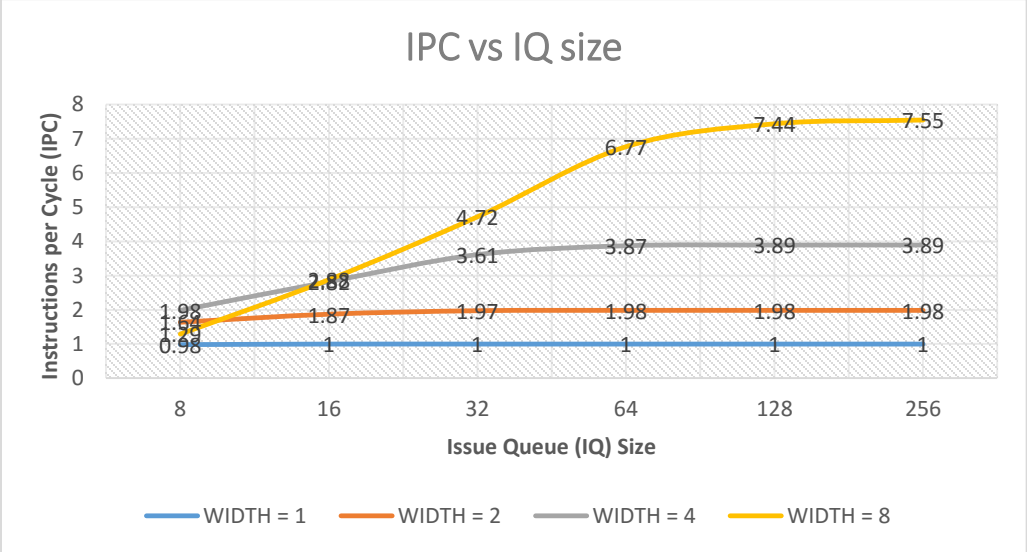
Course number: ECE 521

Large ROB, effect of IQ_SIZE

1) Graphs:
   a. Benchmark: **gcc1**



   b. Benchmark: **perl1**



2) Graph Analysis:

Optimized IQ_Size per WIDTH		
	Benchmark = gcc1	Benchmark = perl1
WIDTH = 1	8	8
WIDTH = 2	16	32
WIDTH = 4	32	64
WIDTH = 8	128	128

3) Discussion:

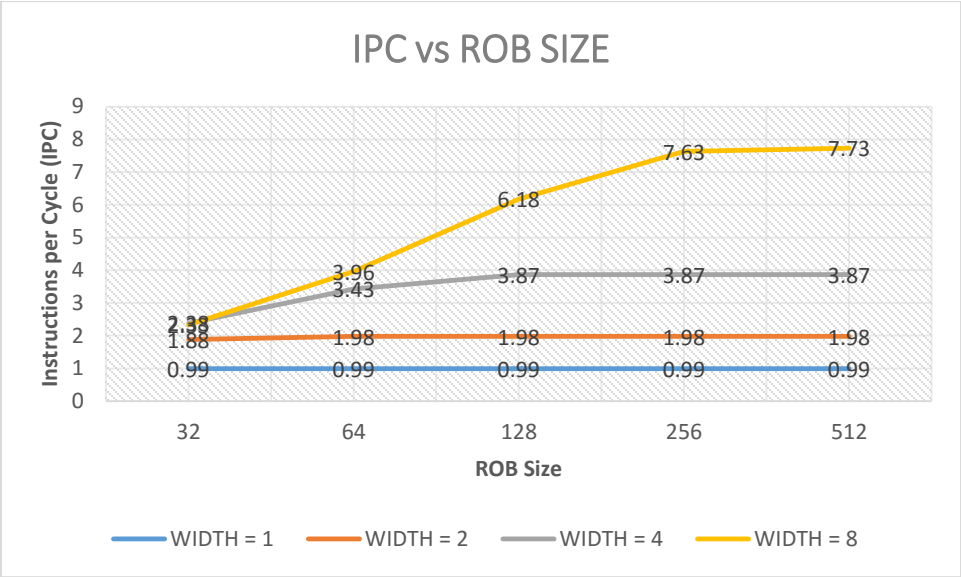
- Given that the goal of a superscalar processor is to achieve an IPC that is close to WIDTH and given the results from the graphs above, we can infer that as the Issue Queue size increases, for higher values of WIDTH, we get increasingly better IPC. This means that if the IQ Size doesn't commensurately increase with WIDTH, the IPC count doesn't justify the increase in the hardware complexity to build a superscalar processor.

- For the Benchmarks provided for this project, we find that *gcc1* shows higher values of IPC that *perl1* for the same microarchitecture configuration. One reason for this might be that the *perl1* benchmark contains more long latency instructions which are close together in program order. This would lead to a longer wait in the Issue Queue for the dependent instructions, thus increasing the latency and decreasing the IPC. Another reason might be that the *perl1* benchmark has more dependent instructions than the *gcc1* benchmark, which leads to a more packed issue queue.

Effect of ROB SIZE

Graphs (With optimized IQ Size):

a. Benchmark: gcc1



b. Benchmark: perl1