



VIT[®]

Vellore Institute of Technology

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Subject: FPGA-Based System Design Lab

Subject Code: BECE406E

Assignment-1

Carry Look Ahead Adder

1. Dataflow Modeling

```
`timescale 1ns/1ps

module cla_four_bit(input [3:0] A,B, input Cin, output [3:0] S, output Cout);

wire [3:0] G, P, C;

assign G=A&B;
assign P=A|B;
assign C[0]=Cin;
assign C[1]=G[0]|(P[0]&C[0]);
assign C[2]=G[1]|(P[1]&C[1]);
assign C[3]=G[2]|(P[2]&C[2]);
assign Cout=G[3]|(P[3]&C[3]);

assign S=A^B^C;

endmodule
```

2. Dataflow Modeling TestBench

```
`timescale 1ns/1ps

module cla_four_bit_tb;
reg [3:0] A,B;
reg Cin;
wire [3:0] S;
wire Cout;

cla_four_bit uut(.A(A),.B(B),.Cin(Cin),.S(S),.Cout(Cout));

initial begin
/*$monitor("%0t\t%b\t%b\t%b\t\t\t%b\t%b\t" , $time,A,B,Cin,S,Cout);*/
A=4'b0001;B=4'b0010;Cin=0;#10;
A=4'b1111;B=4'b0001;Cin=1;#10;
A=4'b1010;B=4'b0101;Cin=1;#10;
A=4'b1111;B=4'b1111;Cin=1;#10;

$finish;
end
endmodule
```

3. Behavioral Modeling

```
`timescale 1ns/1ps

module cla_four_bit_behavioural(input [3:0] A,B, input Cin, output reg[3:0] S,
output reg Cout);

reg [3:0] G, P, C;

always@(*)
begin

G=A&B;
P=A|B;
C[0]=Cin;
C[1]=G[0] | (P[0]&C[0]);
C[2]=G[1] | (P[1]&C[1]);
C[3]=G[2] | (P[2]&C[2]);
Cout=G[3] | (P[3]&C[3]);
S=A^B^C;
end

endmodule
```

4. Behavioral Modeling TestBench

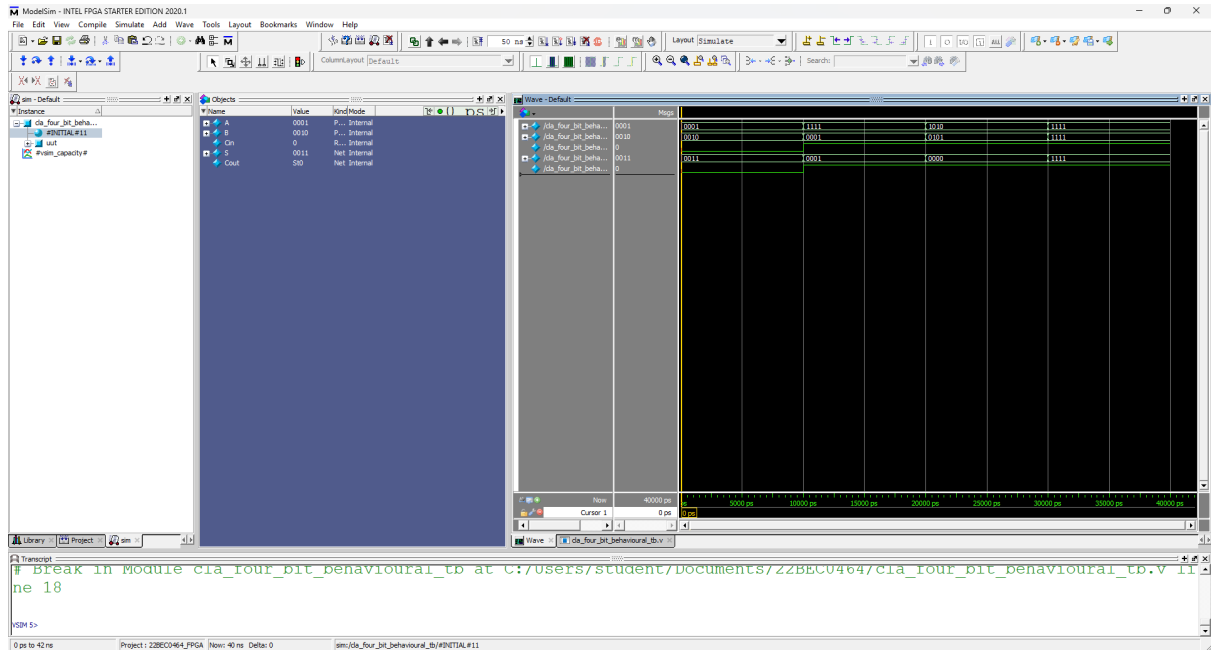
```
`timescale 1ns/1ps

module cla_four_bit_behavioural_tb;
reg [3:0] A,B;
reg Cin;
wire [3:0] S;
wire Cout;

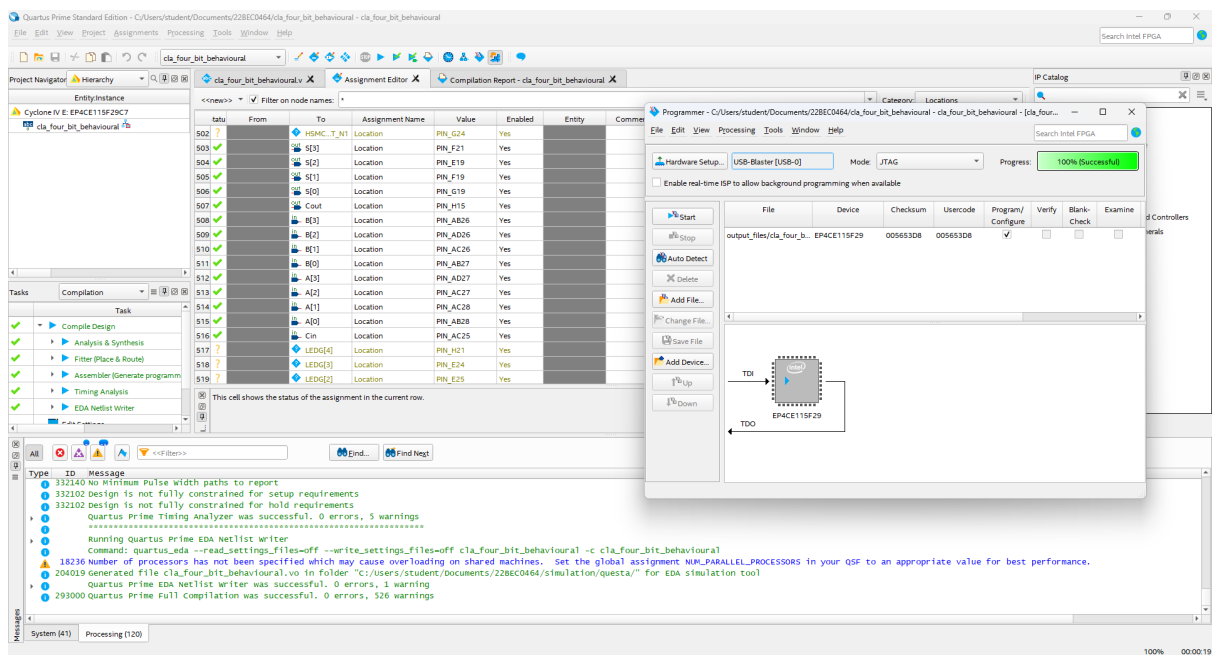
cla_four_bit_behavioural uut(.A(A),.B(B),.Cin(Cin),.S(S),.Cout(Cout));

initial begin
/*$monitor("%0t\t%b\t%b\t%b\t\t\t%b\t%b\t" , $time,A,B,Cin,S,Cout);*/
A=4'b0001;B=4'b0010;Cin=0;#10;
A=4'b1111;B=4'b0001;Cin=1;#10;
A=4'b1010;B=4'b0101;Cin=1;#10;
A=4'b1111;B=4'b1111;Cin=1;#10;

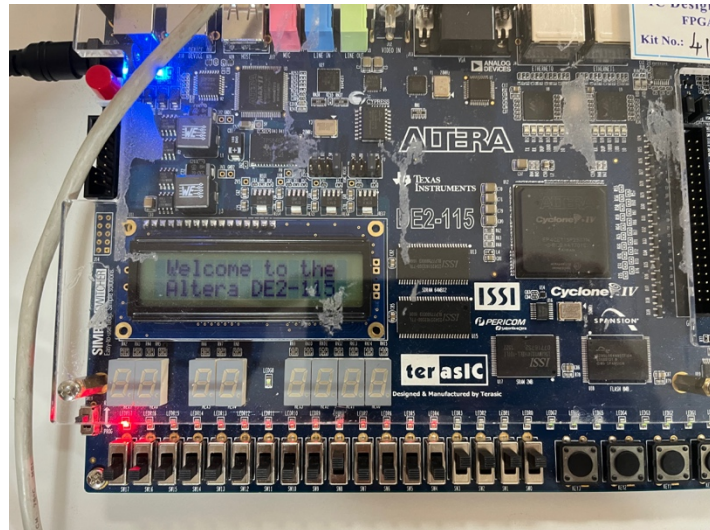
$finish;
end
endmodule
```



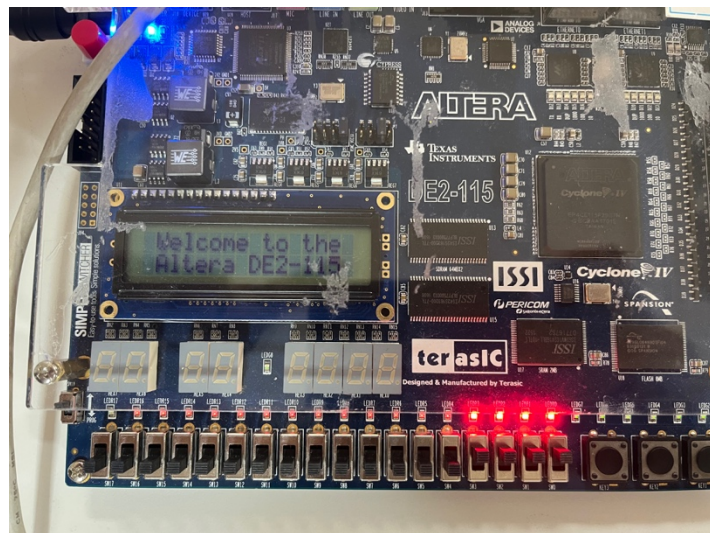
Output Verification Using ModelSim



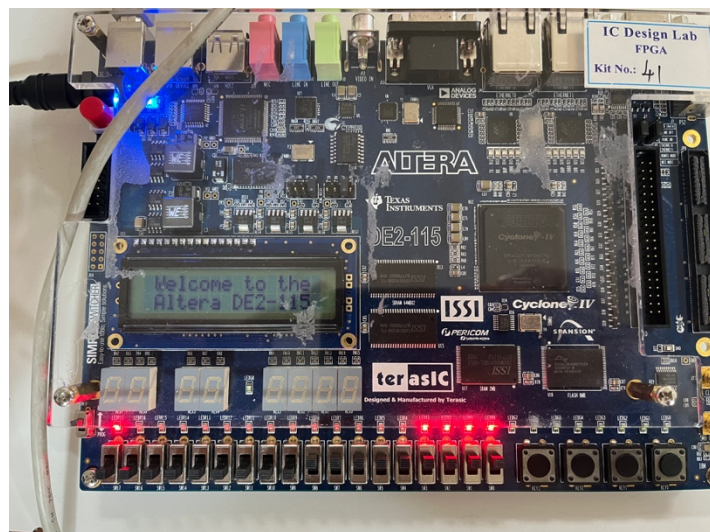
Pin Assignment on FPGA Using Quartus Prime



A=1111; B=0000; Cin=1; S=0000; Cout=1



A=1111; B=0000; Cin=0; S=1111; Cout=0



A=1111; B=1111; Cin=1; S=1111; Cout=1