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Name: UJJVAL RAGHAVENDRA L

Reg no: 22BEC0464

Subject: FPGA-Based System Design Lab

Subject Code: BECE406E

Assignment-3

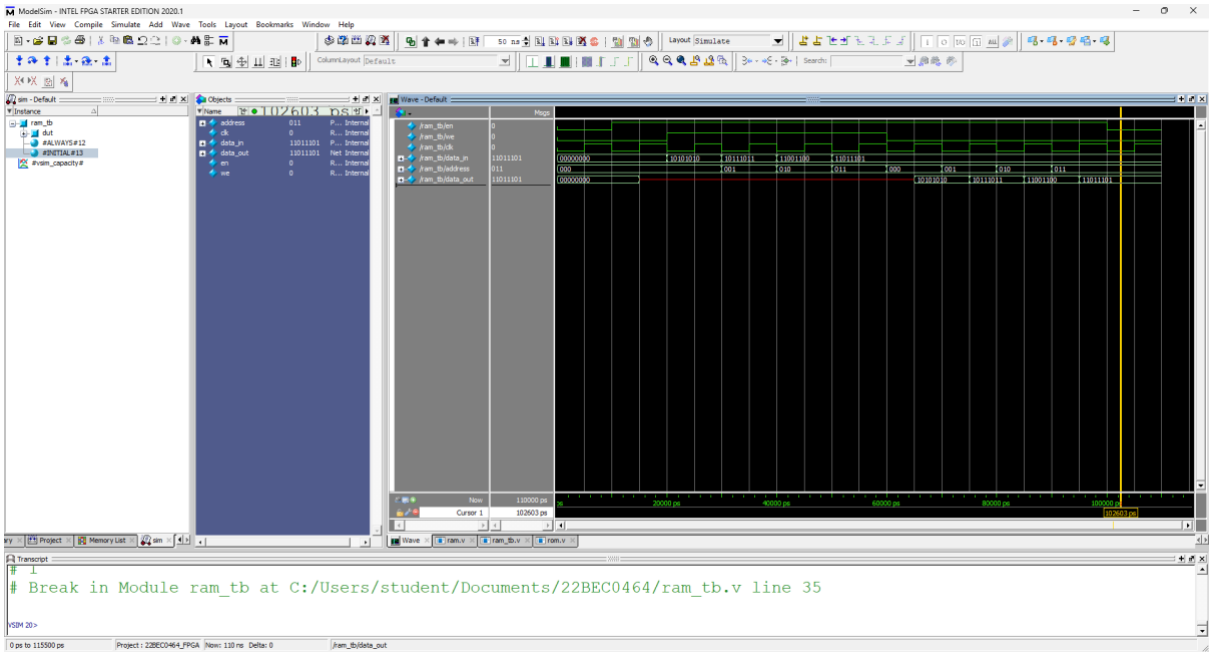
Single Port RAM

1. Behavioral Modeling

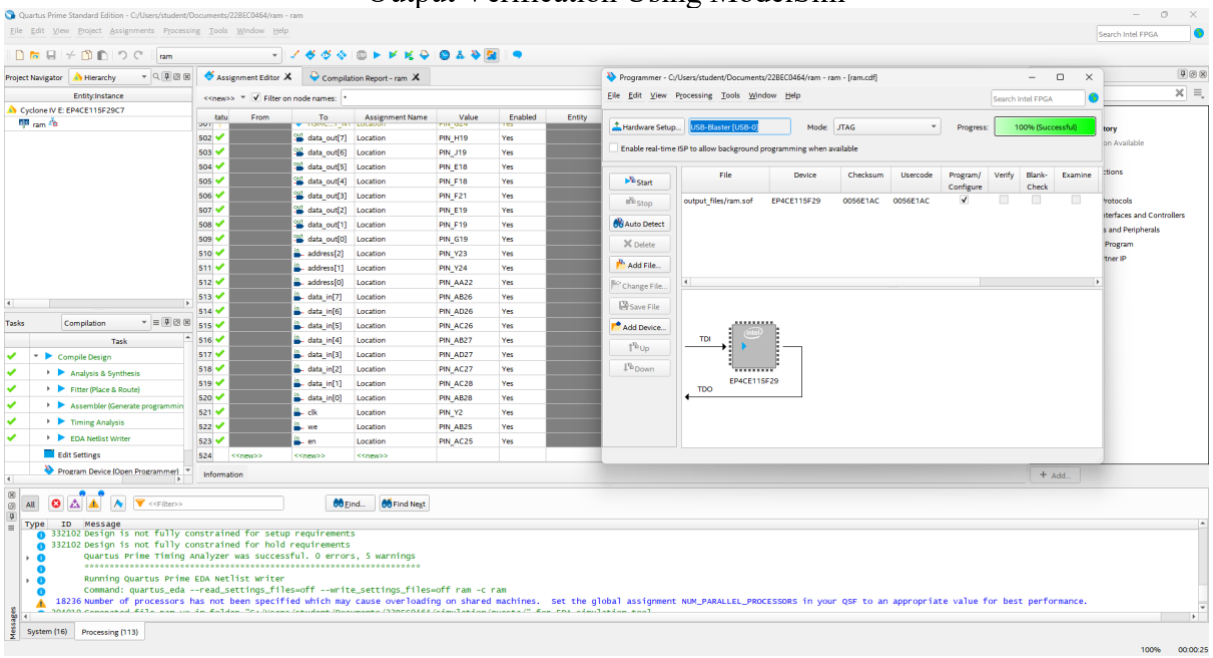
```
`timescale 1ns/1ps

module ram(input clk,en,we,input[2:0] address,input[7:0] data_in,output reg [7:0] data_out);
reg [7:0] mem [0:7];

initial begin
data_out = 8'b0;
end

always@(posedge clk)
if(en)begin
if(we)
mem[address]=data_in;
else
data_out=mem[address];
end
else
data_out = data_out;
endmodule
```

2. Behavioral Modeling TestBench

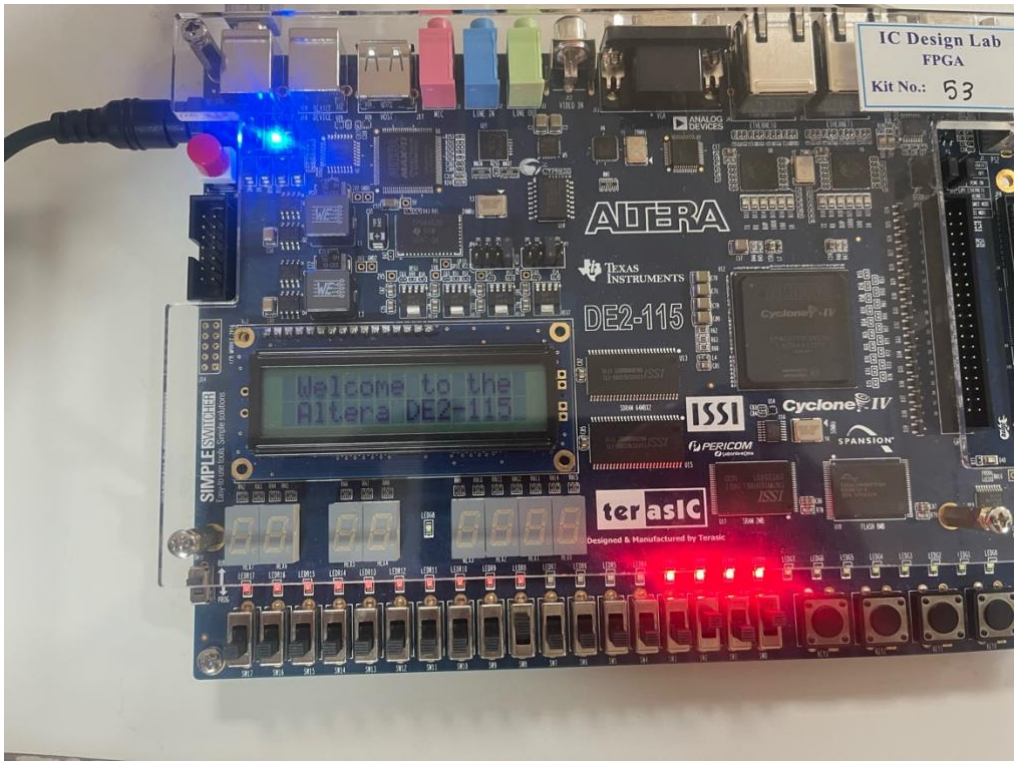
```
`timescale 1ns/1ps

module ram_tb();

reg clk,en,we;
reg [2:0] address;
reg [7:0] data_in;
wire [7:0] data_out;

ram dut(.clk(clk),.en(en),.we(we),.data_in(data_in),.address(address),.data_out(data_out));

always #5 clk=~clk;
initial begin
clk=0;
en=0;
we=0;
address=3'b0;
data_in=8'h00;


#10 en=1;


#10 we=1; address = 3'b0; data_in=8'hAA;
#10 we=1; address = 3'b1; data_in=8'hBB;
#10 we=1; address = 3'b10; data_in=8'hCC;
#10 we=1; address = 3'b11; data_in=8'hDD;

#10 we=0; address = 3'b0;
#10 we=0; address = 3'b1;
#10 we=0; address = 3'b10;
#10 we=0; address = 3'b11;

#10 en=0;
#10 $finish;

end
endmodule
```



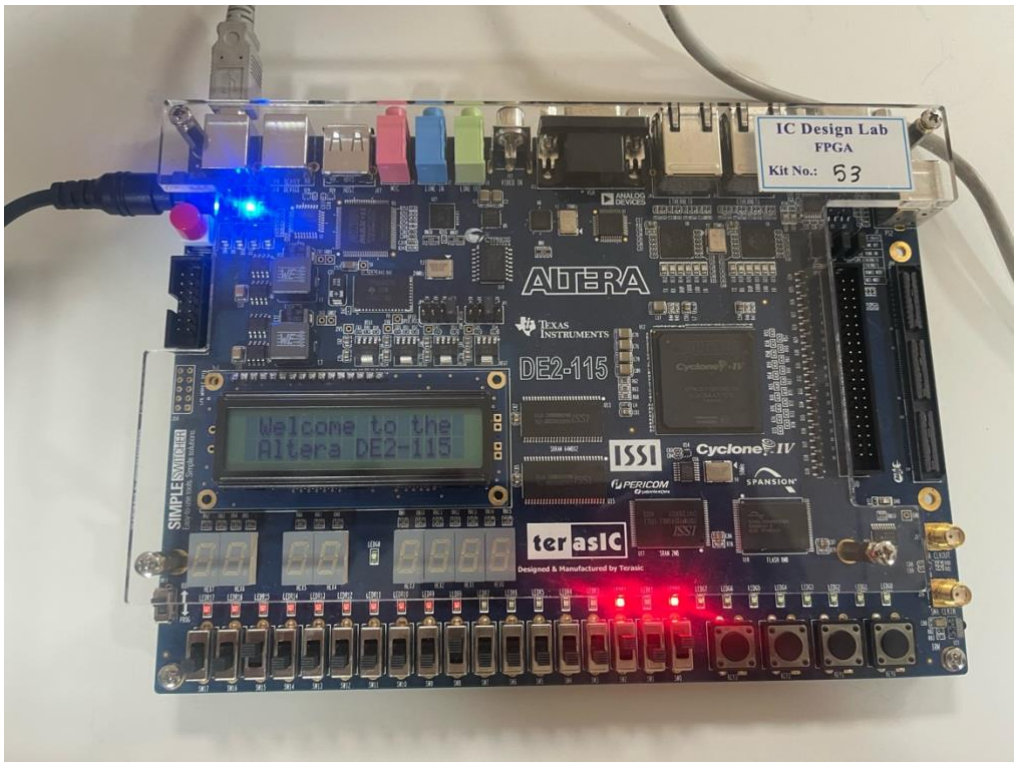
Output Verification Using ModelSim



Pin Assignment on FPGA Using Quartus Prime



Address =000(SW17-15); Write Enable=0(SW9); Enable=1(SW8); Data In=0000_0101(SW7-SW0); Data Out=0000_1111(LEDR7-LEDR0)



Address =001(SW17-15); Write Enable=0(SW9); Enable=1(SW8); Data In=0000_0101(SW7-SW0); Data Out=0000_1010(LEDR7-LEDR0)

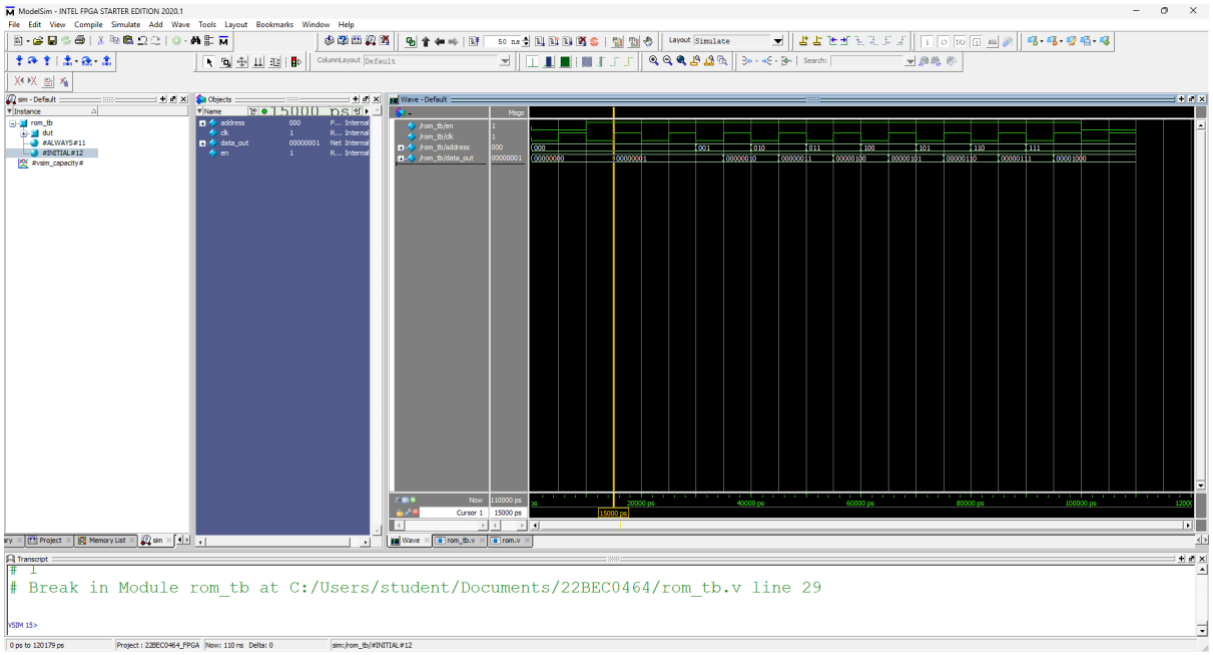
Single Port ROM

1. Behavioral Modeling

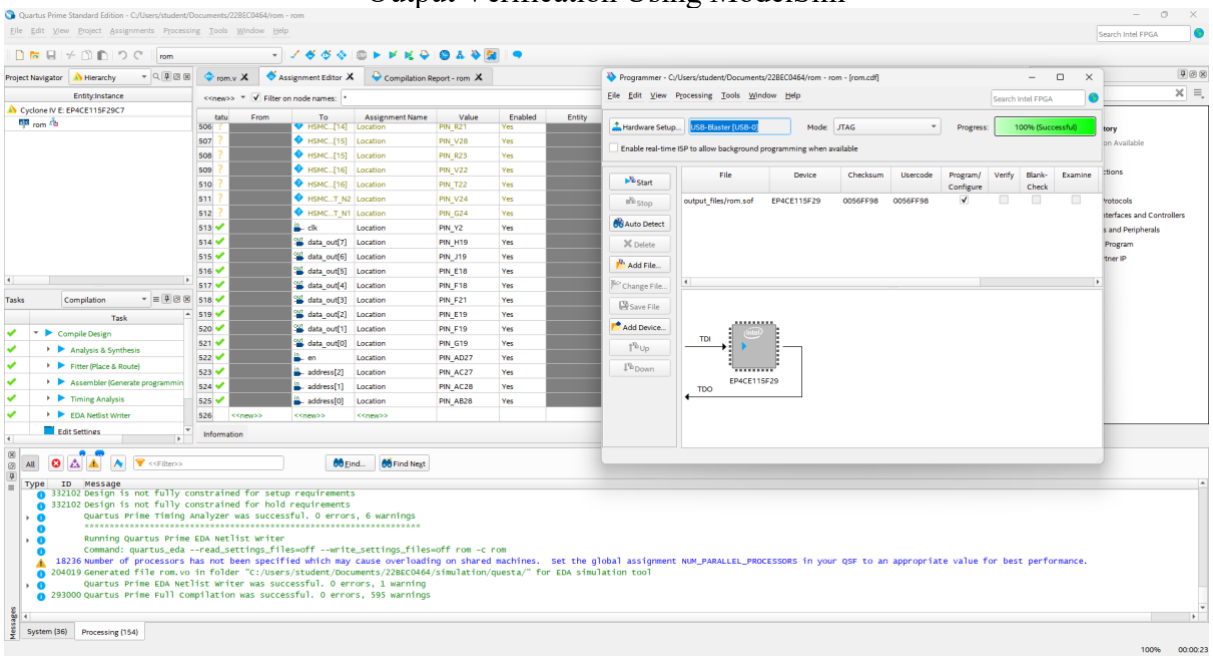
```
`timescale 1ns/1ps

module rom(input clk,en,input [2:0] address,output reg [7:0] data_out);

reg [7:0] mem [0:7];

initial
begin
data_out = 8'b0;
end

always @ (address)
case (address)
3'b000 : mem[address] = 8'b1;
3'b001 : mem[address] = 8'b10;
3'b010 : mem[address] = 8'b11;
3'b011 : mem[address] = 8'b100;
3'b100 : mem[address] = 8'b101;
3'b101 : mem[address] = 8'b110;
3'b110 : mem[address] = 8'b111;
3'b111 : mem[address] = 8'b1000;
default : mem[address] = 8'b0;
endcase

always@(posedge clk)
begin
if(en)begin
data_out <= mem[address];
end else
data_out <= data_out;
end
endmodule
```

2. Behavioral Modeling TestBench

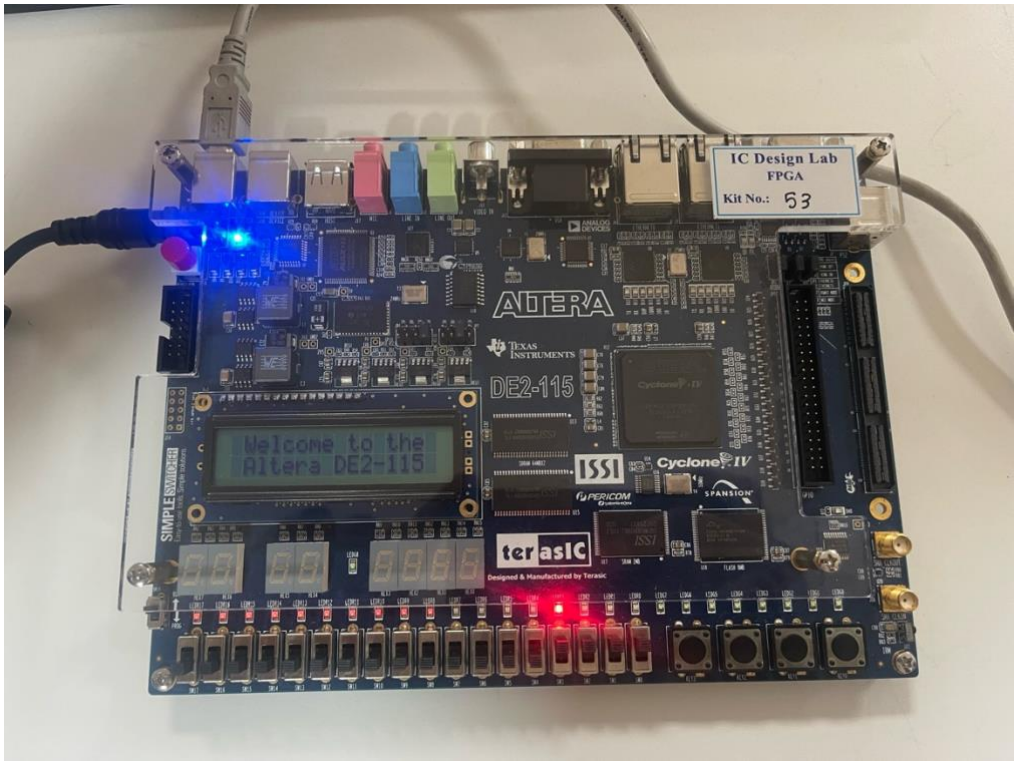
```
`timescale 1ns/1ps

module rom_tb();

reg clk,en;
reg [2:0] address;
wire [7:0] data_out;

rom dut(.clk(clk),.en(en),.address(address),.data_out(data_out));

always #5 clk=~clk;
initial begin
clk=0;
en=0;
address=3'b0;

#10 en=1;
#10 address=3'b0;
#10 address=3'b1;
#10 address=3'b10;
#10 address=3'b11;
#10 address=3'b100;
#10 address=3'b101;
#10 address=3'b110;
#10 address=3'b111;


#10 en=0;
#10 $finish;
end
endmodule
```



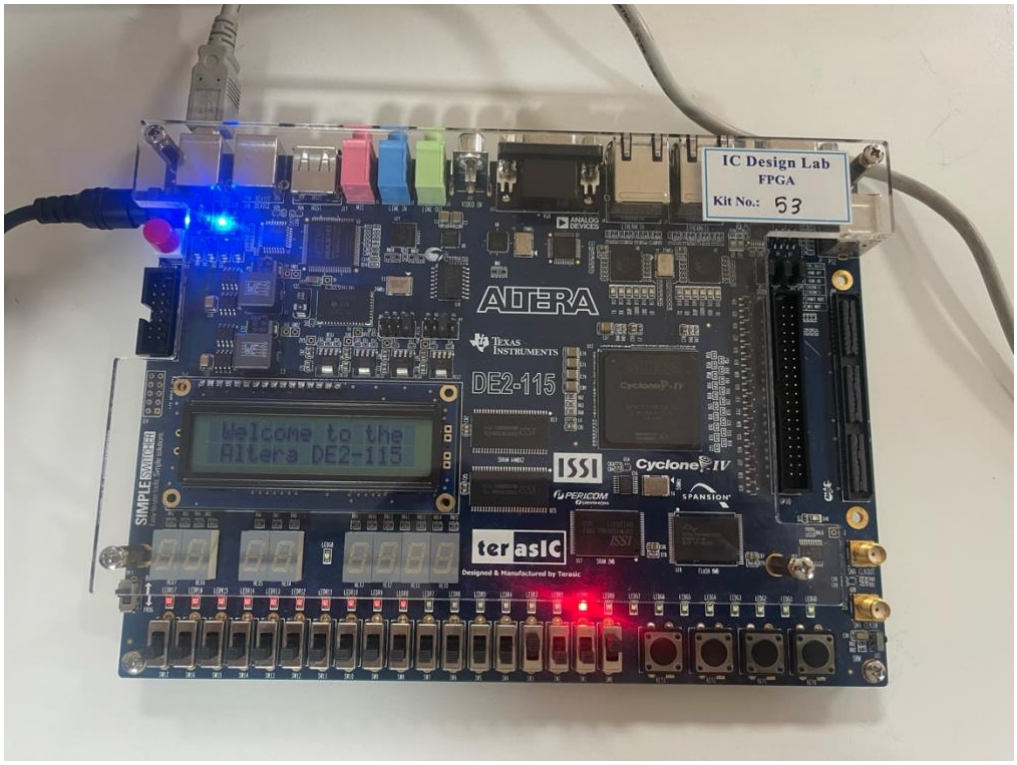
Output Verification Using ModelSim



Pin Assignment on FPGA Using Quartus Prime



Enable=1(SW3);Address=111(SW2-SW0); Data Out=0000_1000(LEDR7-LEDR0)



Enable=1(SW3);Address=001(SW2-SW0); Data Out=0000_0010(LEDR7-LEDR0)