E3: 245 Processor System Design

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Laboratory Exercise 2

Objective of this Lab exercise is to implement a Single Cycle Processor

2. Design and Implement a Single Cycle RISC-V processor on Digilent BASYS3 FPGA Board. Target Device is Xilinx Artix-7 XC7A35T- ICPG236C (Family Artix-7, Part XC7A35T, Package CPG236, Speed Grade -1).

The Processor is a 32-bit RISC-V Processor. The processor should support basic arithmetic-logic instructions, *lui*, branch instructions, and load-store instructions. Atomic instructions, jump instructions, *auipc* and CSR instructions need not be supported.

You can assume aligned transfer for *word*, *half-word* and *byte* data. For data and instruction memory, you can use the memory IP made of distributed RAM of FPGA. Distributed RAM would allow asynchronous read. Memory size can be 1 Kword.

You need to implement only the user mode of RISC-V. Test the processor with a suitable algorithm, check if you can write the program in C and get the required assembly/binary code and use it.

Design the Datapath block schematic first. Then do the HDL coding. Give the IO Constraints and Timing Constraints to achieve maximum delay performance. Do the Timing Analysis and Timing simulation with proper testbench.

Refer to the User manual of BASYS3 Board for resources available, external circuit, and pin numbers where external resources are connected. Use LVCMOS33 IO standard on pins. You can do the pin assignment and give timing constraints using GUI or manually creating “xdc” file in proper format and adding it to the project.

Submit the block schematic of the datapath design, state diagram of the controller (if any), source VHDL codes, Constraint files, Timing Report, and brief report on the resource utilization.