E3: 245 Processor System Design

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Laboratory Exercise 1

The objective of this Lab exercise is to implement a simple Multi-Cycle Processor

1. Design and implement a 16-bit Processor on Digilent BASYS3 FPGA Board. Target Device is Xilinx Artix-7 XC7A35T- ICPG236C (Family Artix-7, Part XC7A35T, Package CPG236, Speed Grade -1). Refer to the processor example discussed in the Prerequisite course, E3 231 Digital system design with FPGAs.

The Processor is a 16-bit RISC CPU with 16-bit Address space with RISC type instructions. The processor is a multi-cycle processor which does fetch, decode, execution, and write stages sequentially in multiple cycles. It should support minimal arithmetic, logic, and branch instructions with a program counter. It must support a branch on condition to implement loops. Assume 3 operand instructions. It need not have external interrupts or exception handling. The processor has two internal buses such that two concurrent transfers can happen. Also assume that an Instruction prefetch register (IPR) is available, the output of which goes to instruction register (IR) so that instruction fetch of the next instruction can happen concurrently with the processing of the current instruction. Since the FPGA does not have internal tri-state gates, use a regular multiplexer to multiplex outputs on to the data buses. Test the processor with an algorithm to find the maximum number from a set of ten random numbers.

Design the Datapath block schematic (Level 0 and Level 1) and FSM state diagram first. Then do the HDL coding. Give the IO Constraints and Timing Constraints to achieve maximum delay performance. Do the Timing Analysis and Timing simulation with proper testbench.

Refer to the user manual of BASYS3 Board for resources available within FPGA and on the board, and for pin numbers where external resources are connected. Use LVCMOS33 IO standard on pins. You can do the pin assignment and give timing constraints using GUI or by manually creating an “xdc” file in proper format and adding it to the project.

Submit the block schematic of the datapath, state diagram of the controller, source HDL codes, the “coe” file of the binary code. Timing Report, and a brief report on the resource utilization.