E3: 245 Processor System Design

DESE, Indian Institute of Science, Bangalore

Laboratory Exercise 3

The objective of this Lab exercise is to implement a Pipelined RISC-V Processor with Instruction Cache.

2. Design and Implement a 5-stage Pipelined RISC-V processor on Digilent BASYS3 FPGA Board. Target Device is Xilinx Artix-7 XC7A35T- ICPG236C (Family Artix-7, Part XC7A35T, Package CPG236, Speed Grade -1).

The Processor is a 32-bit RISC-V Processor. The processor should support basic arithmetic-logic instructions, branch instructions, *lui*, load-store instructions, and jump instructions. Atomic instructions, *auipc* and CSR instructions need not be supported. Implement hazard detection and forwarding (from EX, MEM and WB stage outputs). Implement the Stall unit for load, and branch instructions.

You can assume aligned transfer for *word*, *half-word* and *byte* data. Implement instruction cache. Data cache is not required and the data access is from data memory. The instruction cache is direct mapped with a block size of four words. The main instruction memory is to be implemented in Block RAM. There is no need to support any burst transfer for filling the cache.

Test the processor with a suitable algorithm, with a procedure call. Check if you can write the program in C and get the required assembly/binary code and use it.

Design the Datapath block schematic first. Then do the HDL coding. Give the IO Constraints and Timing Constraints to achieve maximum delay performance. Do the Timing Analysis and Timing simulation with proper testbench.

Submit the block schematic of the Datapath design, state diagram of the controller (if any), source Verilog codes, Constraint files, Timing Report, resource utilization and software code.