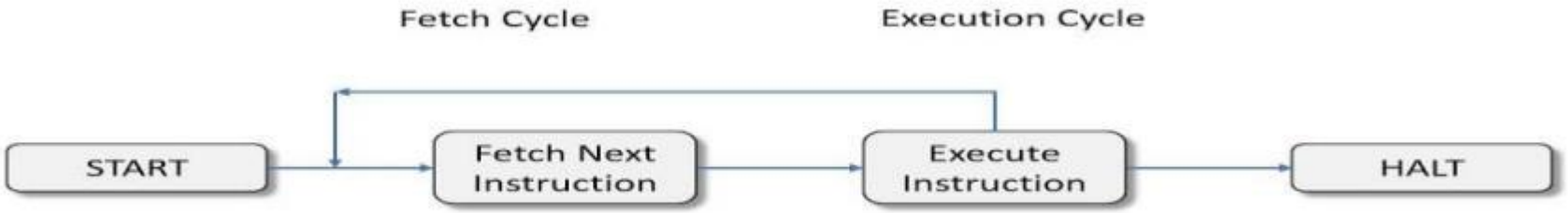
Unit 3

Instruction Cycle

Instruction Cycle

- An instruction is fetched from the memory address stored in the program counter (PC) and is stored in the instruction register (IR). The PC is incremented.
- The decoder interprets the instruction. If it is a jump, the PC is reset and the cycle ends. Otherwise, any required data is fetched from main memory and is placed in data registers.
- The CPU executes the instruction by reading values from registers, performing arithmetic or logical functions on them, and writing the result into a register.
- The result is stored in main memory or is sent to an output device.
- Interrupts are handled.

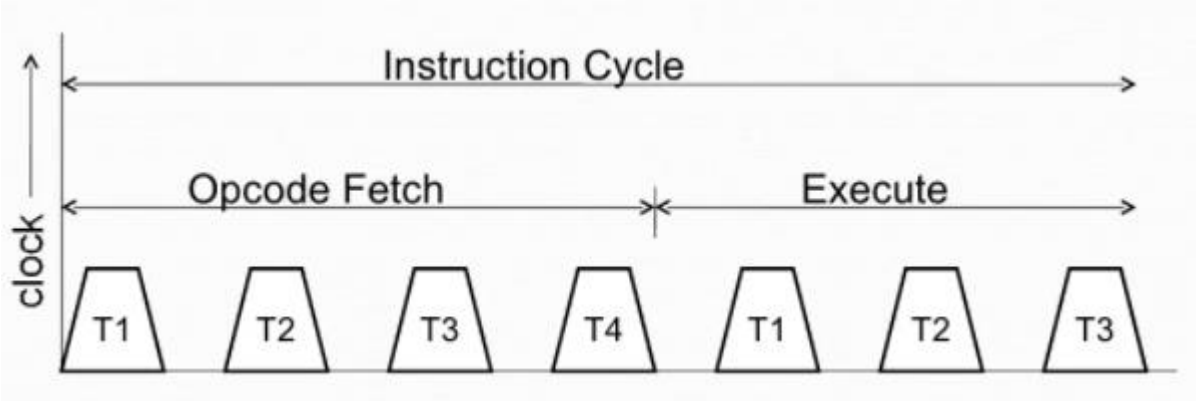
The instruction cycle (also known as the fetch–decode–execute cycle or simply the fetch-execute cycle) is the cycle which the central processing unit (CPU) follows from boot-up until the computer has shut down in order to process instructions. It is composed of three main stages: the fetch stage, the decode stage, and the execute stage.



- This is a simple diagram illustrating the individual stages of the fetch-decode execute cycle.
- In simpler CPUs, the instruction cycle is executed sequentially, each instruction being processed before the next one is started. In most modern CPUs, the instruction cycles are instead executed concurrently, and often in parallel, through an instruction pipeline: the next instruction starts being processed before the previous instruction has finished, which is possible because the cycle is broken up into separate.

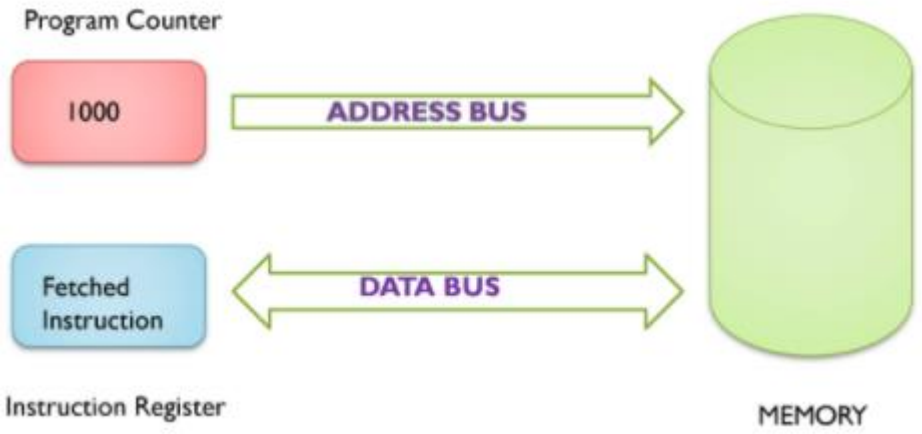
- The CPU fetches one instruction from the memory at a time and execute it . It executes all the instructions of a program one by one to produce to the final result .
- Instruction cycle consist of fetch and execute cycle.
- In fetch cycle a CPU fetches opcode from the memory.
- Specific operation in an instruction constitute an execute cycle.

IC=FC+EC



Instruction Fetching

- In this phase program counter (PC) plays vital role.
- Program Counter is a register which stores the address of the next instruction to be executed
- Hence depending on the value of PC address is send through Address Bus to the memory and then specific instruction is sent back through Data Bus



Instruction Decode

- After fetching an instruction, it is decoded from "user friendly language" to "machine language" which is familiar to the Processor of computer system

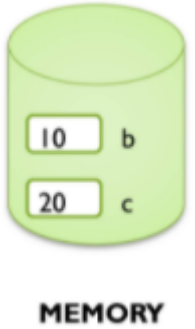
Data Fetching

- In this phase Data is fetched through Data Bus
- Fetch the operand from the memory for instance

a=b+c;

The above instruction requires the values of b and c to be fetched from the memory

Only then it can move to execution



Instruction Execution

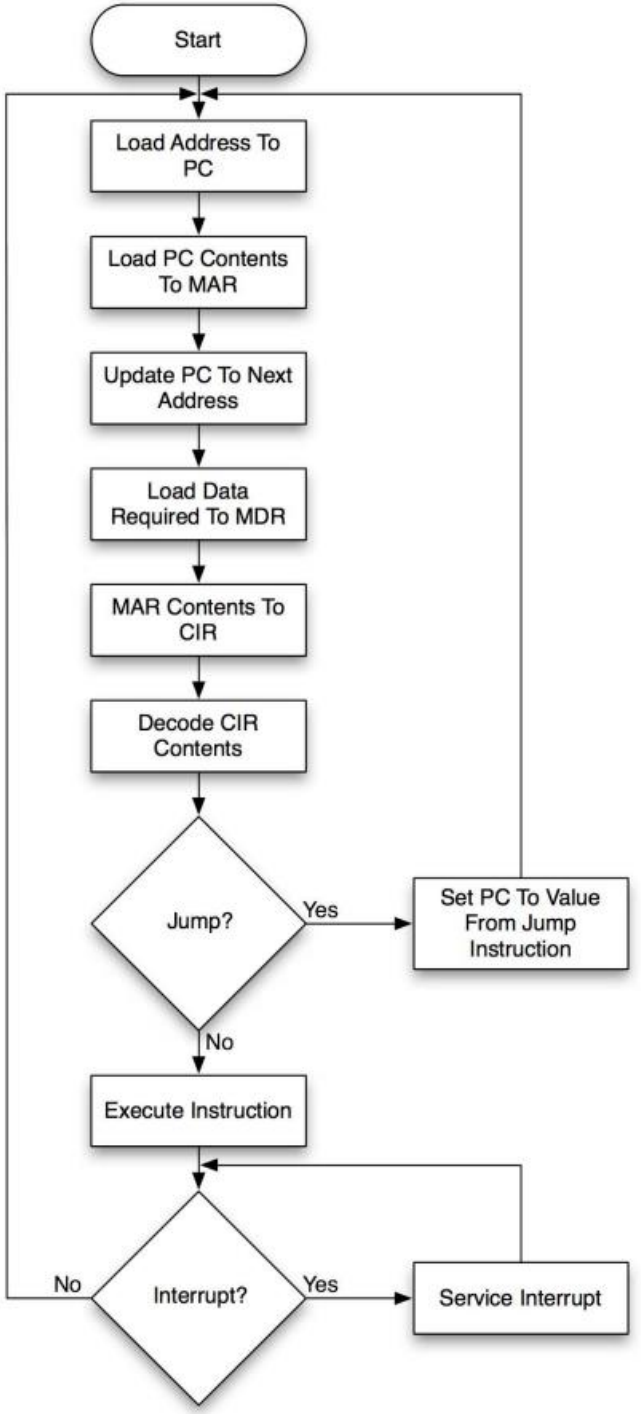
- Once the instruction gets decoded the processor executes the instruction
- In this phase, processor performs the actions specified by the given instruction

Writing Result

- Once the instruction is executed the result produced is written back to the memory
- Generally Accumulator (AC) stores input and output data
- Results is send back to memory through data bus

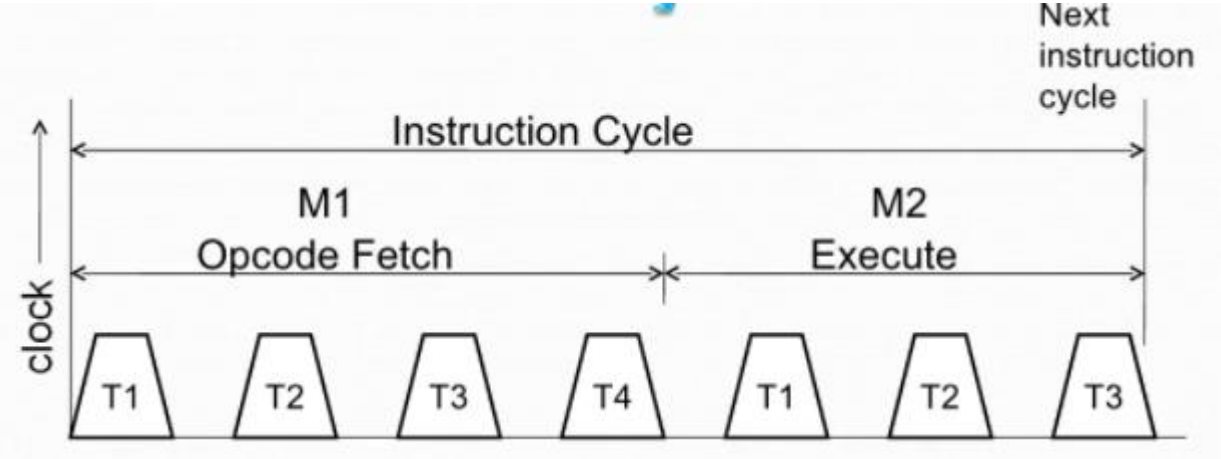
- After completion of instruction cycle program counter is incremented by one
- In this way again a new cycle starts and goes on in the same way Until all the instructions are executed.

Execution of a complete instruction



Machine Cycle

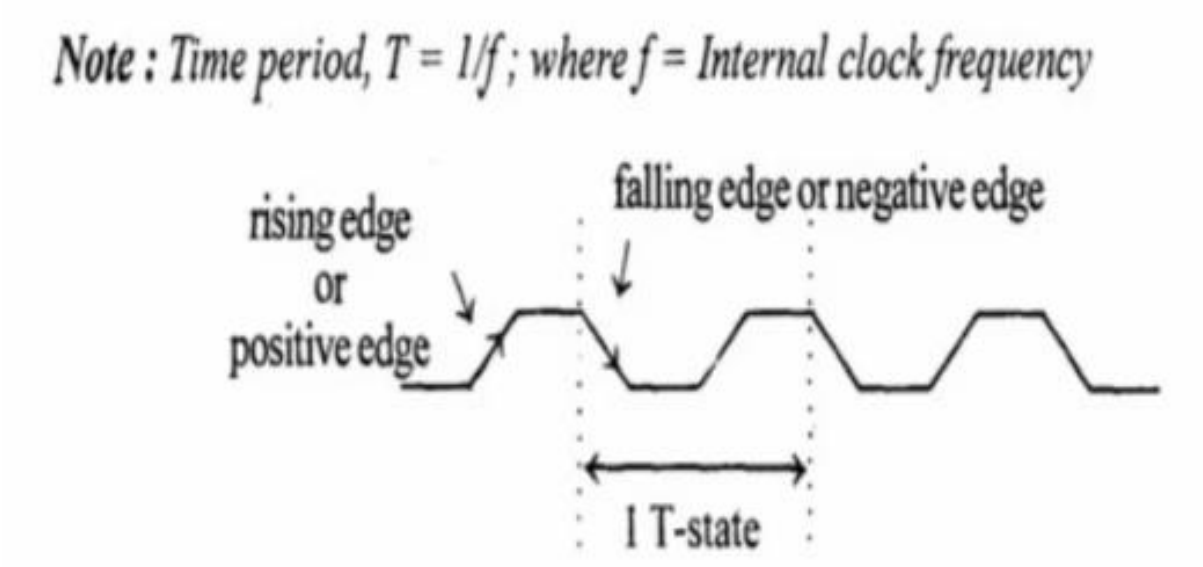
- The necessary steps carried out to perform the operation of accessing either memory or I/O device, constitute a machine cycle.
- Necessary steps carried out to perform a fetch, a read or write operation constitute a machine cycle.
- One basic operation such as opcode fetch, memory read, memory write, I/O read, or I/O write.
- Instruction cycle consist of several machine cycle.
- Machine cycle: the time required to access the memory or input/output devices



T-State

- One subdivision of an operation performed in one clock cycle is called a state or T-state.
- The subdivisions are internal states synchronized with the system clock .
- So one clock cycle of the system is referred to as a state.
- T-state: the machine cycle and instruction cycle takes multiple clock periods. A portion of an operation carried out in one system clock period is called as T-State.

- Timing Diagram: is graphical representation. It represents the execution time taken by each instruction in a graphical format. The execution time is represented in T-states.
- Instruction cycle: the time required to execute an instruction



Instruction Execution and Timing Diagram

- Each instruction in 8085 microprocessor consists of two part- operation code (opcode) and operand. The opcode is a command such as ADD and the operand is an object to be operated on, such as a byte or the content of a register.
- Instruction Cycle: The time taken by the processor to complete the execution of an instruction. An instruction cycle consists of one to six machine cycles.
- Machine Cycle: The time required to complete one operation; accessing either the memory or I/O device. A machine cycle consists of three to six T-states.
- T-State: Time corresponding to one clock period. It is the basic unit to calculate execution of instructions or programs in a processor.

- To execute a program, 8085 performs various operations as:
- Opcode fetch
- Operand fetch
- Memory read/write
- I/O read/write

External communication functions are:

- Memory read/write
- I/O read/write
- Interrupt request acknowledge

Opcode Fetch Machine Cycle

It is the first step in the execution of any instruction. The timing diagram of this cycle is given in Fig. 7.

The following points explain the various operations that take place and the signals that are changed during the execution of opcode fetch machine cycle:

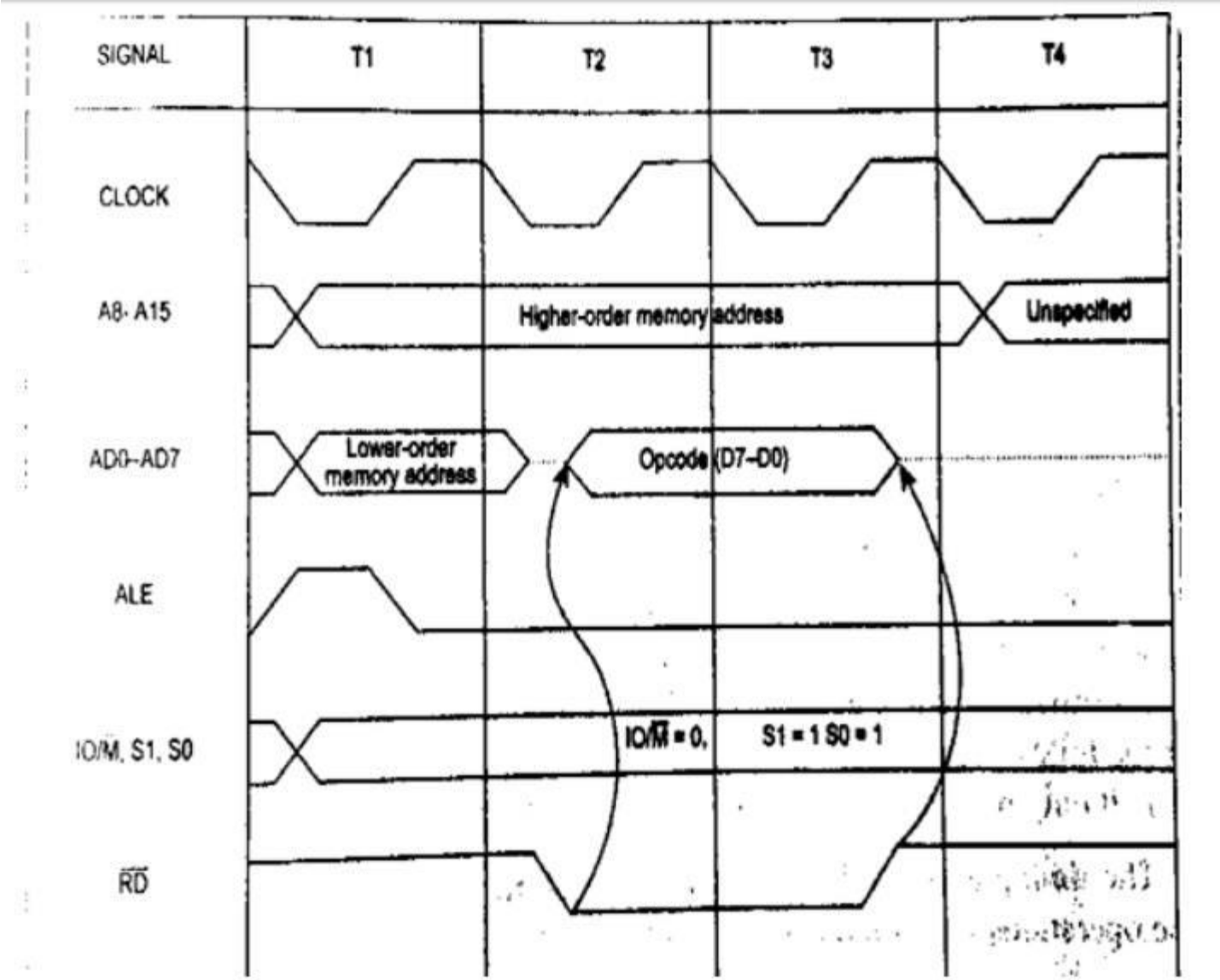


Fig. 7 Timing diagram for opcode fetch cycle

T1 clock cycle

i. The content of PC is placed in the address bus; AD0 - AD7 lines contains lower bit address and A8 – A15 contains higher bit address.

ii. IO/^M signal is low indicating that a memory location is being accessed. S1 and S0 also changed to the levels as indicated in Table 1.

iii. ALE is high, indicates that multiplexed AD0 – AD7 act as lower order bus.

T2 clock cycle

i. Multiplexed address bus is now changed to data bus.
ii. The ^(RD) signal is made low by the processor. This signal makes the memory device load the data bus with the contents of the location addressed by the processor.

T3 clock cycle

i. The opcode available on the data bus is read by the processor and moved to the instruction register.
ii. The ^(RD) signal is deactivated by making it logic 1.

T4 clock cycle

i. The processor decode the instruction in the instruction register and generate the necessary control signals to execute the instruction. Based on the instruction further operations such as fetching, writing into memory etc takes place.

Memory Read Machine Cycle

- The memory read cycle is executed by the processor to read a data byte from memory. The machine cycle is exactly same to opcode fetch except: a) It has three T-states b) The S0 signal is set to 0. The timing diagram of this cycle is given in Fig. 8.

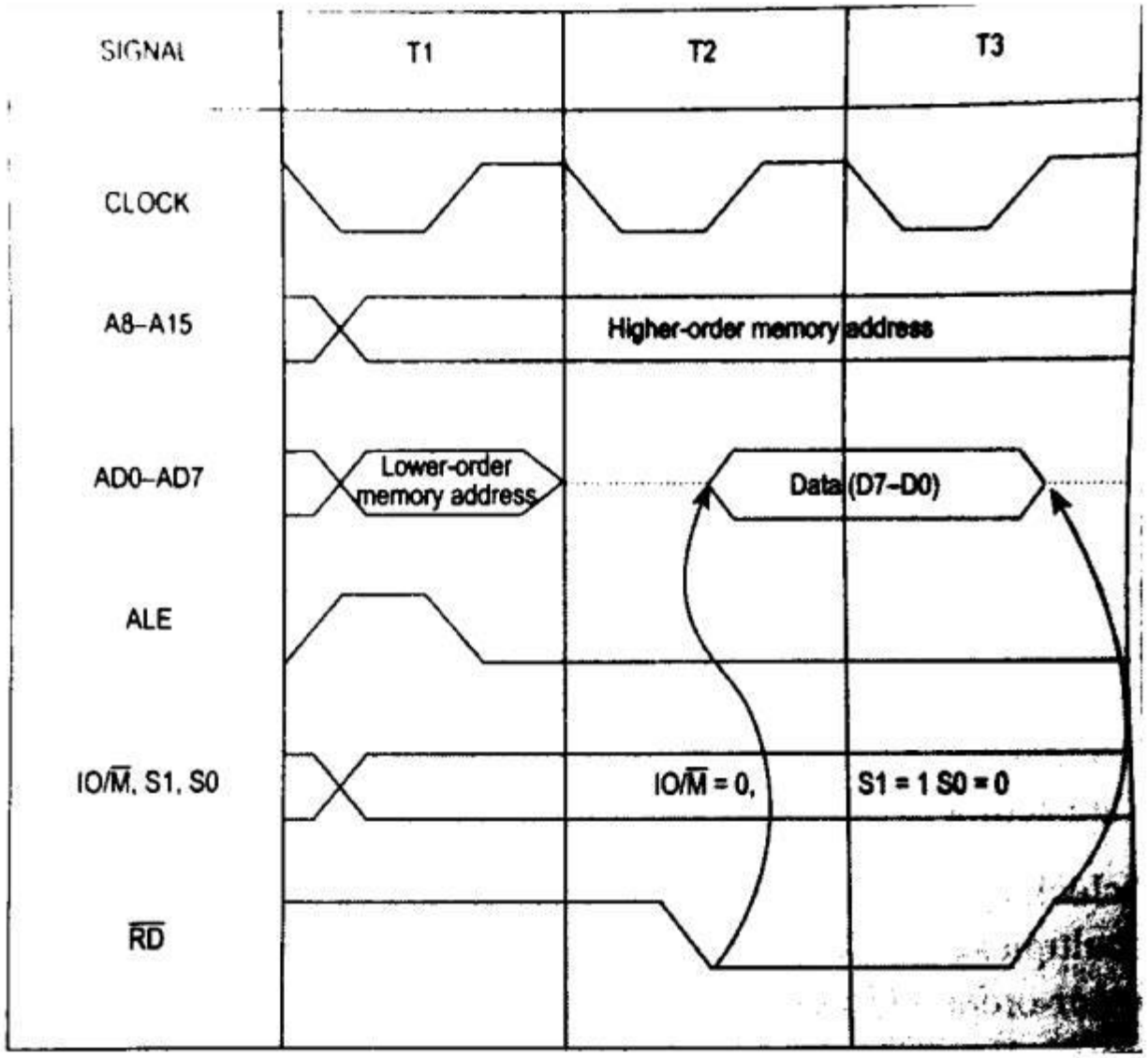


Fig. 8 Timing diagram for memory read machine cycle

Memory Write Machine Cycle

- The memory write cycle is executed by the processor to write a data byte in a memory location. The processor takes three T-states and ^(WR) signal is made low. The timing diagram of this cycle is given in Fig. 9.

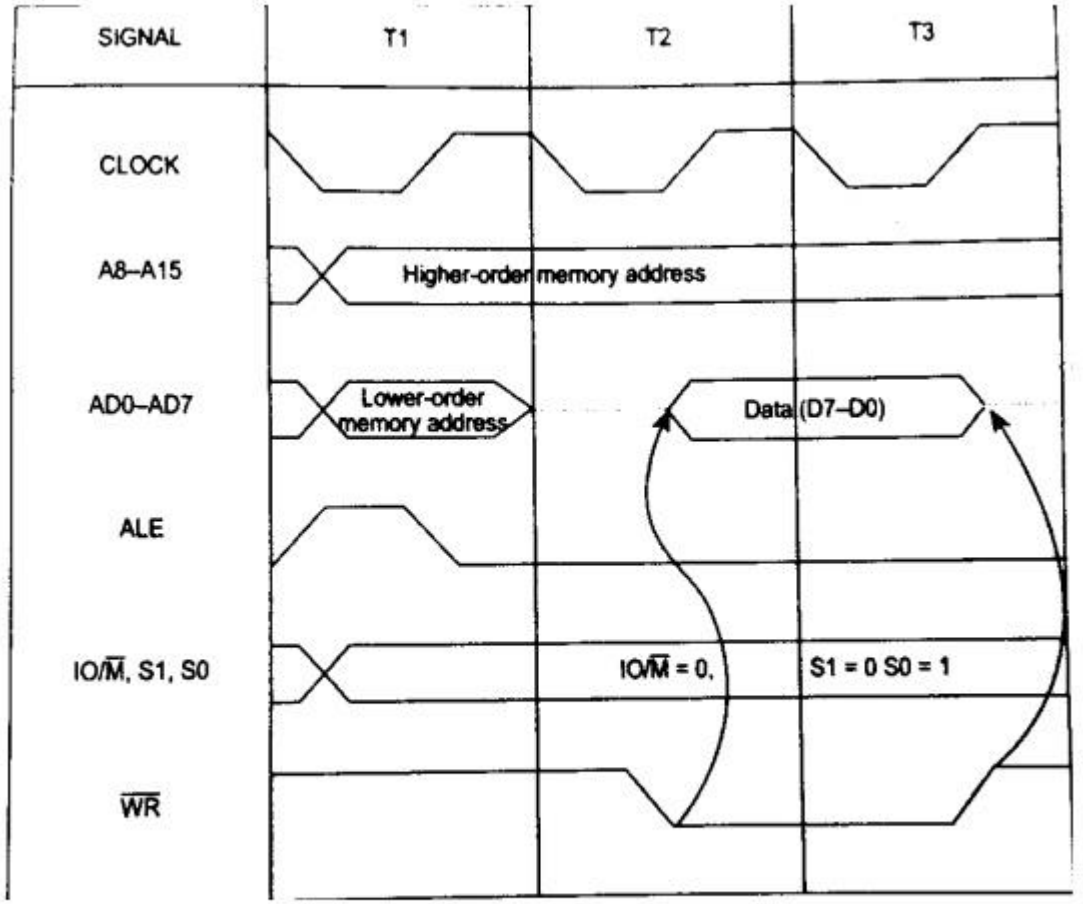


Fig. 9 Timing diagram for memory write machine cycle

I/O Read Cycle

- The I/O read cycle is executed by the processor to read a data byte from I/O port or from peripheral, which is I/O mapped in the system. The 8-bit port address is placed both in the lower and higher order address bus. The processor takes three T-states to execute this machine cycle. The timing diagram of this cycle is given in Fig. 10.

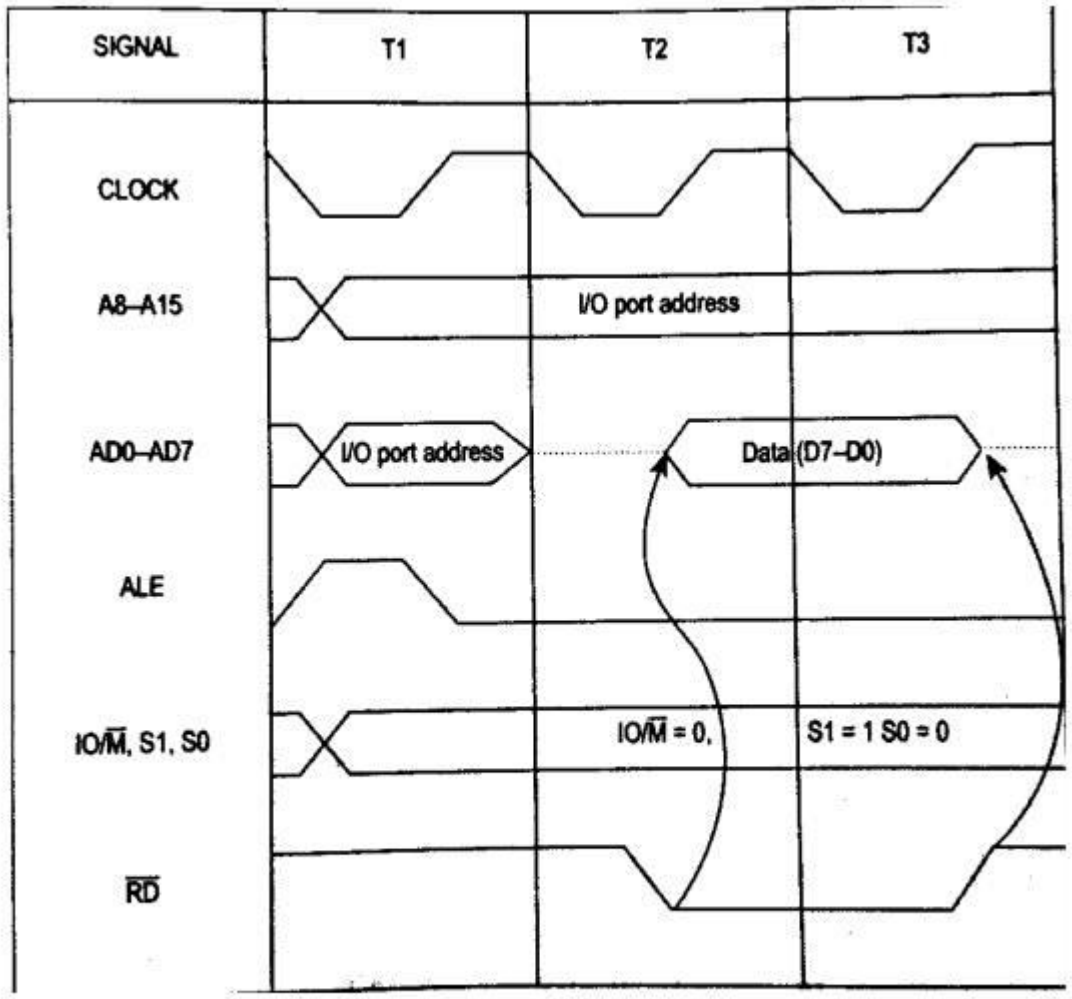


Fig. 10 Timing diagram I/O read machine cycle

I/O Write Cycle

- The I/O write cycle is executed by the processor to write a data byte to I/O port or to a peripheral, which is I/O mapped in the system. The processor takes three T-states to execute this machine cycle. The timing diagram of this cycle is given in Fig. 11.

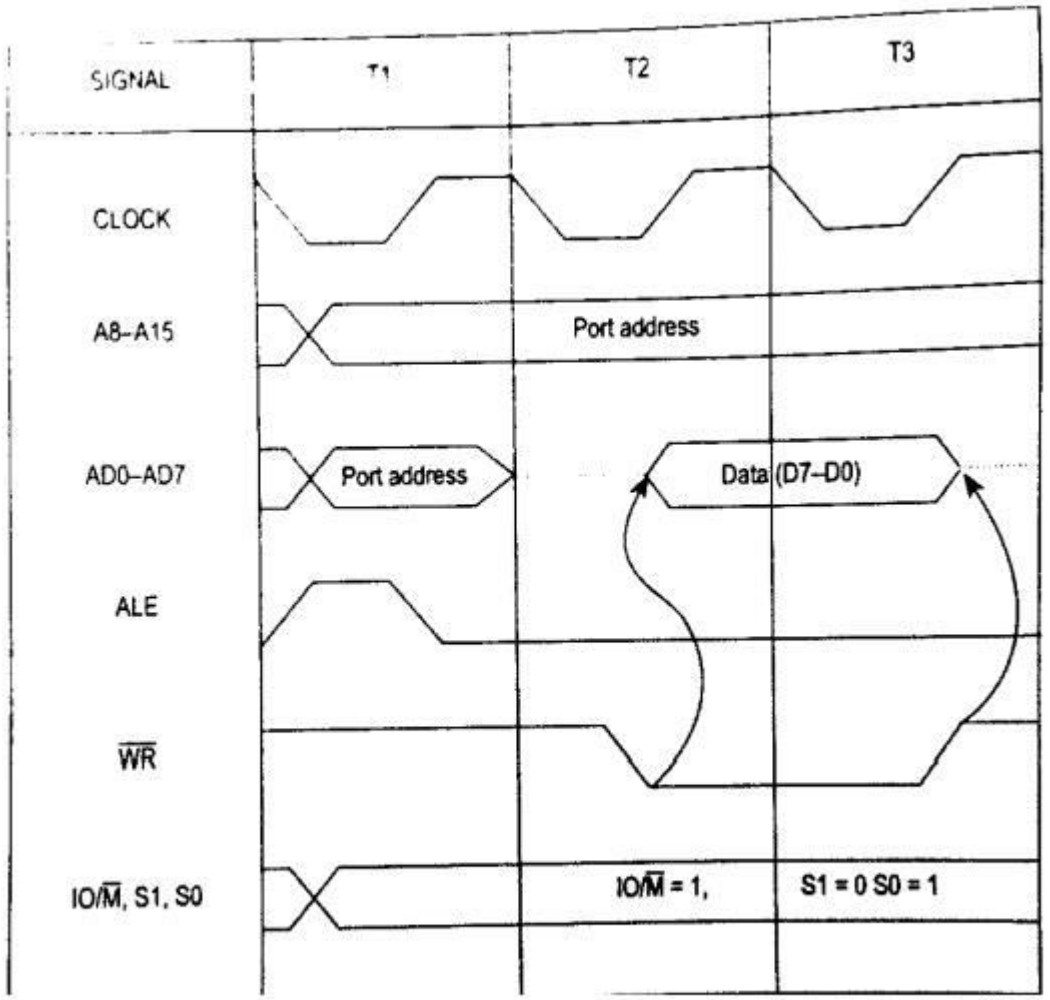


Fig. 11 Timing diagram I/O write machine cycle

Ex: Timing diagram for IN 80H.

Table 5 IN instruction

Address	Mnemonics	Opcode
800F	IN 80H	DB
8010		80

The instruction and the corresponding codes and memory locations are given in Table 5.

i. During the first machine cycle, the opcode DB is fetched from the memory, placed in the instruction register and decoded.

ii. During second machine cycle, the port address 80H is read from the next memory location.

iii. During the third machine cycle, the address 80H is placed in the address bus and the data read from that port address is placed in the accumulator.

The timing diagram is shown in Fig. 12.

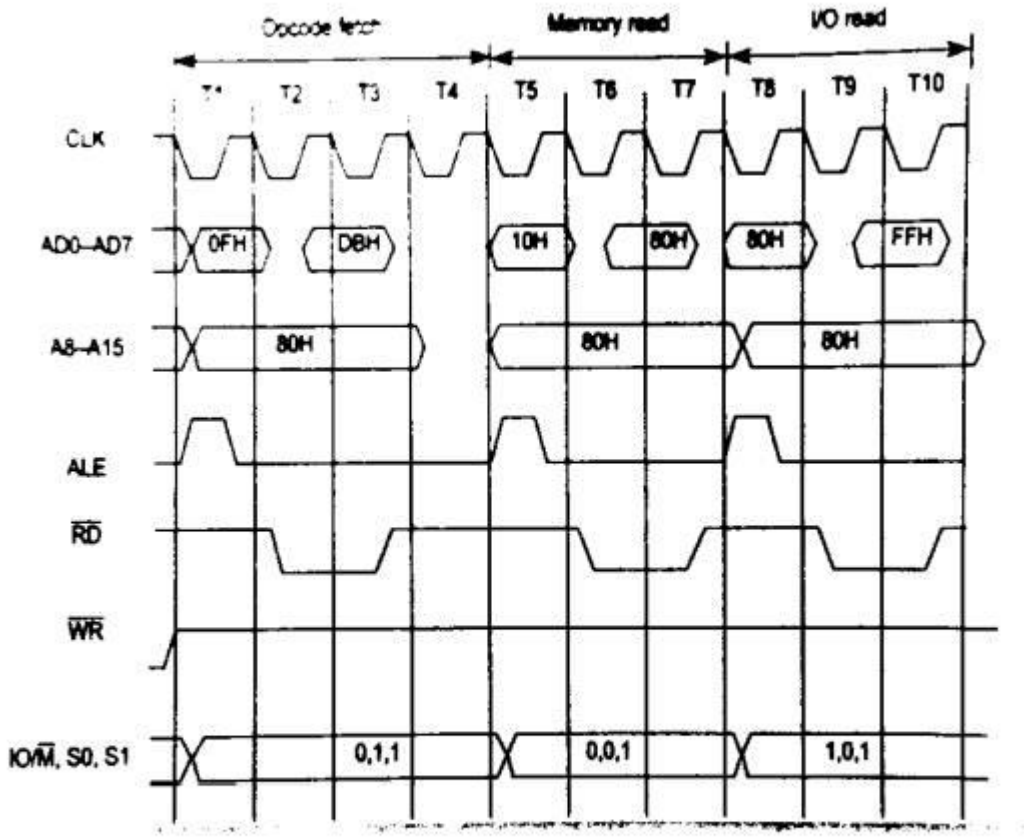


Fig. 12 Timing diagram for the IN instruction

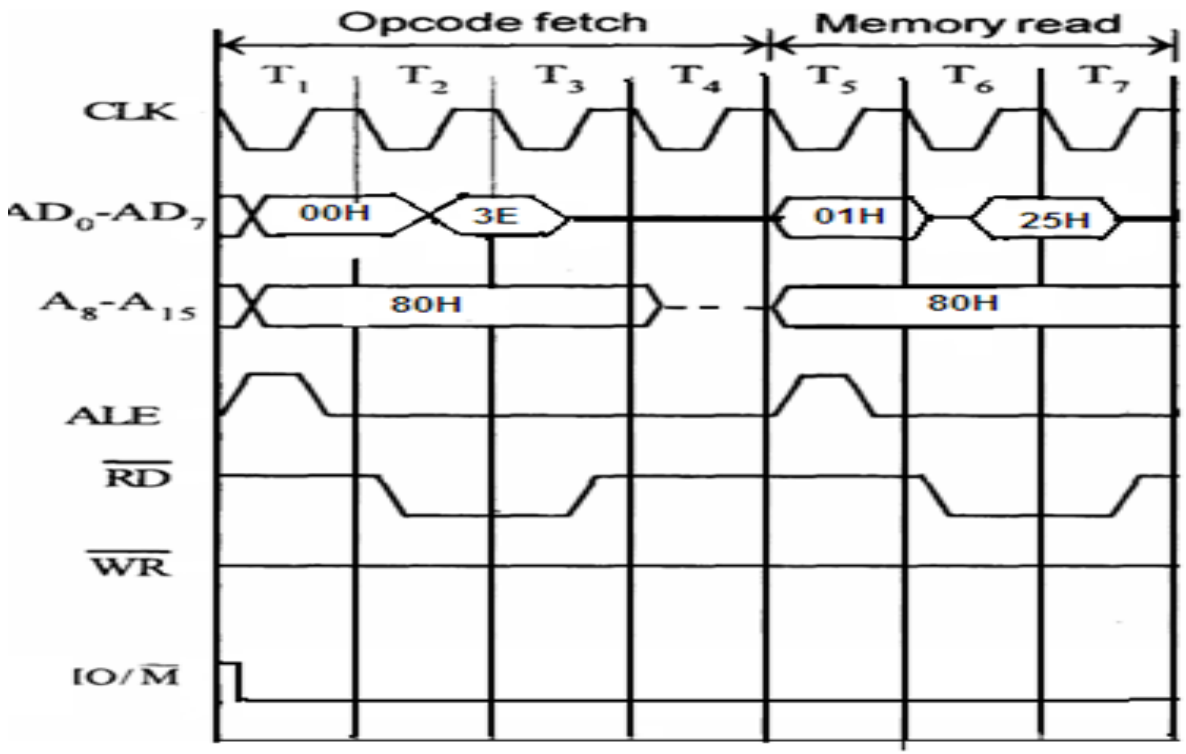
Timing Diagrams

The 8085 Microprocessor has 7 basic machine cycle. They are

1. Opcode Fetch Cycle (4T or 6T)
2. Memory Read Cycle (3T)
3. Memory Write Cycle (3T)
4. I/O Read Cycle (3T)
5. I/O Write Cycle (3T)
6. Interrupt Acknowledge Cycle (6T or 12T)
7. Bus Idle Cycle

Opcode fetch Machine cycle:

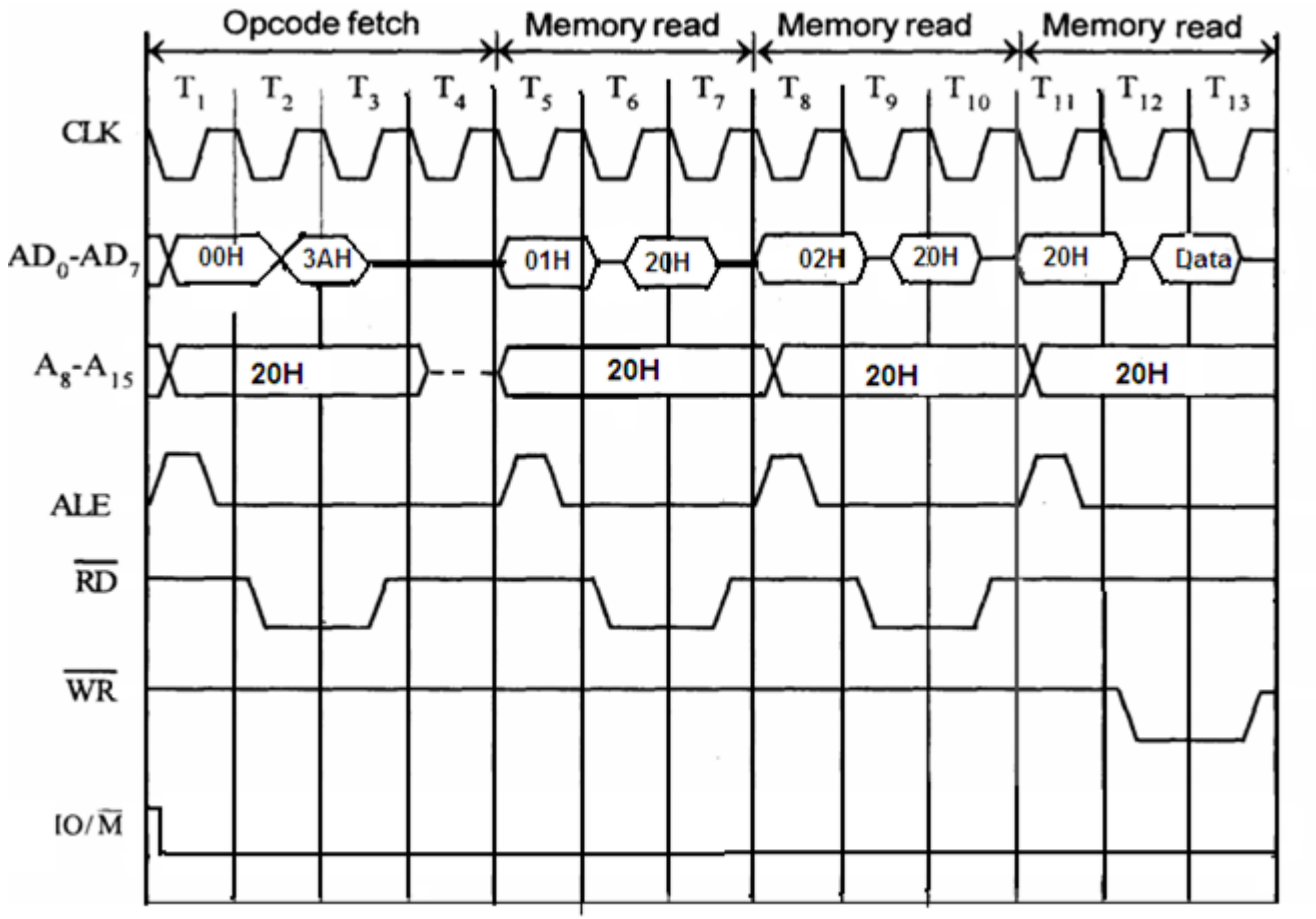
- The first operation in every instruction is the opcode fetch.
- The opcode fetch cycle is called the M_1 machine cycle and is usually for four T-states or clock cycles (certain instructions may also have 6T states in their opcode fetch machine cycle).
- During T_1-T_3 states the address is placed on the address bus and the opcode is returned on the data bus.
- The T_4-state is used to decode and execute the opcode. The next machine cycles (M_2, M3------) that follow depend upon what the instruction actually is.
- The timing diagram for execution of MVI A, 25 machine cycle is shown in **Fig** as shown in the timing diagram, in T_1 state, the 8085 places the contents of the program counter on the address bus.


Opcode fetch
Memory read
T1
T2
T3
T4
T5
T6
T7
CLK
AD0-AD7
00H
3E
01H
25H
A8-A15
80H
80H
ALE
RD
WR
IO/M

- The high order byte of the P.C (80) is placed on the A_{8}-A_{15} lines.
- The low-order byte of the P.C(00) is placed on the AD_{0}-AD_{7} line which stays only on only during T_1.
- So, the microprocessor activates the ALE (Address Latch Enable) pin which is used to latch the low-order byte of the address in external latch before it vanishes.
- During T_1 state, 8085 also sends status signals IO/ , S_1 and S_0. The IO/ signal specifies whether the operation is read or write. In opcode fetch machine cycle status signals are IO/ =0, S_1 =1 and S_0=0
- In T_2 state, the lower order address disappears from AD_{0}-AD_{7} lines and 8085 sends signal low to enable the addressed memory location.
- The memory device then places the contents of the addressed memory location on the data bus (AD_{0}-AD_{7})
- During T_3 state, the microprocessor loads the data from the data bus in its instruction register and raises to high which disables the memory device
- In T_4 state, the microprocessor decodes the opcode and based on the instruction it decides whether to T_0 state T_5 or to enter state $T_1$of the next machine cycle (M_2).
- All the one byte instructions which operate on 8-bit data like MOV A, B, ADDB, DCRC, RAL etc…..are executed T_4 state. One byte instructions which operate on 16-bit data are executed in T_5 and T_6 states.

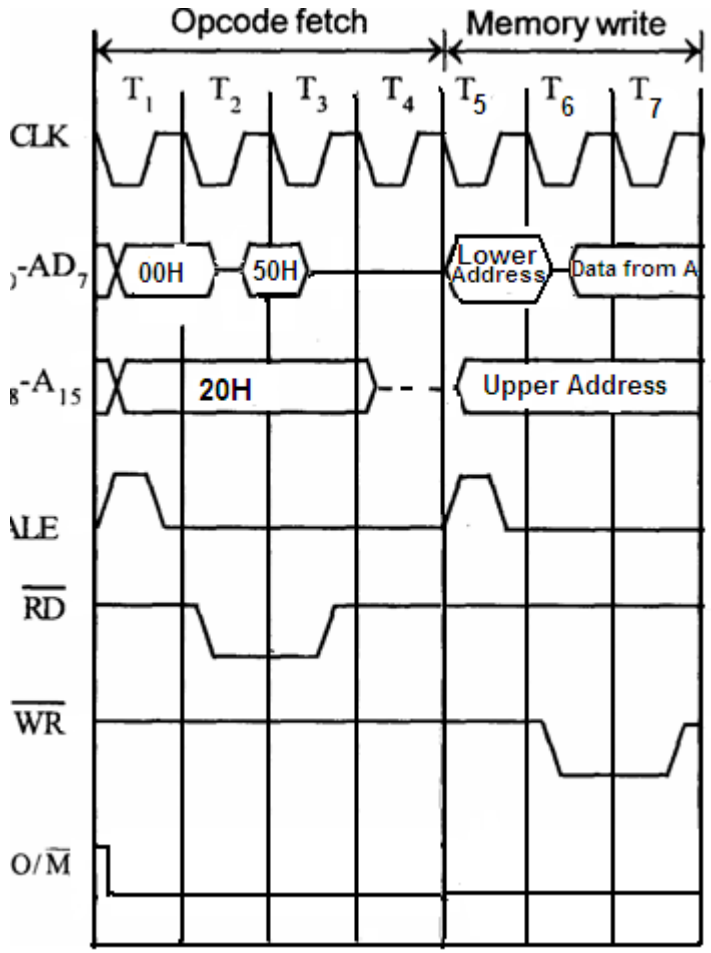
Memory Read cycle:

- Memory read machine cycle is a machine cycle during which memory is read.
- For example, the instruction LDA 8900H which is a 3-byte instruction has three memory read cycles immediately after the opcode fetch cycle.
- The first two cycles are to get the memory address, in two 8-bit groups (the low-order part of the address and then the high-order address).
- The third read cycle is needed to read the data located at the address previously retrieved. This data is then loaded into accumulator.
- The timing diagram for memory read cycle [For Ex: LDA 2020H] is shown in **Fig** As shown in the memory read timing diagram, after the opcode fetch cycle, the first two read cycles have the address going out over the address bus first for the low-order of the address (2001H) and then for the high-order of the address(2002H).
- In the third read cycle, the address of the instruction just read from memory (2020H) is sent back over the address bus in T_1 and then data from that memory location is returned over the data bus in T_2-T_3. IO/M goes low at the beginning of the opcode fetch cycle and remain low during the next three cycles.
- On the other hand goes low each time data on the data bus is to be read into the microprocessor.


Opcode fetch
Memory read
Memory read
Memory read
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13
CLK
AD0-AD7
00H
3AH
01H
20H
02H
20H
20H
Data
A8-A15
20H
20H
20H
20H
ALE
RD
WR
IO/M

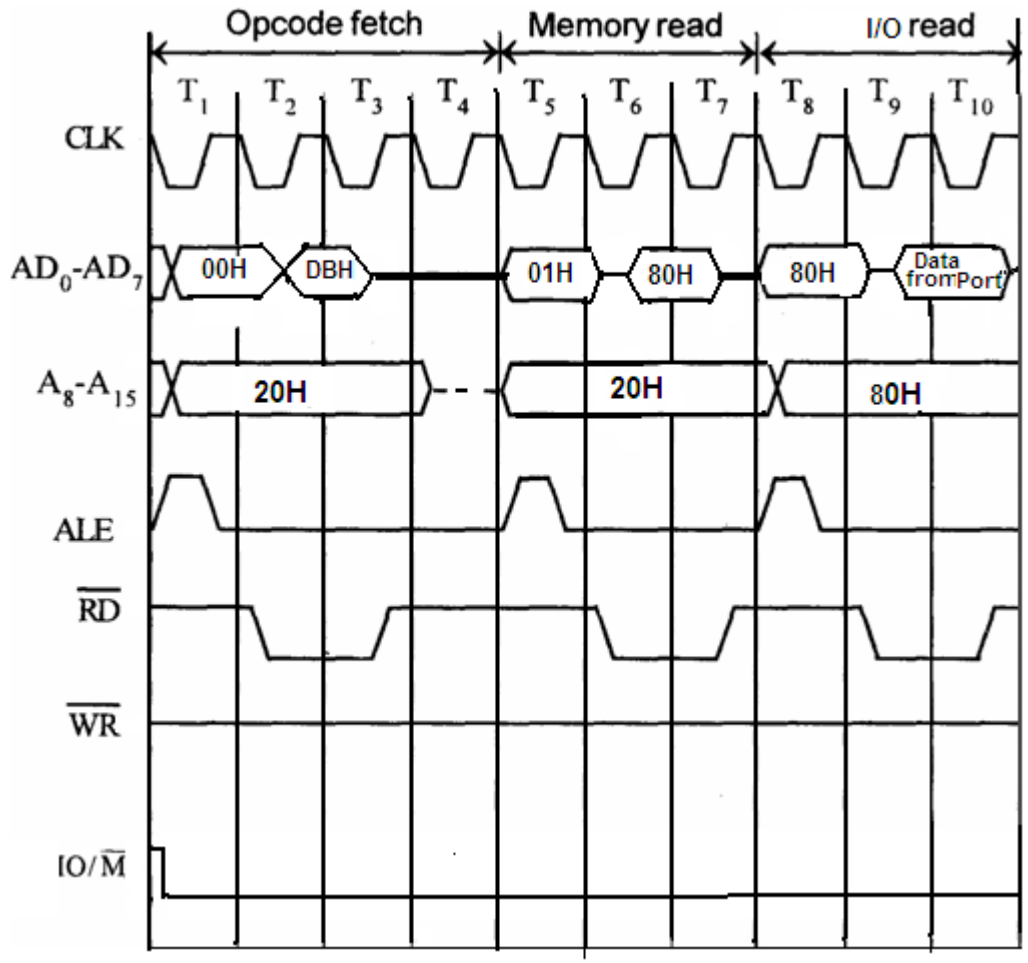
Memory Write cycle:

- This memory write cycle is used when the microprocessor needs to send data out from accumulator or specific register and then write into the memory.
- As an example let us consider the instruction MOV M, A (50H).
- This instruction requires two machine cycles-an opcode fetch machine cycle followed by one write cycle
- Because, after fetching the opcode, the instruction has to write the data in the accumulator out to memory at the address location in the H-L register.
- This operation requires 7-T states for opcode fetch and three –T states for the memory write.


Opcode fetch
Memory write
T1
T2
T3
T4
T5
T6
T7
CLK
-AD7
00H
50H
Lower Address
Data from A
-A15
20H
Upper Address
ALE
RD
WR
O/M

I/O Read cycle:

- This I/O read cycle occurs when the microprocessor executes IN instruction and during the I/O read cycle, data is read in from an I/O device. In the case of IN PORT, there are three machine cycles.
- The opcode fetch cycle, a memory read cycle and an I/O read cycle.
- The three machine cycles combinedly taken 10-states.
- The **Fig** Shows the timing diagram of the instruction IN 80H, Here 80H is the port address of the device being read.
- The opcode fetch cycle shows the address of the instruction (2000H) going out over the address bus and the opcode (DBH) for the IN instruction returning on the data bus.
- The memory read cycle (M_2) displays the address of the second byte of the instruction (8001H) going out over the address bus and the port address (80H) returning on the data bus.
- During the I/O read cycle, the port address of the device being read is sent over the address bus and the lower 8-bits carry the same 8-bit port address and the data from the input device is returned on the data bus during T2-T3.


Opcode fetch
Memory read
I/O read
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10
CLK
AD0-AD7
00H
DBH
01H
80H
80H
Data from Port
A8-A15
20H
20H
80H
ALE
RD
WR
IO/M