



पत्र संख्या :-

Direct Memory Access (DMA):

मिति :-

च.नं. :-

Direct memory access (DMA) is a process for data transfer between memory and I/O, controlled by an external circuit called DMA controller, without involvement of CPU.

Most of the data that is input or output from computer is processed by the CPU, but some data does not require processing, or can be processed by another device. In this situation, DMA can save processing time and is a more efficient way to move data from the computer's memory to other devices.

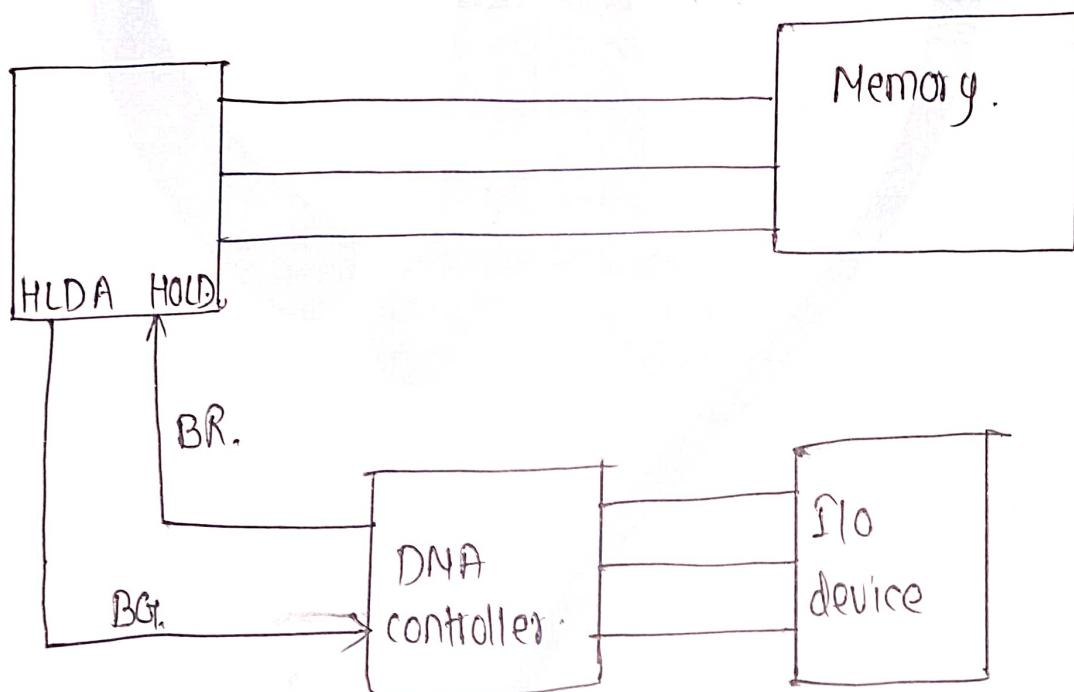
Basic DMA operation with required timing diagram.

fig: DMA.

8085 microprocessor HOLD and HLDA which are used for DMA operation. first DMA controller sends a request by making Bus request (BR) control line high. After receiving HLDA through bus grant (BG) pin of DMA controller, the DMA controller takes control over system bus and transfers data directly between memory and I/O without involvement of CPU.

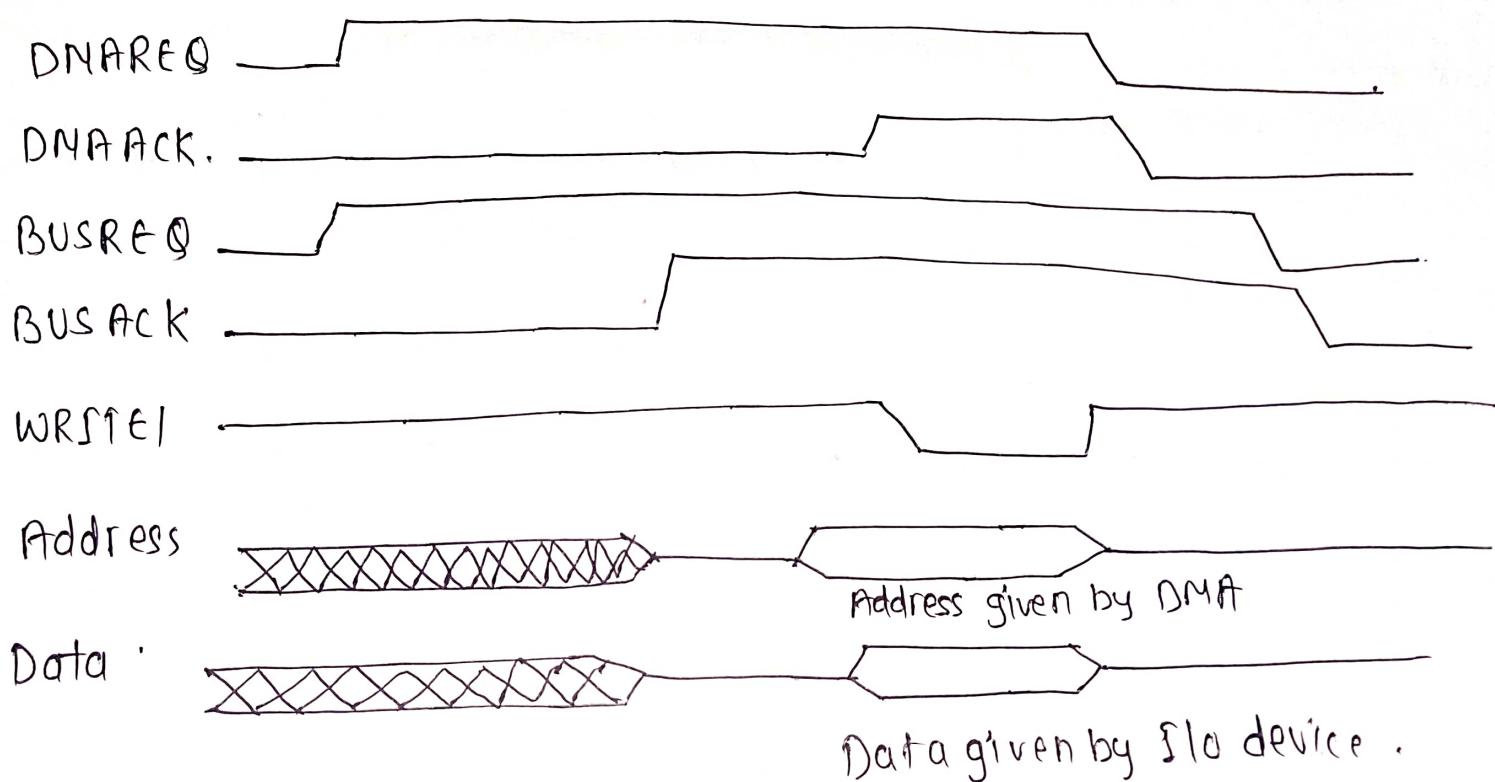


fig: DMA Timing diagram

internal.

पत्र संख्या :- Draw the architecture of 8237

च.नं :- DMAc along with a timing diagram illustrating the process
of DMA transfers. मिति :-

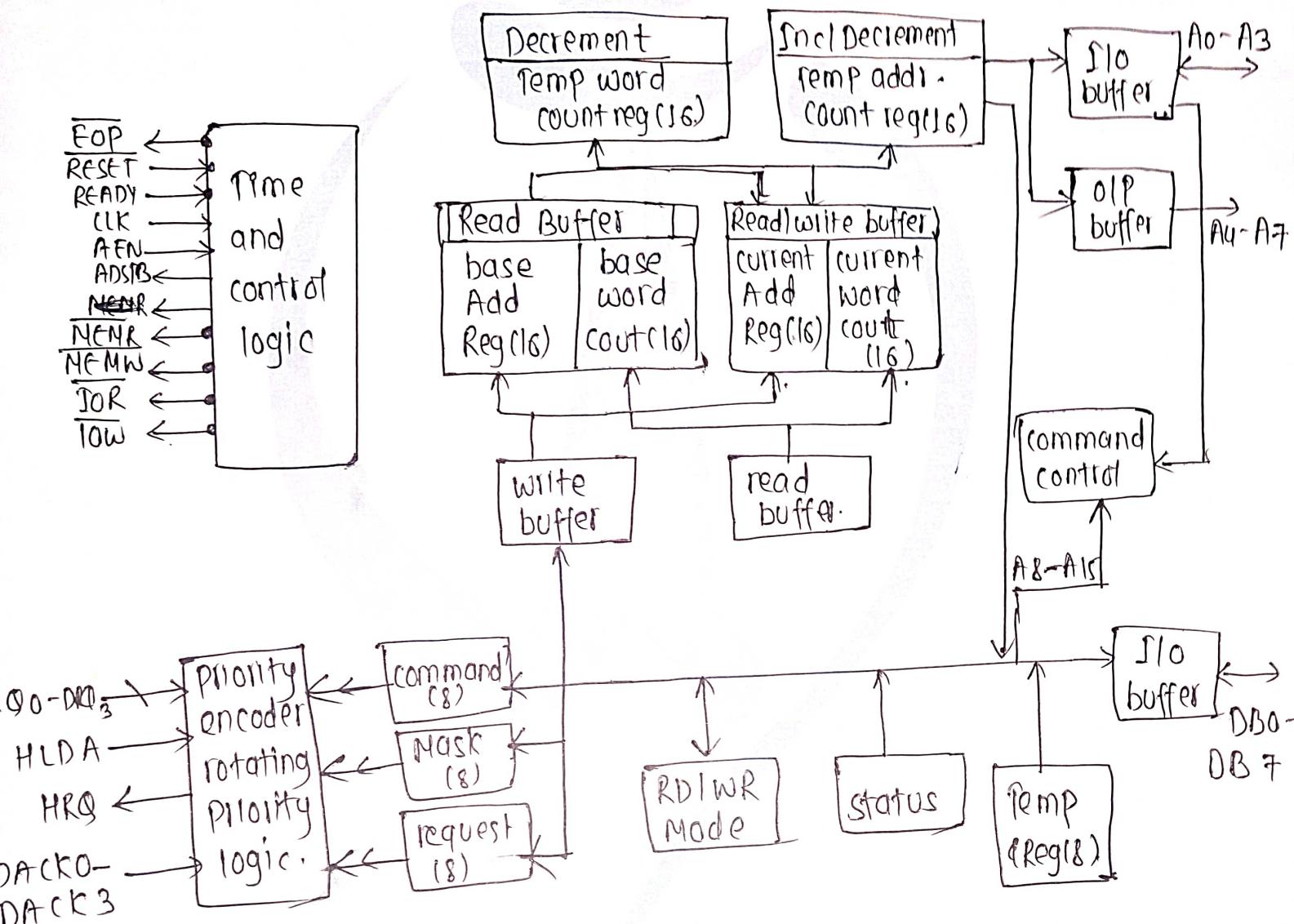


fig: Internal architecture of the 8237 DMAc

<u>DOR</u>	1	40	A7
<u>DOW</u>	2	39	A6
<u>NENR</u>	3	38	A5
<u>NENW</u>	4	37	A4
NC	5	36	<u>TOP</u>
READY	6	35	A3
HLDA	7	34	A2
ADSTB	8	33	A1
AEN	9	32	A0
HREQ	10	31	VCC
<u>CS</u>	11	30	DB0
CLK	12	29	DB1
RESET	13	28	DB2
DACK2	14	27	DB3
DACK3	15	26	DB4
DREQ3	16	25	DACK0
DREQ2	17	24	DACK1
DREQ1	18	23	DB5
DREQ0	19	22	DB6
VSS	20	21	DB7

fig: pin diagram of DNA



पत्र संख्या :- DMA and its working its the time मिति :-

च.नं :- to analyze modes of DMA Transfer:

- During the DMA transfer CPU can perform only those operation in which it doesn't require the access of system Bus which means mostly CPU will be ~~be~~ in blocked state.
- for how much time CPU remains in the blocked state or we can say for how much time CPU will give the control of DMAC of system buses will actually depend upon the following modes of DMA transfer and after that CPU will take back control of system buses from DMAC.

Mode-1: Burst Mode :

- In this mode Burst of data is transferred before CPU takes control of the buses back from DMAC.
- This is quickest mode of DMA transfer since at once a huge amount of data is being transferred.
- Since at once only the huge amount of data is being transferred so time will be solved in huge amount.

Mode-2: cycle stealing mode :

- So device will take some time to prepare data and within that time CPU keeps the control of the buses.
- Once the data or the word is ready CPU give back control of system buses to DMAC for 1-cycle in which the prepared word is transferred to memory.
- As compared to Burst mode this mode is little bit slowest since it requires little bit of time which is actually consumed by So device while preparing the data.

नेपाल दूरसंचार कर्पोरेशन लिमिटेडको

पश्चिमाञ्चल क्षेत्रीय निर्देशनालय, भैरहवा

पडसरी-१, कटैया, खुन्सा, रुपन्देही,

(.....) शाखा।

गामगाढ़ा गाइडको

निर्देशक :- (०७१) ४२९९२७

लेखा प्रमुख :- ४२९४५४

प्रशासन शाखा :- ४२९३९९ / ४२९४९९

फैक्टरी : ४२९४४८ / ४२९४९६

mode 3 : Interleaving mode :

- whenever CPU does not require the system buses then only control of buses will be given to DMA controller.
- In this mode, CPU will not be blocked due to DMA at all.
- This is the slowest mode of DMA transfer since DMA controller has to wait might be for so long time to just even get the access of system buses from the CPU itself.
- Hence due to which less amount of data will be transferred.

④ Diff between vectored and non-vectored interrupt .

- vectored interrupt : In this type of interrupt, processor knows the address of interrupt. In other word processor knows the address of interrupt service routine.

Example: RST 7·5, RST 6·5, RST 5·5, TRAP

- Non-vectored Interrupt : In this type of interrupt, processor cannot know the address of interrupt. It should give externally. In the device will have to send the address of interrupt service routine to processor for performing interrupt .

Example: INTR



पत्र संख्या :- Explain how interrupt controller
मिति :-
च.नं. :- (8259) can be used to handle interrupts .

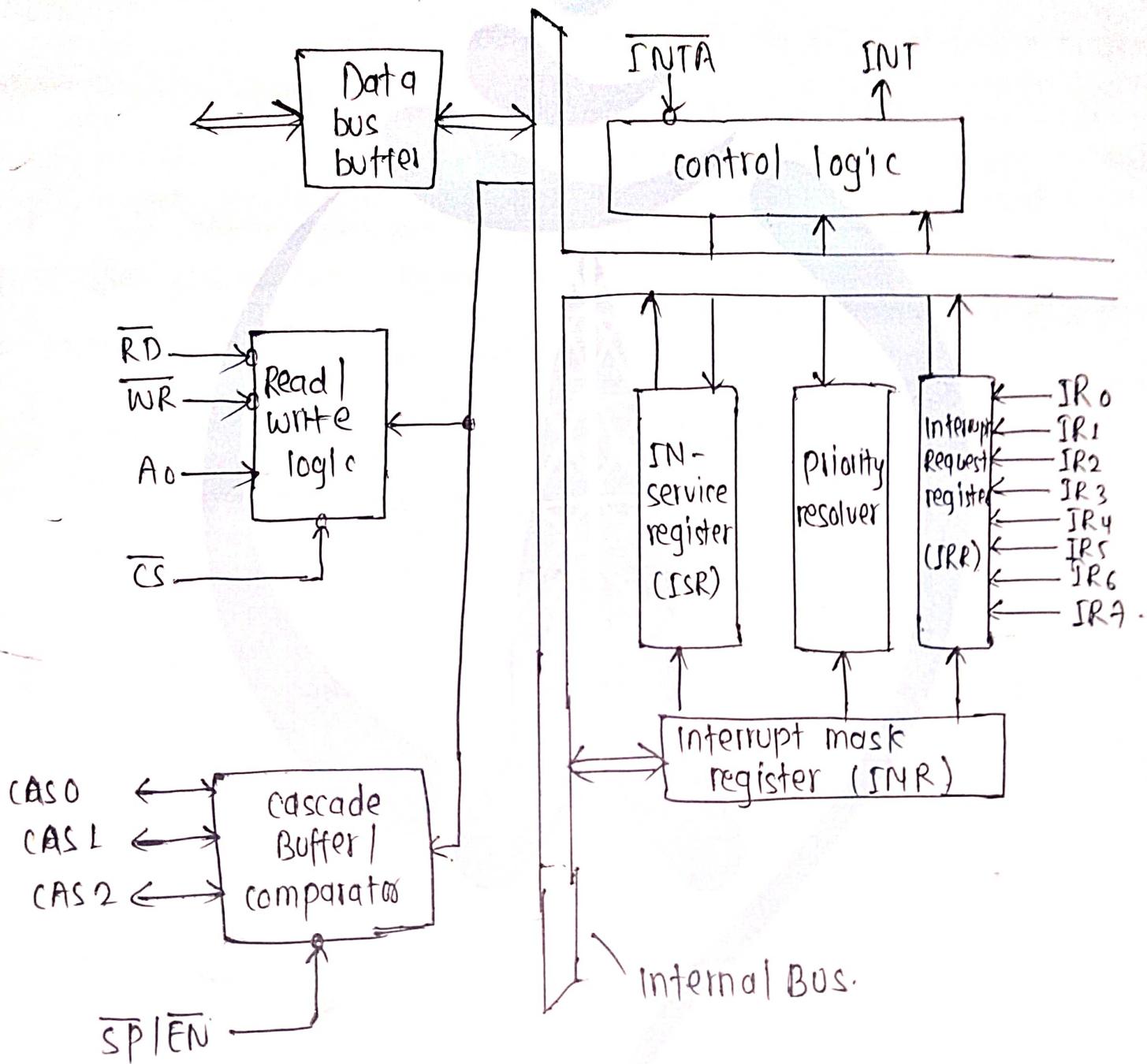


fig: block diagram of 8259A PDC

The following steps take place during the operation of 8259 A :

- One or more interrupt request lines go high requesting the service
- The 8259A resolves the priorities and sends an INT signal to the MP.
- The MP acknowledges the interrupt by sending INTA.
- After a INTA has been received (the opcode for the call instruction (CDH) is placed on the data bus)
- Because of the call instruction, the MP sends two or more INTA signals.
- At the first INTA, the 8259A places the low order 8-bit address on the data bus and at the second INTA, it places the high order 8-bit address of the interrupt vector. This completes the 8 byte call instruction.
- The program sequence of the MP is transferred to the memory location specified by the CALL instruction.

Q) Define maskable and non-maskable interrupt. Explain the role of TRAP in 8085 microprocessor.

→ Maskable interrupt are those which can be disabled or ignored by the microprocessor. These interrupt are either edge-triggered or level-triggered, so they can be disabled. ~~INT~~, RST 7·5, RST 6·5, RST 5·5 are maskable interrupts in 8085 microprocessor.

Non-maskable interrupt are those which cannot be disabled or ignored by microprocessor. TRAP is a non-maskable interrupt.

TRAP is a non-maskable restart interrupt and has the highest priority among all 8085 interrupt. TRAP is edge and level triggered i.e. the TRAP must go high and remain high until it is acknowledged.

In sudden power failure, it executes a ISR and send the data from main memory to backup memory.

It transfers the control to 0024H. When this interrupt is triggered the program control is transferred to the location 0024H without any external Hardware or the interrupt enable instruction. It is generally used for such critical events as power failure and emergency shutoff. The execution of the ~~RE~~ instruction enables/disables the interrupt according to the bit pattern of the accumulator.

② Why interrupt is required? Draw the block diagram of interrupt handler and explain it.

→ Interrupt is a mechanism by which an I/O or an instruction can suspend the normal execution of processor and get itself serviced. It is a signal sent by an external device to the processor, to perform a particular task or work. Interrupts are used for the data transfer between the peripheral and the microprocessor. When peripheral is ready for data transfer it interrupts the processor by sending an appropriate signal to interrupt pin of the processor. If the processor accepts the interrupt then the processor signal suspends its current activity and executes an interrupt service subroutine to complete the data transfer b/w the peripheral and the processor.

What is an interrupt? Explain software interrupt in details.

→ Interrupt is a mechanism by which an I/O or an instruction can suspend the normal execution of processor and get itself serviced. In response of interrupt, the processor stops what it is currently doing and executes a service routine. The interrupt is initiated by an external device and is asynchronous.

Software interrupt is a special call instruction that behaves like an interrupt rather than a subroutine call. It can be used by the programmer to initiate an interrupt procedure at any desired point in the program. The most common use of software interrupt is associated with a supervisor call instruction. This instruction provides means for switching from a CPU user mode to the supervisor mode. If 8085 the instruction like RST0, RST1, RST2, RST3--- etc causes a software interrupt.

Explain briefly on keyboard and display controller:

Keyboard and display controller is designed by Intel..

It supports 64 contact key matrix with 2 mole keys

"CONTROL" and "SHIFT". It provides three operating modes. They are:-

- Scanned keyboard mode
- Scanned sensor matrix mode

- ~~Strobed~~ Strobed Input mode.

It has inbuilt debounce key. It provides 16 bytes display RAM to display 16 digits and interfacing

16 digits. It provides 2 output modes. They are:

- left entry mode
- right entry mode.

The interrupt output of keyboard and display controller can be used to tell CPU that the key press is detected, this eliminates the need of software polling .