PART-A

1

SYNCHRONOUS CIRCUIT	ASYNCHRONOUS CIRCUIT
It is a system whose behaviour depends on the input signals at discrete instants of time	It is a system whose behaviour depends on its input signals at any instant of time.
The storage elements are affected by a common clock signal.	The storage elements are not affected by common clock signal.

2 ELIMINATION OF HAZARDS:-

The remedy for eliminating a hazard is to enclose the two minterms with another product term that overlaps both groupings.

3. ESSENTIAL HAZARD IN ASYNCHRONOUS:-

The type of hazards that may occur in asynchronous sequential circuits are called essential hazard. It is caused by unequal delays propagation delays and occurs at output.

4 RACE CONDITION IN ASYNCHRONOUS:

A race condition occurs in an asynchronous sequential circuit when there is more than 1 bit change ie when two or more binary state variable change value in response to a change in an input variable

5 WORD SIZE OF INTEL

The width of the internal bus determines the word size of the microprocessor for example If the internal bus of microprocessor has n lines then it is called as an n bit microprocessor. Hence an 8-bit microprocessor like 8085 can handle 8 bits of data at a time.

6. PROGRAM COUNTER:-

It keeps track of the address of next instruction byte to be fetched from memory. After fetching an instruction byte from memory the processor increments the program counter by one.

7.

AUXILIARY CARRY FLAG	CARRY FLAG
If there is a carry out of bit D_3 of an arithmetic operation it is set otherwise reset.	If the arithmetic operation results in a carry or borrow out of D_7 then this flag is set otherwise reset.

8. ROLE OF DMA CONTROLLER:-

HOLD and HLDA signals are used for direct Access memory Mode of data transfer.

When DMA is required DMA controller sends a HOLD request to 8085. Then processor issuses a HOLD acknowledge (HLDA) signal to the DMA controller and

after reception of HLDA the bus control is totally taken over by the DMA controller.

9 ADD ACC ← A+B

ADD Accumulator ← 45H + 7EH.

10. ROLE OF ADDRESS LATCH ENABLE:

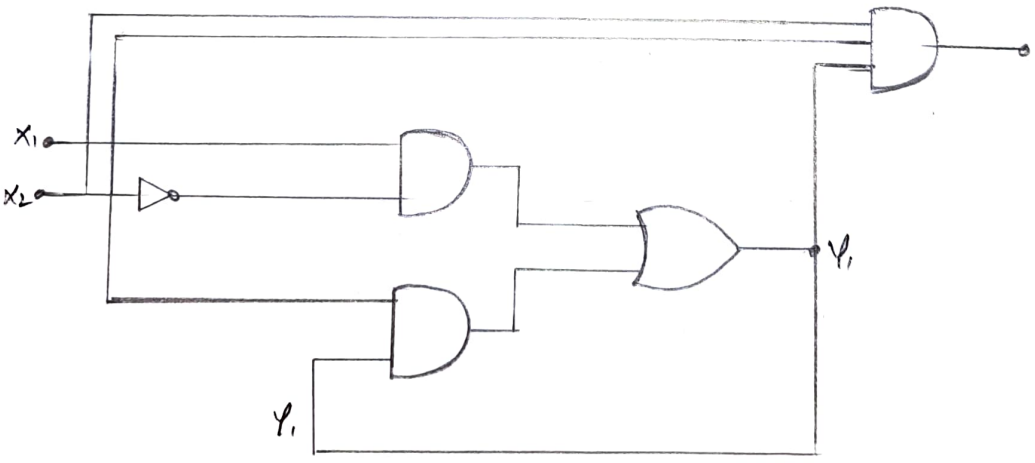
* It is an active high output signal used to demultiplex the time multiplexed lower order Address bus/ data by (AD_7 - AD_0). The ALE never gets tristated.

* If ALE is high (ALE = 1) then the time multiplexed bus (AD_7 - AD_0) carries lower order Address (A_7 - A_0).

* If ALE is low (ALE = 0) then the time multiplexed bus (AD_7 - AD_0) carries data (D_7 - D_0).

PART - B

11). a)



ANALYSIS PROCEDURE OF ASYNCHRONOUS SEQUENTIAL CIRCUIT:

Determine the feedback loops in the circuit.

Designate it as y_i and its input as $y_i = 1, 2, \ldots k$

Derive the boolean function of Y and the output as a function of y and external input.

Plot each Y and the output function in a map using y variables for rows and external inputs for columns.

Combine all maps to one table i.e transition table $Y = Y_1 . Y_2$.

Circle those values of Y in each square that all equal to value of $Y = Y_1, Y_2, \ldots Y_k$. Determine the stable and unstable states.

Derive stable table.

Derive Flow table

i). Boolean Function of Y and output secondary

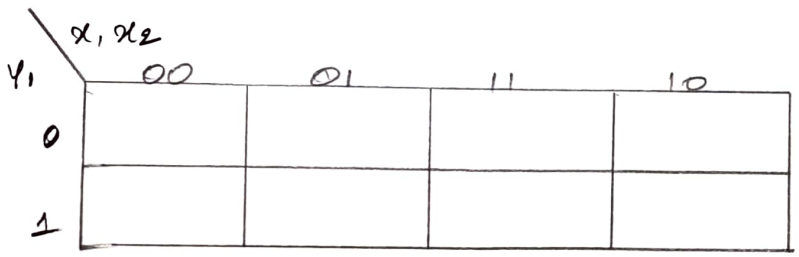
Variables : y_1

Excitation Variables : Y_1

Input : x_1, x_2

Then the Boolean function $Y_1 = x_1 . x_2 + \overline{x_2} . y_1$

ii). k-Map for Y_1



$$Y_1 = x_1 . x_2 + \overline{x_2} . y_1$$

iii) Transition Table.

It is similar to state table. It shows the values of next state inside each square.

Y_1 \ x_1x_2	00	01	11	10
0	(0)	(0)	1	(0)
1	1	(0)	1	1

STATE (STABLE): Present states and next states are the same.

STABLE STATES: 000, 001, 010, 100, 110, 111

UNSTABLE STATE: 011, 101

iv). STATE TABLE:

The table which represents the relationship between present states and next states is called state table.

PRESENT STATE	NEXT STATE			
Y_1	00	01	11	10
0	0	0	1	0
1	1	0	1	1

V). FLOW TABLE

Assigning letters to binary values

0 = a , b = 1

Y_1 \ x_1x_2	00	01	11	10
a	(a)	(a)	b	(a)
b	(b)	a	(b)	(b)

ii) DESIGN PROCEDURE OF ASYNCHRONOUS SEQUENTIAL CIRCUITS

Draw the state diagram for the given problem

Derive primitive flow table.

State reduction using Implication table.

Determine minimal compatible pairs using merger graph.

State assignment for primitive flow table.

Derive reduced primitive flow table.

Assign binary values for reduced states.

Derive transition table.

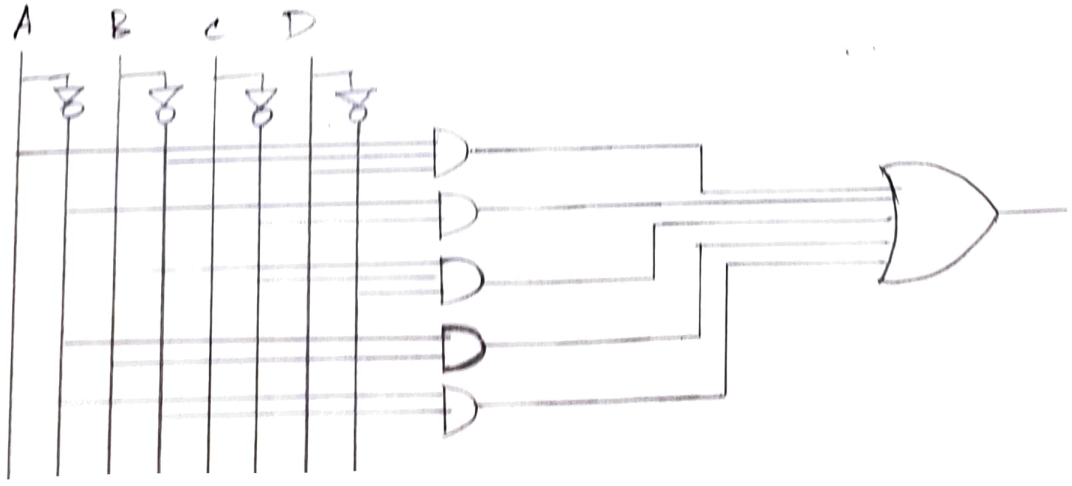
Obtain logical expression for next state and output using k-map.

Draw logic diagram.

iii) $F(A,B,C,D) = \sum m(0,2,6,7,8,10,12)$

AB \ CD	00	01	11	10
A'B'	1			1
A'B			1	1
AB	1			
AB'	1			1

$AB'D + A'B'C' + BC'D' + B'C'D + A'B + A'B'$



12 i) Boolean Function Y and output

Secondary variables : y_1, y_2

Excitation variables : Y_1, Y_2

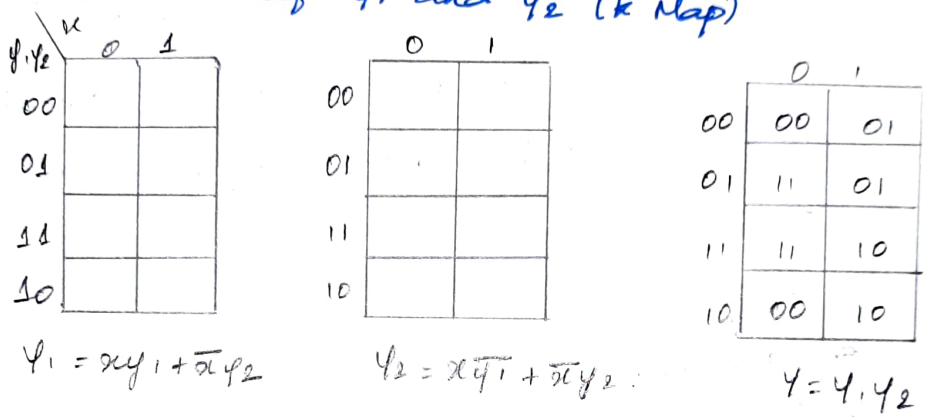
Input x

The Boolean Function of Y_1 and Y_2 are

$$Y_1 = xy_1 + \bar{x}y_2$$

$$Y_2 = x\bar{y}_1 + \bar{x}y_2$$

Boolean function of Y_1 and Y_2 (k Map)



ii) Transition Table:

For a state to be stable, present states (y_1, y_2) should be same as next states (Y_1, Y_2).

STABLE STATES:- 000, 011, 010, 101

UNSTABLE STATES : 001, 010, 111, 100

iii) STATE TABLE

The relationship between present states and next state is called state table.

PRESENT STATE		NEXT STATE			
		x=0		x=1	
Y_1	Y_2				
0	0	0	0	0	1
0	1	1	1	0	1
1	1	1	1	1	0
1	0	0	0	1	0

(iv). Flow Tables:

00 → a 01 → b 11 → c 10 → d

Y_1Y_2 \ x	0	1
a	(a)	b
b	c	(b)
c	(c)	d
d	a	(d)

(v). Hazard

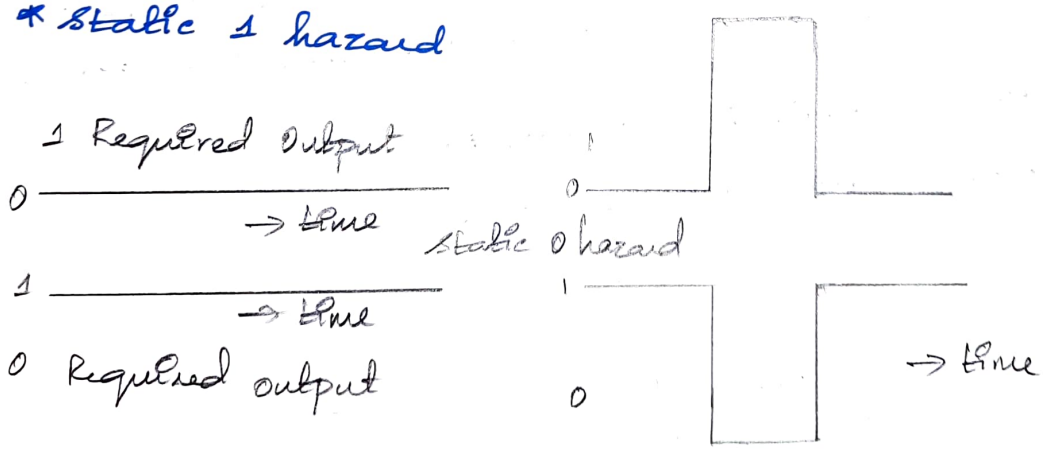
It is a phenomenon that causes malfunction in the circuit. It is an unwanted switching transients that may appear at the output of a circuit because different paths exhibit different propagation delays. It causes false output.

TYPES OF HAZARDS:

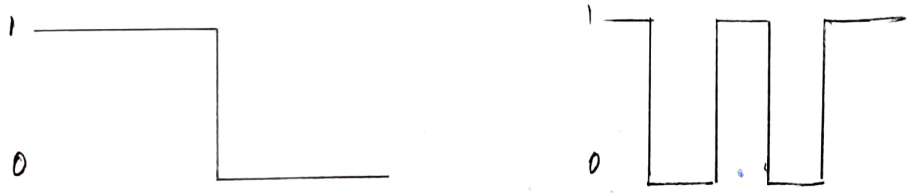
* Static hazard
* Dynamic hazard

STATIC HAZARD:

* Static 0 hazard
* Static 1 hazard



Static 1 hazard.



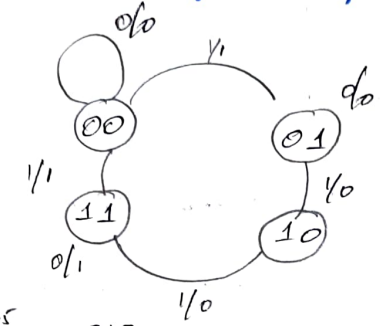
Required Output Dynamic Hazard

iii) MEALY MODEL:-

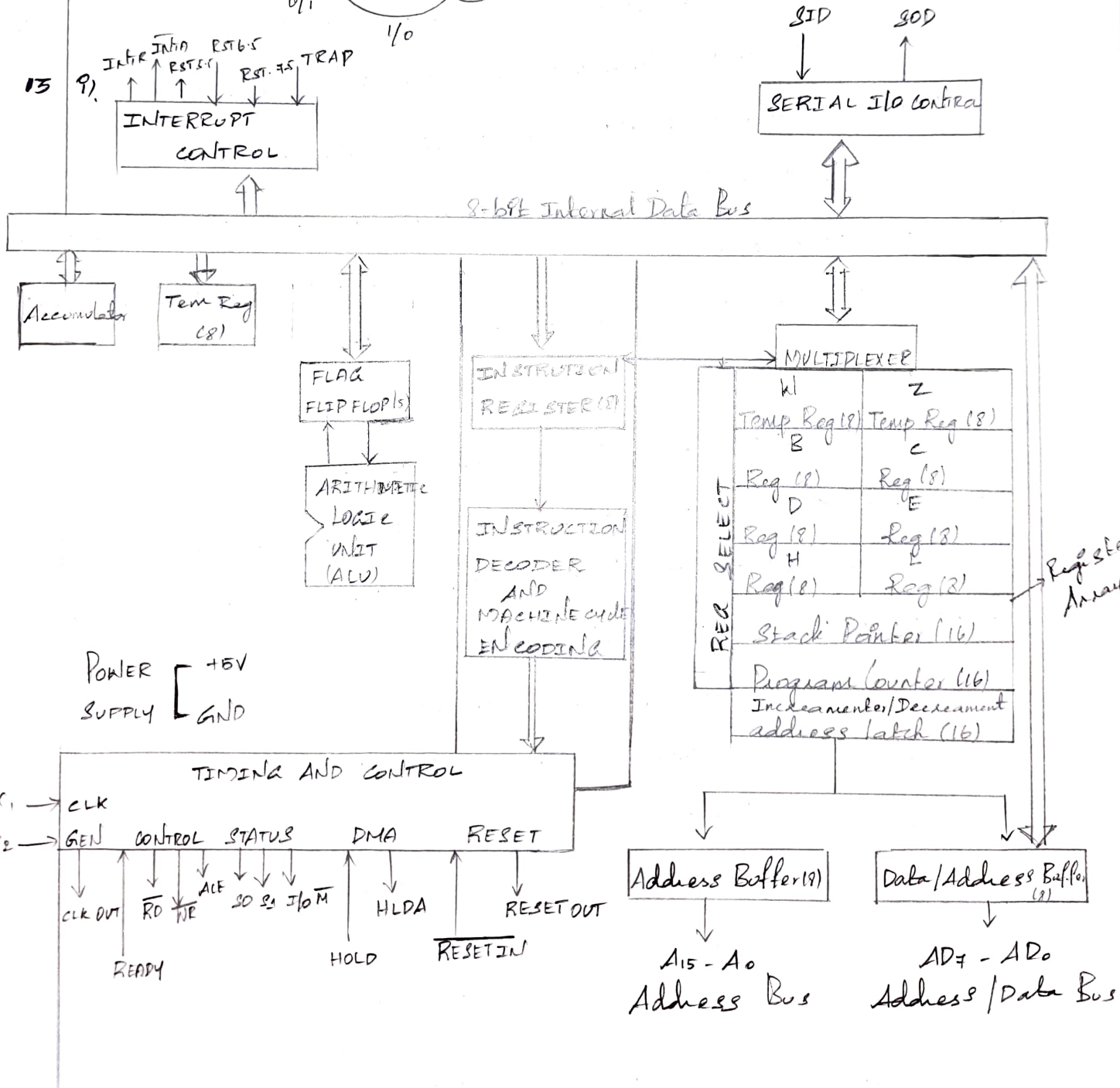
The output depends on the present state of the flip flop as well as present inputs

It required less number of states for implementing the function.

Input changes may affect the output of the circuit.



13 9)



(ii). STACK POINTER

It is a 16-bit register which points the memory address of the top of the 'stack'. It is simply an area of random access memory (RAM) defined by the user / programmer. The stack operation is LIFO Manner. Stack memory is used to store (push) and retrieve (pop) the intermediate data or return address. In 8085 we have a descending stack. Whenever a data is pushed into the stack the stack pointer gets decreamented and whenever a data is popped out from stack, the stack pointer gets increamented. The program area should not get overlap. Hence it is preferred to store the program at the initial address and assign the stack memory at the end address.

(iii) Register Pairs in 8085:

It is used to store data during program execution for processing the data. There are 6 general purpose registers in 8085 microprocessor. B, C, D, E, H and L registers.

To register / store 16-bit data/address in registers the GPRS are paired together as register pairs.

REGISTER PAIRS	SYSTEM REFERENCE	REGISTER REFERENCE
BC	B	B and C
DE	D	D and E
HL	H	H and L (has memory reference M)

14. 9) WORD FORMAT OF FLAG REGISTER:

It is an 8 bit register used to indicate the status of the result. There are 5 flag bits sign(s), zero(z), auxillary carry(Ac), parity(P) and carry(CY). Each of the 5 flags is a 1-bit flip-flops.

S	Z	X	Ac	X	P	X	CY
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Sign(s) flag- If the MSB of the result of an arithmetic and logical operation is 1, this flag is set otherwise it is reset.

Zero(z) flag If the result of an arithmetic and logical operation is 0, this flag is set otherwise reset.

Auxilliary carry(Ac) flag: If there is a carry out of bit D_3 of an arithmetic operation it is set otherwise reset

carry(cy) flag: If arithmetic operation results in a carry or borrows out of bit D_7, then the flag is set, otherwise reset.

Parity flag:- The flag is set when the result of an Arithmetic and logical operation contains an even parity number of 1's and is reset otherwise.

9). CONTROL AND SIGNAL OF 8085:

These signals are used to control the read and write operation of the CPU with externally connected memory IO devices.

ALE (OUTPUT SIGNAL)

Address Latch Enable is an active high output signal used to demultiplex the time multiplexed lower order Address bus/data bus (AD_7-AD_0). The ALE never gets tristated. If ALE is 1, then time multiplexed (AD_7-AD_0) carries lower order Address (A_7-A_0). If ALE is 0. then time multiplexed (AD_7 - AD_0) carries data.

$\overline{RD}$ / $\overline{WR}$

Read and $\overline{WR}$ are read and write signals of 8085 microprocessor respectively. Both are active low output signals which are used for performing the read and write operations by the processor. $\overline{RD}$ signal is used to read data from memory. $\overline{WR}$ signal is used to write data into memory.

READY:

It is an active high input signal of the processor It is used to synchronise the I/o or memory with the processor. Without the READY signal of the processor I/o or memory devices states communicating then data loss may happen. The interfacing of 8085 with an I/o devices using control signal.

iv) HARDWARE INTERRUPTS:

* RST 5.5
* RST 6.5
* RST 7.5
* TRAP (High Priority Interrupt)
* INTR (Low Priority Interrupt)

SOFTWARE INTERRUPTS:-

* RST 1
* RST 2
* RST 3
* RST 4
* RST 5
* RST 6
* RST 7