HD74LS78A

Dual J-K Flip-Flops
(with Preset, Common Clear, and Common Clock)

REJ03D0419–0300
Rev.3.00
Jul.22.2005

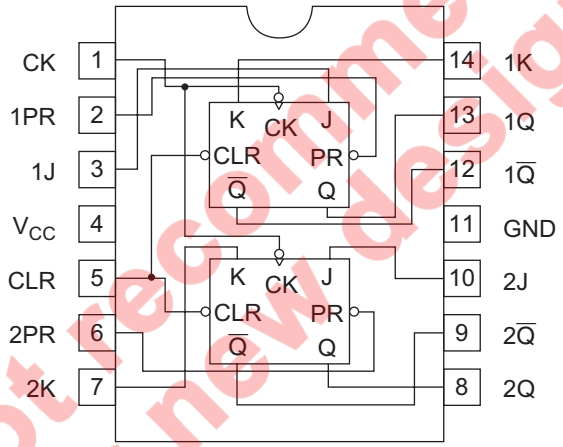
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS78AFPEL	SOP-14 pin (JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



(Top view)

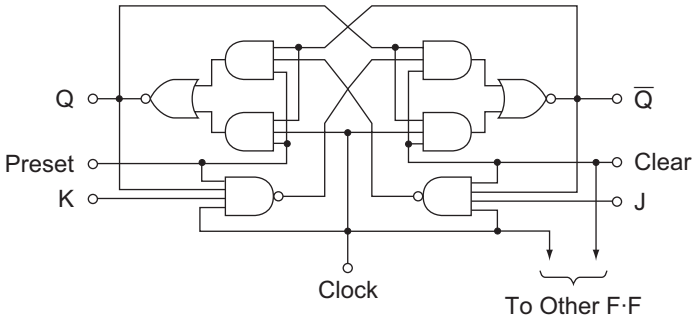
Function Table

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$

Notes: H; high level, L; low level, X; irrelevant, ↓; transition from high to low level,
Q_0; level of Q before the indicated steady-state input conditions were established.
$\overline{Q}_0$; complement of $\overline{Q}_0$ or level of Q before the indicated steady-state input conditions were established.
Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Block Diagram (1/2)



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	–400	µA
		I_{OL}	—	—	8	mA
Operating temperature		T_{opr}	–20	25	75	°C
Clock frequency		f_{clock}	0	—	30	MHz
Pulse width	Clock High	t_w	20	—	—	ns
	Clear Preset Low	t_w	25	—	—	
Setup time	“H” Data	t_{su}	20↓	—	—	ns
	“L” Data	t_{su}	20↓	—	—	
Hold time		t_h	0↓	—	—	ns

Electrical Characteristics

(Ta = –20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition
Input voltage		V_{IH}	2.0	—	—	V	
		V_{IL}	—	—	0.8	V	
Output voltage		V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2.7 V, V_{IL} = 0.8 V, I_{OH} = –400 µA
		V_{OL}	—	—	0.5	V	I_{OL} = 8 mA, V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V
			—	—	0.4		I_{OL} = 4 mA
Input current	J, K	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V, V_I = 2.7 V
	Clear		—	—	120		
	Preset		—	—	60		
	Clock		—	—	160		
	J, K	I_{IL}**	—	—	–0.4	mA	V_{CC} = 5.25 V, V_I = 0.4 V
	Clear		—	—	–1.6		
	Preset		—	—	–0.8		
	Clock		—	—	–1.6		
	J, K	I_I	—	—	0.1	mA	V_{CC} = 5.25 V, V_I = 7 V
	Clear		—	—	0.6		
	Preset		—	—	0.3		
	Clock		—	—	0.8		
Short-circuit output current		I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V
Supply current***		I_{CC}	—	4	6	mA	V_{CC} = 5.25 V
Input clamp voltage		V_{IK}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA

Notes: * V_{CC} = 5 V, Ta = 25°C

** I_{IL} should not be measured when preset and clear inputs are low at same time.

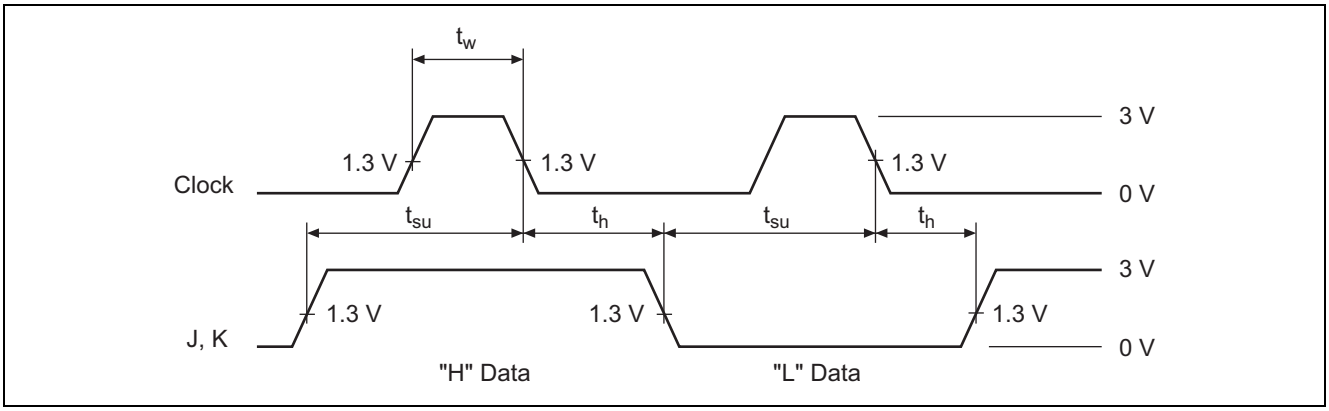
*** With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn.
At the time of measurement, the clock input is grounded.

Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f_{max}	Clear, Preset, Clock	Q, $\overline{Q}$	30	45		MHz	C_L = 15 pF, R_L = 2 kΩ
Propagation delay time	t_{PLH}			—	15	20	ns	
	t_{PHL}			—	15	20	ns	

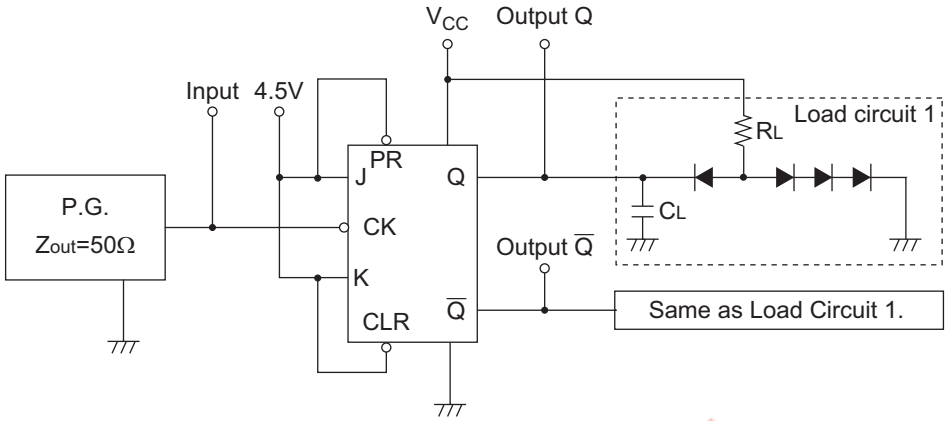
Timing Definition



Testing Method

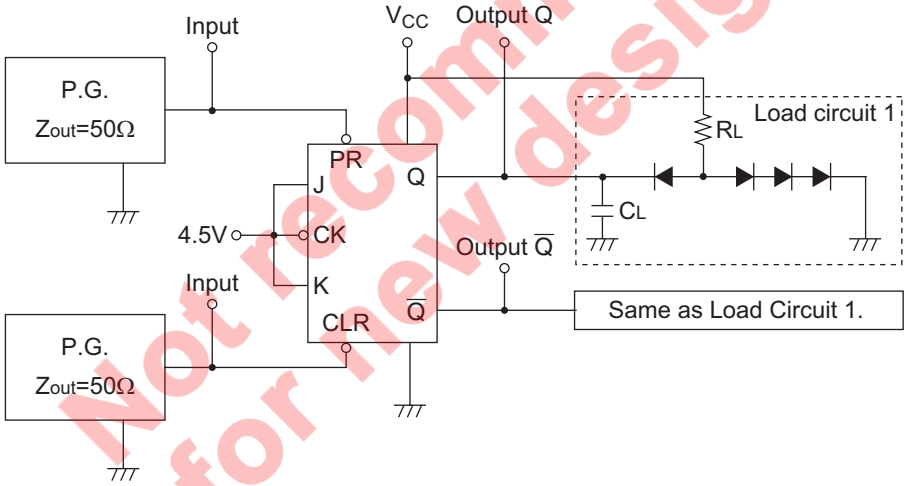
Test Circuit

1. f_{max}, t_{PLH}, t_{PHL}, (Clock→Q, $\overline{Q}$)



Notes:
1. Test is put into the each flip-flop.
2. C_L includes probe and jig capacitance.
3. All diodes are 1S2074(H).

2. t_{PHL}, t_{PLH} (Clear, Preset→ Q, $\overline{Q}$)



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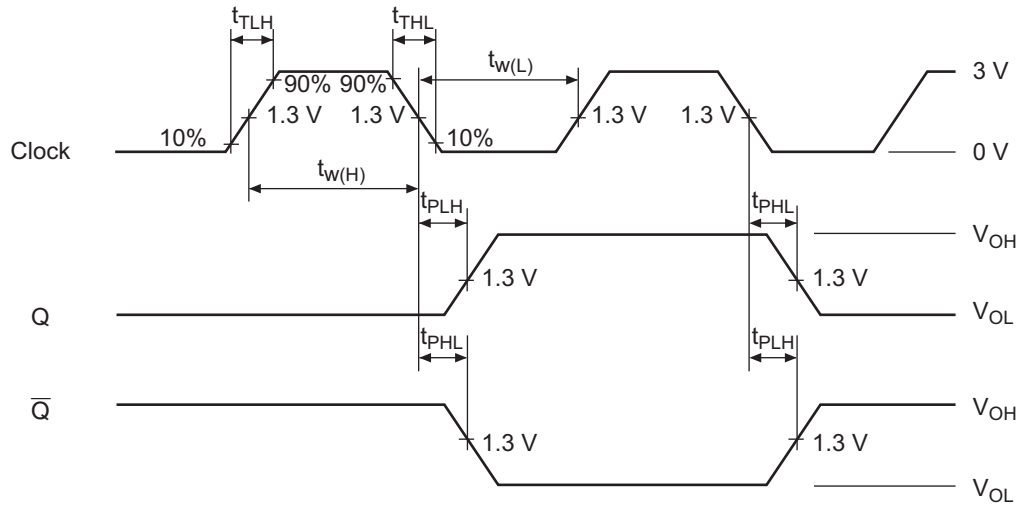
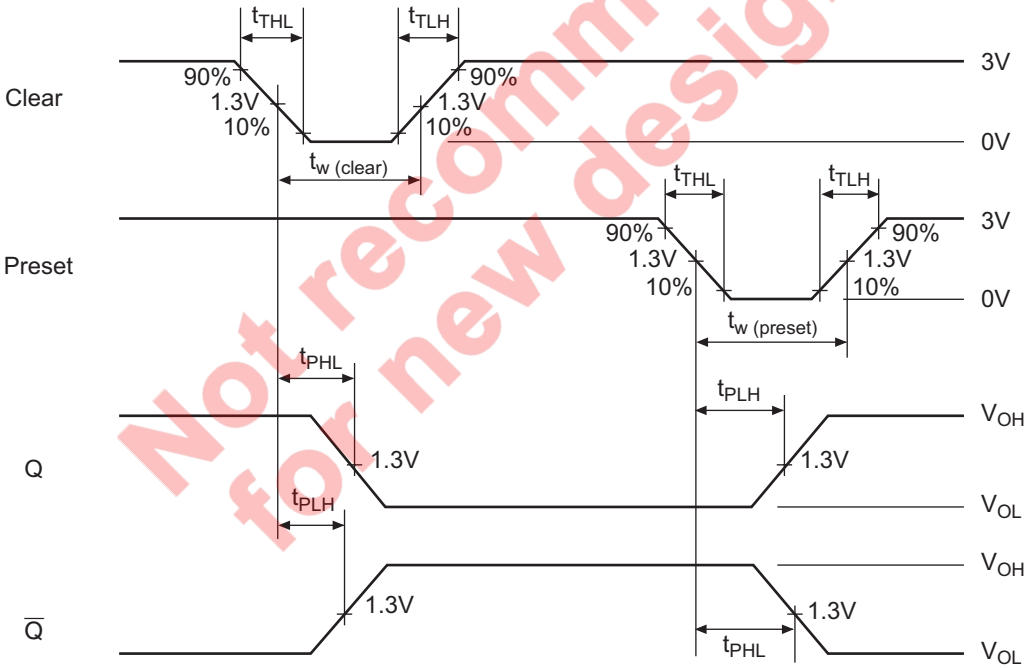
Waveforms 1



Note: Clock input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle = 50% and for fmax., $t_{TLH} = t_{THL} \leq 2.5$ ns

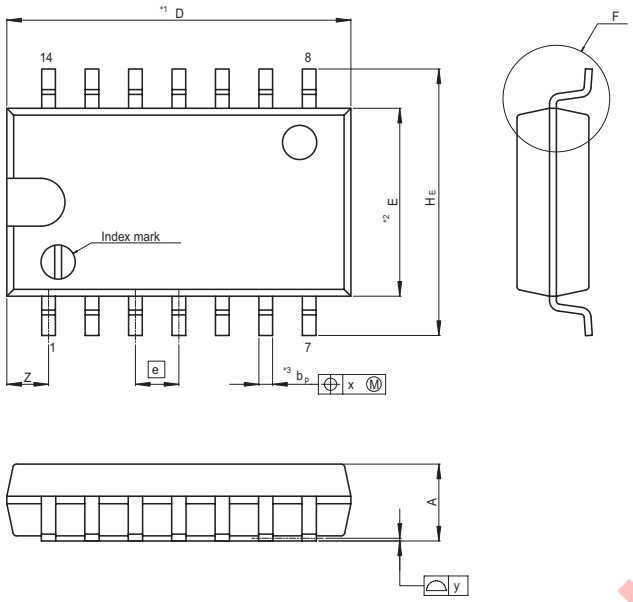
Waveforms 2



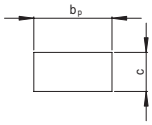
Note: Crear and preset input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz,

Package Dimensions

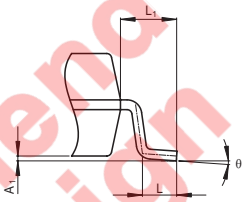
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP14-5.5x10.06-1.27	PRSP0014DF-B	FP-14DAV	0.23g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	10.06	10.5
E	—	5.50	—
A_2	—	—	—
A_1	0.00	0.10	0.20
A	—	—	2.20
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	7.50	7.80	8.00
e	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	1.42
L	0.50	0.70	0.90
L_1	—	1.15	—

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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http://www.renesas.com

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Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

Renesas Technology Malaysia Sdn. Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510

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