HEF4028B

BCD to decimal decoder

Rev. 06 — 25 November 2009   **Product data sheet**

1. General description

The HEF4028B is a 4-bit BCD to decimal decoder, a 4-bit BCO to octal decoder with active LOW enable or an 8-output (Y0 to Y7) inverting demultiplexer. The outputs are fully buffered for best performance.

When used as a BCD to decimal decoder a 1-2-4-8 BCD code applied to inputs A0 to A3 causes the selected output to be HIGH. The other nine outputs will be LOW.

To use the HEF4028B as a BCO to octal decoder, input A3 is an active LOW enable pin and outputs Y8 and Y9 are not used. A 1-2-4 BCO code applied to inputs A0 to A2 causes the selected output (Y0 to Y7) to be HIGH. The other seven outputs will be LOW. When A3 is HIGH outputs (Y0 to Y7) will be forced LOW.

When used as an 8-output (Y0 to Y7) inverting demultiplexer A0 to A2 are used as address inputs and A3 is the data input. Outputs Y8 and Y9 are not used.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input. It is also suitable for use over the full industrial (-40 °C to +85 °C) temperature range.

2. Features

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Operates across the full industrial temperature range -40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B

3. Applications

- Industrial

4. Ordering information

Table 1.   Ordering information
All types operate from -40 °C to +85 °C.

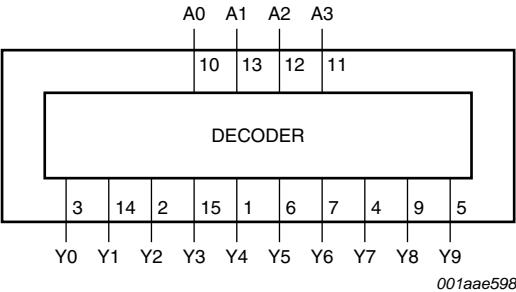| Type number	Package			
	Name	**Description**		**Version**
HEF4028BP	DIP16	plastic dual in-line package; 16 leads (300 mil)		SOT38-4
HEF4028BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm		SOT109-1

5. Functional diagram
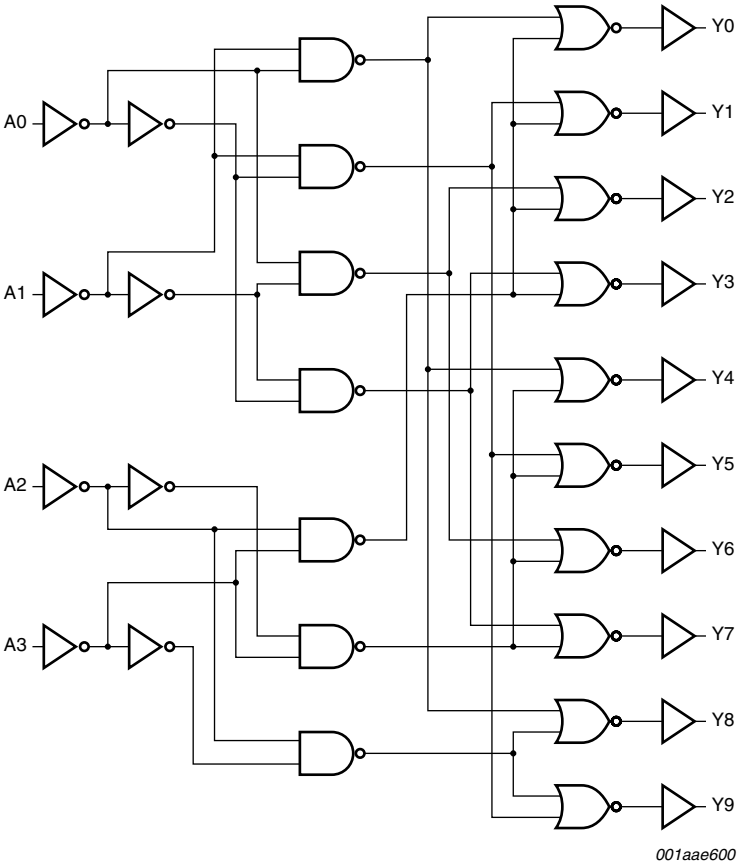

Fig 1. Functional diagram
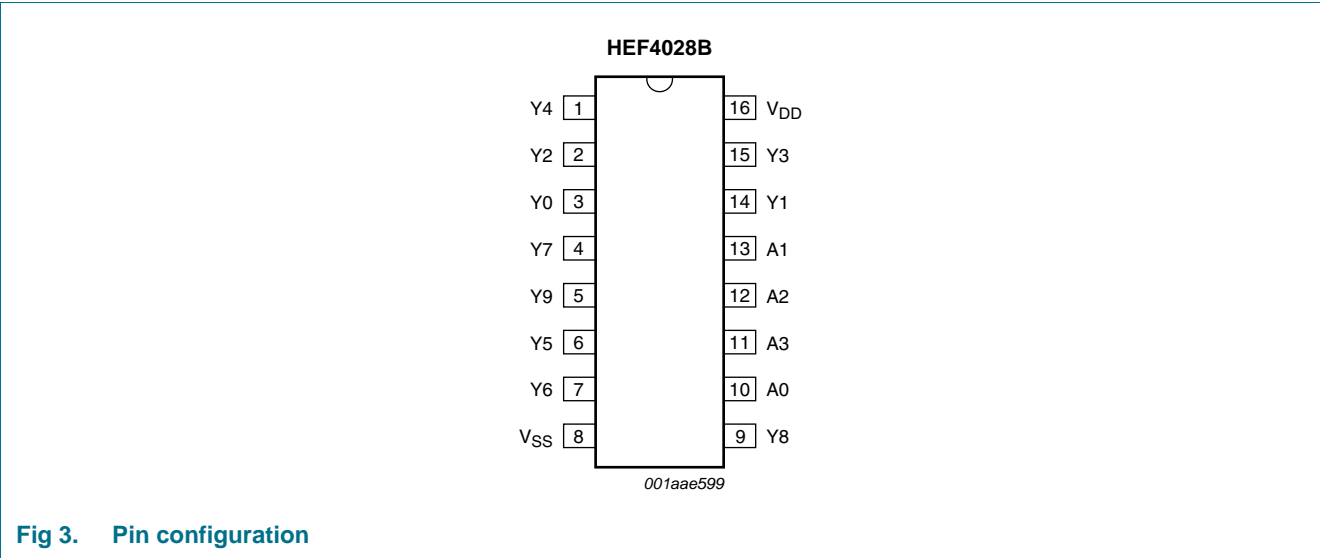

Fig 2. Logic diagram

6. Pinning information

6.1 Pinning

HEF4028B

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        ┌───────┐
Y4  1 │       │ 16  V_DD
Y2  2 │       │ 15  Y3
Y0  3 │       │ 14  Y1
Y7  4 │       │ 13  A1
Y9  5 │       │ 12  A2
Y5  6 │       │ 11  A3
Y6  7 │       │ 10  A0
V_SS 8 │       │  9  Y8
        └───────┘
```

001aae599

Fig 3. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Y0 to Y9	3, 14, 2, 15, 1, 6, 7, 4, 9, 5	output (active HIGH)
V_{SS}	8	ground supply voltage
A0 to A3	10, 13, 12, 11	address input
V_{DD}	16	supply voltage

7. Functional description

Table 3. Function table [1]

Inputs				Outputs									
A3	**A2**	**A1**	**A0**	**Y0**	**Y1**	**Y2**	**Y3**	**Y4**	**Y5**	**Y6**	**Y7**	**Y8**	**Y9**
L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	L	L	H	L	H	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	H	L	L	L	L	L	L	H	L	L	L	L	L
L	H	L	H	L	L	L	L	L	H	L	L	L	L
L	H	H	L	L	L	L	L	L	L	H	L	L	L
L	H	H	H	L	L	L	L	L	L	L	H	L	L
H	L	L	L	L	L	L	L	L	L	L	L	H	L

Table 3. **Function table** [1] *…continued*

Inputs				Outputs										
A3	**A2**	**A1**	**A0**	**Y0**	**Y1**	**Y2**	**Y3**	**Y4**	**Y5**	**Y6**	**Y7**	**Y8**	**Y9**	
H	L	L	H	L	L	L	L	L	L	L	L	L	H	
H	L	H	X	L	L	L	L	L	L	L	L	L	L	[2]
H	H	X	X	L	L	L	L	L	L	L	L	L	L	[2]

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

[2] Extraordinary states.

8. Limiting values

Table 4. **Limiting values**
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			−0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V		-	±10	mA
V_I	input voltage			−0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V		-	±10	mA
$I_{I/O}$	input/output current			-	±10	mA
I_{DD}	supply current			-	50	mA
T_{stg}	storage temperature			−65	+150	°C
T_{amb}	ambient temperature			−40	+85	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +85 °C				
		DIP16 package	[1]	-	750	mW
		SO16 package	[2]	-	500	mW
P	power dissipation	per output		-	100	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

9. Recommended operating conditions

Table 5. **Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	−40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5$ V	-	-	6.25	μs/V
		$V_{DD} = 10$ V	-	-	0.5	μs/V
		$V_{DD} = 15$ V	-	-	0.08	μs/V

10. Static characteristics

Table 6.   Static characteristics

$V_{SS} = 0$ V; $V_I = V_{SS}$ or V_{DD}.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = −40 °C		T_{amb} = 25 °C		T_{amb} = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$|I_O| < 1$ μA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$|I_O| < 1$ μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$|I_O| < 1$ μA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$|I_O| < 1$ μA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	$V_O = 2.5$ V	5 V	−1.7	-	−1.4	-	−1.1	-	mA
		$V_O = 4.6$ V	5 V	−0.52	-	−0.44	-	−0.36	-	mA
		$V_O = 9.5$ V	10 V	−1.3	-	−1.1	-	−0.9	-	mA
		$V_O = 13.5$ V	15 V	−3.6	-	−3.0	-	−2.4	-	mA
I_{OL}	LOW-level output current	$V_O = 0.4$ V	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5$ V	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5$ V	15 V	3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	μA
I_{DD}	supply current	$I_O = 0$ A	5 V	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μA
			15 V	-	80	-	80	-	600	μA
C_I	input capacitance		-	-	-	-	7.5	-	-	pF

11. Dynamic characteristics

Table 7.   Dynamic characteristics

$V_{SS} = 0$ V; $T_{amb} = 25$ °C.

Symbol	Parameter	Conditions	V_{DD}		Extrapolation formula	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	An to Yn; see Figure 4	5 V	[1]	73 ns + (0.55 ns/pF)C_L	-	100	200	ns
			10 V		29 ns + (0.23 ns/pF)C_L	-	40	80	ns
			15 V		22 ns + (0.16 ns/pF)C_L	-	30	60	ns
t_{PLH}	LOW to HIGH propagation delay	An to Yn; see Figure 4	5 V	[1]	63 ns + (0.55 ns/pF)C_L	-	90	180	ns
			10 V		29 ns + (0.23 ns/pF)C_L	-	40	80	ns
			15 V		22 ns + (0.16 ns/pF)C_L	-	30	60	ns

Table 7.   Dynamic characteristics *…continued*

$V_{SS} = 0 \text{ V}; T_{amb} = 25\ ℃.$

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula	Min	Typ	Max	Unit
t_t	transition time	see Figure 4	5 V	[1] $10 \text{ ns} + (1.00 \text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9 \text{ ns} + (0.42 \text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6 \text{ ns} + (0.28 \text{ ns/pF})C_L$	-	20	40	ns

[1]   The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

Table 8.   Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. $V_{SS} = 0 \text{ V}; t_r = t_f \le 20 \text{ ns}; T_{amb} = 25\ ℃.$

Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 350 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}{}^2$	f_i = input frequency in MHz;
		10 V	$P_D = 2200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}{}^2$	f_o = output frequency in MHz;
		15 V	$P_D = 7350 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}{}^2$	C_L = output load capacitance in pF;
				V_{DD} = supply voltage in V;
				$\Sigma(f_o \times C_L)$ = sum of the outputs.

12. Waveforms

Output shown going high when address input goes low, see Table 3.

Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 4.   Input rise and fall times, propagation delays and output transition times
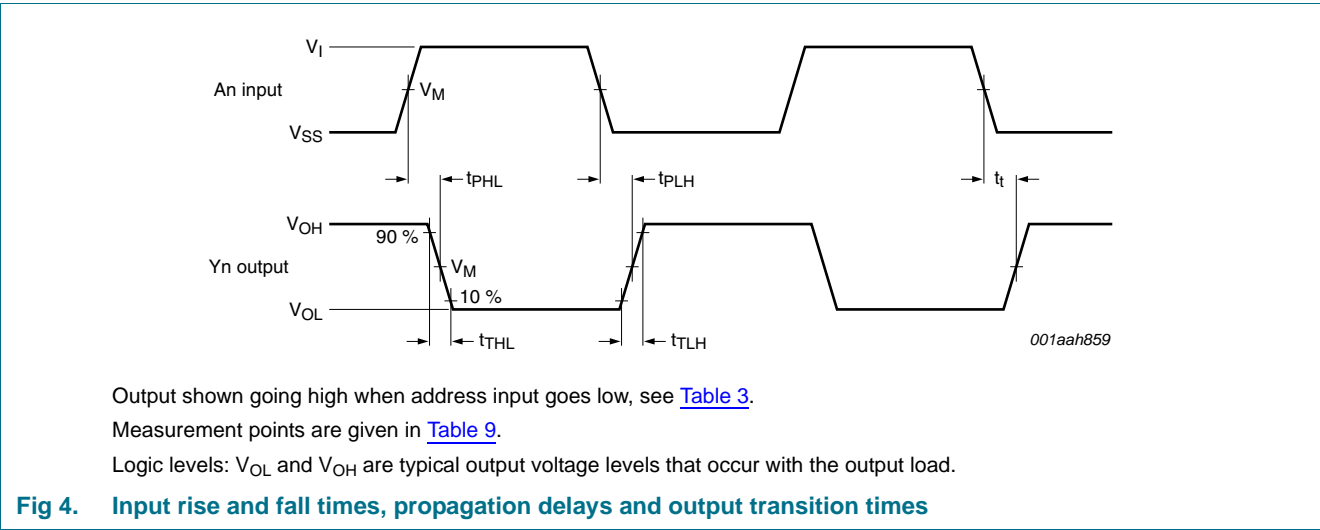
Table 9.   Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$
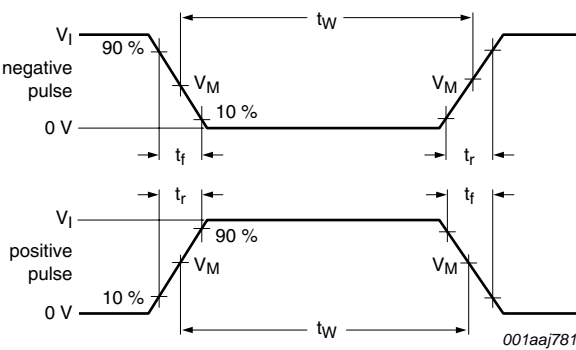
a. Input waveforms
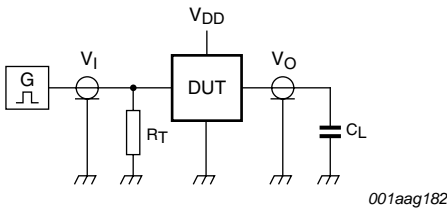
b. Test circuit

Test data is given in Table 10.

Definitions for test circuit:

DUT = Device Under Test;

C_L = load capacitance including jig and probe capacitance;

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

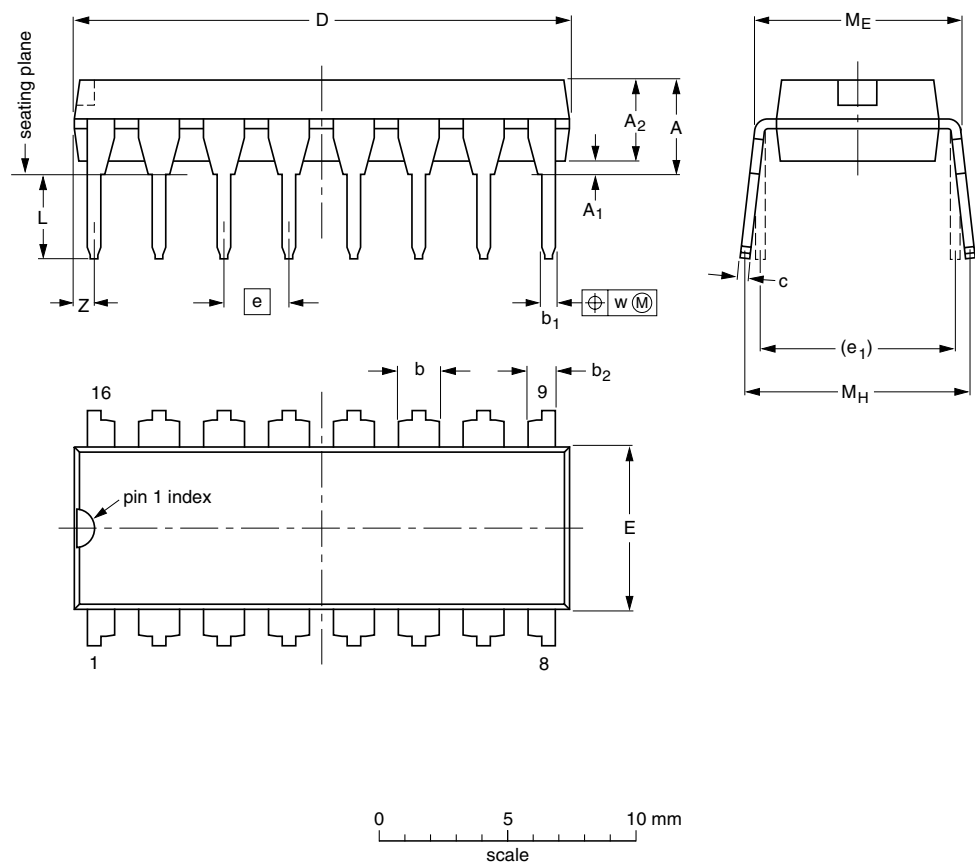**Fig 5. Test circuit for switching times**

Table 10. Test data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)　　　　　　　　　　　　**SOT38-4**

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A$_1$ min.	A$_2$ max.	b	b$_1$	b$_2$	c	D$^{(1)}$	E$^{(1)}$	e	e$_1$	L	M$_E$	M$_H$	w	Z$^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

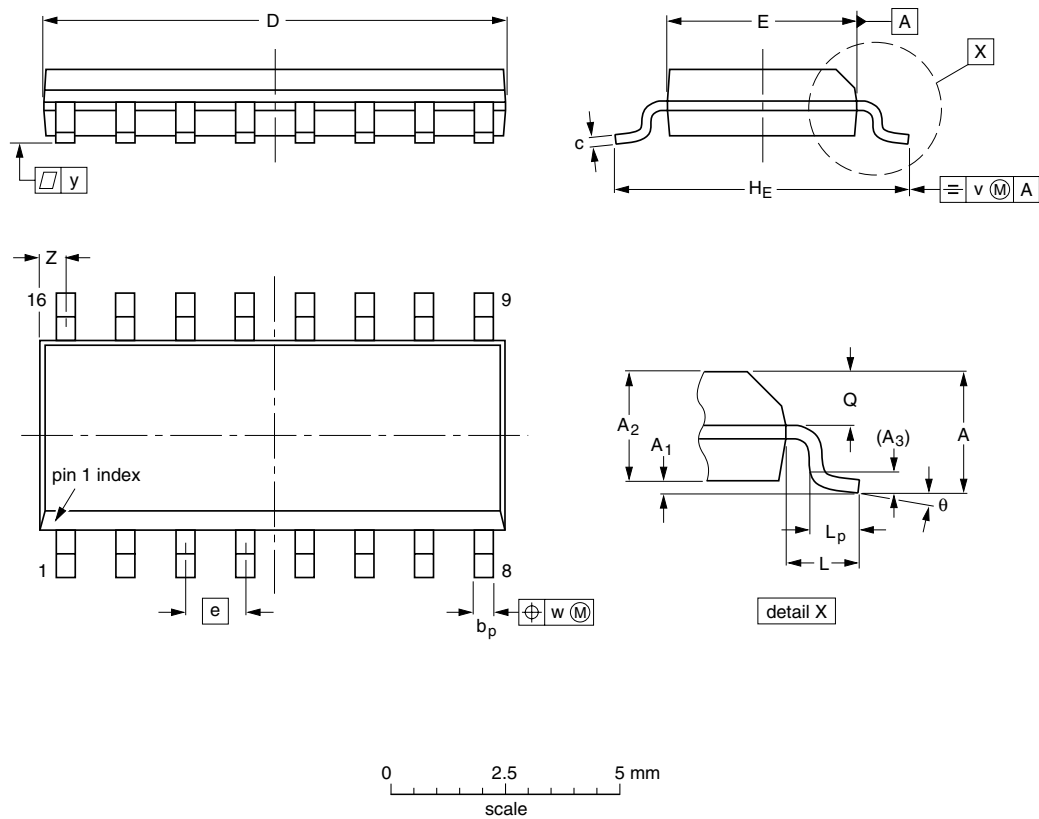1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.
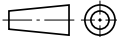
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						95-01-14 03-02-13

Fig 6.　Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁	A₂	A₃	b_p	c	D[1]	E[1]	e	H_E	L	L_p	Q	v	w	y	Z[1]	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 7.   Package outline SOT109-1 (SO16)

14. Abbreviations

Table 11.   Abbreviations

Acronym	Description
BCD	Binary Coded Decimal
BCO	Binary Coded Octal

15. Revision history

Table 12.   Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4028B_6	20091125	Product data sheet	-	HEF4028B_5
Modifications:	• Section 9 "Recommended operating conditions", $\Delta t/\Delta V$ values updated.			
HEF4028B_5	20090707	Product data sheet	-	HEF4028B_4
HEF4028B_4	20090304	Product data sheet	-	HEF4028B_CNV_3
HEF4028B_CNV_3	19950101	Product specification	-	HEF4028B_CNV_2
HEF4028B_CNV_2	19950101	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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18. Contents

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