

HD74LS78A

Dual J-K Flip-Flops
(with Preset, Common Clear, and Common Clock)

REJ03D0419-0300

Rev.3.00

Jul.22.2005

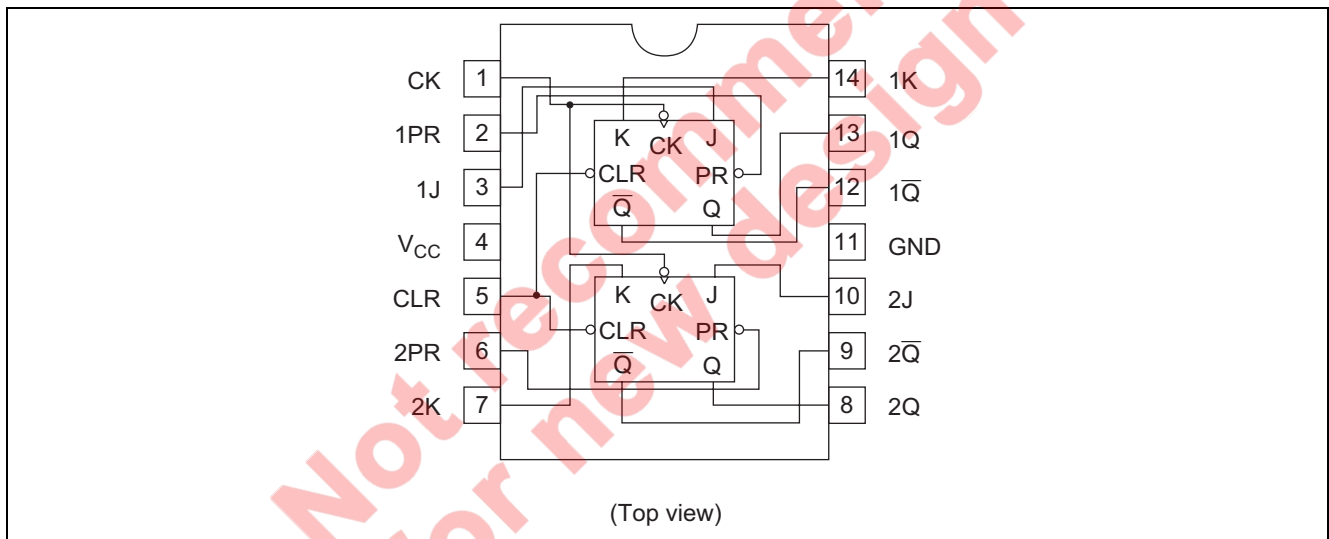
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS78AFPEL	SOP-14 pin (JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



Function Table

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	\bar{Q}_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	\bar{Q}_0

Notes: H; high level, L; low level, X; irrelevant, ↓; transition from high to low level,

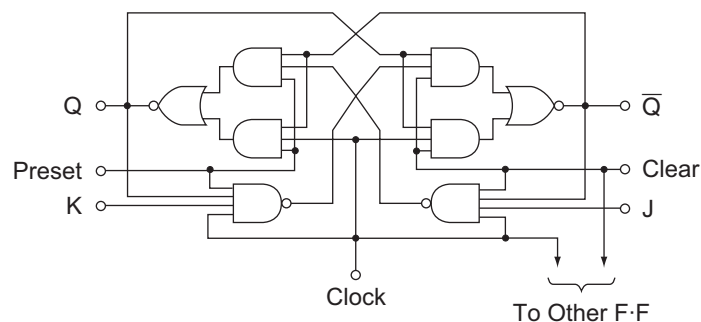
Q_0 ; level of Q before the indicated steady-state input conditions were established.

\bar{Q}_0 ; complement of Q_0 or level of Q before the indicated steady-state input conditions were established.

Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Block Diagram (1/2)



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	T_{stg}	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}	—	—	-400	μA
	I_{OL}	—	—	8	mA
Operating temperature	T_{opr}	-20	25	75	°C
Clock frequency	f_{clock}	0	—	30	MHz
Pulse width	Clock High t_w	20	—	—	ns
	Clear Preset Low t_w	25	—	—	
Setup time	"H" Data t_{su}	20↓	—	—	ns
	"L" Data t_{su}	20↓	—	—	
Hold time	t_h	0↓	—	—	ns

Electrical Characteristics

(Ta = -20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition
Input voltage		V _{IH}	2.0	—	—	V	
		V _{IL}	—	—	0.8	V	
Output voltage		V _{OH}	2.7	—	—	V	V _{CC} = 4.75 V, V _{IH} = 2.7 V, V _{IL} = 0.8 V, I _{OH} = -400 µA
		V _{OL}	—	—	0.5	V	I _{OL} = 8 mA
			—	—	0.4		I _{OL} = 4 mA
Input current	J, K	I _{IH}	—	—	20	µA	V _{CC} = 5.25 V, V _I = 2.7 V
	Clear		—	—	120		
	Preset		—	—	60		
	Clock		—	—	160		
	J, K	I _{IL} **	—	—	-0.4	mA	V _{CC} = 5.25 V, V _I = 0.4 V
	Clear		—	—	-1.6		
	Preset		—	—	-0.8		
	Clock		—	—	-1.6		
	J, K	I _I	—	—	0.1	mA	V _{CC} = 5.25 V, V _I = 7 V
	Clear		—	—	0.6		
	Preset		—	—	0.3		
	Clock		—	—	0.8		
Short-circuit output current		I _{OS}	-20	—	-100	mA	V _{CC} = 5.25 V
Supply current***		I _{CC}	—	4	6	mA	V _{CC} = 5.25 V
Input clamp voltage		V _{IK}	—	—	-1.5	V	V _{CC} = 4.75 V, I _{IN} = -18 mA

Notes: * V_{CC} = 5 V, Ta = 25°C** I_{IL} should not be measured when preset and clear inputs are low at same time.*** With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn.

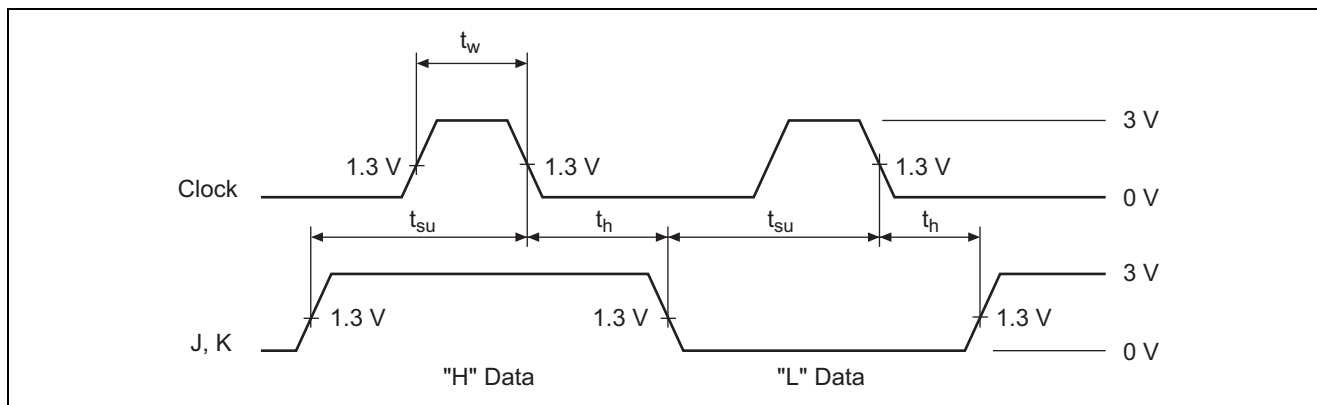
At the time of measurement, the clock input is grounded.

Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f _{max}			30	45		MHz	
Propagation delay time	t _{PLH}	Clear	Q, \bar{Q}	—	15	20	ns	C _L = 15 pF, R _L = 2 kΩ
	t _{PHL}	Preset Clock		—	15	20	ns	

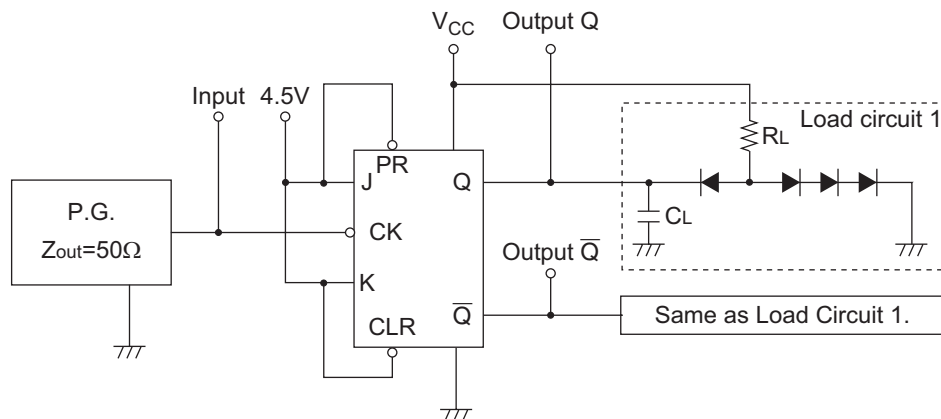
Timing Definition



Testing Method

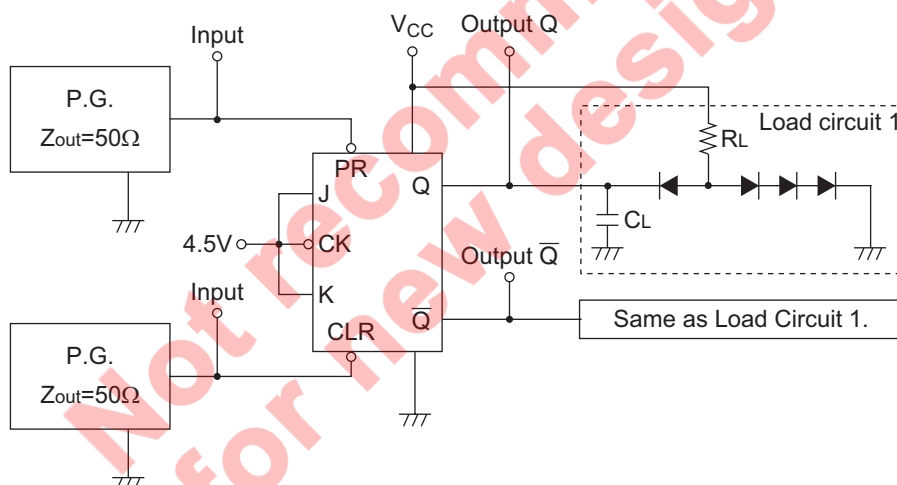
Test Circuit

1. f_{\max} , t_{PLH} , t_{PHL} , (Clock \rightarrow Q, \bar{Q})



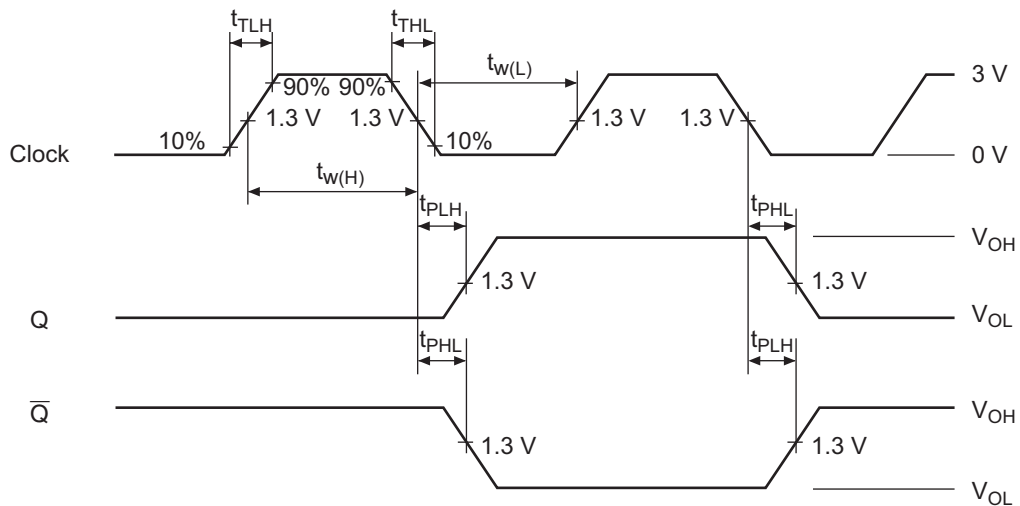
- Notes:
1. Test is put into the each flip-flop.
 2. C_L includes probe and jig capacitance.
 3. All diodes are 1S2074(H).

2. t_{PHL} , t_{PLH} (Clear, Preset \rightarrow Q, \bar{Q})



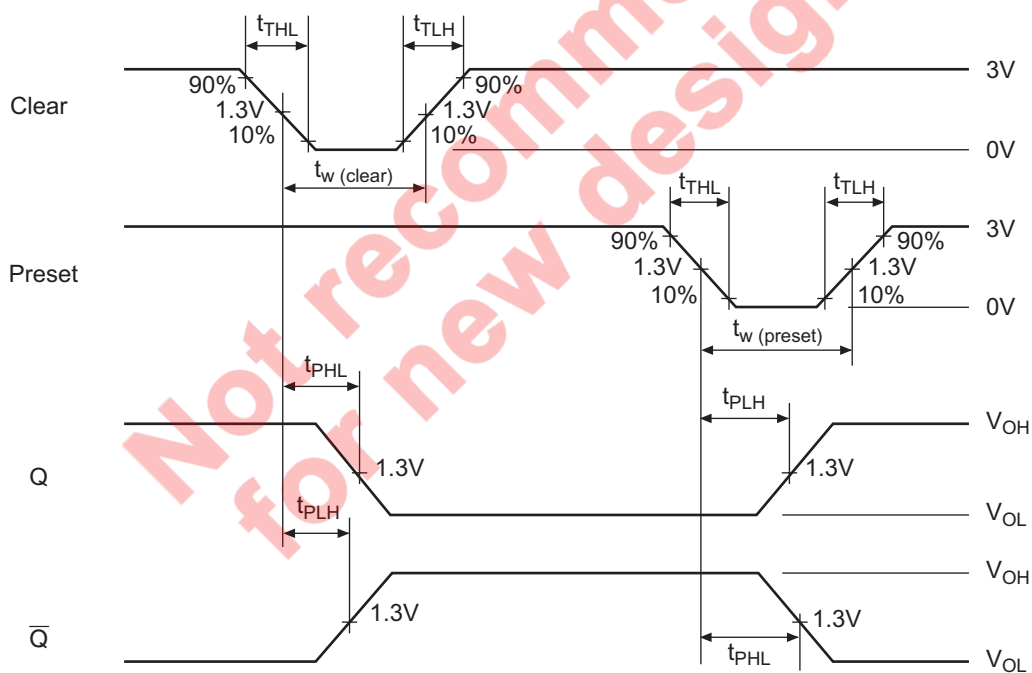
- Notes:
1. Test is put into the each flip-flop.
 2. C_L includes probe and jig capacitance.
 3. All diodes are 1S2074(H).

Waveforms 1



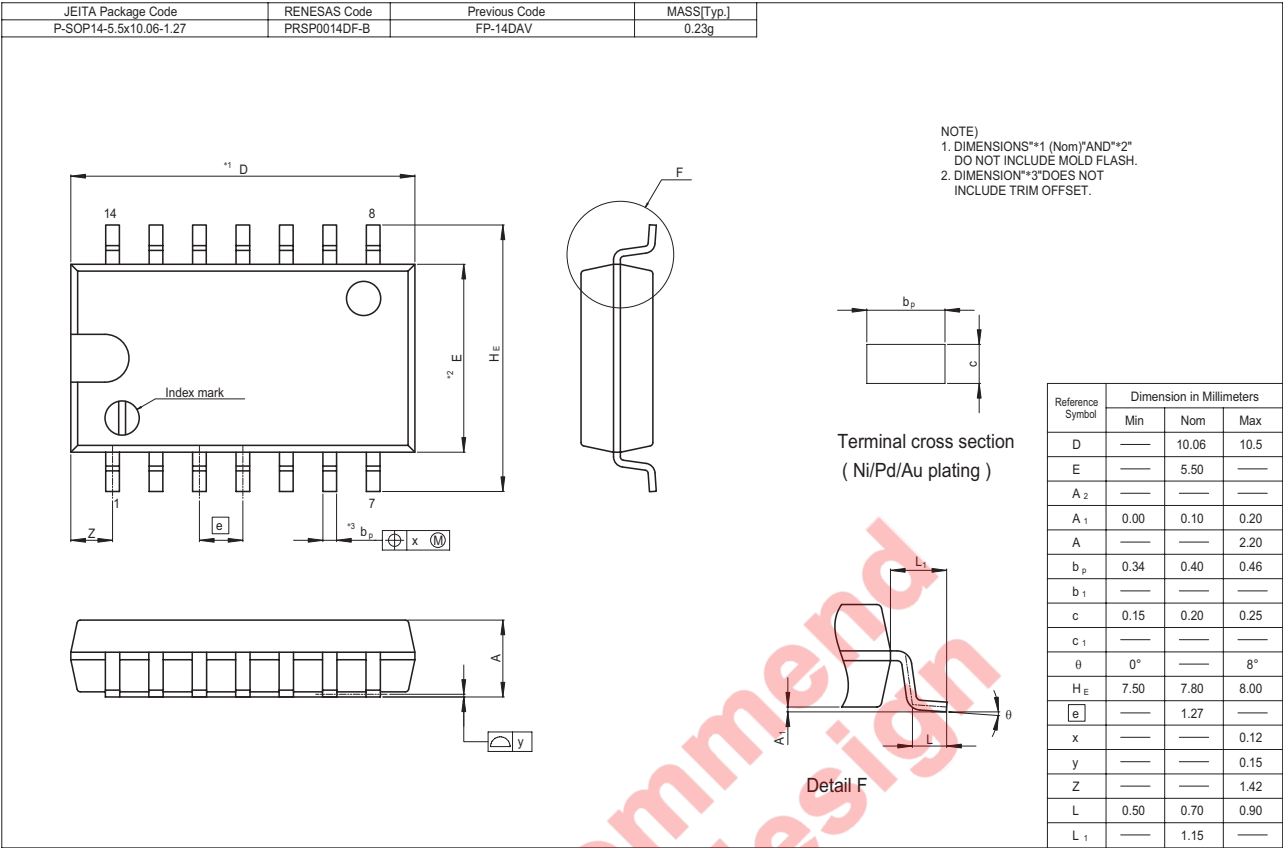
Note: Clock input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle = 50% and for f_{max} , $t_{TLH} = t_{THL} \leq 2.5$ ns

Waveforms 2



Note: Clear and preset input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz,

Package Dimensions



Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

Renesas Technology Malaysia Sdn. Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510