數位IC設計

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資訊工程系 特聘教授 兼 計算機與網路中心主任

Syllabus (1/3)

- Time and Place
  - Monday : 9:10 ~ 12:00 資訊系 4F 65405
- Contact Information
  - 資訊系11F Rm:65B13 (06-2757575 EXT 62547)
  - E-mail: pychen@mail.ncku.edu.tw
- Office Hour
  - Tuesday: 8:00~12:00
- Assistants
  - 資訊系10F 數位IC設計實驗室(65A01)
    博士生 廖國佑 p78121506@gs.ncku.edu.tw

Syllabus (2/3)

上課方式:

a. 上課1~15週(期末考)。

出席 + 投影片講解

b. 三週非同步線上(需於第2週上課前看完)。

參考書目：

1. HDL chip design (Douglas J. Smith), Doone Publications
2. Principles of digital design (Daniel D. Gajski), Prentice Hall
3. Modeling, synthesis, and rapid prototyping with the Verilog HDL (Michael. D. Ciletti), Prentice Hall
4. 數位IC設計--Verilog,(陳培殷),滄海書局
5. 教育部P&L聯盟課程講義– FPGA系統設計實務

Syllabus (2/2)

評分方式:

期中考(筆試15%，上機考10%)；

期末上機考(25%)；

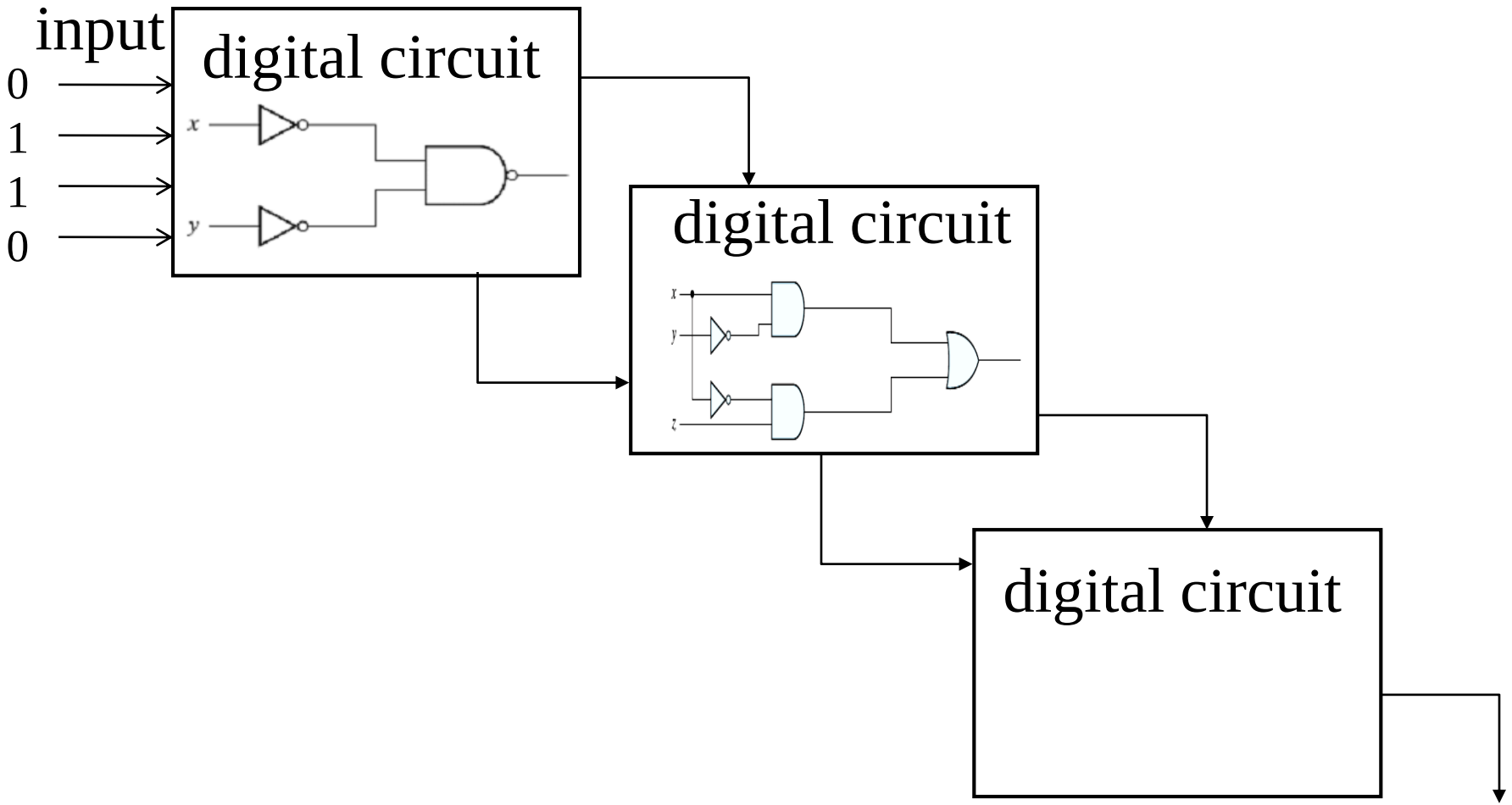
作業含Demo(50%)

a. 兩次上機考試皆為Verilog實作測驗。

b. 因修課人數與作業較多，上機考試與作業皆以pass與fail評分，不會部分給分

c. 考試作業嚴禁作弊，抄襲者與提供他人抄襲者以0分計算。

Digital System

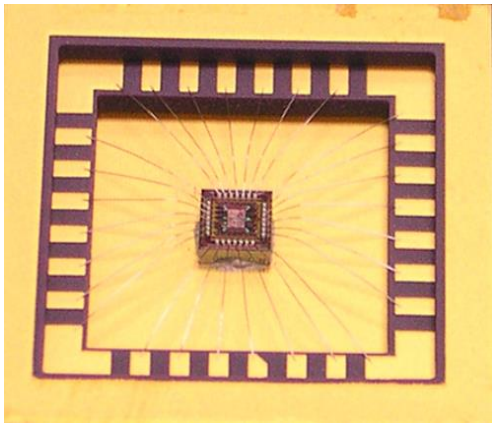


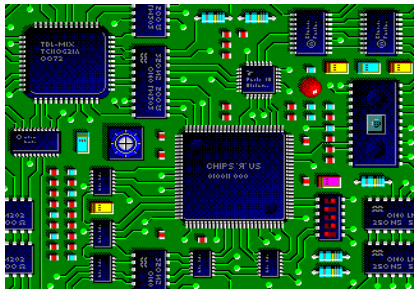
digital circuit === IC (integrated circuit)

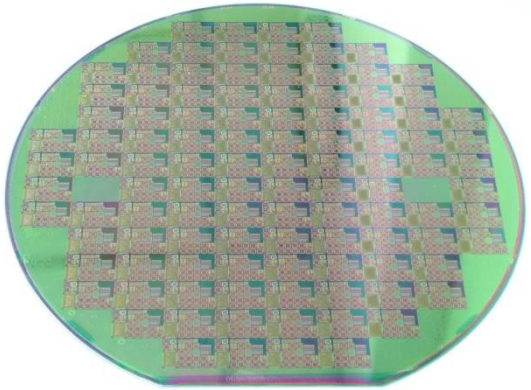
semiconductor

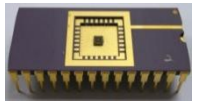
Chip/Circuit Everywhere!

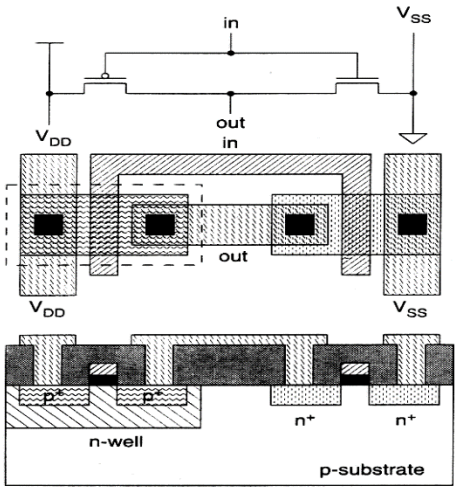
Applications

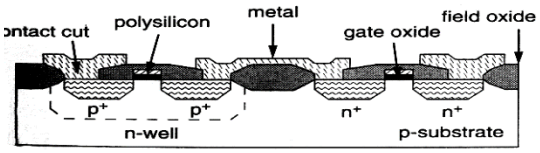












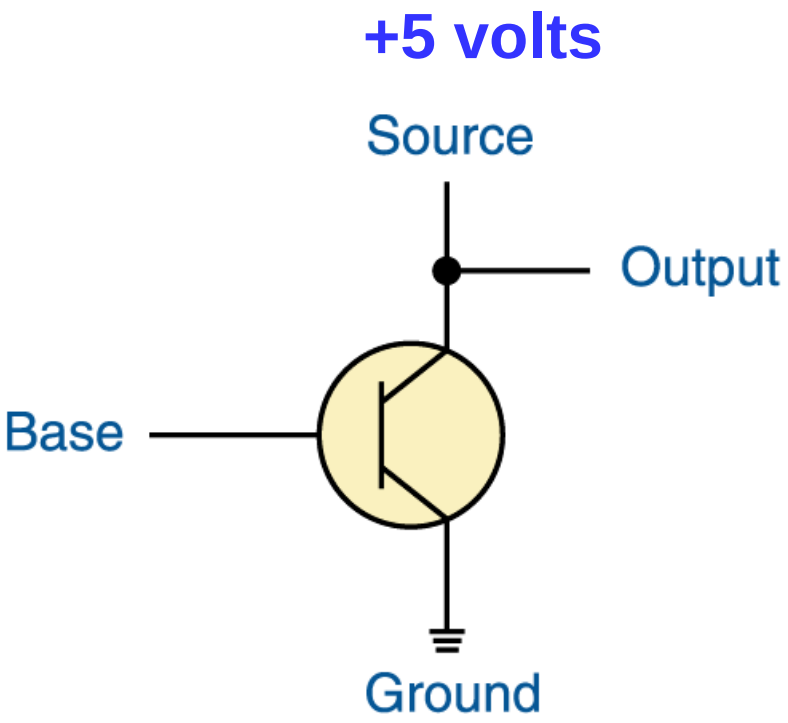
Circuits

- **Transistor**
- **Gate (1 gate ~= 2~14 transistors)**

  A combination of interacting transistors
- **Circuit**

  A combination of interacting gates designed to accomplish a specific logical function
- **IC (Integrated Circuit)**
- **System➔ PCB (printed circuit board)**
- **SoC (system on a chip) ➔ How many gates in a chip?**

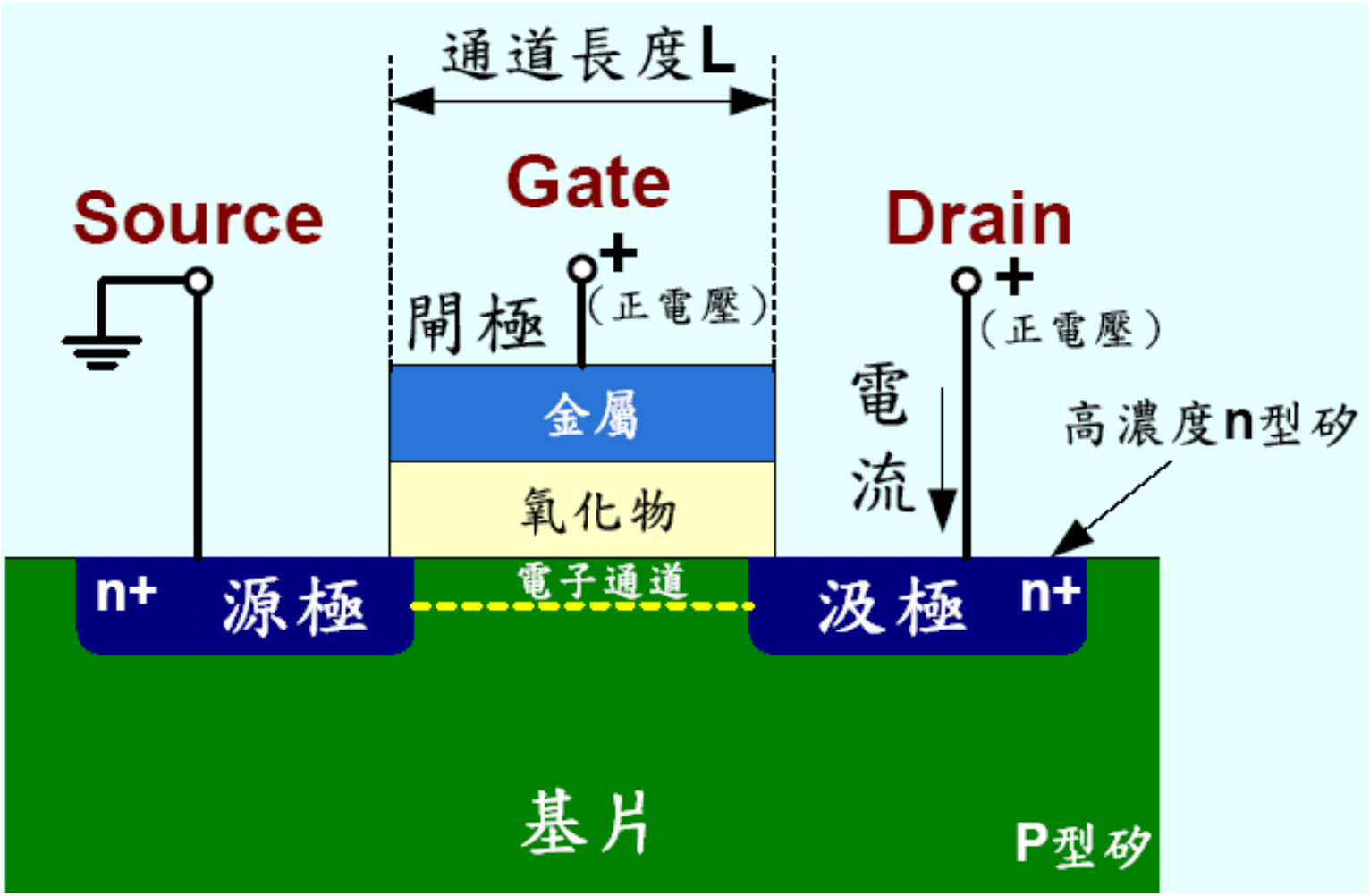
Transistor(電晶體)



- A transistor has three terminals
  - A source (feed with 5 volts)
  - A base
  - An emitter, typically connected to a ground wire
- If the base signal is high (close to +5 volts), the source signal is grounded and the output signal is low (0). If the base signal is low (close to 0 volts), the source signal stays high and the output signal is high (1)

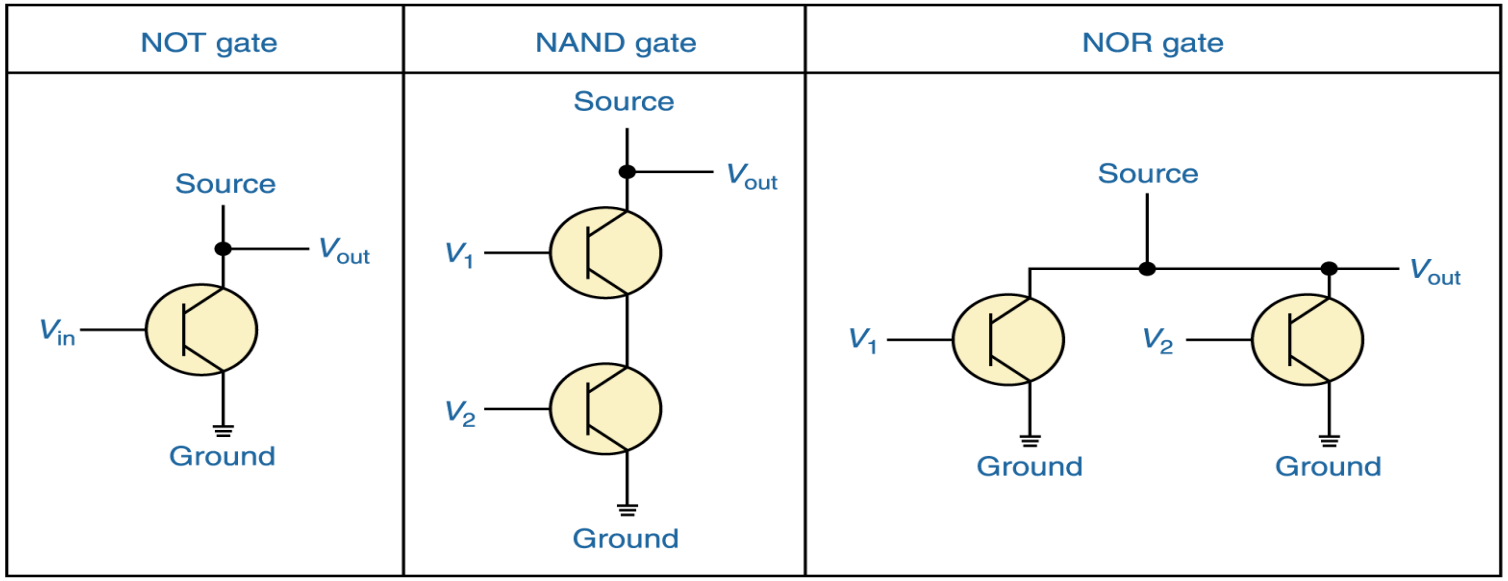
N-channel MOS Transistor

Transistor (電晶體)– Semiconductor(半導體)



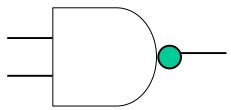
Constructing Gates (semiconductor)

- It turns out that, because the way a transistor works, the easiest gates to create are the NOT, NAND, and NOR gates

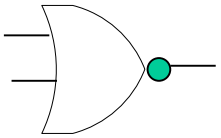


V_{in}	V_{out}
0	1
1	0

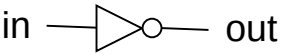
V_1	V_2	V_{out}
0	0	1
0	1	1
1	0	1
1	1	0



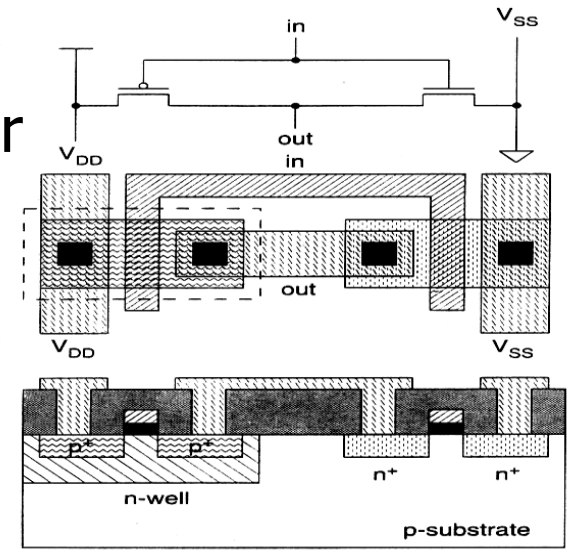
V_1	V_2	V_{out}
0	0	1
0	1	0
1	0	0
1	1	0

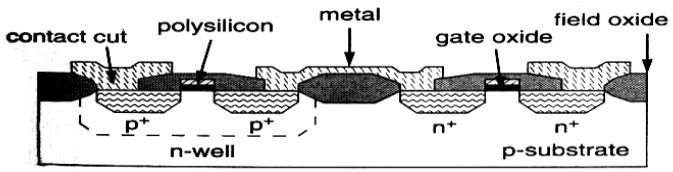


IC Design (with CMOS)

CMOS Inverter 

One npn transistor and one pnp transistor are used to construct one inverter.





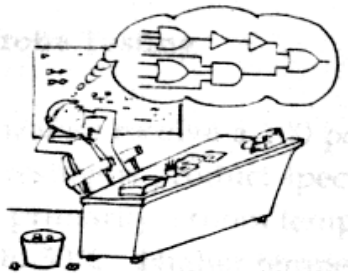
done by chip designer

masking

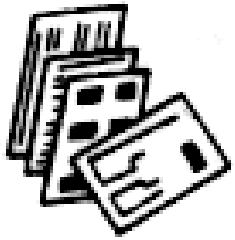
done by TSMC, UMC

Packing, Testing

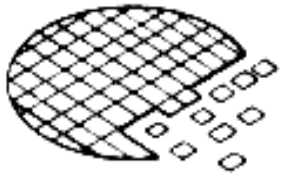
IC Industry in Taiwan



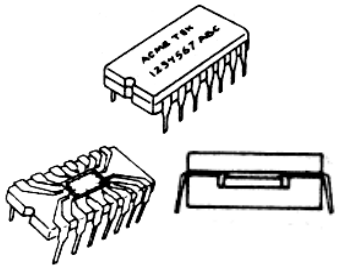
邏輯設計



光罩設計



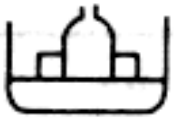
晶粒測試及切割



封 裝

成品測試

設計 → 光罩 → 製造 → 封裝 → 測試

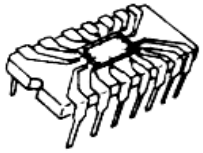


長晶

晶圓切割

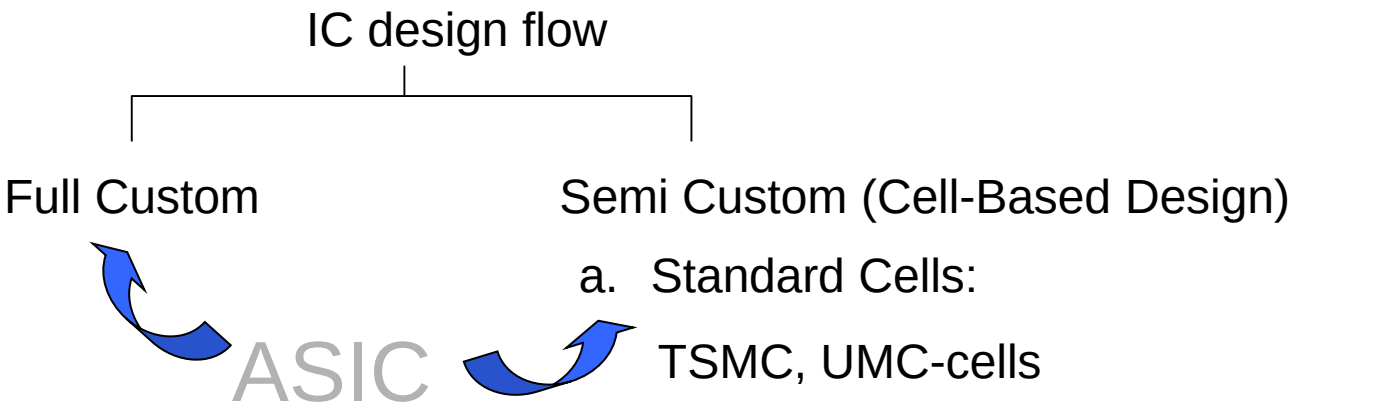
晶圓

化學品



導線架

IC Design flow



Full (Fully) Custom Design:

a. For analog circuits and digital circuits requiring custom optimization
b. Gates, transistors and layout are designed and optimized by the engineer

Semi Custom Design:

a. For larger digital circuits
b. Real gates, transistors and layout are synthesized and optimized by related software tools
c. Realization with hardware description language (HDL) such as VHDL and Verilog

Goal of Course

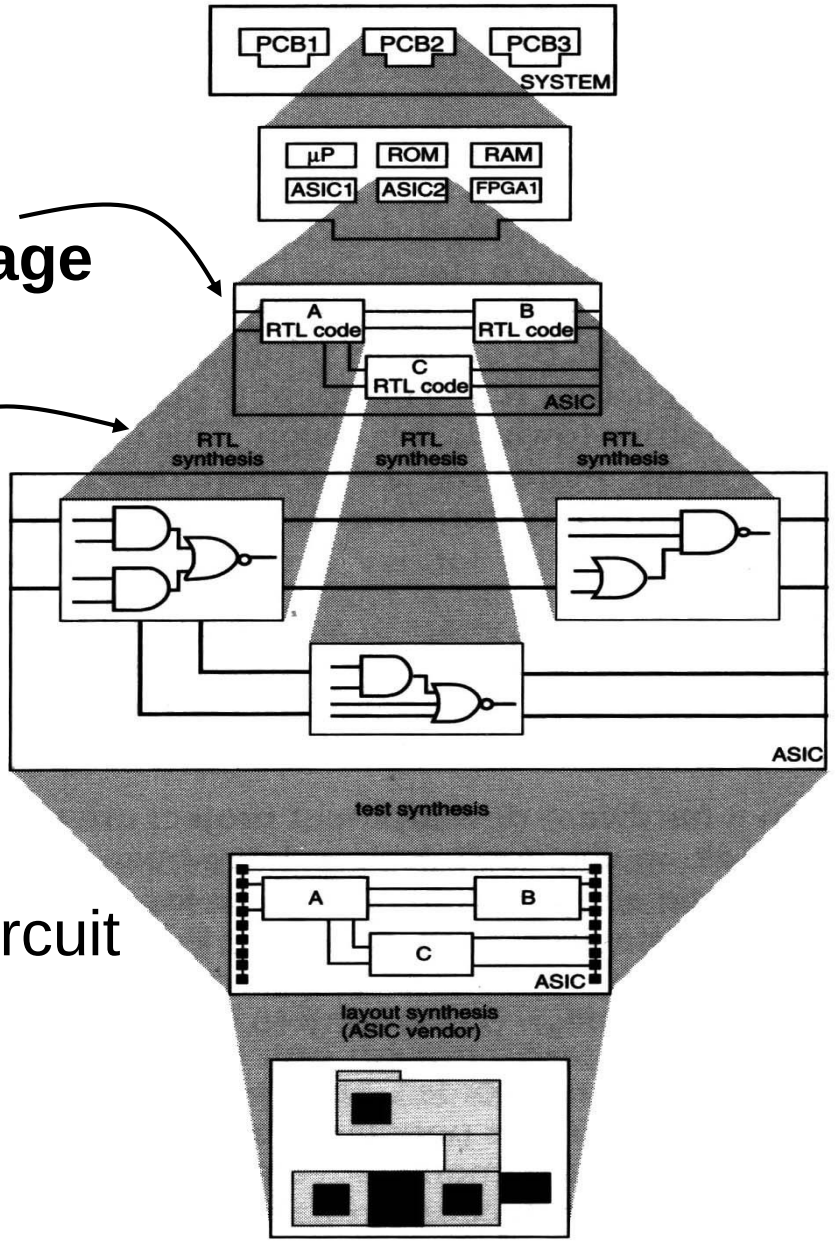
- Digital IC Design
- Cell-Based Design
- Verilog
- PC-based simulation

Hierarchical Components in PCB

1. **Describe the circuits with Hardware Description Language (HDL硬體描述語言)**

2. **Synthesis (合成) the circuits**

….



application specific integrated circuit (ASIC晶片)

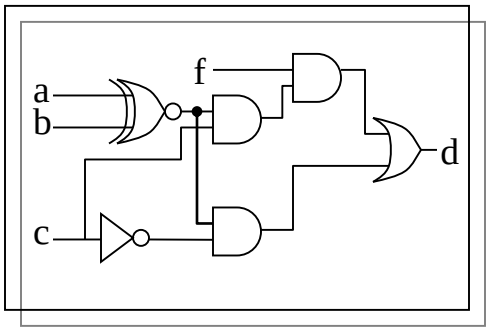
Synthesis

- *Synthesis = Translation+Optimization+Mapping*

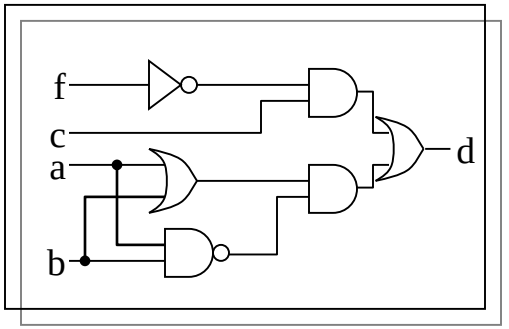
```
always @(…)
   if (a==b)
      if (c==1)
         d=f;
      else
         d=1;
   else
      d=0;
```

HDL Source

Translate into Boolean Representation



Optimize + Map



Target Technology

Process of logic synthesis

2022 Top 10 Fabless IC Suppliers

2022年排名	公司名稱	2022年營收 (百萬美元)
1	高通(Qualcomm)	36,722
2	輝達(Nvidia)	24,503
3	博通(Broadcom Ltd.)	23,972
4	超微半導體(AMD)	23,601
5	**聯發科(MediaTek)**	**18,506**
6	蘋果(Apple)	17,824
7	邁威爾(Marvell)	5,894
8	**瑞昱半導體(Realtek)**	**3,774**
9	**聯詠科技(Novatek)**	**3,734**
10	比特大陸(BitMain)	2,135

聯發科 ★

瑞昱 ★

聯詠 ★

37億

2022年臺灣IC設計主要廠商

2022年排名	公司名稱	2022年營收 單位：新臺幣/億元
1	聯發科	5,488
2	瑞　昱	1,118
3	聯　詠	1,100
4	群　聯	603
5	奇　景	358
6	慧　榮	282
7	瑞　鼎	228
8	天　鈺	197
9	矽　創	180
10	晶　豪	162

Outline

- **Chapter 1**: Introduction
- **Chapter 2**: Semi Custom Design Flow
- **Chapter 3**: RTL Coding-Part I
- **Chapter 4**: RTL Coding-Part II
- **Chapter 5**: Digital System Design
- **Chapter 6**: Control Unit
- **Chapter 7**: Datapath
- **Chapter 8**: Case Study
- **Chapter 9**: System on a Chip
- **Chapter 10**: Low-Power Design

數位IC公司? 大學生? 研究生?