

Homework 4: Max-Priority Queue

NAME		黃偉峰																																	
Student ID		E34106010																																	
Simulation Result																																			
Functional simulation	100	Gate-level simulation	100	Clock width	17 ns	Gate-level simulation time	P0:1269.271ns P1:1643.271ns P2:1779.271ns P3:2204.271ns																												
<pre># ***** # ** # ** Congratulations !! # ** # ** Simulation PASS !! # ** # ** Your score =100 # ** # ***** # ** Note: \$finish : C:/Users/kartg/Desktop/IC_v2/DIC_HW4/testfixture.v(158) # ** Time: 1259500 ps Iteration: 0 Instance: /test</pre>				<pre># ***** # ** # ** Congratulations !! # ** # ** Simulation PASS !! # ** # ** Your score =100 # ** # ***** # ** Note: \$finish : C:/Users/kartg/Desktop/IC_v2/DIC_HW4/testfixture.v(158) # ** Time: 1269271 ps Iteration: 0 Instance: /test</pre>																															
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Synthesis Result																																			
Total logic elements				761																															
Total memory bit				0																															
Embedded multiplier 9-bit element				0																															
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Description of your design
<p>Idx register:此值代表正在處理的 element 在陣列中的位置。</p> <p>Size register:為陣列中最後一個 valid element 所在的位置。</p> <p>INPUT:直接將資料輸入進陣列中，輸入完再進行 Heapify，Heapify 我將其分成三個 state，HEAPIFY、EXCHANGE_WITH_LARGEST、NEXT_HEAPIFY，在 HEAPIFY 時將比較 left child 和 right child 哪個是較大的，EXCHANGE_WITH_LARGEST 時將現在的 idx 跟 largest 者進行交換，NEXT_HEAPIFY 判斷還有沒有下次 HEAPIFY。</p> <p>EXTRACT_MAX:將最後的元素擺到第一個位置上，並將狀態接到 HEAPIFY 上。</p> <p>INCREASE:一路往 parent 比較，若現在的 idx 較大則跟 parent 做交換。</p> <p>WRITE:透過 WRITE_DELAY 來穩定確認資料有正確讀到後，下一個 state 接到 WRITE 上將 RAM_VALID 拉起進行輸出。</p>

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (Total cycle used*clock width)*