

2024 Digital IC Design

Homework 3: matrix multiplier

NAME	黃偉峰																																		
Student ID	E34106010																																		
Simulation Result																																			
Functional simulation	100	Gate-level simulation	100	Clock width	18 ns	Gate-level simulation time	99036 ns																												
<pre># 4:Pattern 1035 is PASS ! # 6:Pattern 1036 is PASS ! # 6:Pattern 1037 is PASS ! # 4:Pattern 1038 is PASS ! # 4:Pattern 1039 is PASS ! # 4:Pattern 1040 is PASS ! # 4:Pattern 1041 is PASS ! # 1:Pattern 1042 is PASS ! # 1:Pattern 1043 is PASS ! # 6:Pattern 1044 is PASS ! # 4:Pattern 1045 is PASS ! # 6:Pattern 1046 is PASS ! # 4:Pattern 1047 is PASS ! # 1:Pattern 1048 is PASS ! # 6:Pattern 1049 is PASS ! # 6:Pattern 1050 is PASS ! # 4:Pattern 1051 is PASS ! # 6:Pattern 1052 is PASS ! # 6:Pattern 1053 is PASS ! # 4:Pattern 1054 is PASS ! # 1:Pattern 1055 is PASS ! # 1:Pattern 1056 is PASS ! # Pattern 3 pass # ----- Simulation FINISH !!----- # score = 100/100 # ----- # \(\^o\^)/ CONGRATULATIONS!! The simulation result is PASS!!! # ----- # ** Note: \$stop : C:/Users/kartg/Desktop/IC_v2/DIC_HW3/testfixture.v(351) # Time: 99036 ns Iteration: 0 Instance: /testfixture1</pre>				<pre># 4:Pattern 1035 is PASS ! # 6:Pattern 1036 is PASS ! # 6:Pattern 1037 is PASS ! # 4:Pattern 1038 is PASS ! # 4:Pattern 1039 is PASS ! # 4:Pattern 1040 is PASS ! # 4:Pattern 1041 is PASS ! # 1:Pattern 1042 is PASS ! # 1:Pattern 1043 is PASS ! # 6:Pattern 1044 is PASS ! # 4:Pattern 1045 is PASS ! # 6:Pattern 1046 is PASS ! # 4:Pattern 1047 is PASS ! # 1:Pattern 1048 is PASS ! # 6:Pattern 1049 is PASS ! # 6:Pattern 1050 is PASS ! # 4:Pattern 1051 is PASS ! # 6:Pattern 1052 is PASS ! # 6:Pattern 1053 is PASS ! # 4:Pattern 1054 is PASS ! # 1:Pattern 1055 is PASS ! # 1:Pattern 1056 is PASS ! # Pattern 3 pass # ----- Simulation FINISH !!----- # score = 100/100 # ----- # \(\^o\^)/ CONGRATULATIONS!! The simulation result is PASS!!! # ----- # ** Note: \$stop : C:/Users/kartg/Desktop/IC_v2/DIC_HW3/testfixture.v(351) # Time: 99036 ns Iteration: 0 Instance: /testfixture1</pre>																															
Synthesis Result																																			
Total logic elements				399																															
Total memory bit				0																															
Embedded multiplier 9-bit element				1																															
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Description of your design																																			
透過兩個 counter 紀錄矩陣的 row 跟 column 並將兩個輸入的矩陣記下，先判斷是否可相乘，若否則直接 output，若可則重複使用上述兩個 counter 和一個外加的 counter 來代表正在乘的 row,column,element 並重複使用同個乘法器，最後直接 output 答案出去不再做儲存。																																			

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (Total cycle used*clock width)*