2024 Digital IC Design

Homework 3: matrix multiplier

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| **Simulation Result** | | | | | | | | |
| Functional simulation | 100 | | Gate-level simulation | 100 | Clock  width | 18 ns | Gate-level simulation time | 99036 ns |
|  | | | | |  | | | |
| **Synthesis Result** | | | | | | | | |
| Total logic elements | | | | | 399 | | | |
| Total memory bit | | | | | 0 | | | |
| Embedded multiplier 9-bit element | | | | | 1 | | | |
|  | | | | | | | | |
| **Description of your design** | | | | | | | | |
| 透過兩個counter紀錄矩陣的row跟column並將兩個輸入的矩陣記下，先判斷是否可相乘，若否則直接output，若可則重複使用上述兩個counter和一個外加的counter來代表正在乘的row,column,element並重複使用同個乘法器，最後直接output答案出去不再做儲存。 | | | | | | | | |

*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) (Total cycle used\*clock width)*