2024 Digital IC Design

Homework 4: Max-Priority Queue

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| **Simulation Result** | | | | | | | | |
| Functional simulation | 100 | | Gate-level simulation | 100 | Clock  width | 17 ns | Gate-level simulation time | P0:1269.271ns  P1:1643.271ns  P2:1779.271ns  P3:2204.271ns |
|  | | | | |  | | | |
| **Synthesis Result** | | | | | | | | |
| Total logic elements | | | | | 761 | | | |
| Total memory bit | | | | | 0 | | | |
| Embedded multiplier 9-bit element | | | | | 0 | | | |
|  | | | | | | | | |
| **Description of your design** | | | | | | | | |
| Idx register:此值代表正在處理的element在陣列中的位置。  Size register:為陣列中最後一個valid element所在的位置。  INPUT:直接將資料輸入進陣列中，輸入完再進行Heapify，Heapify我將其分成三個state，HEAPIFY、EXCHANGE\_WITH\_LARGEST、NEXT\_HEAPIFY，在HEAPIFY時將比較left child和right child哪個是較大的，EXCHANGE\_WITH\_LARGEST時將現在的idx跟largest者進行交換，NEXT\_HEAPIFY判斷還有沒有下次HEAPIFY。  EXTRACT\_MAX:將最後的元素擺到第一個位置上，並將狀態接到HEAPIFY上。  INCREASE:一路往parent比較，若現在的idx較大則跟parent做交換。  WRITE:透過WRITE\_DELAY來穩定確認資料有正確讀到後，下一個state接到WRITE上將RAM\_VALID拉起進行輸出。 | | | | | | | | |

*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) (Total cycle used\*clock width)*