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MILITARY STANDARD

Interoperability and Performance Standards for Tactical Digital Information Link

(TADIL) A

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AREA TCTS

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DEPARTMENT OF DEFENSE
Washington, DC 20363-5100

Interoperability And Performance Standards For
Tactical Digital Information Link (TADIL) A

MIL-STD-188-203-1A

1. This Military Standard is approved and mandatory for use by all Departments and Agencies of the Department of Defense (DoD) in accordance with the Office of the Assistant Secretary of Defense (OASD) (CCCI) Memorandum, dated 10 May 1977, (see APPENDIX A).

2. Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Commander, Space and Naval Warfare Systems Command, ATTN: 003-121, Washington, DC 20360-5100, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

FOREWORD

1. Originally, MIL-STD-188 covered technical standards for tactical and long-haul communications, but later evolved through revisions (MIL-STD-188A, MIL-STD-188B) into a document applicable to tactical communications only (MIL-STD-188C).

2. The Defense Communications Agency (DCA) published DCA Circulars (DCAC) promulgating standards and engineering criteria applicable to the long-haul Defense Communications System (DCS) and to the technical support of the National Military Command System (NMCS).

3. As a result of a Joint Chiefs of Staff (JCS) action, standards for all military communications are now being published in a MIL-STD-188 series of documents. The MIL-STD-188 series is subdivided into a MIL-STD-188-100 series covering common standards for tactical and long-haul communications, a MIL-STD-188-200 series covering standards for tactical communications only, and a MIL-STD-188-300 series covering standards for long-haul communications only. Emphasis is being placed on developing common standards for tactical and long-haul communications published in the MIL-STD-188-100 series.

4. The MIL-STD-188-203 series of documents results from the JCS action requiring that the technical characteristics of Tactical Digital Information Links (TADILs) A, B, and C formerly contained in JCS-PUB-10 be updated and published in the MIL-STD-188 series. This document contains the technical requirements for TADIL A, MIL-STD-188-203-2 contains the requirements for TADIL B, and MIL-STD-188-203-3 contains the requirements for TADIL C. The MIL-STD-188-203 series of documents does not contain TADIL message formats and related information. These requirements will continue to be contained in JCS-PUB-10 and revisions thereto. It is intended that technical characteristics of other TADILs currently under development, such as the Joint Tactical Information Distribution System (JTIDS), will be included as part of the MIL-STD-188-203 series.

IDENTIFICATION OF INTERNATIONAL STANDARDIZATION AGREEMENT

Certain provisions of this document are the subject of International Standardization Agreement (STANAG) 5511. When a change notice, revision, or cancellation of this document is proposed which will affect or violate the international agreement concerned, the preparing activity shall take appropriate reconciliation action through international standardization channels, including departmental standardization offices, if required.

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APPENDIXES

1. SCOPE

1.1 Purpose. The purpose of this document is to establish technical standards and design objectives (DOs) that are necessary to ensure interoperability and to promote commonality for communications equipment and subsystems used in TADIL A (see APPENDIX C). Another purpose of this document is to establish acceptable overall system performance and maximum flexibility of system layout in order to satisfy diverse user requirements without the restrictions caused by interface and incompatibility problems. Standard message formats are not included in this document. The TADIL A message formats are contained in JCS-PUB-10, Tactical Command and Control and Communication System Standards.

1.2 Application. This document is applicable to the design and development of new equipment, assemblages, and subsystems used in TADIL A. This document is applicable also to the engineering and operation of existing TADIL A facilities. It is not intended that existing TADIL A facilities be immediately converted to comply with the standards contained in this document. New TADIL A facilities and those undergoing major modification or rehabilitation shall comply with the standards contained in this document subject to the applicable requirements of current procurement regulations. TADIL A can be used over common long-haul and tactical communication circuits. In this case, both this standard and MIL-STD-188-100 shall apply.

1.3 Objectives. The main objectives of this document are to provide subsystem performance requirements that ensure interoperation of equipment and subsystems consistent with military requirements and to achieve the necessary degree of performance and interoperation in the most economical way. These objectives will be accomplished by continuing efforts in the following areas:

a. Standardizing user-to-user performance characteristics.

b. Standardizing the type of signals at various interface points in the applicable subsystem.

c. Specifying maximum permissible degradation of a signal in the process of transmission, and allocating the permissible degradation among various parts of a system.

d. Establishing performance parameters and operating features of equipment that govern the interface characteristics with subsystems in which the TADIL A equipment will be used.

e. Defining performance parameters without specifying the technology that should be used to obtain the required performance.

An additional objective of this document is to prevent proliferation of equipment serving the same or a similar function. The variety of equipment shall be the minimum necessary to effectively support the missions of the tactical forces in accordance with Department of Defense Directive (DoDD) 4630.5, Compatibility and Commonality of Equipment for Tactical Command and Control, and Communications.

1.4 System standards and DOs. The parameters and other requirements specified in this document are mandatory system standards (See APPENDIX A) if the word "shall" is used in connection with the parameter value or requirement under consideration. Nonmandatory DOs are indicated as optional by the word "should" in connection with the parameter value or requirement under consideration. For a definition of the terms System Standard and Design Objective, see FED-STD-1037. Information paragraphs, shown as notes, have been included to better define certain methods currently in use with TADILs.

2. REFERENCED DOCUMENTS

2.1 Government documents.

2.1.1 Standards and handbooks. Unless otherwise specified, the following standards and handbooks of the issue listed in that issue of the Department of Defense Index of Specifications and Standards (DoDISS) specified in the solicitation form a part of this standard to the extent specified herein.

STANDARDS

FEDERAL

FED-STD-1037	Glossary of Telecommunication Terms

MILITARY

MIL-STD-188-100	Common Long Haul and Tactical Military Communication System Technical Standards
MIL-STD-188-114	Electrical Characteristics of Digital Interface Circuits
MIL-STD-188-124	Grounding, Bonding, and Shielding for Common Long Haul/Tactical Communication Systems
MIL-STD-461	Electromagnetic Emission and Susceptibility Requirements for the Control of Electromagnetic Interference
MIL-STD-462	Electromagnetic Interference Characteristics, Measurement of
MIL-STD-1397	Input/Output Interfaces, Standard Digital Data, Navy Systems

HANDBOOKS

MILITARY

MIL-HDBK-232	RED/BLACK Engineering-Installation Guidelines
MIL-HDBK-237	Electromagnetic Compatibility Management Guide for Platforms, Systems, and Equipments
MIL-HDBK-241	Design Guide for Electromagnetic Interference Reduction in Power Supplies

(Copies of standards and handbooks required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

2.1.2 Other Government documents. The following other Government documents and publications form a part of this standard to the extent specified herein.

PUBLICATIONS

North Atlantic Treaty Organization (NATO) Standardization Agreements

STANAG 5511	Tactical Data Exchange - LINK 11 (U)

(Application for copies of NATO standardization documents required by contractors in connection with specific procurement functions should be made to the appropriate NATO Subregistry.)

National Security Agency

NACSIM 5100	Compromising Emanation Laboratory Test Requirements Electromagnetics (U) (This document was downgraded to unclassified by Revision A.)
NACSEM 5200	Compromising Emanations Design Handbook (U)

(Application for copies of NACSIM and NACSEM standardization documents required by contractors in connection with specific procurement functions should be made to the Director, National Security Agency, Fort George G. Meade, MD 20755.)

2.2 Other publications. The following publication forms a part of this document to the extent specified herein. Unless otherwise indicated, the issue in effect on date of invitation for bids or request for proposal shall apply.

International Regulations

General Secretariat of the International Telecommunications Union (ITU)	Radio Regulations

(Application for copies should be addressed to the ITU, Consultant Committee International Radio, Geneva, Switzerland.)

2.3 Order of precedence. In the event of a conflict between the text of this standard and the references cited herein, the text of this standard shall take precedence.

3. DEFINITIONS

3.1 Definition of terms. Definitions of terms used in this standard shall be as specified in FED-STD-1037. The following term is unique to TADIL A:

3.1.1 TADIL A single tone attenuability (STA). The TADIL A STA expressed in decibels (dB) is used as an overall figure of merit for TADIL A system equipments. When the STA test is conducted, the composite 16-tone signal is adjusted to a specified level (such as 0 dBm). The level of a single data tone is attenuated until a specified bit error rate (BER) is observed at the data terminal set (DTS) receiver. This is repeated for each of the other data tones. The smallest value of attenuation observed among these 15 measurements is referred to as the TADIL A STA.

3.2 Abbreviations and acronyms. The abbreviations and acronyms used in this document are listed in APPENDIX B.

4. GENERAL REQUIREMENTS

(A tutorial describing TADIL A operation and equipments is provided in APPENDIX C.)

4.1 NATO interoperability. The interchange of information among NATO member nations using TADIL A shall comply with applicable requirements of the current edition of STANAG 5511.

4.2 Communications security equipment. Communications security equipment shall be located between the DTS and the Tactical Data System (TDS) computer as illustrated in FIGURE 1. Communications security equipment employed in any TADIL A system shall be transparent and shall not change the standard TADIL A transmission frame format. Any change in the DTS-to-TDS computer interface timing (see APPENDIX D2) caused by the use of security equipment must be accounted for in either the security equipment design or in the TDS computer.

4.3 Compromising emanations (TEMPEST). All communication equipment, subsystems, and systems shall comply with the applicable TEMPEST criteria of the current edition of the NACSIM 5100 series. NACSEM 5200 provides design guidance and MIL-HDBK-232 provides installation guidelines for avoiding compromising emanations.

4.4 Electromagnetic interference (EMI) and electromagnetic compatibility (EMC).

4.4.1 Equipment. Any item, including subassemblies and parts, serving functionally in an electromagnetic environment in the broadest sense, shall comply with the applicable requirements of MIL-STD-461. Techniques used for the measurement and determination of EMI characteristics shall comply with the applicable requirements of MIL-STD-462. MIL-HDBK-241 provides guidance for EMI reductions in equipment power supplies.

4.4.2 Systems and subsystems. Communications systems and associated subsystems shall be designed to achieve intrasystem and intersystem EMC. There shall be neither unacceptable responses nor malfunctions of any item of the system or subsystem beyond the tolerances established by the applicable requirements of MIL-STD-461. MIL-HDBK-237 provides guidance for implementing an EMC program.

4.5 Grounding, bonding, and shielding. Methods and practices for grounding, bonding, and shielding of ground-based telecommunications equipment and facilities, including buildings and structures supporting tactical communications, shall comply with the applicable requirements of MIL-STD-188-124.

4.6 Radio regulations. For subsystem and equipment design, the choice and performance of the equipment, as well as frequencies and emissions of any radio subsystem, shall comply with the applicable requirements of the International Telecommunications Union (ITU) Radio Regulations. Adequate familiarity with these regulations is therefore required of designers and users of radio subsystems. Final approval of frequency bands, operating modes, and equipment characteristics rests within DoD with the Military Communications-Electronics Board (MCEB).

4.7 Radio regulations information. The use of the frequency spectrum is regulated by international agreeements embodied in the ITU Radio Regulations published by the General Secretariat of the ITU, Geneva, Switzerland, and modified periodically by a World Administrative Radio Conference (WARC). These radio regulations are further qualified at the national level through Federal Government agencies, such a the Department of Commerce, the Interdepartment Radio Advisory Committee (IRAC), and through military agencies, such as the JCS and the MCEB. Military frequency planning, including joint functional frequency allocation tables, is established as a joint action area under the MCEB.

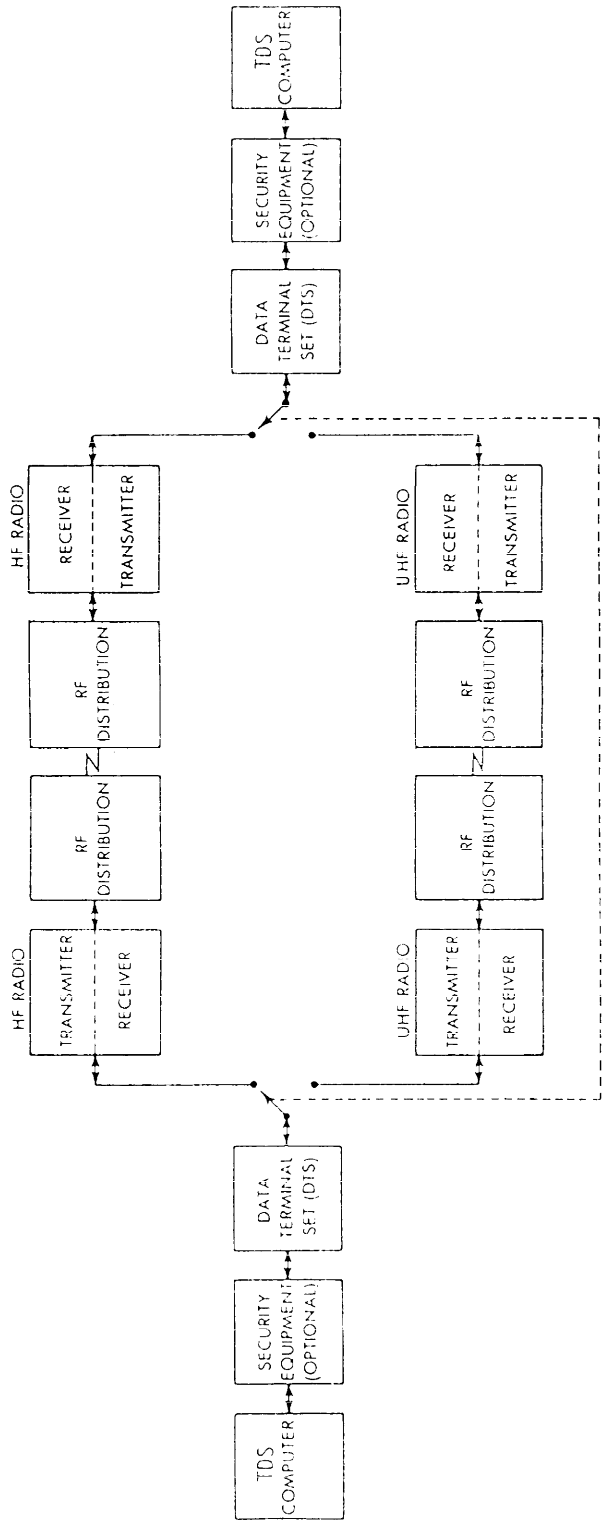


FIGURE 1. TADIL A system.

5. DETAILED REQUIREMENTS

5.1 TADIL A system requirements.

5.1.1 Frequency coverage. TADIL A data communications shall be capable of operation in either the high frequency (HF) or ultrahigh frequency (UHF) bands. In the HF band, the radio equipment shall be capable of being tuned to any integral multiple of 100 hertz (Hz) in the frequency range of 2.0000 megahertz (MHz) through 29.9999 MHz. In the UHF band, the radio equipment shall be capable of being tuned to any integral multiple of 25 kilohertz (kHz) in the frequency range of 225.000 MHz through 399.975 MHz.

5.1.2 Radio frequency (RF) emissions. At HF, the radio equipment should be capable of providing omnidirectional gapless coverage of up to 300 nautical miles (nm) from the transmitter. The equipment shall be capable of operating on upper sideband (USB), lower sideband (LSB), or independent sideband (ISB) diversity (DIV), also referred to as DIV (ISB) operation. The accuracy and stability of the HF emission are contained in 5.3.2.1.2. At UHF, the radio equipment should be capable of providing omnidirectional gapless coverage line-of-sight from the transmitter (approximately 23 nm ship-to-ship, 150 nm ship-to-air). Frequency modulation (FM) shall be employed. The accuracy and stability of the UHF emissions are contained in 5.3.3.1.2.

5.1.3 Subcarrier characteristics and modulation. The RF signal shall be modulated by a signal consisting of 2 or 16 multiplexed audio frequency tones.

5.1.3.1 Tone frequency. The tone frequencies shall be 605 Hz (used for Doppler correction), 2915 Hz (used for data and synchronization), and 935 Hz, 1045 Hz, 1155 Hz, 1265 Hz, 1375 Hz, 1485 Hz, 1595 Hz, 1705 Hz, 1815 Hz, 1925 Hz, 2035 Hz, 2145 Hz, 2255 Hz, and 2365 Hz. After being set, the tone frequencies shall remain within ±0.1 Hz for at least 6 months of either continuous or intermittent operation.

5.1.3.2 Data subcarrier modulation. With the exception of the preamble (see 5.1.4.1), all information shall be conveyed by differential quadrature phase shift keying modulation of the 15 data subcarrier tones. The 605 Hz Doppler correction tone shall remain unmodulated. Each of the 15 data subcarrier tones shall represent 2 data bits, resulting in a total of 30 data bits. The two binary digits represented by each data subcarrier tone shall be encoded by phase changes as defined in TABLE I and illustrated in FIGURE 2. The phase of each data subcarrier tone shall remain unchanged until new data are obtained for transmission. The phase transition of each data subcarrier tone shall occur at the frame boundary of each 13.33-millisecond or 22-millisecond frame and shall be referenced to the phase of that data subcarrier tone in the previous frame. The relationship of the data bits and the data subcarrier tones is illustrated in TABLE II.

5.1.3.3 Relative subcarrier levels. During any portion of the signal in any transmission format (see 5.1.4), the 605 Hz Doppler tone shall be 6 dB ±1 dB greater than any of the other sync or data subcarrier tones.

5.1.3.3.1 Preamble frame level. During the preamble (see 5.1.4.1), the level of the 605 Hz tone shall be 12 dB ±1 dB above the level of a phase reference frame (see 5.1.3.3.2) data subcarrier tone and the 2915 Hz tone shall be 6 dB ±1 dB above the level of a phase reference frame data subcarrier tone.

5.1.3.3.2 Phase reference frame level. The phase reference frame (see 5.1.4.2) shall be comprised of the 16-tone composite signal described in 5.1.3.1 and TABLE II. The difference in amplitude between the maximum level data subcarrier tone and the minimum level data subcarrier tone shall not exceed 1.5 dB.

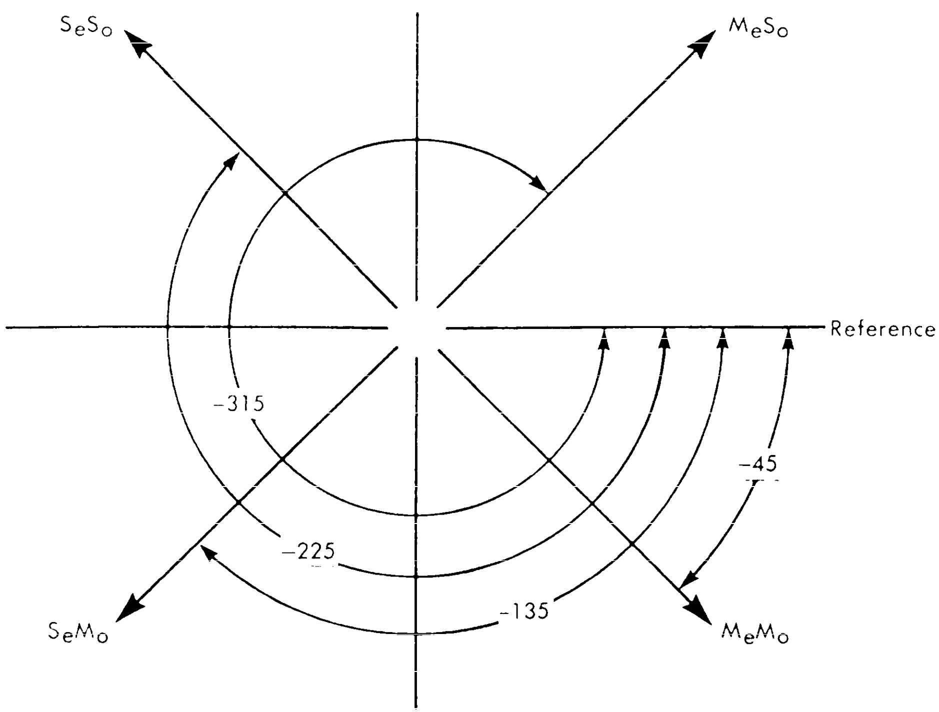
5.1.3.3.3 Information segment frame level. The requirements for the information segment frames shall be the same as the requirements for the phase reference frame (see 5.1.3.3.2). For 0 dBm composite audio signal level across 600 ohms, the signal should have the following voltage levels:

Frame	Tones and voltage levels
Preamble:	605 Hz Doppler = 0.692 volts root-mean-square (Vrms) (1 tone) 2915 Hz sync = 0.346 Vrms (1 tone)
Phase reference and information segment:	605 Hz Doppler = 0.356 Vrms (1 tone) Data subcarrier = 0.178 Vrms (each of 15 tones)

TABLE I. Data subcarrier modulation.

1/Even bit locations	1/Odd bit locations	Tone phase relative to the tone phase during the preceding frame interval
1	1	-45 degrees
0	1	-135 degrees
0	0	-225 degrees
1	0	-315 degrees

1/The even bit locations are defined as carrying even numbered bits from 0 through 28. The odd bit locations are defined as carrying the odd numbered bits from 1 through 29.



M = Mark (Logical 1)
S = Space (Logical 0)
Subscript e refers to even bit locations
Subscript o refers to odd bit locations

FIGURE 2. Modulation vector diagram.

TABLE II. Tone library.

Number	Frequency (Hz)	Description	Bit location
1	605	Doppler	1/
2	935	Data	0 and 1
3	1045	Data	2 and 3
4	1155	Data	4 and 5
5	1265	Data	6 and 7
6	1375	Data	8 and 9
7	1485	Data	10 and 11
8	1595	Data	12 and 13
9	1705	Data	14 and 15
10	1815	Data	16 and 17
11	1925	Data	18 and 19
12	2035	Data	20 and 21
13	2145	Data	22 and 23
14	2255	Data	24 and 25
15	2365	Data	26 and 27
16	2915	Data/sync	28 and 29 1/

1/There is no bit location associated with the 2915 Hz sync tone during preamble (see 5.1.4.1) or with the 605 Hz Doppler tone.

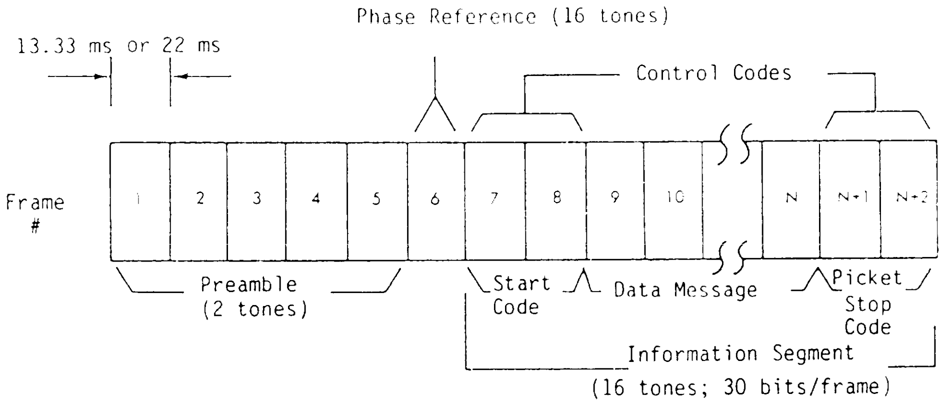
5.1.3.4 Data rate. The data rates shall be 2250 bits per second (bps) corresponding to a frame length of 13.33 milliseconds, or 1364 bps corresponding to a frame length of 22 milliseconds.

5.1.4 Transmission format. Each transmission shall be composed of preamble, phase reference, and information segment frames as shown in FIGURES 3 and 4.

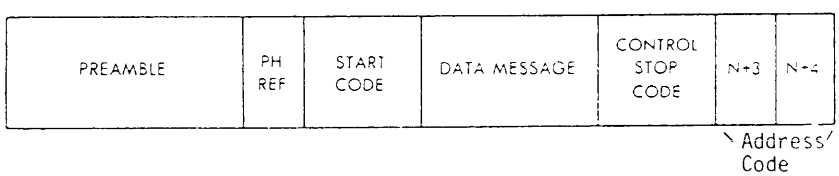
5.1.4.1 Preamble. The preamble shall be the first five frames of every transmission and shall be a 2-tone signal consisting of a 605 Hz and a 2915 Hz tone. The 605 Hz tone shall be used for Doppler correction (see 5.2.7) and the 2915 Hz tone shall be used for synchronization (see 5.2.6). The 2915 Hz tone shall be phase shifted 180 degrees each successive frame, enabling the receiving unit to detect frame transitions.

5.1.4.2 Phase reference frame. Except for a net sync transmission (see 5.1.6.5), the phase reference frame shall immediately follow the preamble, shall be composed of the normal 16-tone composite, and shall serve as the phase reference for the first frame of the information segment.

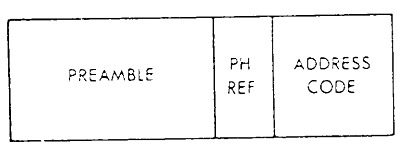
5.1.4.3 Information segment. The information segment shall be a 16-tone composite signal consisting of control code frames and data message frames. The first control code frame shall immediately follow the phase reference frame.



Picket Reply Transmission

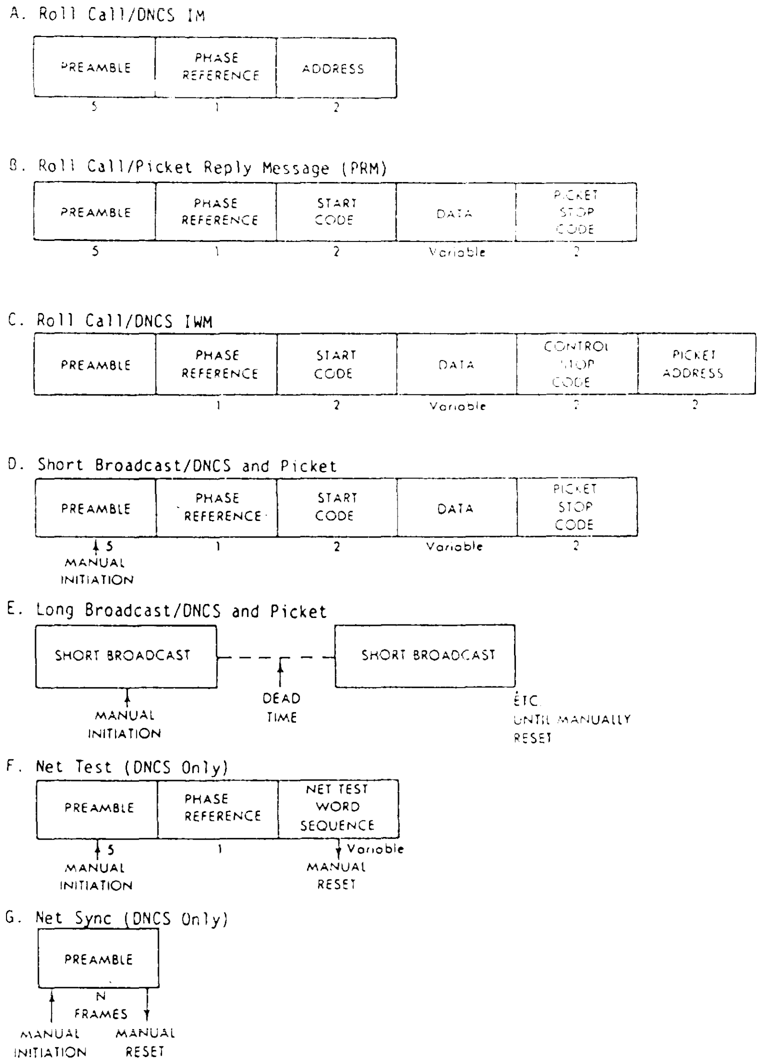


Data Net Control Station (DNCS) Transmission with Data (Roll Call/DNCS Interrogation with Message (IWM)).



DNCS Transmission without Data (Roll Call/DNCS Interrogation Message (IM)).

FIGURE 3. Roll call transmission formats.



H. Radio Silence: Receive Only -- No Transmission

NOTE: Numbers indicate the number of frames

FIGURE 4. Transmission frame structure.

5.1.4.3.1 Control code frames. The three basic control codes which are used to operate the net shall be the start code, stop code, and address code. Each control code shall consist of two 30-bit frames, encoded according to TABLE III. The receiving terminal shall be capable of correctly recognizing a control code containing four or fewer bit errors per frame.

5.1.4.3.1.1 Start code. With the exception of the roll call DNCS interrogation message (see 5.1.6.1.1), the start code shall be the first two frames of the information segment of the transmission and shall be used by the receiving system (DNCS or picket) to signal the associated TDS computer in accordance with APPENDIX D1, D2, or D3 as applicable (see 5.1.11) to prepare to receive a data message. The start code shall be encoded as described in TABLE III.

5.1.4.3.1.2 Stop code. The stop code shall be a 2-frame code immediately following the last data message frame (see 5.1.4.3.2) to signify the end of the data message. There are two unique stop codes which are identified in 5.1.4.3.1.2.1 and 5.1.4.3.1.2.2.

5.1.4.3.1.2.1 Control stop code. The control stop code shall be a 2-frame code consisting of all "zeros" and shall be only used following a data message in a transmission from the DNCS when in the roll call mode. The control stop code shall be a signal to all participating units that an address code follows immediately. Receipt of the control stop code shall cause each picket unit to: (a) signal the associated TDS computer in accordance with APPENDIX D1, D2, or D3 as applicable (see 5.1.11) that the end of the message has occurred, and (b) search for an address code in the next two received frames.

5.1.4.3.1.2.2 Picket stop code. The picket stop code shall be a 2-frame code consisting of all "ones"s that shall follow the data message in a picket transmission or a short or long broadcast transmission (see 5.1.6). Receipt of the picket stop code by net member units shall cause them to signal the associated TDS computers in accordance with APPENDIX D1, D2, or D3 as applicable (see 5.1.11) that the end of the message has occurred. Receipt of a picket stop code by the DNCS operating in the roll call mode additionally shall cause the DNCS to initiate the processing necessary to generate an interrogation message or an interrogation with message as appropriate (see 5.1.6.1).

5.1.4.3.1.3 Address code. Each net participating unit (PU) shall be identified by a unique 6-bit PU address, octal 01 through 76. The address code shall be a 2-frame code generated by the DNCS to identify the next picket to transmit. The address code shall immediately follow the control stop code if the DNCS transmitted data or the phase reference frame if the DNCS did not transmit data (see 5.1.6.1.1). The PU addresses shall be encoded as defined in TABLE III. All DTSs shall be capable of generating and recognizing all address codes defined in TABLE III. Each PU address shall be operator-selectable based on the octal address shown in TABLE III. Two methods of address generation shall be provided (see 5.2.1).

TABLE III. Library of control codes.

	Bit Locations in First Frame of Code																													
Start	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1
Control stop 1/ 2/	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Picket stop 1/ 2/	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
PU Address	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
01	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1
03	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1
07	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1
17	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1
37	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1
76	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0
75	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1
72	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0
65	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1
52	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0
25	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1
53	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1
26	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0
54	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0
31	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1
63	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1
46	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0
15	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1
33	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1
67	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1
56	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0
35	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1
73	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1
66	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0
55	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1
32	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0
64	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0
51	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1
22	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0
44	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0
11	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1
23	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1
47	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1
16	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0

TABLE III. Library of control codes. (continued)

PU Address	Bit Locations in First Frame of Code																													
	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
34	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0
70	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0
61	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1
42	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0
05	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1
13	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1
27	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1
57	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1
36	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0
74	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0
71	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1
62	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0
45	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1
12	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0
24	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0
50	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0
21	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1
43	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1
06	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0
14	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0
30	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0
60	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0
41	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1
02	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0
04	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0
10	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0
20	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0
40	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0

TABLE III. Library of control codes. (continued)

	Bit Locations in Second Frame of Code																													
Start	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0
Control stop	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Picket stop	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
PU Address	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
01	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1
03	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0
07	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0
17	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0
37	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1
76	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1
75	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1
72	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1
65	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1
52	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0
25	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0
53	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1
26	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0
54	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1
31	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0
63	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0
46	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0
15	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1
33	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1
67	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0
56	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0
35	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0
73	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0
66	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1
55	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0
32	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0
64	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0
51	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0
22	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0
44	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1
11	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1
23	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1
47	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1

TABLE III. Library of control codes. (concluded)

PU Address	Bit Locations in Second Frame of Code																													
	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
16	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1
34	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1
70	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0
61	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1
42	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0
05	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1
13	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0
27	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1
57	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1
36	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0
74	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0
71	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1
62	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1
45	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0
12	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1
24	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1
50	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1
21	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0
43	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1
06	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1
14	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0
30	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1
60	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0
41	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0
02	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1
04	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0
10	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0
20	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1
40	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1

1/ With the exception of control stop and picket stop codes, the two-frame control codes listed are equivalent to 60-bit portions of the maximum-length shift register sequence with generator polynomial: $G(X) = X^5 + X + 1$

2/ With the exception of control stop and picket stop codes, the first six bits of the control codes listed (bits 0 through 5 of the first frame) are the binary equivalents of the octal PU addresses.

5.1.4.3.2 Data message frames. The data message shall be that portion of the transmission containing tactical information. The data message shall be composed of any number of frames, each consisting of 30 data bits, and shall immediately follow the start code.

5.1.5 Error detection and correction (EDAC). An EDAC capability shall be provided as described in 5.2.4.

5.1.6 Modes of operation. The modes of operation and structure of transmission shall be as defined in 5.1.6.1 through 5.1.6.6.

5.1.6.1 Roll call . The roll call (see FIGURE 4) mode is the normal mode of operation of a TADIL A net. In the roll call mode, data are disseminated throughout the net by the automatic reporting of pickets in response to the interrogations by the DNCS. The DNCS shall be capable of interrogating all stations in the net in any sequence and inserting its own data transmission at any point in the sequence.

5.1.6.1.1 Roll call (DNCS) . A manual initiation shall be required at the DNCS (see FIGURES 4A and 4C) to start the automatic interrogation of the pickets. The order of the interrogation shall be as established by the operator in the DTS PU address table or as supplied by the TDS computer (see 5.2.1). The DNCS in the roll call mode shall normally allot 15 frames for reception of the responding picket's start code. The allotted number of frames shall be measured from the end of the second frame of the address code at the DNCS audio output to the end of the second frame of the picket's start code at the DNCS audio input. If the start code is not received within the allotted number of frames, the DNCS shall automatically send another interrogation to the addressed picket. This second interrogation shall be accomplished without requesting the TDS computer or DTS PU address table to resupply the picket address. If the DNCS does not receive the start code in response to the second interrogation within the allotted number of frames, it shall proceed as indicated in 5.1.6.1.1a or 5.1.6.1.1b. The DNCS shall be capable of extending the allowable response time for designated pickets to accommodate satellite or other special links. The extended allowable response time shall be in the range of 15 frames to 250 frames, in 1 frame increments, as an operator-selectable parameter. Designation of pickets for the extended time allowance in lieu of the normal 15 frames shall be under operator control. A manual action shall be required at the DNCS in order to stop the automatic interrogation of the pickets. (See APPENDIX C for a description of the roll call mode.) The structure of the transmissions of the DNCS in the roll call mode shall be one of the following:

a. IM. The DNCS shall transmit a frame structure (FIGURE 4A) consisting of the preamble, phase reference, and address code of the next picket to be interrogated if the next station in the reporting sequence is not the DNCS and any of the following occurs:

1. A picket stop code is recognized after a start code is recognized.

2. Loss of signal presence (see 5.2.5) is determined.
3. A picket reply to the second interrogation is not received.

b. IWM. The DNCS shall transmit a frame structure (FIGURE 4C) consisting of the preamble, phase reference, start code, any number of data message frames, control stop code, and address code of the next picket to be interrogated if the next station in the reporting sequence is the DNCS and either of the following occurs:

1. A picket stop code is recognized after a start code is recognized.
2. Loss of signal presence (see 5.2.5) is determined.
3. A picket reply to the second interrogation is not received.

5.1.6.1.2 Roll call (picket). Upon recognizing its own address code, a picket in the roll call (see FIGURE 4B) mode shall automatically transmit a PRM which has the following structure:

a. Preamble and phase reference
b. Start code
c. Any number of message frames
d. Picket stop code

5.1.6.2 Short broadcast. After manual initiation, any station in the short broadcast (see FIGURE 4D) mode shall send a single transmission with the following structure:

a. Preamble and phase reference
b. Start code
c. Any number of message frames
d. Picket stop code.

5.1.6.3 Long broadcast. After manual initiation, any station in the long broadcast (see FIGURE 4E) mode shall send a series of short broadcast transmissions. After each picket stop code, the station shall automatically inhibit the transmitter output for a 2-frame interval. The station shall then automatically send another transmission with the same structure. Once set as a result of manual initiation of transmissions, the radio transmit keyline (see 5.2.8.1.5) shall remain set until the series of transmissions is terminated. A manual action shall be required to terminate the series of transmissions.

5.1.6.4 Net test. The net test (see FIGURE 4F) mode shall allow the DNCS to transmit a known test signal and shall allow all pickets to verify their equipment performance by comparing the transmitted signal with an identical locally generated signal. The net test transmission shall be initiated and terminated manually.

5.1.6.4.1 Net test (DNCS). After manual initiation, the DNCS in the net test mode shall send a transmission with the following frame structure:

a. Preamble and phase reference

b. Word sequence shown in TABLE IV. The transmitted sequence shall begin with word 1 and shall end with word 21. After word 21 is transmitted, the word sequence shall be repeated until the transmission is terminated.

5.1.6.4.2 Net test (picket). A picket in the net test mode shall remain in the receive state awaiting receipt of the net test signal from the DNCS. Receipt of the net test signal shall cause the picket to compare the received digital word sequence with a locally generated digital word sequence identical to the sequence shown in TABLE IV. A net test error indicator shall be provided to the operator when the received word sequence is at variance with the locally generated word sequence. In addition, a capability shall be provided to permit measurement of BER while receiving the net test signal.

5.1.6.5 Net sync (DNCS). After manual initiation, the DNCS in the net sync (see FIGURE 4G) mode shall continuously transmit preamble frames. A manual action shall be required to terminate transmission. A picket shall indicate receipt of the preamble frames as specified in 5.2.5.1.

5.1.6.6 Radio silence. In the radio silence (see FIGURE 4H) mode, the radio set keyline and the DTS audio output shall be inhibited. The receive capability shall not be degraded. The radio silence mode shall be manually initiated and terminated. If the DTS is placed in radio silence while it is in the transmit mode, the DTS shall respond as follows:

a. Upon receipt of radio silence command, the DTS shall immediately inhibit both the radio set keyline and the transmit audio output.

b. After receipt of radio silence command, the DTS shall continue with normal operation of the DTS-to-TDS computer interface (see 5.1.11 and APPENDIX D1, D2, or D3 as applicable) until the in-process transmission sequence is terminated by the computer. The DTS shall then revert to normal receive operations.

5.1.7 Switching time. A time period shall be allocated to allow for the switching between the transmit and receive states. This switching shall be automatic and shall conform with the timing diagram illustrated in FIGURE 5.

a. Receive-to-transmit switching occurs when the picket recognizes its address code, the DNCS recognizes a picket stop code, or the DNCS detects loss of signal presence. When switching from the receive to transmit state, a silent period of 10 milliseconds shall be required during which the audio output from the DTS to the transmitter shall be inhibited. The audio composite signal shall be applied to the transmitter by the DTS within three frame intervals of the beginning of the silent period. The DTS shall apply the radio keyline a minimum of 7 milliseconds and a maximum of one frame

TABLE IV. Net test word sequence.

PU ADDRESS OCTAL	FRAME	Word Number	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
START (77)	1	1	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1
	2	2	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0
72	1	3	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0
	2	4	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1
25	1	5	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1
	2	6	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0
54	1	7	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0
	2	8	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1
46	1	9	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0
	2	10	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0
67	1	11	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1
	2	12	0	1	0	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0
72	1	13	1	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1
	2	14	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0
32	1	15	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0
	2	16	0	1	1	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0
22	1	17	1	1	1	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0
	2	18	1	0	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0
23	1	19	1	1	1	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1
	2	20	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1
34	1	21	0	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0	1	1	1	0	0

interval prior to the application of the audio composite signal. After application of the audio composite signal and radio set keyline, the transmitter RF output shall reach at least 90 percent of its rated power within 7.0 milliseconds.

b. Transmit-to-receive switching occurs at the end of the transmission, that is, the picket stop code or address code. When switching from the transmit to receive state, the transmitter RF output shall be reduced to the quiescent noise level of 0.1 microvolt (μV) or less in a 6 kHz bandwidth centered on the nominal carrier frequency, and the receiver shall be capable of maximum receive sensitivity within 23 milliseconds or less after reset of the radio set keyline.

5.1.8 Diversity operation. For a TADIL A net employing HF transmission, frequency diversity operation shall be obtained by transmitting identical signals simultaneously on the USB and LSB of the HF transmitter (ISB). At the receiver, both sidebands shall be separately and independently demodulated. A means shall be provided to allow operator selection of USB, LSB, or the diversity operating modes as described in 5.1.8a and 5.1.8b. For HF operation in the SSB mode or for UHF operation, only one sideband of the DTS is utilized.

a. DIV. Data words derived from the DIV combination of the USB and LSB shall be provided to the computer.

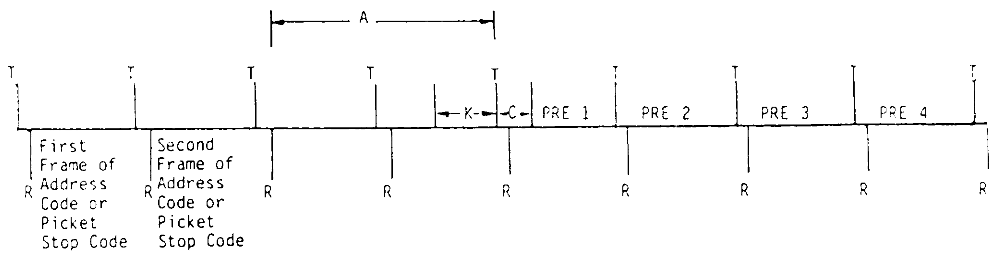
b. Automatic. The receiving station shall automatically select the version that represents the best information available from the USB, LSB, or DIV version of the received data word. When the criteria do not establish a clear choice, the DIV version shall be selected. DIV operation is used to help combat multipath interference that can be very prevalent in the HF band.

5.1.9 Frame synchronization. The capability of the DTS to synchronize to a TADIL A signal shall be as specified in 5.2.6.

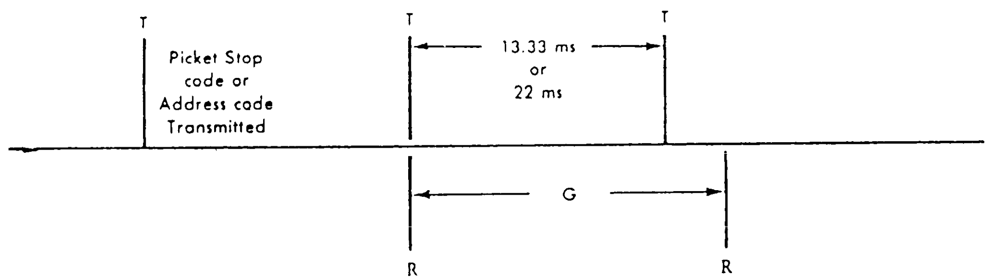
5.1.10 Doppler correction. The receiving DTS shall correct for Doppler frequency shifts resulting from relative motion between terminals, variations of the HF channel, and HF carrier frequency (f_C) inaccuracy. The standards for Doppler frequency shift and rate of change are specified in 5.2.7.

5.1.11 DTS-to-TDS computer interface characteristics. The DTS-to-TDS computer interface shall be in accordance with the requirements of one of the following: APPENDIX D1 for the NTDS parallel interface, APPENDIX D2 for the ATDS Serial interface, or APPENDIX D3 for the MIL-STD-188-114 interface. If any device, for example, control or encryption, is inserted between the system and the tactical computer, consideration must be given by the device designer and the tactical software designer to time delays introduced by that device and its effects on the interface timing relationships.

5.1.12 Radio-to-RF distribution interface. The radio-to-RF distribution interface (for example, couplers, tuners, antennas, and so forth) shall satisfy the applicable HF and UHF radio requirements of 5.3.



RECEIVE-TO-TRANSMIT TIMING



TRANSMIT-TO-RECEIVE TIMING

LEGEND:
A - DTS audio output inhibit period equals 10 milliseconds, minimum; 3 frames maximum
C - Time during which transmitter must reach 90 percent rated power equals 7 milliseconds or less
R - Receive timing frame boundaries
T - Transmit timing frame boundaries
K - Period during which transmitter key command sent by DTS prior to application of audio equals 7 milliseconds, minimum; 1 frame maximum
G - Automatic gain control (AGC) release time for maximum sensitivity equals 23 milliseconds maximum

FIGURE 5. Receive and transmit switching.

5.1.13 TADIL A STA. The TADIL A STA expressed in dB is used as an overall figure of merit for a TADIL A system. When the STA test is conducted, the composite 16-tone signal at the output of the DTS shall be adjusted to a level of 0 dBm. Then, with the DTS operating in the net test mode, the level of a single transmit data tone shall be reduced until a specified BER for that tone is observed at the receive DTS. The amount of attenuation is recorded, and the tone level is reset to its nominal value. The same procedure shall be repeated for each data tone. Among all the data tones, the smallest of the 15 values of attenuation is referred to as the STA. The system STA shall be measured with the DTS audio output connected to a radio transmitter, the transmitter RF output coupled to a receiver input, and the receiver audio output connected to a DTS receive input. The STA of the TADIL A system shall be a minimum of 13 dB with a design objective of 17 dB for a receiver BER of 10^{-3} using a data rate of 2250 bps. This STA shall be achieved for receiver RF input levels between -85 dBm and -6 dBm. For HF equipments, the STA shall be applicable to the USB and LSB modes individually.

5.2 DTS. The DTS shall support the TADIL A system as defined in 5.1 by performing the functions of data conversion, data error detection, and control code generation and recognition for 2-way data transfer. In addition, the DTS equipment shall perform the functions of synchronization, modulation and demodulation, radio keyline control, and computer or security equipment data transfer control.

5.2.1 Address code generation and operation. The DTS shall support the TADIL A system by generating the address codes defined in 5.1.4.3.1.3. The six-bit PU address, octal 01 through 76, shall be provided by the TDS computer or DTS PU address table, and shall be encoded according to TABLE III. The operator shall select the PU address source.

5.2.1.1 DTS PU address selection. The DTS shall provide the operator a means to enter a PU address table defining the sequence in which the net participants are to report. It shall be possible to change the reporting sequence without disrupting net operations. The PU address table shall have a capacity of at least 20 addresses, with a provision for expansion up to 62 addresses. When operating as DNCS, the DTS shall use the DTS PU address table whenever the operator has not enabled TDS computer PU address selection.

5.2.1.2 TDS computer PU address selection. When operating as DNCS, the DTS shall accept PU addresses from the TDS computer when the operator has enabled TDS computer PU address selection. The 6-bit PU address and message control bit will be provided by the TDS computer in accordance with APPENDIX D1, APPENDIX D2, or APPENDIX D3. If the message control bit is a logical one, the DTS shall generate an IWM using the address provided. If the message control bit is a logical zero, the DTS shall generate an IM using the address provided. In the event the TDS computer does not respond with a PU address within the allotted time (see APPENDIX D1, D2, or D3 as applicable), the DTS shall automatically disable the TDS computer PU address selection and revert to the operator-established DTS PU address table to continue net operation. The operator shall have the capability to reinitiate TDS computer PU address selection without the termination of net operation.

5.2.2 Recognition of control codes. The DTS shall support the TADIL A system by recognizing the control codes defined in 5.1.4.3.1. Any control code frame containing four or less bit errors per frame shall be correctly recognized.

5.2.2.1 DTS start code recognition. When the DTS recognizes a start code, it shall signal the TDS computer in accordance with APPENDIX D1, D2, or D3 as applicable (see 5.1.11) to prepare to receive a data message. Once having recognized a start code, the DTS shall not recognize another start code until recognizing a stop code or determining loss of signal presence (see 5.2.5).

5.2.2.2 DTS stop code recognition. When the DTS recognizes a stop code after having recognized a start code or determines loss of signal presence (see 5.2.5) after having detected a start code, it shall signal the TDS computer in accordance with APPENDIX D1, D2, or D3, as applicable, (see 5.1.11) that the data message reception has been terminated. When the DTS is operating as DNCS in the roll call mode and recognizes a picket stop code after recognizing a start code, or determines loss of signal presence (see 5.2.5) after having recognized a start code, it shall initiate the processing necessary to generate an IM or IWM (see 5.1.6.1.1). When the DTS is operating as a picket in the roll call mode and recognizes a control stop code after recognizing a start code, it shall decode the address code following the control stop code.

5.2.2.3 DTS address code recognition. When the DTS is operating as a picket in the roll call mode and recognizes its own address code immediately after the phase reference frame or control stop code, it shall signal the TDS computer in accordance with APPENDIX D1, D2, or D3 as applicable (see 5.1.11) to initiate the processing needed to transmit a PRM.

5.2.2.4 Control code search sequence. When the operator-selected source of received data is diversity combination, USB only, or LSB only, the data from that particular source shall be examined for control codes. When the automatic mode is selected, all three sources of received data shall be examined for control codes. The first source of data having four or less bit errors per frame shall be used by the DTS. Two successive frames containing four or less bit errors per frame, when compared to valid control codes, shall be the basis for recognition by the DTS.

5.2.3 Data message frames. The data message frames follow the start code and contain the information content of each transmission. Each data message frame shall consist of 30 bits composed of a 24-bit word provided by the TDS computer and 6 Hamming parity bits provided by the DTS. The Hamming parity bits shall be used by the DTS for error detection and correction.

5.2.4 DTS EDAC. The DTS shall add six Hamming parity bits to each 24-bit data word sent by the TDS computer. The resultant 30-bit word shall be used to phase modulate the 15 audio frequency tones generated by the DTS as described in 5.1.3.2. Only data messages shall contain Hamming parity bits. Start codes, stop codes, and address codes shall not be Hamming parity encoded. Hamming parity bit locations and parity check assignments for each message frame shall be as shown in TABLE V.

5.2.4.1 Error detection code generation. The DTS shall have the capability to determine the accuracy of the received data. An encoding scheme using the hamming method and overall odd parity shall be employed. Bit locations 24 through 29 of each message frame of every transmission shall be encoded as shown in a through f:

a. Bit 29 (column K_{16} in TABLE V) is set such that when added to bits in locations 11 through 23, the number of ones will be an odd number.

b. Bit 28 (column K_8 in TABLE V) is set such that when added to bits in locations 4 through 10 and 18 through 23, the number of ones will be an odd number.

c. Bit 27 (column K_4 in TABLE V) is set such that when added to bits in locations 1, 2, 3, 7, 8, 9, 10, 14, 15, 16, 17, 22, and 23, the number of ones will be an odd number.

d. Bit 26 (column K_2 in TABLE V) is set such that when added to bits in locations 0, 2, 3, 5, 6, 9, 10, 12, 13, 16, 17, 20, and 21, the number of ones will be an odd number.

e. Bit 25 (column K_1 in TABLE V) is set such that when added to bits in locations 0, 1, 3, 4, 6, 8, 10, 11, 13, 15, 17, 19, 21, and 23, the number of ones will be an odd number.

f. Bit 24 (column K_0 in TABLE V) is set such that when all the bits in the frame are added, the number of ones will be an odd number. Bit 24 is called the overall parity bit.

5.2.4.2 Error detection. The DTS shall be capable of detecting two bit errors or any odd number of bit errors in each received data frame using the parity bits described in 5.2.4.1. The DTS shall provide error status information to the TDS computer in accordance with the requirements of APPENDIX D1, D2, or D3 as applicable (see 5.1.11) to indicate the quality of the received frame in terms of bit errors.

5.2.4.3 Error correction. The DTS shall also be capable of correcting single bit errors in each receive data frame. This mode shall be operator selectable.

5.2.5 Signal presence. Paragraphs 5.2.5.1 and 5.2.5.2 describe the minimum signal needed for the DTS to recognize a transmission from a DNCS or picket is as specified in 5.2.5.1 and 5.2.5.2.

TABLE V. EDAC bit distribution.

Bit locations		K_0	K_1	K_2	K_4	K_8	K_{16}
1/29		x					x
28		x				x	
27		x			x		
26	EDAC	x		x			
25		x	x				
24		x					
23		x	x		x	x	x
22		x			x	x	x
21		x	x	x		x	x
20		x		x		x	x
19		x	x			x	x
18		x				x	x
17		x	x	x	x		x
16		x		x	x		x
15		x	x		x		x
14		x			x		x
13		x	x	x			x
12		x		x			x
11	DATA	x	x				x
10		x	x	x	x	x	
09		x		x	x	x	
08		x	x		x	x	
07		x			x	x	
06		x	x	x		x	
05		x		x		x	
04		x	x			x	
03		x	x	x	x		
02		x		x	x		
01		x	x		x		
00		x	x	x			

1/Parity bits occupying bit locations 24, 25, 26, 27, 28, and 29 shall be set such that when added to data bits in the indicated bit locations, each associated matrix column summation K_0, K_1, K_2, K_4, K_8, and K_{16} shall be odd.

5.2.5.1 Signal presence set and reset. The DTS shall be capable of detecting a preamble signal over the input signal-plus-noise (S+N) range of -10 dBm to +6 dBm having a signal-to-noise ratio (SNR) of 10 dB (3 kHz bandwidth) or more for a time period of at least one frame interval when in the DIV mode. This detection process is referred to as setting the signal presence function, and an indicator shall be provided to the operator upon receipt of three successive frames of preamble signal having an SNR of 10 dB or more. Once set, the signal presence function shall remain set for a 16-tone composite signal having an SNR as low as 2 dB. The signal presence function shall be reset under any of the following conditions:

a. Address code (picket station only) or start code is not recognized within two frames of detecting the phase reference frame.
b. A picket stop code is recognized.
c. A picket station recognizes its own address.
d. Two frames after a control stop is recognized.
e. Six successive frames of signal having an SNR of less than 2 dB after detection of a start code.

5.2.5.2 DTS input signal noise immunity. The signal presence detector shall not set on white Gaussian noise having a level of less than +6 dBm measured in the 300 Hz to 3050 Hz bandwidth or on impulse noise. One continuous tone at a level of 0 dBm and at any audio frequency specified in 5.1.3.1 shall not result in the signal presence detector being set.

5.2.6 DTS frame synchronization. In order for two stations to transfer data, the DTS receive frame boundaries must be in alignment with the frame boundaries of the received signal data frames. This can be accomplished by adjusting the DTS receive time base to the phase transitions occurring at the received signal frame boundaries. The synchronization modes specified in 5.2.6.1 and 5.2.6.2 shall be provided and shall be selectable by the operator. When the DTS is operating in diversity or automatic, the input exhibiting the greatest signal-to-noise (S/N) ratio shall be used to derive synchronization.

5.2.6.1 Fast synchronization. This mode of synchronization shall function on phase transitions of the 2915 Hz sync tone during the preamble. The DTS shall be capable of correcting its receive time base to a resolution of one millisecond or less with respect to the 2915 Hz sync tone after detection of two successive phase transitions of the preamble. After detecting the phase reference frame, the fast synchronization function shall be disabled for the duration of the received signal.

5.2.6.2 Fast continuous synchronization. This mode of synchronization shall use the fast synchronization mode to quickly correct the receive time base during the preamble. After fast synchronization is complete, the DTS shall continue to refine the initial resolution by adjusting its receive time base relative to the frame boundaries of the received signal. The DTS shall be capable of maintaining the resolution required to comply with the performance requirements specified in 5.2.9.1 for a receive signal the time base of which differs from its own by up to 0.1 percent.

5.2.7 DTS Doppler correction. The DTS shall use the 605 Hz tone to correct for Doppler frequency shifts up to ±75 Hz during the preamble and shall be capable of tracking the Doppler error during the ensuing data frames up to a maximum rate of 3.5 Hz per second. Under these Doppler shift conditions, the DTS shall comply with the performance requirements specified in 5.2.9.1 with a maximum SNR degradation of 1 dB. A means shall be provided whereby an operator may disable the Doppler correction.

5.2.8 DTS-to-radio interface characteristics. The interface characteristics between the DTS and the radio equipment is as specified in 5.2.8.1 through 5.2.8.1.5.2. The DTS interface with the HF and UHF radios is shown in FIGURE 6.

5.2.8.1 DTS transmit requirements. The DTS shall produce an output signal in accordance with 5.1.3.

5.2.8.1.1 Audio output impedance and level. The DTS shall provide two identical 600-ohm balanced audio outputs in accordance with the Channel Input/Output Impedances paragraph of MIL-STD-188-100 (see 4.4.3.1.4), except that the frequency range shall be 450 Hz to 3050 Hz. One output shall be designated as the USB output and the other output shall be designated as the LSB output. The output level shall be adjustable over the range of -3 dBm to +3 dBm, with a resolution of 0.3 dB, when terminated with a 600-ohm resistive load. An indication shall be provided to the operator when the DTS is in the transmit mode.

5.2.8.1.2 Peak envelope-to-rms voltage. A design objective is to minimize the peak envelope voltage (PEV)-to-rms ratio of the DTS composite 16-tone output signal without resorting to audio clipping. This may be accomplished through control of the relative phases of the 16 tones at the start of the phase reference frame. The PEV-to-rms ratio of the DTS output in all modes and data rates shall not exceed 8.5 dB (voltage ratio of 2.661).

NOTE: PEV = Peak voltage x 0.707. For a nominal 0 dBm, the rms output into 600 ohms is 0.775 Vrms. The maximum allowable peak would be (0.775 x 2.661) ÷ 0.707 = 2.92 volts (V).

5.2.8.1.3 Reserved for future use.

5.2.8.1.4 Audio output inhibit. The audio output signal level shall not exceed -60 dBm during the time that the radio transmit keyline is set to the receive condition. When a transmission is begun, audio shall be applied to the radio set in accordance with 5.1.7.

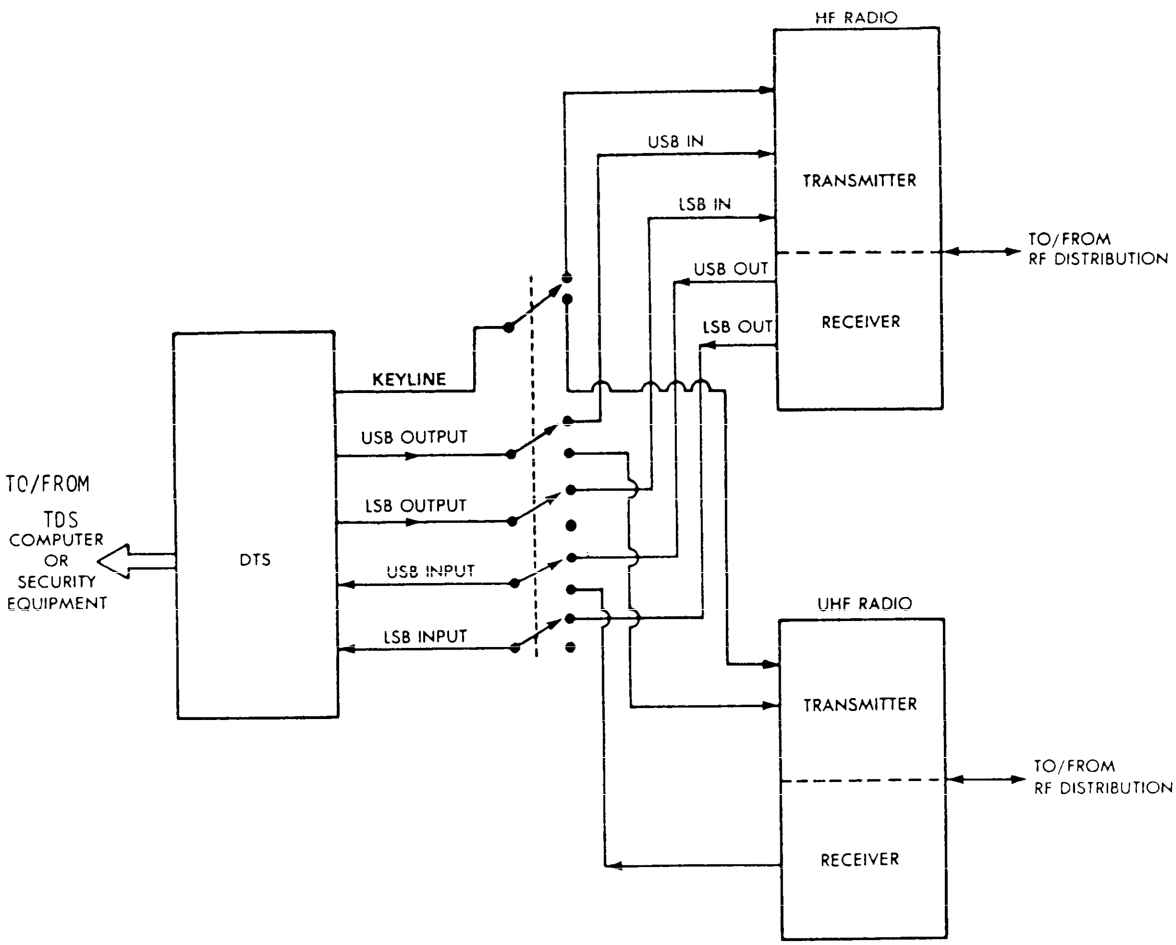


FIGURE 6. DTS-to-radio interface.

5.2.8.1.5 Radio transmit keyline. The radio transmit keyline shall be used to control the transmit and receive states of the radio equipment. Keyline timing shall be in accordance with 5.1.7. Three methods of controlling the transmit and receive states of the radio as specified in 5.2.8.1.5.1 and 5.2.8.1.5.2 shall be provided. The transmit keyline command shall be transmitted simultaneously on all keylines.

5.2.8.1.5.1 Simplex method. A signal of +6 volts direct current (VDC) (+1.0, -0.25 VDC) on the centertap of either DTS audio output shall switch the radio to the transmit state. The application of 0 VDC (+0.75, -0.25 VDC) on the centertap shall cause the radio to switch to the receive state. The minimum impedance to ground shall be 3000 ohms and current transients shall not exceed 30 milliamperes (mA).

5.2.8.1.5.2 Unbalanced-to-ground methods.

a. A signal of +6 V (+1.0, -0.25 V) on a separate unbalanced-to-ground keyline shall switch the radio to the transmit state. The application of 0 VDC (+0.75, -0.25 VDC) on the keyline shall cause the radio to switch to the receive state. The minimum impedance to ground shall be 3000 ohms and current transients shall not exceed 30 mA.

b. A ground (0 V ±0.25 V) on a separate unbalanced-to-ground keyline shall switch the radio to the transmit state. An open circuit shall cause the radio to switch to the receive state. The circuit shall be capable of sinking 10 mA. The steady-state, open circuit (unkeyed) voltage on this line shall not exceed 35 VDC.

5.2.8.2 DTS receive requirements.

5.2.8.2.1 DTS audio input impedance and level. Two balanced 600-ohm audio inputs in accordance with the Channel Input/Output Impedances paragraph of MIL-STD-188-100 (see 4.4.3.1.4) shall be provided, except the frequency range shall be 450 Hz to 3050 Hz. One input shall be designated as the USB input and the other input shall be designated as the LSB input. The nominal DTS input level(s) shall be 0 dBm. A means shall be provided to determine the DTS input levels.

5.2.8.2.2 Sidetone monitoring. The DTS shall be capable of receiving sidetone audio when in the transmit state. The sidetone audio will be provided by the TADIL A radio as specified in 5.3.1.5. Data resulting from demodulation of the received sidetone shall be compared with the transmitted data and the operator shall be informed by an indicator whenever the sidetone data does not match the transmitted data.

5.2.9 DTS performance measures. Any DTS designed to meet TADIL A technical requirements shall satisfy both the performance requirements of 5.2.9.1 and 5.2.9.2 for BER and STA, respectively.

5.2.9.1 BER. After signal acquisition (see 5.2.5 and 5.2.6), the DTS shall operate back-to-back (DTS output connected to DTS input) with an average BER of not more than 10^{-3} over the input signal range of -20 dBm to +3 dBm, without error correction or diversity. When using nondiversity operation, the DTS shall operate at 2250 bps with an average BER of not more than 10^{-3} over the input S+N range of -3 dBm to +3 dBm without error correction, when the input signal (USB or LSB) has an SNR of 12 dB using externally injected white Gaussian noise measured in a 3 kHz bandwidth. When using diversity operation, the DTS shall operate at 2250 bps with an average BER of not more than 10^{-3} over the input S+N range of -3 dBm to +3 dBm without error correction when the input signal (USB or LSB) has an SNR of 9.5 dB using externally injected white Gaussian noise measured in a 3 kHz bandwidth.

5.2.9.2 DTS STA. The DTS STA shall be measured as specified in 5.1.13, except that a DTS audio output is connected to a DTS audio input. The STA of the DTS shall be 20 dB with a design objective of 22 dB for a received BER of 10^{-3} using a data rate of 2250 bps. This STA shall apply to the USB and LSB modes individually.

5.3 TADIL A radio requirements. The TADIL A radio equipment shall support the TADIL A system as specified in 5.1 by performing the functions of amplification, translation from audio to HF or UHF, and transmit and receive switching under the control of the DTS. Radio equipments used for TADIL A communications shall satisfy the requirements stated in the applicable MIL-STD-188 series documents.

5.3.1 General requirements. The requirements specified in 5.3.1.1 through 5.3.1.9 apply to both HF and UHF radio equipments, except where separately specified.

5.3.1.1 Audio interface. The audio interface for the transmitter input and the receiver output is specified in 5.3.1.1.1 through 5.3.1.1.3.

5.3.1.1.1 Audio impedances. The audio input and output impedances of the radio equipment shall be 600 ohms balanced in accordance with the Channel Input/Output Impedances paragraph of MIL-STD-188-100 (see 4.4.3.1.4).

5.3.1.1.2 Audio input level. The nominal transmitter audio input level shall be 0 dBm.

5.3.1.1.3 Audio output level. The nominal receiver audio output level shall be 0 dBm. The level of the output(s) shall be adjustable over the range of +3 dB to -3 dB when terminated with a 600-ohm resistive load. At installation, the output(s) shall be adjusted to provide a nominal 0 dBm input(s) to the DTS. The audio output(s) shall be inhibited during periods of frequency tuning.

5.3.1.2 Radio keyline. The transmit and receive states of the radio equipment shall be capable of being controlled by the simplex keyline method specified in 5.2.8.1.5.1.

5.3.1.3 Transmit and receive switching time. The switching time requirements shall be in accordance with 5.1.7.

5.3.1.4 Phase jitter (stability). The rms phase jitter shall not exceed 2.5 degrees and the probability of a shift greater than 30 degrees shall be less than or equal to 0.01 percent when measured at the signal output terminals of a transmitter or a receiver. Measurements shall be performed over a sufficient number of adjacent frame pairs to establish the specified probability with a confidence of at least 95 percent. Measured values shall be the average phase in an averaging time of 9.09 milliseconds or 18.18 milliseconds for frame lengths of 13.3 milliseconds or 22 milliseconds, respectively.

5.3.1.5 Sidetone. During transmitter operation, a sidetone signal having the same characteristics as specified for normal received data shall be provided at the receiver audio output. For UHF systems, the sidetone shall be provided at the receive audio output; for HF systems, the sidetone shall be provided at the receiver USB or LSB audio output, or both, depending on operating mode.

5.3.1.6 Frequency selection time. The time from the selection of new frequency channel to the time that the radio set is operative for either transmission or reception on the new channel shall not exceed 10 seconds. If the radio is operated with an external automatic antenna coupler or multicoupler, the coupler tuning time should not exceed 60 seconds.

5.3.1.7 Duty cycle. The radio equipment shall be capable of operating with a 100-percent transmit duty cycle. This duty cycle requirement shall apply under all applicable service conditions.

5.3.1.8 Radio equipment delay. The radio equipment delay is specified in terms of maximum time delay and differential time delay. The maximum time delay is defined as the maximum time required for an in-band signal to propagate through the equipments, resulting in the desired output. Receiver AGC and transmitter automatic level control operation are assumed to be stabilized for the purpose of this measurement. The differential time delay between two in-band signals is defined as the difference in time for each of the two signals to propagate through the equipment or result in the desired output.

5.3.1.8.1 Maximum time delay. The maximum time delay measured between input and output of either the transmitter or receiver for any single frequency over the range of 500 Hz to 3050 Hz shall be less than 3.5 milliseconds (DO of 2.5 milliseconds) (see FIGURE 7).

5.3.1.8.2 Differential time delay. The differential time delay that results between any two audio tones within the frequency range of 815 Hz to 3050 Hz for either the transmitter or receiver shall not exceed 500 microseconds (see FIGURE 7).

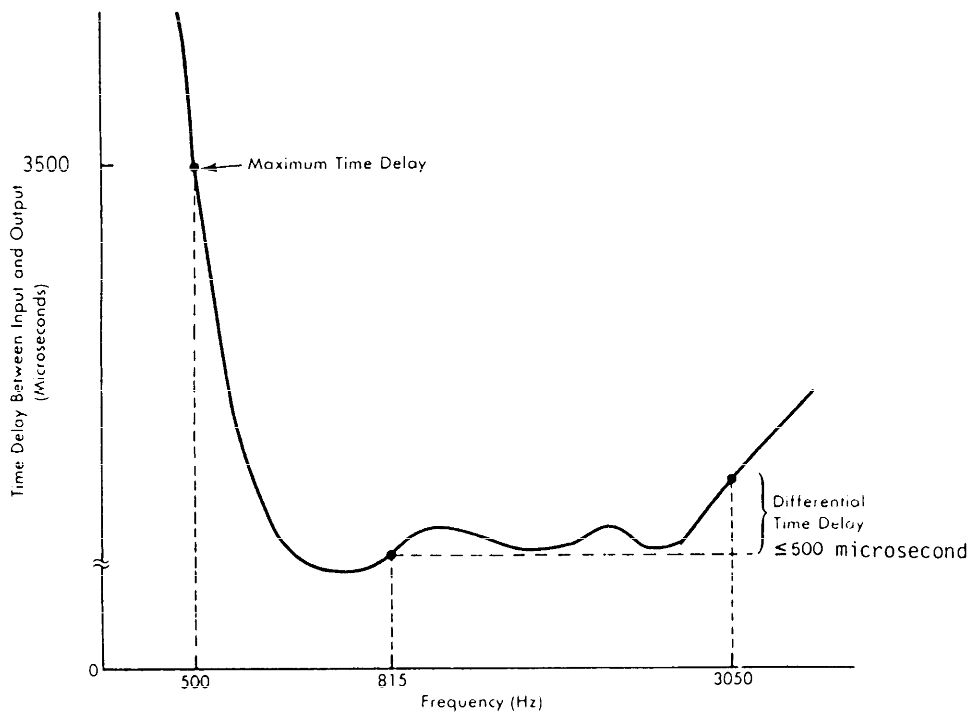


FIGURE 7. Time delay definitions.

5.3.1.9 RF terminations. The nominal impedance at the receiver RF input terminal shall be 50 ohms unbalanced to ground. The transmitter RF output load impedance shall be a nominal 50 ohms, unbalanced to ground. The transmitter shall be protected against failures induced by a voltage standing wave ratio (VSWR) greater than 4:1.

5.3.2 HF radio requirements. The HF radio set shall provide TADIL A data transmission and reception in the HF band of the RF spectrum.

a. The HF transmitter shall have the capability to:
   1. Transmit on USB only
   2. Transmit on LSB only
   3. Transmit on both USB and LSB simultaneously [DIV (ISB)]
b. The HF receiver shall have the capability to:
   1. Receive on USB only
   2. Receive on LSB only
   3. Receive on both USB and LSB independently [DIV (ISB)]

5.3.2.1 General HF requirements.

5.3.2.1.1 HF frequency coverage. The frequency coverage shall be as specified in 5.1.1. The frequency readout shall be calibrated in terms of the suppressed f_c.

5.3.2.1.2 HF accuracy and stability. The frequency adjustment control of a transmitter and receiver shall permit either equipment to be periodically calibrated or aligned within 1 part in 10^9 of any designated frequency. The frequency stability with respect to the initial frequency, shall be within 1 part in 10^8 per day, 5 parts in 10^8 during the first 30 days after calibration. The stability shall not be degraded by more than 4 parts in 10^8 per each 30-day period thereafter.

5.3.2.2 HF receiver characteristics. The receiver design shall satisfy the TADIL A system STA requirements of 5.1.13.

5.3.2.2.1 HF audio outputs to the DTS. Separate USB and LSB audio outputs with the characteristics described in 5.3.1.1 shall be provided. When the receiver is operated in the USB or LSB mode, the audio output shall be at the respective audio output channel. When operating in the ISB mode, the audio output shall be on both audio output channels.

5.3.2.2.2 Audio balance. When operating in the ISB mode and with equal USB and LSB signals applied to the RF input, the difference in output level between USB and LSB audio outputs shall not exceed 0.5 dB.

5.3.2.2.3 HF receiver sensitivity. The sensitivity of the receiver in the USB or LSB mode over the specified frequency range shall be such that an RF input signal of -110 dBm applied to the receiver input terminals of the HF radio set shall produce a minimum signal-plus-noise-to-noise (S+N/N) ratio of 10 dB. The same sensitivity applies to either sideband when in the ISB mode of operation.

5.3.2.2.4 HF receiver selectivity. The overall selectivity of the receiver shall satisfy the following limits (with respect to f_c and peak in-band response from 450 Hz to 3050 Hz):

a. USB:
Not more than 2.0 dB down at f_c +450 Hz to f_c +3050 Hz
Not more than 3.0 dB down at f_c +300 Hz
More than 60.0 dB down at f_c -400 Hz and f_c +4400 Hz

b. LSB:
Not more than 2.0 dB down at f_c -450 Hz to f_c -3050 Hz
Not more than 3.0 dB down at f_c -300 Hz
More than 60.0 dB down at f_c +400 Hz and f_c -4400 Hz

c. ISB: Same as USB and LSB

The peak-to-valley ratio shall not be more than 2.0 dB from 450 Hz to 3050 Hz and the slope of the response between the 2.0 dB and 60.0 dB points shall be a monotonic transition (free from regeneration).

5.3.2.2.5 HF input signal protection. The receiver shall not be damaged by the application of any input RF signal up to +53 decibels referred to one milliwatt (dBm) (open circuit peak value) applied to the receiver input terminals.

5.3.2.2.6 HF in-band intermodulation. With two input signals of -53 dBm each, at frequencies selected to produce audio outputs in the 450 Hz to 3050 Hz range, the intermodulation distortion products measured at the audio output shall be at least 35 dB (DO of 40 dB) below the output level of either audio tone.

5.3.2.2.7 HF receiver AGC. Receiver AGC shall be developed for each sideband. The gain shall be such that the sideband of greater magnitude controls the gain of the RF stages. When in the SSB mode, the receiver shall prevent any AGC voltage developed by the unused sideband from controlling the RF amplifier. The amount of gain control per unit bias voltage (dB per V) should be designed to optimize linearity and S/N ratios and to minimize the effect of interfering signals.

5.3.2.2.7.1 Level control. Following the AGC attack time (see 5.3.2.2.7.2), the rms audio output level shall not change more than 6 dB over an RF input range of -100 dBm to -6 dBm. The audio output shall be a nominal 0 dBm (600-ohm resistive load).

5.3.2.2.7.2 AGC attack time. The AGC attack time (see FIGURE 8) is defined as the time between an increase in the RF input signal amplitude and the stabilization of the audio output amplitude to within 3 dB of the steady-state value due to the large signal. The receiver data mode AGC attack time shall be less than 13 milliseconds for an RF signal level increase of 10 dB or more occurring within the range from -93 dBm to +7 dBm. The attack time shall be measured using a single unmodulated RF test signal with frequency chosen to produce a receiver output frequency of 2 kHz.

5.3.2.2.7.3 AGC release time. For a decrease in RF signal amplitude from an upper level within the range of -87 dBm to +7 dBm to a lower level of -107 dBm, the data mode release (see FIGURE 8) characteristics shall be such that the audio output voltage shall be held at less than 10 percent of the steady-state output resulting from the small signal for a minimum period of 10 milliseconds following the downward transition. The total release time, measured from the time of the downward transition until the audio output has stabilized within 3 dB of the steady-state output resulting from the small signal, shall not exceed 23 milliseconds. The release time shall be measured using a single unmodulated RF test signal with frequency chosen to produce a receiver audio output of 2 kHz.

5.3.2.2.7.4 Recycle period. The receiver AGC system shall be capable of providing the specified attack and release characteristics during a repetitive attack and release cycle of 100 milliseconds or greater total duration, with equal large and small signal intervals.

5.3.2.3 HF transmitter characteristics.

5.3.2.3.1 HF transmitter audio inputs. Separate USB and LSB audio inputs with characteristics described in 5.3.1.1 shall be provided.

5.3.2.3.2 HF overall frequency response. The maximum attenuation in respect to the peak response between 450 Hz and 3050 Hz shall not exceed 2 dB. The maximum attenuation at 300 Hz with respect to the peak response between 450 Hz and 3050 Hz shall not exceed 3 dB. The transmitter peak power control and automatic level control shall be disabled during measurement.

5.3.2.3.3 HF transmitter peak envelope power-to-average power ratio (PEP/Pavg). The transmitter shall be designed to maximize the average power output to the extent permitted by equipment peak power constraints with an audio input as described in 5.2.8.1.2 and 5.3.1.1.2. For the 16-tone composite, the PEP/Pavg transmitted RF output shall not exceed 8.5 dB in the USB or LSB modes, or 11.5 dB in the DIV mode. In addition, the difference in average transmitted RF power output between the 2-tone signal of the preamble and the 16-tone composite signal shall not exceed 2 dB in any of the USB, LSB, or ISB modes.

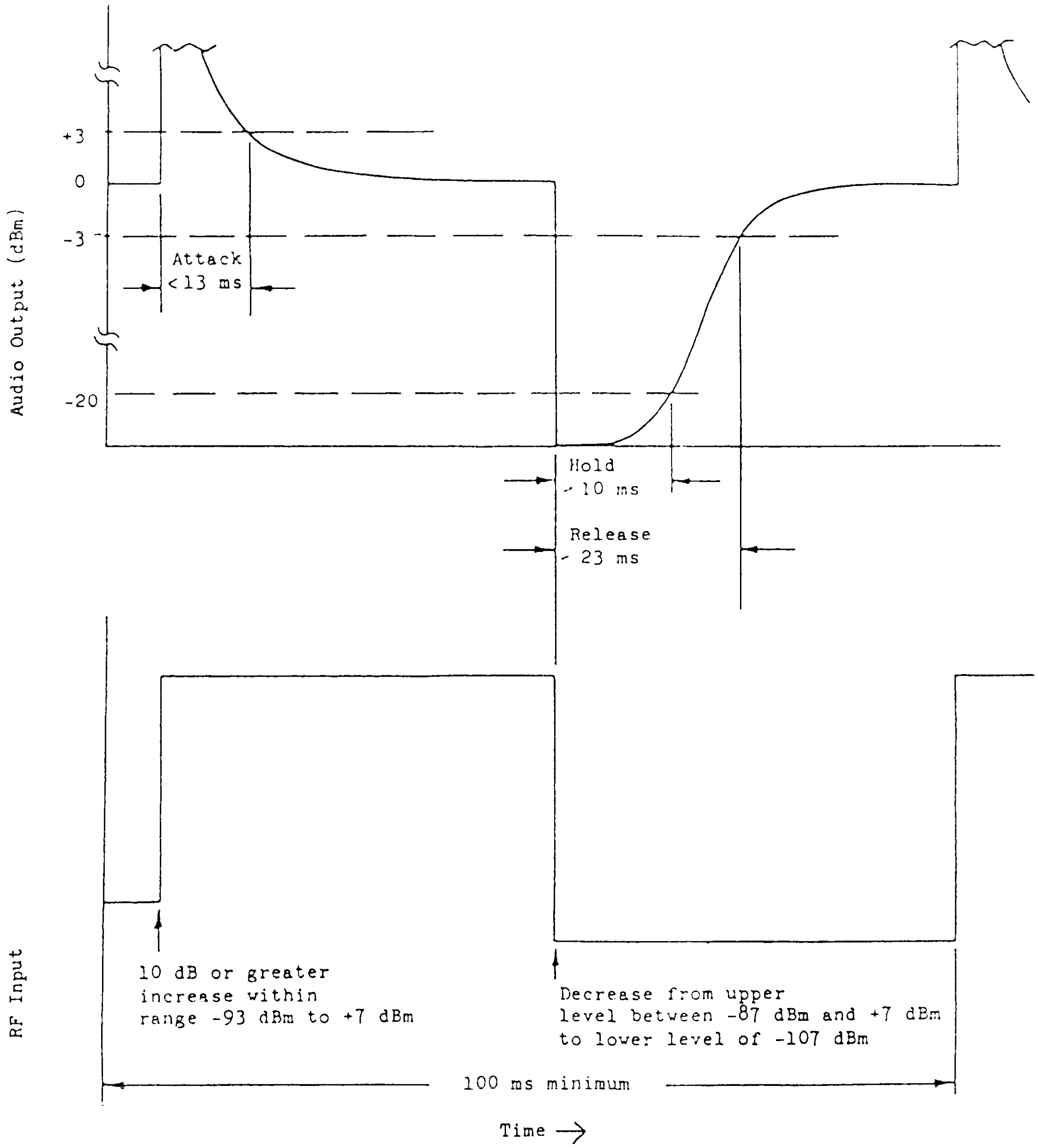


FIGURE 8. AGC attack and release times.

5.3.2.3.4 HF intermodulation. The in-band intermodulation distortion products produced by any two equal level audio tones of 440 Hz spacing within the bandpass of 5.3.2.3.2 adjusted to produce rated PEP shall be a minimum of 30 dB (DO of 35 dB) below the output due to either audio tone.

5.3.2.3.5 HF in-band noise. With the audio input terminated in a 600-ohm resistance, with no audio input signal, and no automatic level control or peak power control voltages applied, the transmitter in-band noise output into a 50-ohm resistive termination shall not exceed the levels specified in a and b for the 3 kHz information band:

a. With the equipment in the transmit state, the noise output shall be at least 45 dB below the specified PEP level.

b. With the equipment in the receive state, the noise output shall meet the requirements of 5.1.7b.

5.3.3 UHF radio requirements. The UHF radio set shall provide data transmission and reception in the UHF band of the RF spectrum. The interface with the DTS shall be with the USB audio channel.

5.3.3.1 UHF general requirements.

5.3.3.1.1 UHF frequency coverage. The UHF frequency coverage shall be as specified in 5.1.1. The frequency readout shall be in terms of f_c.

5.3.3.1.2 UHF accuracy and stability. The unmodulated transmitted carrier and receiver center frequencies shall be within ±0.0005 percent of the selected f_c after a warmup period of 5 minutes under any combination of specified service conditions.

5.3.3.1.3 Intermediate frequency (IF) selectivity (transmitter and receiver). The 6 dB bandwidth shall be at least 50 kHz and the 60 dB bandwidth shall be no more than 200 kHz. The peak-to-peak ripple over 90 percent of the 6 dB bandwidth shall not exceed 3 dB.

5.3.3.2 UHF receiver characteristics.

5.3.3.2.1 UHF audio output. A single audio output with the characteristics specified in 5.3.1.1 shall be provided.

5.3.3.2.2 UHF receiver sensitivity. The sensitivity of the receiver over the specified frequency range shall be such that an RF input test signal results in a minimum output S+N/N ratio of 20 dB as measured in a 3 kHz bandwidth. The RF input test signal shall have a level of -99 dBm and shall be FM modulated at a rate of 1 kHz with a peak deviation of ±10 kHz.

NOTE: Peak deviation is defined as the absolute maximum frequency excursion of the outer spectral component from the assigned frequency.

5.3.3.2.3 UHF frequency response. With an RF input signal level of -73 dBm with peak deviation of ±20 kHz applied to the receiver input terminals, the attenuation of the audio output relative to the peak response between 450 Hz and 3050 Hz shall not exceed 2 dB. The attenuation of the audio output, at 300 Hz, relative to the peak response between 450 Hz and 3050 Hz shall not exceed 3 dB.

5.3.3.2.4 Input signal protection. A receiver protection circuit shall be activated by RF signal level. The receiver shall not be damaged by the continuous application of a +15 dBm (DO of +35 dBm) RF signal.

5.3.3.2.5 UHF in-band intermodulation. With an input signal level of -53 dBm modulated by any two equal level tones selected to produce audio outputs in the 450 Hz to 3050 Hz range, and each producing ±10 kHz peak deviation, the intermodulation distortion products measured at the audio output shall be at least 35 dB (DO of 40 dB) below the output level of either audio tone.

5.3.3.2.6 UHF S+N/N. With a receive input signal of -53 dBm modulated at ±8 kHz peak deviation at a 1 kHz rate, the S+N/N ratio shall be 40 dB or greater as measured in a 3 kHz bandwidth.

5.3.3.2.7 UHF receiver output level stability. The audio output shall be +2.25 dBm (1.0 Vrms) ±3 dB across a 600-ohm resistive load for any receive input signal frequency modulated at a 1 kHz rate with peak deviation of ±10 kHz and with any level between -93 dBm and +1 dBm.

5.3.3.2.8 Output level and distortion. With a -53 dBm input signal modulated by a 1 kHz sine wave, and adjusted to produce a ±20 kHz peak deviation, the audio output level shall be +8.25 dBm (2.0 Vrms) ±0.5 dB into a 600-ohm resistive load. The output shall be adjustable over the range of -3 dB to +3 dB from the nominal. This procedure will result in a 0 dBm output for a 2-tone or 16-tone TADIL A signal from a transmitter adjusted in accordance with 5.3.3.3.4.

5.3.3.3 UHF transmitter characteristics.

5.3.3.3.1 UHF audio input. A single audio input with the characteristics described in 5.3.1.1 shall be provided. The center tap of the audio input shall be used for the keyline function.

5.3.3.3.2 UHF overall frequency response. The attenuation of the RF output relative to the peak response between 450 Hz and 3050 Hz shall not exceed 2 dB. The attenuation of the RF output, at 300 Hz, relative to the peak response between 450 Hz and 3050 Hz shall not exceed 3 dB.

5.3.3.3.3 UHF intermodulation. The in-band intermodulation distortion products produced by any two equal level audio tones within the bandpass specified in 5.3.3.3.2 adjusted to produce a peak deviation of ±20 kHz shall be a minimum of 35 dB below the level of either tone. Measurements shall be performed on the demodulated transmitter output.

5.3.3.3.4 UHF frequency deviation. A peak deviation of ±20 kHz shall be obtained when a 1 kHz sine wave signal at a level of +8.25 dBm (2.0 Vrms) is applied to the audio input. This procedure will result in the generation of signal exhibiting a 40 dB bandwidth of approximately 40 kHz with a 0 dBm input from the DTS operating in all modes (see 5.1.6), except net sync (see 5.1.6.5) and radio silence.

5.3.3.3.5 UHF transmitter in-band noise. With the equipment operating in the transmit state at full rated RF power output and with the audio input terminated with a 600-ohm resistor, the audio output detected in a nominal 50 Hz audio bandwidth by a test receiver shall be at least 50 dB below the audio output detected when a carrier at the same RF power level deviated ±20 kHz at a 1 kHz rate is applied to the test receiver RF input.

6. NOTES

6.1 Key words.

Data Link
Digital information link
DTS
Information link
Link
Link 11
Long-haul circuits
MIL-STD-188-203-1A
STA
Tactical Digital Information Link (TADIL)
Tactical communications circuits
TADIL A
TDS

Custodians:
Army - CR
Navy - EC
Air Force - 90

Preparing activity:
NAVY - EC

(Project TCTS-2030)

Review activities:
Army - SC
Navy - SH, AS, OM
Air Force 2, 11, 13, 19
Other - DC, TT

User activities:
Army -
Navy - MC
Air Force - 17, 89

APPENDIX A

MEMORANDUM FROM THE ASSISTANT SECRETARY OF DEFENSE FOR COMMUNICATIONS, COMMAND, CONTROL AND INTELLIGENCE, 16 AUG 1983, SUBJECT: MANDATORY USE OF MILITARY STANDARDS IN THE 188 SERIES.

This APPENDIX contains information related to MIL-STD-188-203-1A. APPENDIX A is a mandatory part of this standard.

THE UNDER SECRETARY OF DEFENSE
WASHINGTON, D.C. 20301

RESEARCH AND ENGINEERING

16 AUG 1983

MEMORANDUM FOR ASSISTANT SECRETARY OF THE ARMY (INSTALLATIONS, LOGISTICS & FINANCIAL MANAGEMENT)
ASSISTANT SECRETARY OF THE NAVY (SHIPBUILDING & LOGISTICS)
ASSISTANT SECRETARY OF THE AIR FORCE (RESEARCH DEVELOPMENT & LOGISTICS)
COMMANDANT OF THE MARINE CORPS
DIRECTOR, DEFENSE COMMUNICATIONS AGENCY
DIRECTOR, NATIONAL SECURITY AGENCY

SUBJECT: Mandatory Use of Military Telecommunications Standards in the MIL-STD-188 Series

On May 10, 1977, Dr. Gerald Dinneen, then Assistant Secretary of Defense(C^3I), issued the following policy statement regarding the mandatory nature of the MIL-STD-188 series telecommunications standards:

"...standards as a general rule are now cited as 'approved for use' rather than 'mandatory for use' in the Department of Defense.

This deference to the judgment of the designing and procuring agencies is clearly appropriate to standards dealing with process, component ruggedness and reliability, paint finishes, and the like. It is clearly not appropriate to standards such as those in the MIL-STD-188 series which address telecommunication design parameters. These influence the functional integrity of telecommunication systems and their ability to efficiently interoperate with other functionally similar Government and commercial systems. Therefore, relevant military standards in the 188 series will continue to be mandatory for use within the Department of Defense.

To minimize the probability of misapplication of these standards, it is incumbent upon the developers of the MIL-STD-188 series to insure that each standard is not only essential but of uniformly high quality, clear and concise as to application, and wherever possible compatible with existing or proposed national, international and Federal telecommunication standards. It is also incumbent upon the users of these standards to cite in their procurement specifications only those standards which are clearly necessary to the proper functioning of the device or systems over its projected lifetime."

This statement has been reviewed by this office and continues to be the policy of the Department of Defense.

APPENDIX B

ACRONYMS AND ABBREVIATIONS

10. SCOPE.

10.1 Scope. This APPENDIX provides the definition for the acronyms and abbreviations used in this standard.

AGC	Automatic gain control
ATDS	Airborne Tactical Data System
BER	Bit error rate
bps	Bits per second
CID	Computer input data
COD	Computer output data
dB	Decibel
dBm	Decibel referred to one milliwatt
DIV	Diversity
DNCS	Data net control station
DO	Design objective
DTS	Data terminal set
EDAC	Error detection and correction
EFA	External function acknowledge
EFR	External frequency response
EIE	External interrupt enable
EIR	External interrupt request
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
EOR	End-of-receive
f_c	HF carrier frequency
FM	Frequency modulation
HF	High frequency
Hz	Hertz
IDA	Input data acknowledge
IDR	Input data request
IF	Intermediate frequency
IM	Interrogation message
IRAC	Interdepartment radio advisory committee
ISB	Independent sideband
ITU	International Telecommunications Union
IWM	Interrogation with message
JTIDS	Joint Tactical Information Distribution System
kHz	Kilohertz
LSB	Lower sideband
mA	Milliamperes
MCEB	Military Communications-Electronics Board

APPENDIX B

ACRONYMS AND ABBREVIATIONS - Continued.

MHz	Megahertz
MSB	Most significant bit
nm	Nautical miles
NTDS	Naval Tactical Data System
ODA	Output data acknowledge
ODR	Output data request
PEV	Peak envelope voltage
PEP/Pavg	Peak envelope power/average power
PRM	Picket reply message
PTR	Prepare-to-receive
PTTA	Prepare-to-transmit address
PTTB	Prepare-to-transmit broadcast
PTTD	Prepare-to-transmit data
PU	Participating unit
RCV	Receive
RF	Radio frequency
S+N	Signal-plus-noise
S+N/N	Signal-plus-noise-to-noise
SNR	Signal-to-noise ratio
STA	Single tone attenuability
TADIL	Tactical Digital Information Link
TDS	Tactical Data System
UHF	Ultra high frequency
USB	Upper sideband
V	Volt
VDC	Volts direct current
Vrms	Volts root-mean-square
VSWR	Voltage-standing-wave-ratio
WARC	World administrative radio conference
XMT	Transmit

APPENDIX C

TUTORIAL INFORMATION

10. SCOPE. This APPENDIX contains general tutorial information and is not a mandatory part of this standard.

10.1 TADIL A description. TADIL A is a tactical digital information link employing netted communication techniques and a standard message format for the exchange of digital information among airborne, land-based, and shipboard tactical data systems. Data from sensors such as radar are entered into a stored program processor and, after conditioning by program routines and other routines, is time multiplexed on either HF or UHF for transmission to all participants in the net. Since each participant has the opportunity to share processor data with other net participants, each net element has access to current information regarding the tactical situation.

10.1.1 Net operation. To effectively achieve automatic netted data communications, all participants in the net must follow an orderly sequence of operation. A common time-shared radio frequency is used, restricting transmission to a single station within any given time. When not transmitting, each station monitors the frequency for transmissions from other stations. Control of net transmissions is provided by designating one participant as the data net control station (DNCS) and all other net units as subordinates (picket stations). While other modes are also available for test and broadcast, this description of net operation describes the roll call mode, which is the primary operational mode. A representative TADIL A net is shown in FIGURE 9. Each participating unit is assigned a unique address code which is used by the DNCS to establish an orderly net transmission sequence. The DNCS transmissions are in the format of an interrogation message or an interrogation with message, and both formats contain the address code of the next picket station in the reporting sequence. The interrogation with message format is used by the DNCS to transmit its own tactical computer output data, while the interrogation message format contains only the picket address. All picket stations receive the transmission, transfer the tactical data (if any) to their respective tactical computers, and compare the received address with their own. The picket station recognizing its own address code switches its data transmission equipment to the transmit condition and transmits its tactical computer output data in a reply message format. Each participating unit in the net receives the picket reply transmission and transfers the data portion to its tactical computer. At the end of the picket reply transmission, the DNCS switches to a transmit condition and again transmits either an IM or an IWM, in accordance with the established reporting sequence. Once initiated by the DNCS, this process is repeated automatically until terminated. The reporting sequence used by the DNCS may be established manually by the operator in conjunction with the address generator; or alternatively, the addresses may be supplied individually by the computer, allowing event-driven dynamic change in the reporting order. The time required for all stations to have a transmit opportunity (net cycle time) is variable and depends upon the number of net members, the amount of data each transmits, and the dynamic sequencing of the station reports when under computer control. The number of active participants in a TADIL A net is limited by the number of unique address codes (62) available in the address code library. In a manually established sequence, it is limited by the number of addresses capable of being queued by the DNCS station equipment, which varies from 15 to 64 in current equipment types. TADIL A employs a parallel transmission of data and control frames, with each frame containing 30 bits of binary coded information. A frame may be either 13.33 ms or 22 ms in duration and is selected manually. The frame length of 13.33 ms corresponds to a data rate of 2250 bps and the frame length of 22 ms corresponds to a data rate of 1364 bps.

10.2 TADIL A equipment. A representative TADIL A system configuration is illustrated in FIGURE 10. The DTS interfaces with a radio set and performs all the control functions related to net operation as described.

10.2.1 Transmission. The DTS requests and accepts tactical data in the form of a 24-bit data word, encodes the word with a 6-bit EDAC code (Hamming), and phase modulates 15 internally generated audio tones with the newly formed 30-bit word. The 15 phase-modulated audio tones and a Doppler correction tone are combined to form the composite audio signal that is applied to either the HF or UHF radio equipment for transmission. For HF transmission, suppressed carrier with ISB (DIV mode) or SSB modulation on either USB or LSB can be used. For UHF transmission, the audio output is used to frequency modulate the UHF carrier. The TADIL A radio equipment transmit and receive operation is controlled by the DTS.

10.2.2 Reception. For HF operation in the DIV mode, the radio equipment at the receiving stations translates the RF signals to audio tones that are applied to the data terminal equipment as USB and LSB composite signals. By separate demodulation of each sideband and a DIV combination, three versions of the 30-bit word are created. Each is checked for errors by Hamming tests. The tactical data selected for transfer to the computer is either manually or automatically selected. When the choice is automatic, the first source with no errors is sent to the tactical computer. If all versions have errors, the DIV combination is sent. The data from the selected source is stripped of its six EDAC bits, corrected (if required), and transferred to the tactical computer along with flag bit(s) that indicate its error content. For HF operation in the SSB mode or for UHF operation, only one sideband of the DTS is utilized.

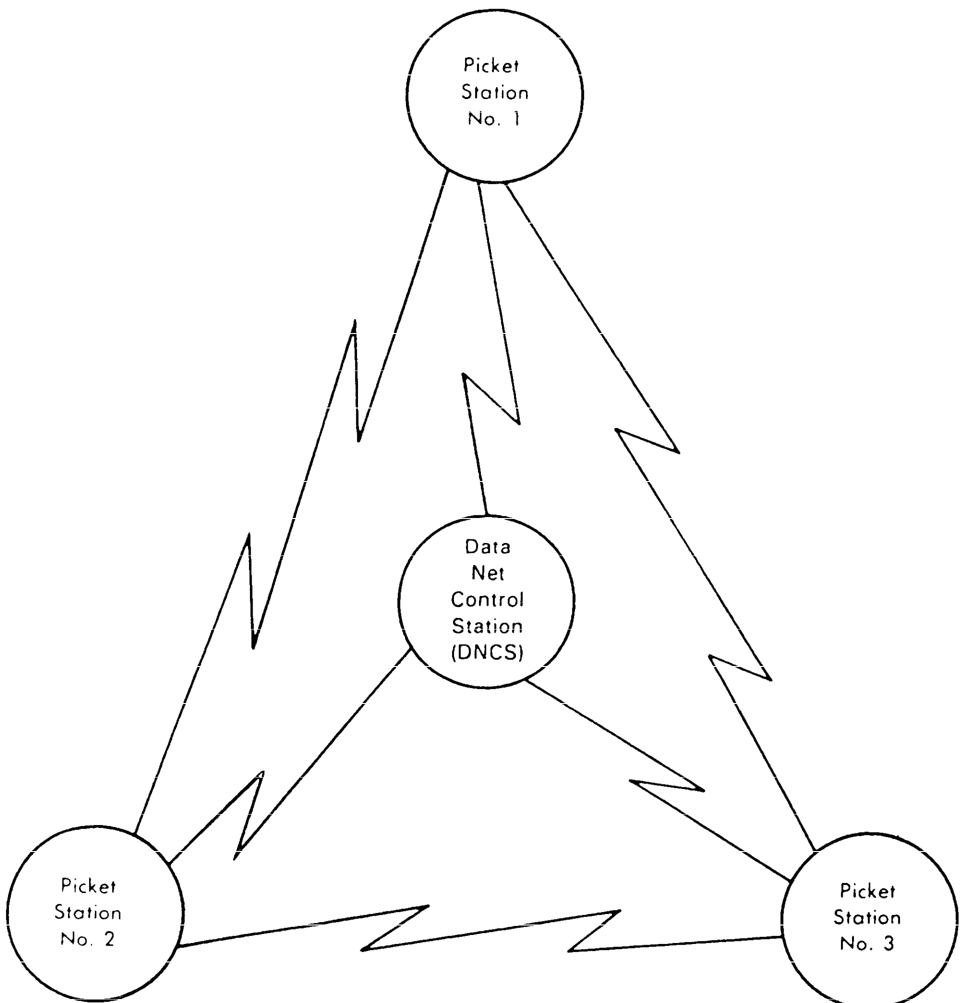


FIGURE 9. Representative TADIL A net.

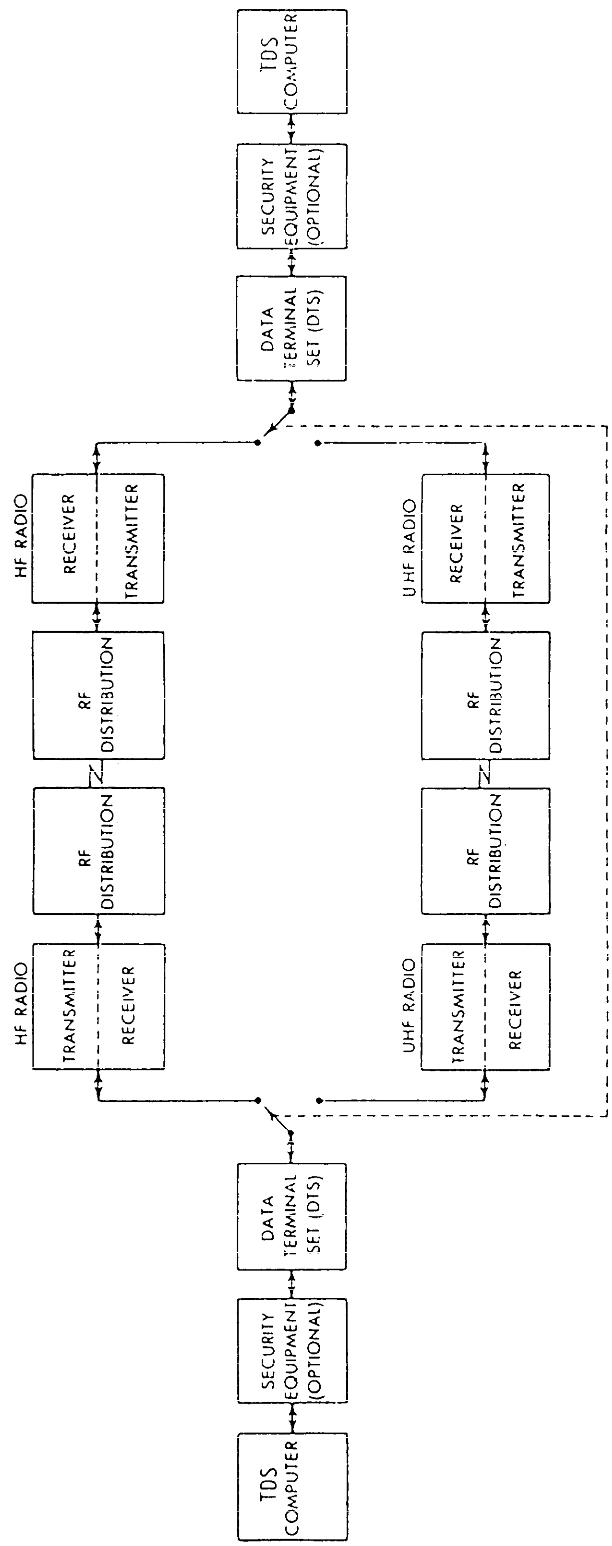


FIGURE 10. TADIL A system.

APPENDIX D1

DTS-TO-TDS COMPUTER INTERFACE - PARALLEL

10. SCOPE. This APPENDIX contains detailed information on the DTS and the TDS computer (parallel) interface and is a mandatory part of this standard.

20. APPLICABLE DOCUMENTS. This section is not applicable to this APPENDIX.

30. System-to-TDS computer interface characteristics. The TDS computer interface and electrical characteristics and timing shall be in accordance with the applicable requirements of MIL-STD-1397 for Type A, Category I (NTDS SLOW - Computer to Peripheral) interface. The TDS computer interface is shown in FIGURE 11. Input lines from the DTS to the TDS computer are described in 30.1, output lines from the TDS computer to the DTS system are described in 30.2, and transmit and receive timing are described in 30.3. By convention, all signals are referenced to the TDS computer's input and output interfaces.

30.1 TDS computer input requirements. The DTS-to-TDS computer communications control shall be via the external interrupt request (EIR), input data request (IDR), and input data acknowledge (IDA) lines as shown in FIGURE 11. The MIL-STD-1397 external interrupt enable (EIE) line is not used for communications. Data from the DTS to the TDS computer shall be transferred via the computer input (CID) lines.

30.1.1 CID lines. Twenty-six parallel CID lines convey receive data (24 bits) and error status summary (2 bits) or interrupt code information from the DTS to the TDS computer. The DTS shall place the information on these lines prior to the activation of an IDR or EIR. Error status summary bit definitions are shown in TABLE VI. Bit assignments relative to the CID lines are shown in TABLE VII.

30.1.2 EIR. The EIR shall be set by the DTS to inform the TDS computer that an external interrupt code has been placed on the CID lines by the DTS. The external interrupt codes shall be as shown in TABLE VIII. The purpose of the interrupt code words shall be as described in 30.1.2.1 through 30.1.2.6. Bit assignments for the interrupt code words shall be as shown in TABLE VII. The DTS shall reset the EIR upon detecting an IDA or after waiting the allotted time as specified in 30.3.

30.1.2.1 Interrupt code 2 - reset. A code 2 interrupt shall be generated only when the DTS is reset. When a reset is initiated during a receive sequence, the DTS shall continue to process the receive data until the end of the receive data is detected and an interrupt code 3 has been sent by the DTS to the TDS computer and acknowledged. The code 2 interrupt shall then be generated by the DTS and sent to the TDS computer one frame later.

TABLE VI. Error status summary.

Mode	Error status	Bit position	
		25 (H_C)	24 (H_0)
Detect and label	No errors detected (K_0 - K_{16} 1/ all odd)	0	0
	Error(s) detected - no correction attempted (one or more of K_0 - K_{16} even)	1	0
Detect and correct	No errors detected (K_0 - K_{16} all odd)	0	0
	Parity error detected (K_0 even, not more than one of K_1 - K_{16} even)	0	1
	Odd error(s) detected - correction attempted (K_0 even, more than one but not all of K_1 - K_{16} even; or K_0 even, more than one but not all of K_2 - K_{16} even)	1	1
	Even errors detected - no correction attempted (K_0 odd, one or more of K_1 - K_{16} even)	1	0

1/ See 5.2.4.1 and TABLE V for K_0 - K_{16} definitions.

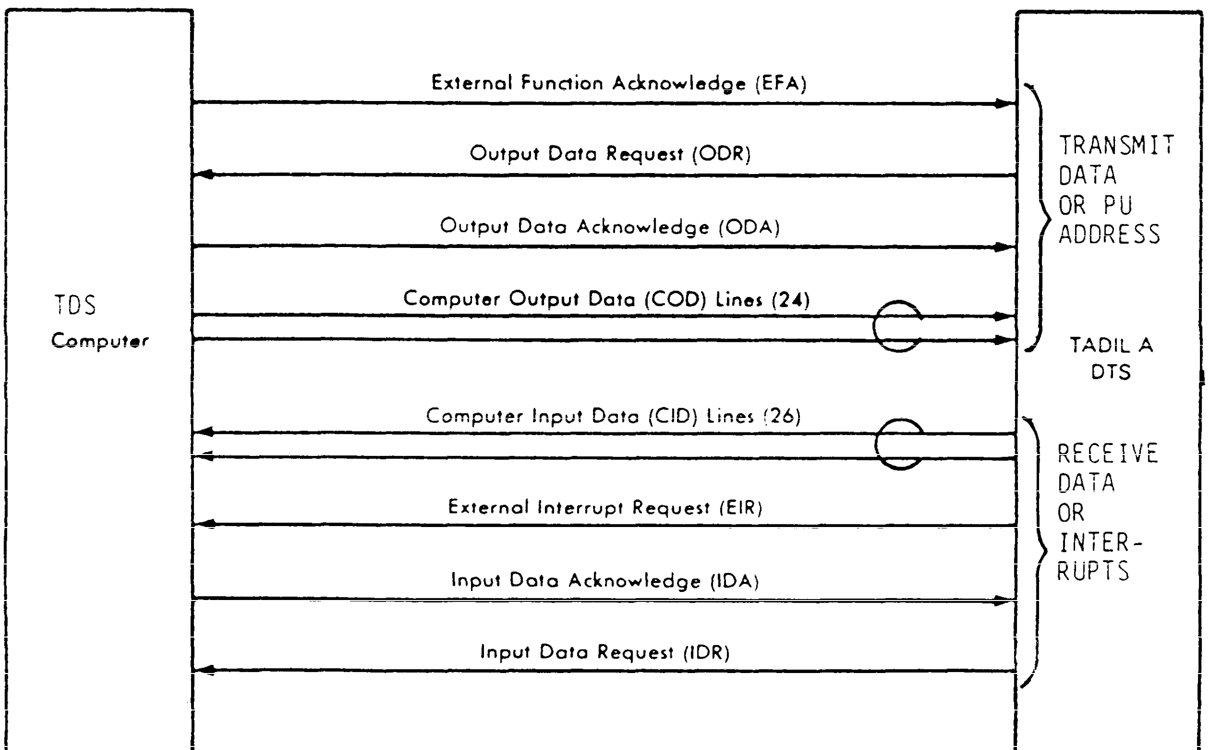


FIGURE 11. DTS-to-TDS computer interface.

TABLE VII. DTS-to-TDS input data bit assignment.

Bit position	External interrupt word	Data word
0	Interrupt code 1/	Data bit 0
1	Interrupt code 1/	Data bit 1
2 2/	Interrupt code 1/	Data bit 2
3		Data bit 3
4		Data bit 4
5		Data bit 5
6		Data bit 6
7		Data bit 7
8		Data bit 8
9		Data bit 9
10		Data bit 10
11		Data bit 11
12		Data bit 12
13		Data bit 13
14		Data bit 14
15		Data bit 15
16		Data bit 16
17		Data bit 17
18		Data bit 18
19		Data bit 19
20		Data bit 20
21		Data bit 21
22		Data bit 22
23		Data bit 23
24		Error status summary 3/
25		Error status summary 3/

1/ See TABLE VIII.
2/ Bits 3 through 25 are not applicable to the interrupt function word.
3/ See TABLE VI.

TABLE VIII. DTS-to-TDS external interrupt codes.

CID Line 2 1 0	Code	Function
0 0 0	0	Not assigned
0 0 1	1	Not assigned
0 1 0	2	Reset
0 1 1	3	End-of-receive (EOR)
1 0 0	4	Prepare-to-transmit, roll call with computer PU address selection enabled (PTTA)
1 0 1	5	Prepare-to-transmit, roll call with computer PU address selection disabled (PTTD)
1 1 0	6	Prepare-to-receive (PTR)
1 1 1	7	Prepare-to-transmit broadcast (PTTB)

30.1.2.2 Interrupt code 3 - EOR. The purpose of a code 3 interrupt shall be to signal the TDS computer that the receive cycle is complete and no more input data is to be transferred. A code 3 interrupt shall be generated whenever the DTS detects a stop code (see 5.1.4.3.1.2 and 5.2.2.2) while receiving data after recognizing a valid start code or when signal presence (see 5.2.5) is lost. The code 3 interrupt shall be output by the DTS to the TDS computer one frame interval after the last IDR completing a receive data sequence.

30.1.2.3 Interrupt code 4 - PTTA. The purpose of the code 4 interrupt shall be to permit PU addresses to be entered from the TDS computer when the DTS is in the DNCS mode of operation and the TDS computer PU address selection is enabled (see 5.1.4.3.1.3 and 5.2.1.2). The DTS (while operating as DNCS) recognizing a picket stop code (see 5.1.4.3.1.2 and 5.2.2.2) or signal presence loss (see 5.2.5), with computer PU address selection enabled, shall output a code 4 interrupt to the TDS computer.

30.1.2.4 Interrupt code 5 - PTTD. The purpose of a code 5 interrupt shall be to signal the TDS computer to transmit data. The DTS operating as a picket shall, upon recognizing its own address code transmitted by DNCS (see 5.1.4.3.1.3 and 5.2.2.3), generate a code 5 interrupt. The DTS operating as DNCS shall, upon determining that an interrogation with message transmission is required (see 5.2.2.3), generate a code 5 interrupt.

30.1.2.5 Interrupt code 6 - PTR. The purpose of a code 6 interrupt shall be to signal the TDS computer to prepare to receive data from the communications channel. The DTS shall, upon recognizing a valid start code (see 5.1.4.3.1.1 and 5.2.2.1), generate a code 6 interrupt.

30.1.2.6 Interrupt code 7 - PTTB. The purpose of a code 7 interrupt shall be to signal the computer to transmit data as described for a code 5 interrupt, except it shall indicate additionally that either the short broadcast (see 5.1.6.2) or long broadcast (see 5.1.6.3) mode of operation has been selected.

30.1.3 IDR. The IDR shall be set by the DTS to indicate the TDS computer that a data word is available on the CID lines. The DTS shall reset the IDR upon detecting an IDA or after waiting the allotted time as specified in 30.3.

30.1.4 IDA. The TDS computer will set the IDA line in response to an EIR or IDR to indicate to the DTS that the TDS computer has read the data on the CID lines.

30.2 TDS computer output requirements. TDS computer-to-DTS communications control shall be via the ODR, ODA, and EFA. Data from the TDS computer shall be transferred via the COD lines. These data lines are shown in TABLE IX. The EFR line is not generated by the DTS for MIL-STD-1397 handshake control.

30.2.1 COD lines. The data or PU addresses to be transferred from the TDS computer to the DTS will be placed on the 24 parallel output data lines by the TDS computer in response to an ODR or a code 4 interrupt. The data or PU address will be accompanied by an ODA or EFA, respectively. See TABLE IX for data bit assignments.

30.2.2 ODR. The ODR shall be set by the DTS to indicate that it is ready to accept an output data word from the TDS computer on the COD lines. The DTS shall reset the ODR upon detecting an ODA or after waiting the allotted time as specified in 20.3.

30.2.3 ODA. The TDS computer will set the ODA line when transmit data has been placed on the COD lines and the DTS ODR is set. When the ODA is set, the DTS shall read the data on the COD lines and reset its ODR line and keep it reset until it is ready for the next word to be placed on the COD lines.

TABLE IX. TDS-to-DTS output data bit assignment.

COD Line	External Function Word Transmit PU Address	Data Word
0	Note: Bits 0 through 14 and bits 22 and 23 are not applicable to the external function word.	Data bit 0
1		Data bit 1
2		Data bit 2
3		Data bit 3
4		Data bit 4
5		Data bit 5
6		Data bit 6
7		Data bit 7
8		Data bit 8
9		Data bit 9
10		Data bit 10
11		Data bit 11
12		Data bit 12
13		Data bit 13
14		Data bit 14
15	XMT PU address 1 (least significant bit)	Data bit 15
16	XMT PU address 2	Data bit 16
17	XMT PU address 3	Data bit 17
18	XMT PU address 4	Data bit 18
19	XMT PU address 5	Data bit 19
20	XMT PU address 6 (most significant bit)	Data bit 20
21	Message control	Data bit 21
22		Data bit 22
23		Data bit 23

30.2.4 EFA. The TDS computer will set the EFA line when PU address data has been placed on the COD lines in response to a code 4 interrupt. When EFA is set, the DTS shall read the PU address data on the COD lines. Bit position 21, the message control bit, shall determine whether the DTS is to generate an interrogation message (see 5.1.6.1.1a) or an interrogation with message (see 5.1.6.1.1b) transmission. If the message control bit is set to a logic 1, an interrogation with message transmission shall be generated. If the message control bit is set to logic 0, an interrogation message transmission shall be generated.

30.3 Transmit and receive timing. The TDS computer interface timing is illustrated in FIGURES 12 through 15 for operation under ideal conditions (that is, all data frames transmitted by the TDS computer are transmitted on the communications channel and all those data frames transmitted are properly received by the DTS without errors). In the figures, the line of frames at the top depicts frames of information either transmitted on the communications channel or received from the communications channel at the selected data rate.

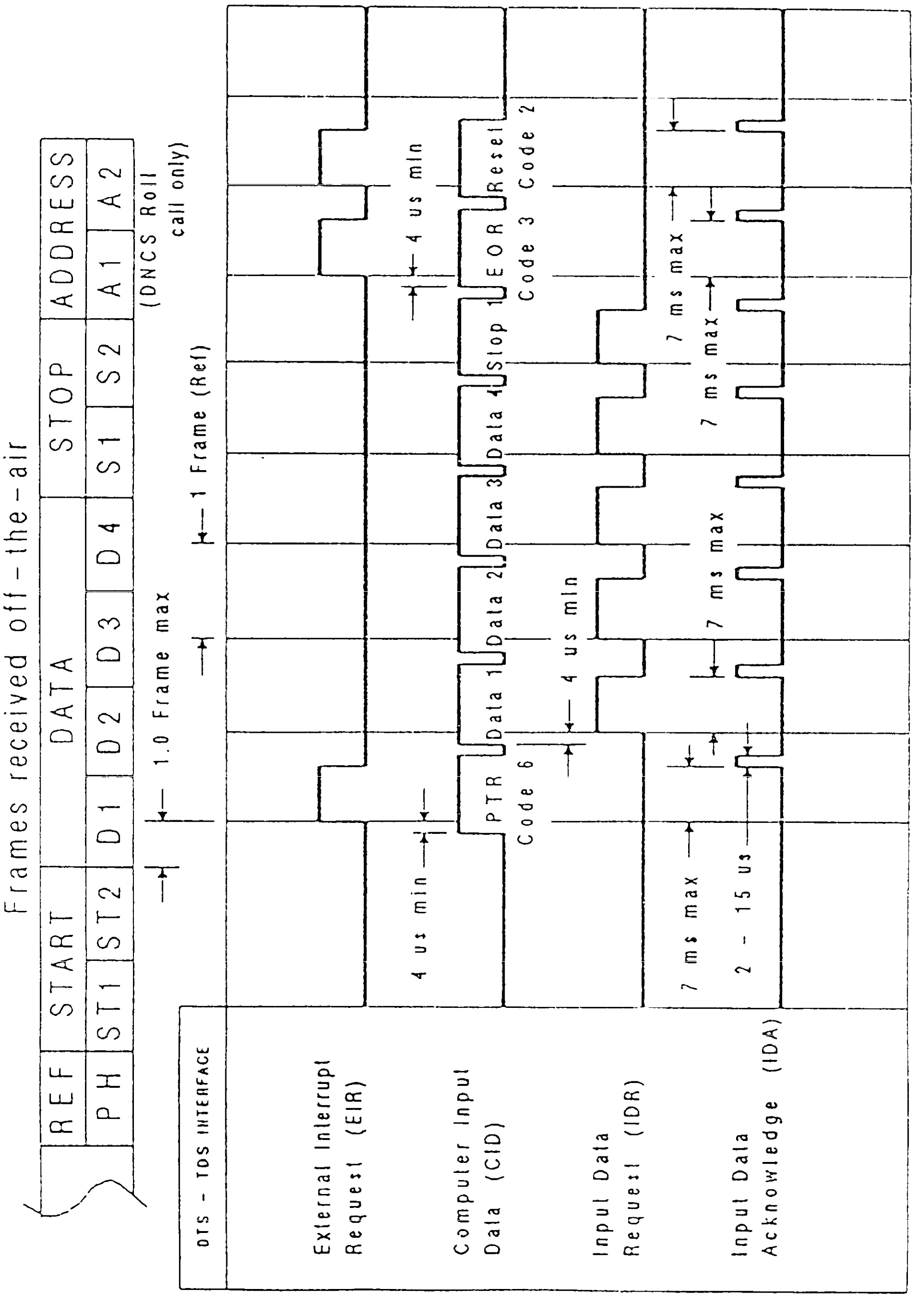


FIGURE 12. Receive timing (reset pending).

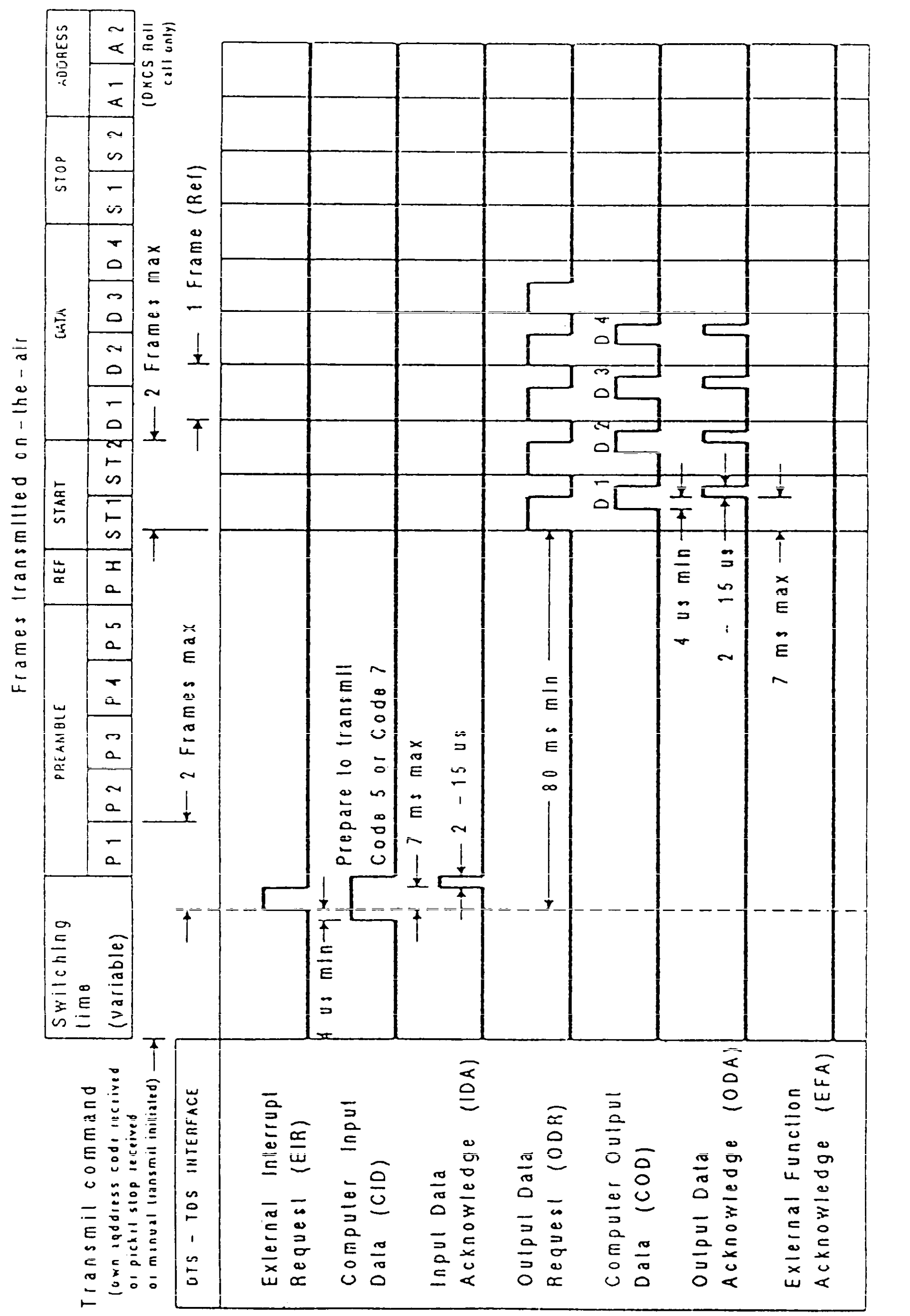


FIGURE 13. Transmit timing (computer PU address selection disabled).

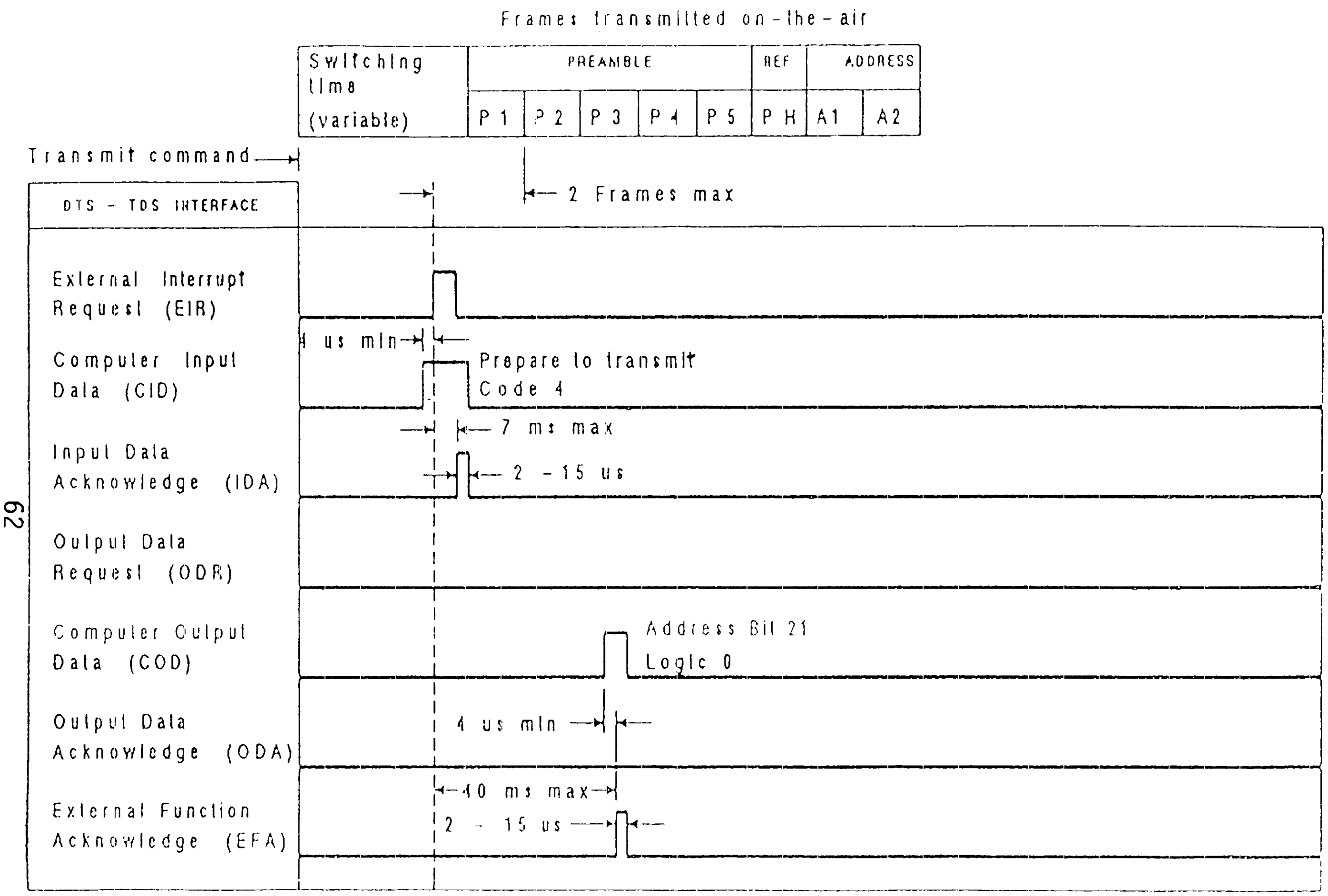


FIGURE 14. Transmit timing (computer PU address selection - interrogation message).

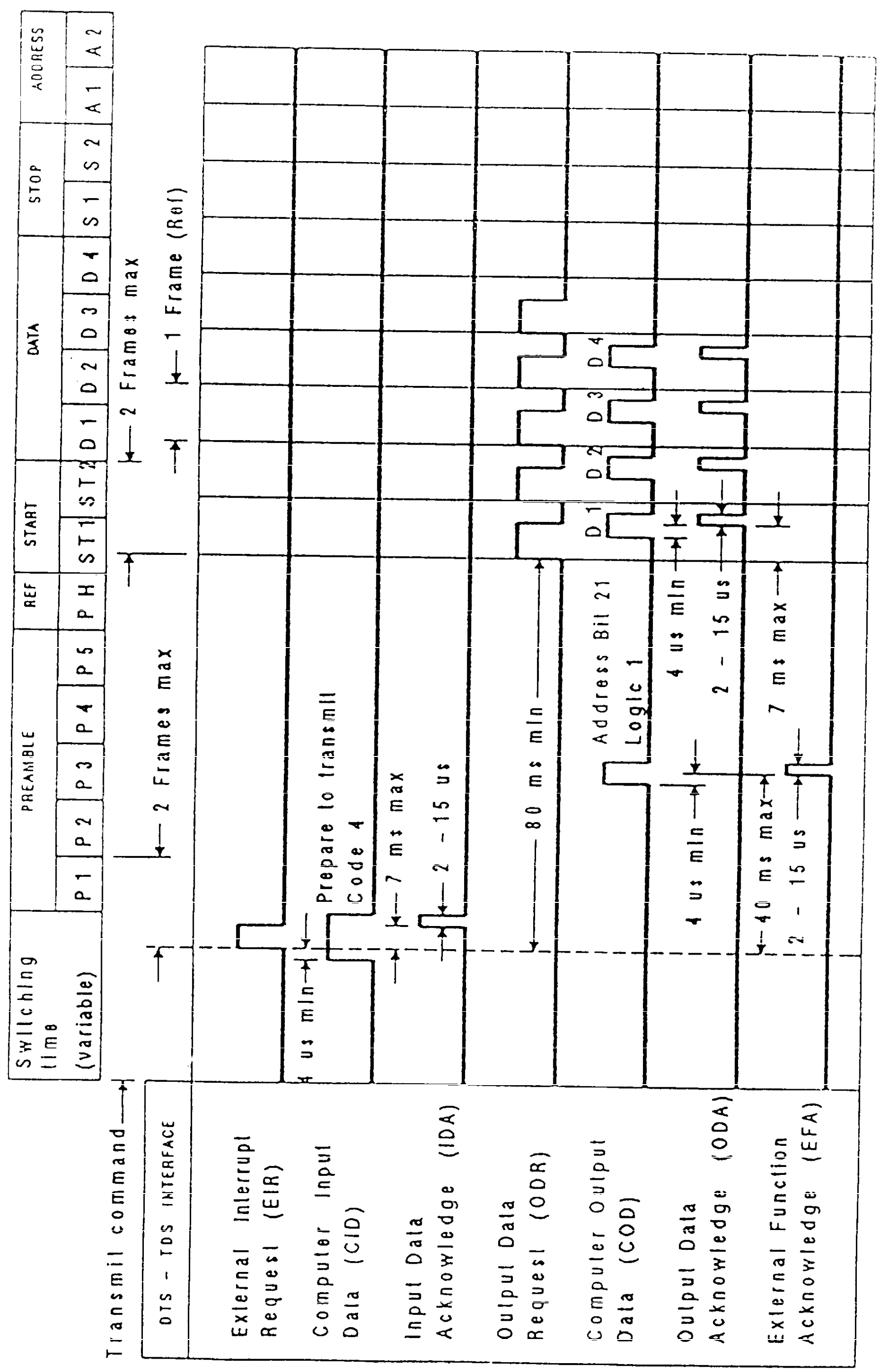


FIGURE 15. Transmit timing (computer PU address selection - interrogation with message).

30.3.1 Receive timing. The timing for the receive sequence shall be as shown in FIGURE 12. During reception, the sequence of events in a through j shall occur as follows:

a. The DTS recognizes the start code (see 5.1.4.3.1.1 and 5.2.2.1).

b. The DTS shall set a code 6 (PTR) interrupt on the CID lines. A minimum of 4 microseconds later, the DTS shall activate the EIR line. Activation of the EIR line shall occur within one frame interval after off-the-air receipt of the start 2 frame.

c. The TDS computer reads the interrupt code on the CID lines and activates the IDA line for a period of 2 microseconds to 15 microseconds. If the TDS computer does not activate the IDA Line within 7 milliseconds from the beginning of the EIR, the DTS shall indicate that the TDS computer did not acknowledge the interrupt.

d. When the first frame of receive data (see 5.1.4.3.2) becomes available, the DTS shall place the data on the CID lines. A minimum of 4 microseconds later, the DTS shall activate the IDR line.

e. The TDS computer reads the data on the CID lines and activates the IDA line for a period of 2 to 15 microseconds. If the TDS computer does not activate the IDA line within 7 milliseconds from the beginning of the IDR, the DTS shall indicate that the TDS did not acknowledge the request.

f. The receive sequence with the CID, IDR, and IDA lines repeats until the DTS recognizes a stop code (see 5.1.4.3.1.2 and 5.2.2.2) or signal presence is lost (see 5.2.5). The first frame of the stop code shall be treated as data and sent to the TDS computer.

g. When signal presence is lost or during the early portion of the frame (2 milliseconds to 4 milliseconds into the frame) following receipt of the second stop code, the DTS shall set a code 3 (EOR) interrupt on the CID lines. A minimum of 4 microseconds later, the DTS shall activate the EIR line.

h. The TDS computer reads the interrupt code and sets the IDA line as described in c.

i. If a reset is activated during the reception, the code 2 interrupt shall be sent to the TDS computer after the EOR interrupt has been acknowledged. The DTS shall then set the code 2 interrupt on the CID lines and a minimum of 4 microseconds later activate the EIR line.

j. The TDS computer reads the interrupt code on the CID lines and activates the IDA line for a period of 2 milliseconds to 15 microseconds. If the TDS computer does not activate the IDA line within 7 milliseconds from the beginning of the EIR, the DTS shall indicate that the TDS computer did not acknowledge the interrupt.

30.3.2 Transmit timing. The transmit timing sequences of 30.3.2.1 through 30.3.2.4 shall be provided for in the DTS.

30.3.2.1 Roll call with computer PU address selection disabled. The transmit timing for a picket reply or a DNCS interrogation with message transmission shall be as shown in FIGURE 13. A DTS operating as a DNCS and transmitting an interrogation message shall not communicate with the TDS computer. A DTS operating as a picket recognizing its own PU address or a DNCS recognizing that an interrogation with message transmission is required shall complete the following sequence of events:

a. The DTS shall wait for the required switching time interval (see 5.1.7) and begin transmitting the preamble frames (see 5.1.4.1).

b. Between the beginning of the first transmitted preamble frame and the end of the second transmitted preamble frame, the DTS shall set a code 5 (PTTD) interrupt on the CID lines. A minimum of 4 microseconds later, the DTS shall activate the EIR line.

c. The TDS computer reads the interrupt code on the CID lines and activates the IDA line for a period of 2 microseconds to 15 microseconds. If the TDS computer does not activate the IDA line within 80 milliseconds from the beginning of the EIR, the DTS shall indicate that the TDS computer did not acknowledge the interrupt and shall transmit the start code and then the stop code (address code shall also be transmitted if the DTS is DNCS) according to the transmission format requirements (see 5.1.4).

d. At the start of the second transmitted start code frame, the DTS shall activate the ODR line to request TDS computer data.

e. The TDS computer detects the ODR and sets the data to be transmitted on the COD lines. The TDS computer then activates the ODA line a minimum of 4 microseconds later for a time period of 2 milliseconds to 15 microseconds. If the TDS computer does not activate the ODA line within 6.8 milliseconds after the DTS sets the ODR line, the DTS shall determine that no more data is to be transmitted on the communications channel and event g is performed.

f. The process described in d and e above repeats until the last data frame has been sent to the DTS by the TDS computer. The next data frame is always obtained from the TDS computer while the current frame is transmitted on the communications channel.

g. After the last data frame has been sent to the DTS, the TDS computer will not respond to the next DTS ODR with an ODA. When an ODA is not detected by the DTS within the allotted time, the DTS shall transmit the stop code on the communications channel. If the DTS is the DNCS, the stop code shall be followed by a picket address code.

h. If a reset should be activated during the transmit sequence, the DTS shall set a code 2 interrupt on the CID line, and then a minimum of 4 microseconds later activate the EIR line.

i. The TDS computer reads the interrupt code on the CID lines and activates the IDA line for a period of 2 microseconds to 15 microseconds. If the TDS computer does not activate the IDA line within 7 milliseconds from the beginning of the EIR, the DTS shall indicate that the TDS computer did not acknowledge the interrupt. The process described in f and g continues until the last data frame has been sent by the TDS computer.

30.3.2.2 Roll call with computer PU address selection enabled (interrogation message transmission). The transmit timing shall be as shown in FIGURE 14. When the DTS operating as a DNCS with computer PU address selection enabled detects a picket stop code during a receive sequence, detects loss of signal presence, or the transmit control is manually activated, the following sequence shall occur:

a. The DTS shall wait for the required switching time interval (see 5.1.7) and begin transmitting the preamble frames (see 5.1.4.1).

b. Between the beginning of the first transmitted preamble frame and the end of the second transmitted preamble frame, the DTS shall set a code 4 (PTTA) interrupt on the CID lines. A minimum of 4 microseconds later, the DTS shall activate the EIR line.

c. The TDS computer reads the interrupt code on the CID lines and activates the IDA line for a period of 2 microseconds to 15 microseconds. If the TDS computer does not activate the IDA line within 7.2 milliseconds from the beginning of the EIR, the DTS shall indicate that the TDS computer did not acknowledge the interrupt. If the TDS computer did not acknowledge the interrupt, the DTS shall revert to DTS PU address selection (see 5.2.1.1) to obtain all further PU addresses and follow the events in 20.3.2.1 for all future transmissions (see 5.2.1.2).

d. The TDS computer sets the external function word containing the PU address and message control bit on the COD lines. The TDS computer then activates the EFA line a minimum of 4 microseconds later for a time period of 2 microseconds to 15 microseconds. If the TDS computer does not activate the EFA line within 40 milliseconds after the DTS sets the EIR in b above, the DTS shall respond as in c above when an IDA is not detected.

e. When the DTS detects that the message control bit (bit 21) in the external function word has been set to a logical 0, it shall transmit an interrogation message.

f. If a reset is activated during the transmit sequence, a code 2 interrupt is placed on the CID lines and the EIR is activated at the next frame boundary. Transmission will then terminate once the transmit sequence is completed.

g. The TDS computer reads the interrupt code on the CID lines and activates the IDA line for a period of 2 microseconds to 15 microseconds. If the TDS computer does not activate the IDA line within 7 milliseconds from the beginning of the EIR, the DTS shall indicate that the TDS computer did not acknowledge the interrupt. The DTS shall terminate transmissions after the address code is transmitted.

30.3.2.3 Roll call with computer PU address selection enabled (interrogation with message transmission). The transmit timing shall be as shown in FIGURE 15. When the DTS operating as DNCS with computer PU address selection enabled detects a picket stop code during a receive sequence, detects loss of signal presence, or the transmit control is manually activated, the following sequence shall occur:

a. The DTS shall wait for the required switching time interval (see 5.1.7) and begin transmitting the preamble frames (see 5.1.4.1).

b. Between the beginning of the first transmitted preamble frame and the end of the second transmitted preamble frame, the DTS shall set a code 4 (PTTA) interrupt on the CID lines. A minimum of 4 microseconds later, the DTS shall activate the EIR line.

c. The TDS computer reads the interrupt code on the CID lines and activates the IDA line for a period of 2 microseconds to 15 microseconds. If the TDS computer does not activate the IDA line within 7.2 milliseconds from the beginning of the EIR, the DTS shall indicate that the TDS computer did not acknowledge the interrupt. If the TDS computer did not acknowledge the interrupt, the DTS shall revert to DTS PU address selection (see 5.2.1.1) to obtain all further PU addresses and follow the events in 30.3.2.1 for all future transmission (see 5.2.1.2).

d. The TDS computer sets the external function word containing the PU address and message control bit on the COD lines. The TDS computer then activates the EFA line a minimum of 4 microseconds later for a time period of 2 microseconds to 15 microseconds. If the TDS computer does not activate the EFA line within 40 milliseconds after the DTS sets the EIR in b above, the DTS shall respond as in c above when an IDA is not detected.

e. When the DTS detects that the message control bit (bit 21) in the external function word has been set to a logical 1, it shall transmit an interrogation with message.

f. At the start of the second transmitted start code frame, the DTS shall activate the ODR line to request TDS computer data.

g. The TDS computer detects the ODR and sets the data to be transmitted on the COD lines. The TDS computer then activates the ODA line a minimum of 4 microseconds later for a time period of 2 microseconds to 15 microseconds. If the TDS computer does not activate the ODA line within 7 milliseconds after the DTS sets the ODR line, the DTS shall determine that no more data is to be transmitted on the communications channel and event i is performed.

h. The process described in f and g above repeats until the last data frame has been sent to the DTS by the TDS computer. The next data frame is always obtained from the TDS computer while the current frame is transmitted on the communications channel.

i. After the last data frame has been sent to the DTS, the TDS computer will not respond to the next DTS ODR with an ODA. When an ODA is not detected by the DTS within the allotted time, the DNCS stop code followed by a picket address code on the communications channel.

j. If the reset should be activated during the transmit sequence, the DTS shall set a code 2 interrupt on the CID line, and then a minumum of 4 microseconds later activate the EIR line.

k. The TDS computer reads the interrupt code on the CID lines and activates the IDA line for a period of 2 to 15 microseconds. If the TDS computer does not activate the IDA line within 7 milliseconds from the beginning of the EIR, the DTS shall indicate that the TDS computer did not acknowledge the interrupt. The process described in h and i continues until the last data frame has been sent by the TDS computer.

30.3.2.4 Short broadcast or long broadcast. The transmit timing for a short broadcast (5.1.6.2) or long broadcast (see 5.1.6.3) transmission shall be as shown in FIGURE 13. When the transmit control is manually activated with the DTS operating in either of the broadcast modes, the following sequence of events shall occur:

a. Prior to the end of the second transmitted preamble frame, the DTS shall set a code 7 (PTTB) interrupt on the CID lines. A minimum of 4 microseconds later, the DTS shall activate the EIR line.

b. The TDS computer reads the interrupt code on the CID lines and activate the IDA line for a period of 2 to 15 microseconds. If the TDS computer does not activate the IDA line within 80 milliseconds from the beginning of the EIR, the DTS shall indicate that the TDS computer did not acknowledge the interrupt and shall transmit the start code and then the stop code according to the transmission format requirements (see 5.1.4).

c. At the start of the second transmitted start code frame, the DTS shall activate the ODR line to request TDS computer data.

d. The TDS computer detects the ODR and sets the data to be transmitted on the COD lines. The TDS computer then activates the ODA line a minimum of 4 microseconds later for a time period of 2 to 15 microseconds. If the TDS computer does not activate the ODA line within 7 milliseconds after the DTS sets the ODR line, the DTS shall determine that no more data is to be transmitted on the communications channel and event f is performed.

e. The process described in events c and d above repeats until the last data frame has been sent to the DTS by the TDS computer. The next data frame is always obtained from the DTS computer while the current frame is transmitted on the communications channel.

f. After the last data frame has been sent to the DTS, the TDS computer will not respond to the next DTS ODR with an ODA. When an ODA is not detected by the DTS within the allotted time, the DTS shall transmit a picket stop code on the communications channel.

g. If a reset should be activated during the transmit sequence, the DTS shall set a code 2 interrupt on the CID line, and then a minumum of 4 microseconds later activate the EIR line.

h. The TDS computer reads the interrupt code on the CID lines and activates the IDA line for a period of 2 microseconds to 15 microseconds. If the TDS computer does not activate the IDA line within 7 milliseconds from the beginning of the EIR, the DTS shall indicate that the TDS computer did not acknowledge the interrupt. The process described in e and f continues until the last data frame has been sent by the TDS computer.

APPENDIX D2

DTS-TO-TDS COMPUTER INTERFACE - SERIAL

10. SCOPE. This APPENDIX contains detailed information on the DTS and the TDS computer (serial) interface and is a mandatory part of this standard.

20. APPLICABLE DOCUMENTS. This section is not applicable to this APPENDIX.

30. DTS-to-TDS computer interface characteristics. The TDS computer interface and electrical characteristics and timing shall be in accordance with the following sections. The TDS computer interface is shown in FIGURE 16. The TDS computer tactical interfaces are described in 30.1. Interface data and address formats are described in 30.2 and 30.3, respectively. Receive and transmit timing are described in 30.4. Electrical characteristics are described in 30.5. The nontactical (sidetone) interfaces are described in 40. By convention, all signals are referenced to the TDS computer input and output interfaces.

30.1 TDS computer tactical interface. The interface lines between the TDS computer and the DTS are shown in FIGURE 16. The tactical interface lines are the frame line, incoming data line, outgoing data line, data clock line, address data line, address clock line, and net control line, and are described in 30.1.1 through 30.1.7, respectively.

30.1.1 Frame line. The DTS shall generate a signal on the frame line to signal the TDS computer that either data is available (frame available), data is requested (demand), or, in conjunction with a coincident incoming data line signal, that a transmission has started (advance demand).

30.1.2 Incoming data line. The incoming data line shall be used by the DTS to input data to the TDS computer when the DTS is in the receive condition, to recirculate data to be transmitted when the DTS is in the transmit condition, or, in conjunction with a coincident frame line signal, to indicate to the TDS computer that a transmission has started. The DTS shall transfer data on the incoming data line in response to TDS computer-generated clocks on the data clock line.

30.1.3 Outgoing data line. The outgoing data line shall be used to transfer data from the TDS computer to the DTS for transmission. The DTS shall accept data from the TDS computer in response to a DTS-generated demand signal when accompanied by coincident TDS computer-generated data clocks on

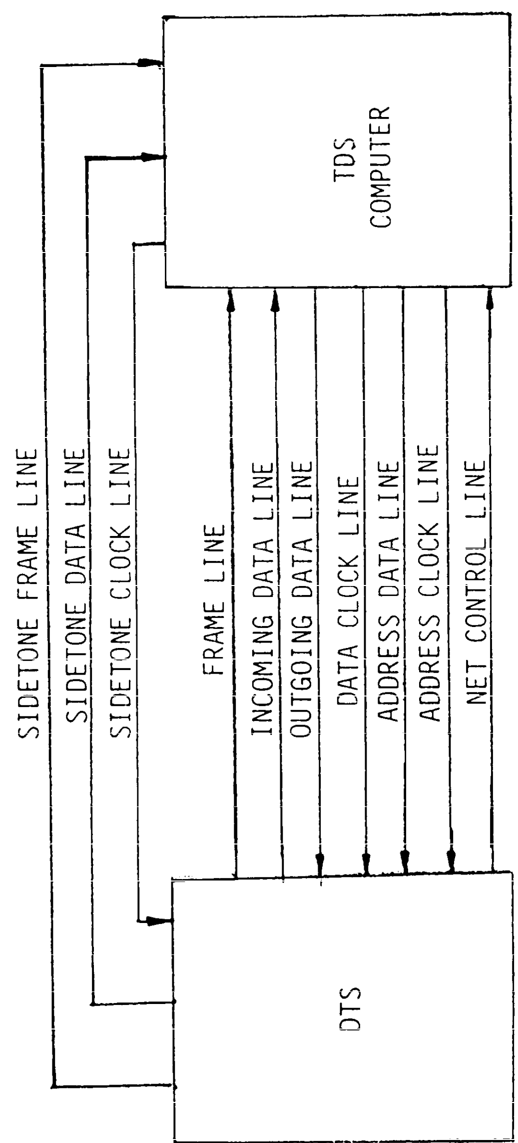


FIGURE 16. DTS-to-TDS computer interface.

the data clock line. The outgoing data line shall also be used to transfer a recirculation fault pulse from the TDS computer to the DTS when the TDS computer detects a recirculation error during a transmission or a reception.

30.1.4 Data clock line. The data clock line shall be used by the DTS to either transfer data to the TDS computer (receive condition) or accept data from the TDS computer (transmit condition).

30.1.5 Address data line. The address data line shall be used by the DTS to obtain a picket station address from the TDS computer when the DTS is operating as the DNCS in the roll call mode with TDS computer PU address selection enabled. The DTS shall accept the address data from the TDS computer in response to a DTS-generated advance demand signal when accompanied by coincident TDS computer-generated address clocks on the address clock line.

30.1.6 Address clock line. The address clock line shall be used by the DTS to accept address data from the TDS computer. The TDS computer will place clocks on the address clock line coincident with the address data on the address data line.

30.1.7 Net control line. The net control line shall be used by the DTS to indicate to the TDS computer the DTS PU address selection mode. When the DTS is operating as the DNCS in the roll call mode with TDS computer PU address selection enabled, it shall place a voltage level of 0 VDC ±1.0 VDC on the net control line. When the DTS is not operating as the DNCS with computer PU address selection enabled, the level placed on the net control line shall be +10.0 VDC ±1.5 VDC.

30.2 Data formats. The DTS to/from TDS computer data format shall be as shown in FIGURE 17 and as described in 30.2.1 and 30.2.2, respectively.

30.2.1 DTS-to-TDS computer. The DTS-to-TDS computer data shall consist of 26 bits of serial information per frame. The first 2 bits transferred to the TDS computer shall be control bits and the remaining 24 bits shall be information data bits. The receive control bits are defined in 30.2.1.1 and 30.2.1.2.

SERIAL DATA FORMAT

23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	C_2	C_1

Control bit C_1 is the first bit transmitted/received in each frame.

SERIAL ADDRESS FORMAT

MESSAGE CONTROL	TX ADDRESS					
7	6	5	4	3	2	1

TX address 1 is the least significant bit of the address and is the first bit transmitted/received in each address transfer.

FIGURE 17. TADIL A serial data format between DTS and TDS computer.

30.2.1.1 Receive control bit 1. Receive control bit 1 (C_1) shall indicate the quality of the received message frame depending on the selected mode of operation as indicated in TABLE X.

TABLE X. Received message frame quality.

Mode	Condition	C_1
Detect and lable	No errors detected (K_0 - K_{16} all odd)	0
	Error(s) detected - no correction attempted (one or more of K_0 - K_{16} even)	1
Detect and correct	No errors detected (K_0 - K_{16} all odd)	0
	Parity error detected (K_0 even, not more than one of K_1 - K_{16} even)	0
	Odd error(s) detected - correction attempted (K_0 even, more than one but not all of K_1 - K_{16} even; or K_0 even, more than one, but not all of K_2 - K_{16} even)	0
	Multiple errors detected - no correction attempted (K_0 odd, one or more of K_1 - K_{16} even; or K_0 even, K_2 - K_{16} all even)	1

See 5.2.4.1 and TABLE V for K_0 - K_{16} definitions.

30.2.1.2 Receive control bit 2. Receive control bit 2 (C_2), or start bit, shall be set by the DTS to indicate the first frame of a receive message. The DTS shall set the bit to a logical 1 for the first frame of data transferred to the TDS computer during a message reception. The bit shall be set to a logical 0 for all other frames of data transferred during the message reception.

30.2.2 TDS computer-to-DTS. The TDS computer-to-DTS data shall consist of 26 bits of serial information per frame. The first 2 bits (C_1 and C_2) transferred from the TDS computer are control bits and the remaining 24 bits are information data bits. The DTS shall examine the first two bits of each frame of data received from the TDS computer. When both control bits are logical 1, the data contained in the remaining 24 bits shall be transmitted by the DTS. When either control bit is a logical 0, the DTS shall discard the remaining 24 bits of information and transmit the appropriate stop code.

30.3 Address data format. The address data shall consist of six address bits and a message control bit. The least significant bit (LSB) of the address shall be transferred first. The message control bit shall be the most significant bit (MSB) and transferred last. The message control bit shall be utilized to determine if an IWM or an IM (see 5.1.6.1.1) is to be transmitted. When the message control bit is a logical 1, the DTS shall transmit an IWM transmission and when a logical 0, an IM transmission.

30.4 Receive and transmit timing. The TDS computer interface receive and transmit timing are illustrated in FIGURES 18 and 19 and described in 30.4.1 and 30.4.2, respectively. Timing relationships between incoming data and data clock, between incoming data and frame (advance demand), and between outgoing data and data clock or address data and address clock are illustrated in FIGURES 20 through 22, respectively. FIGURE 23 illustrates the transmit address timing required for a DTS acting as a DNCS in the roll call mode with TDS computer PU address selection enabled.

30.4.1 Receive timing. The timing for the receive sequence shall be as shown in FIGURE 18. During a reception, the sequence of events a through h shall occur as follows:

a. The DTS recognizes the start code (see 5.1.4.3.1.1 and 5.2.2.1).

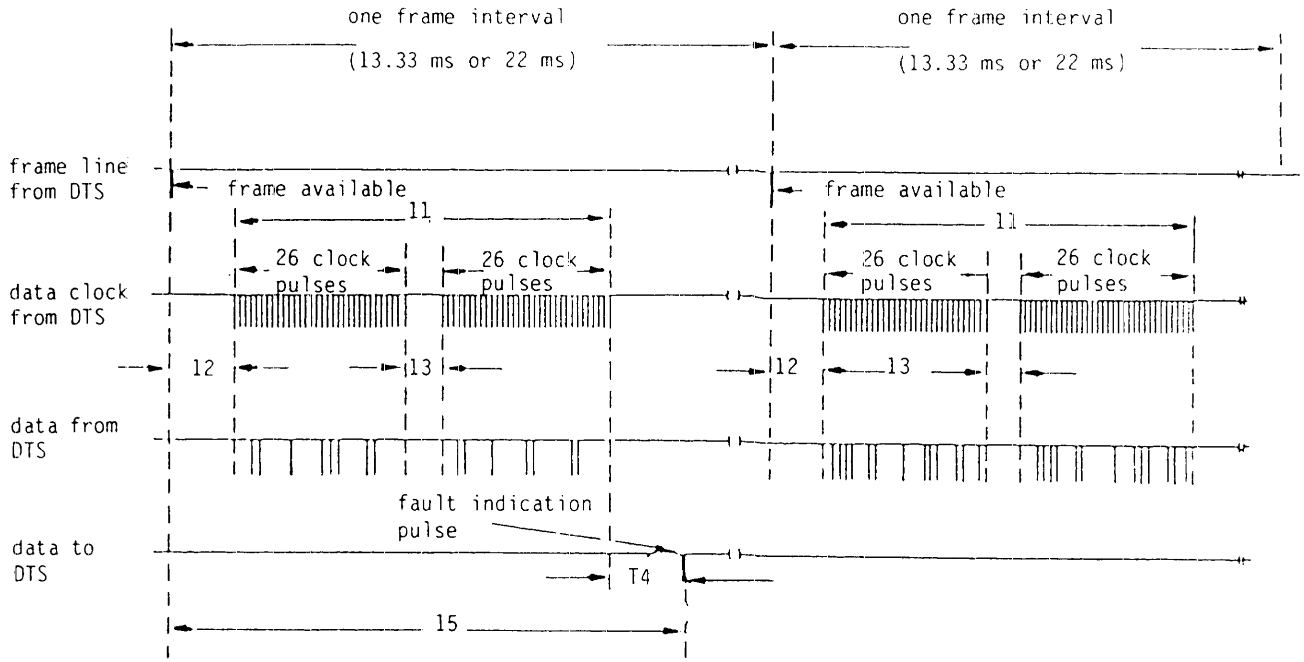
b. When a frame of receive data (see 5.1.4.3.2) becomes available, the DTS shall place a frame available pulse on the frame line to indicate to the TDS computer that receive data is available. The frame available pulse shall occur within one frame interval after off-the-air receipt of the first frame of data.

c. Within 12 milliseconds, the TDS computer sends a series of 26 clock pulses on the data clock line to the DTS.

d. In response to each clock pulse on the data clock line, the DTS shall set a data bit on the incoming data line.

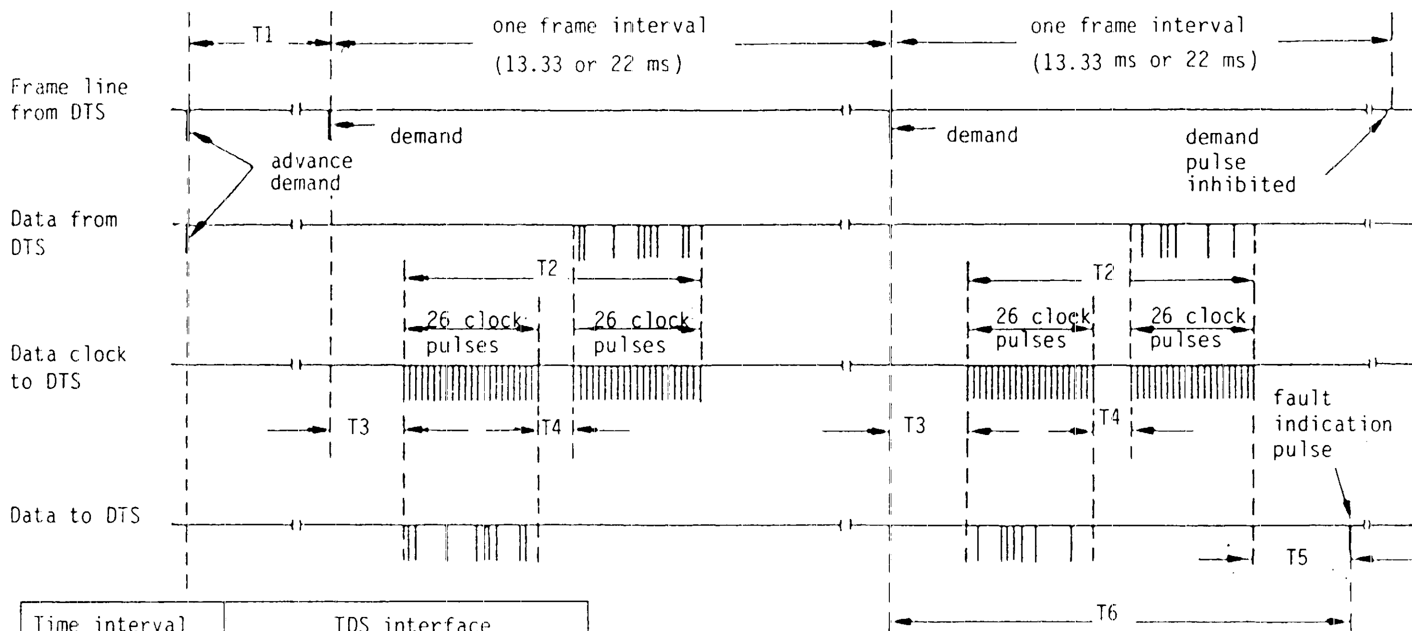
e. After waiting a minimum of 7 microseconds after the twenty-sixth clock pulse in the first series of clocks, the TDS computer sends a second series of 26 clock pulses to the DTS on the data clock line. The total of 52 clock pulses will occur within 500 microseconds.

f. In response to each clock pulse in the second series, the DTS shall set a data bit on the incoming data line identical to the data sent to the TDS computer during the first series of clock pulses.



Time interval	TDS interface
11	600 μs MAX
12	12 ms MAX
13	7 μs MIN
14	7 μs MIN 500 μs MAX
15	13 ms MAX

FIGURE 18. DTS/TDS computer interface timing (receive).



Time interval	TDS interface
T1	6 frames min, 8 frames max
T2	600 μs max
T3	12 ms max
T4	7 μs min
T5	7 μs min 600 μs max
T6	13 ms max

FIGURE 19. DTS/TDS computer interface timing (transmit).

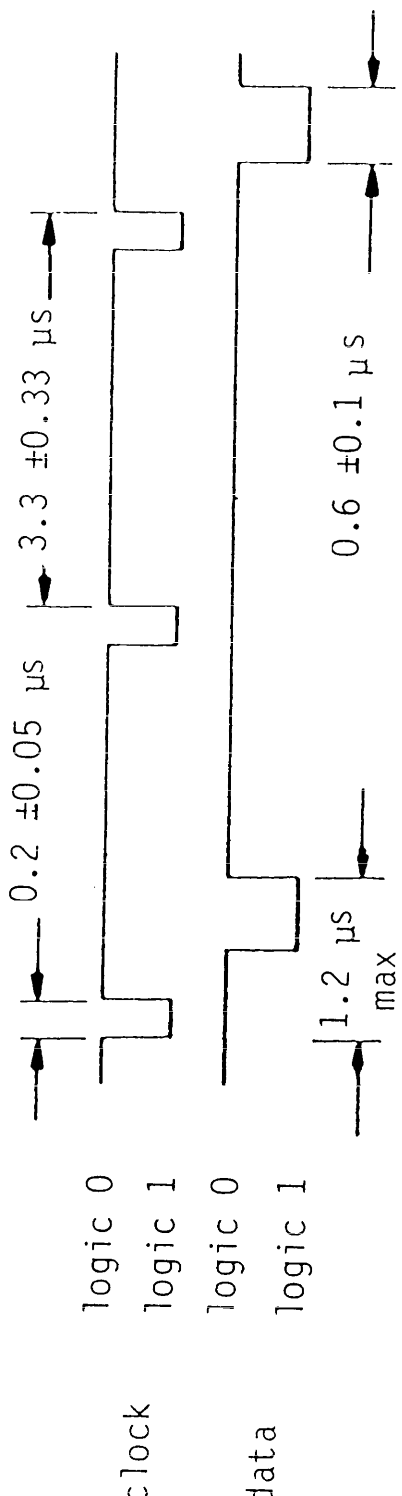


FIGURE 20. Incoming data/data clock relationship.

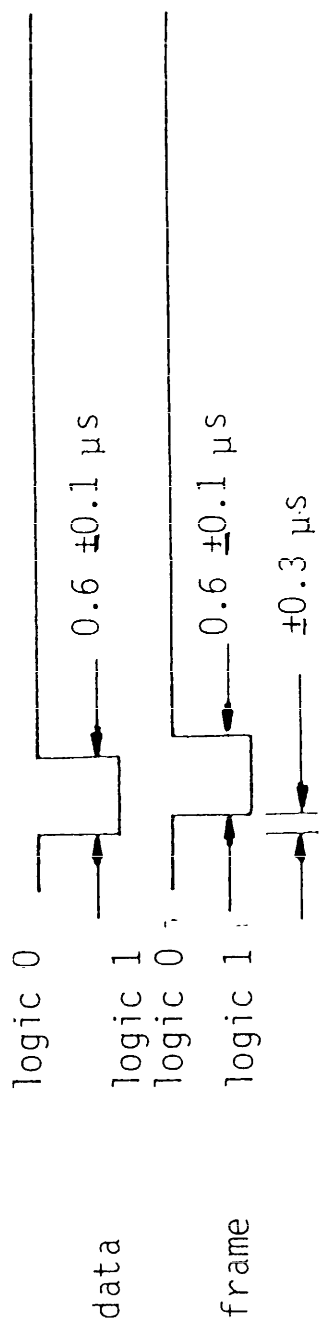


FIGURE 21. Advance demand (incoming data/frame relationship).

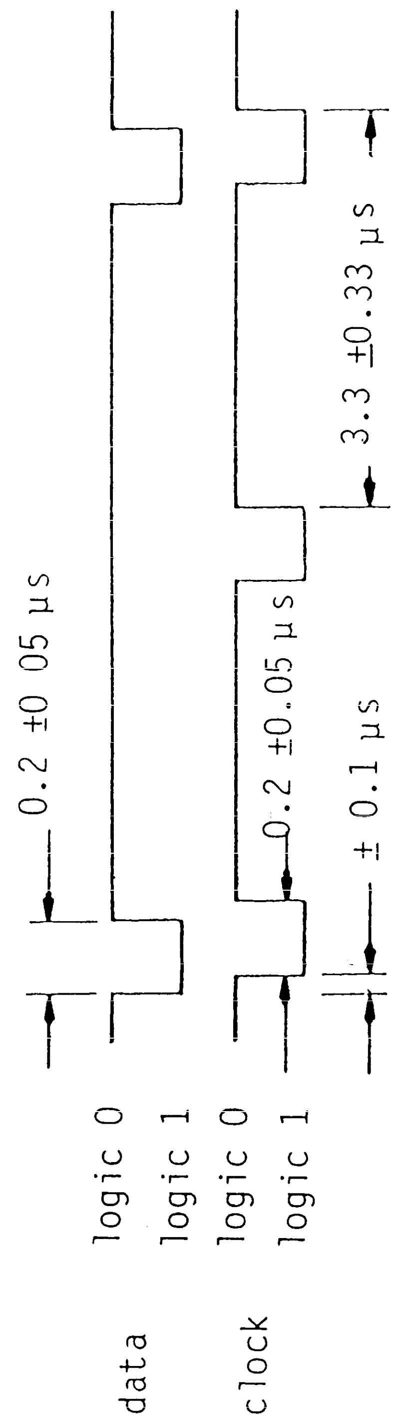


FIGURE 22. Outgoing data/data clock or address data/address clock relationships.

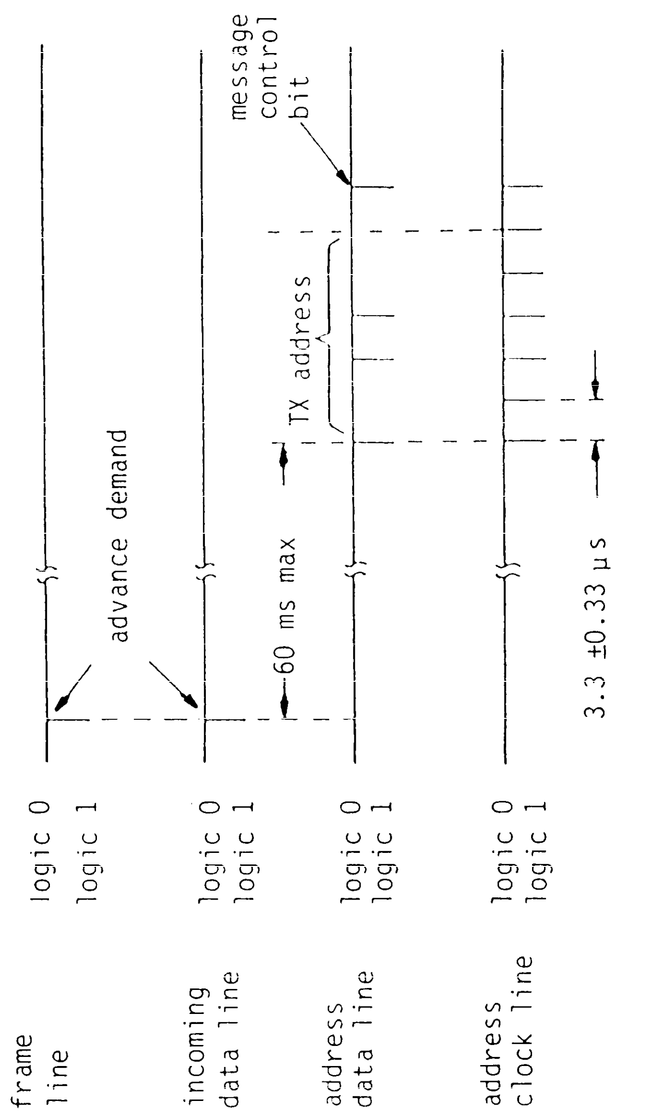


FIGURE 23. Transmit address timing.

g. The TDS computer will compare the two series of 26 data bits and if not identical, send a pulse (recirculation fault pulse) on the outgoing data line to the DTS no sooner than 7 microseconds or later than 500 microseconds after the twenty-sixth clock pulse of the second series of clocks. If a recirculation fault pulse is sent by the TDS computer to the DTS, the DTS shall indicate the occurrence of the recirculation fault. The complete transfer (two series of 26 clocks each and a fault pulse if required) shall be completed within 1 millisecond.

h. The process described in b through g above repeats until the DTS recognizes a stop code (see 5.1.4.3.1.2 and 5.2.2.2) or signal presence is lost (see 5.2.5). The first frame of the stop code shall be treated as data and sent to the TDS computer. Upon recognizing the stop code, the DTS shall inhibit frame available pulses for at least eight frame intervals. The absence of frame available pulses indicates the end of a reception.

30.4.2 Transmit timing. The timing for the transmit sequence shall be as shown in FIGURE 19. During a transmission, the sequence of events in a through j shall occur as follows:

a. The DTS shall wait for the required switching time interval (see 5.1.7) and begin transmitting the preamble frames (see 5.1.4.1).

b. Between the beginning of the switching time interval and the beginning of the first transmitted preamble frame, the DTS shall send an advance demand signal (see FIGURE 21) to the TDS computer. The advance demand signal informs the TDS computer that the DTS has started a transmit sequence.

c. If the DTS is operating as the DNCS in the roll call mode with TDS computer PU address selection enabled as evidenced by the voltage level on the net control line (see 30.1.7), the TDS computer will initiate a series of seven clock pulses on the address clock line within 60 milliseconds after the reception of the advance demand signal (see FIGURE 23). Coincident with each of the first six clock pulses on the address clock line, the TDS computer places the address of the picket station to be interrogated on the address data line. Coincident with the seventh clock pulse on the address clock line, the TDS computer will set the message control bit (see 30.3) on the address data line to indicate either an IWM or an IM is to be transmitted. If an IM is to be transmitted, the DTS shall transmit the picket station address received from the TDS computer at the appropriate time and revert to the receive mode. If an IWM is to be transmitted, the DTS shall at the appropriate time (not less than six nor more than eight frames after the advance demand signal) send a demand pulse on the frame line. If the DTS is not operating as the DNCS in the roll call mode with TDS computer PU address selection enabled, the TDS computer will not supply an address as indicated above and the DTS shall at the appropriate time (not less than six nor more than eight frames after the advance demand signal) send a demand pulse on the frame line.

d. Within 12 milliseconds after receipt of the demand pulse, the TDS computer sends a series of 26 clock pulses on the data clock line to the DTS. In coincidence with each clock pulse, the TDS computer sends an information bit on the outgoing data line.

e. After waiting a minimum of 7 microseconds after the twenty-sixth clock pulse in the first series of clocks, the TDS computer sends a second series of 26 clock pulses to the DTS on the data clock line. The total of 52 clock pulses will occur within 500 microseconds.

f. In response to each clock pulse in the second series, the DTS shall set a data bit on the incoming data line identical to the data received from the TDS computer on the outgoing data line during the first series of clock pulses.

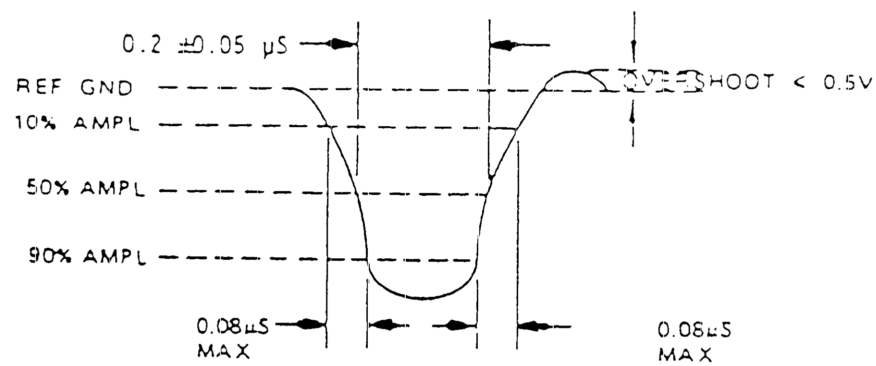
g. The TDS computer will compare the data placed on the outgoing data line to the data received on the incoming data line, and if not identical, send a pulse (recirculation fault pulse) on the outgoing data line to the DTS no sooner than 7 microseconds nor later than 500 microseconds after the twenty-sixth clock pulse of the second series of clocks. If a recirculation fault pulse is sent by the TDS computer to the DTS, the DTS shall indicate the occurrence of the recirculation fault and terminate the current transmission by transmitting the appropriate stop code in place of the data. The complete transfer (two series of 26 clocks each and a fault pulse if required) shall be completed within 1 millisecond.

h. If no recirculation fault occurs, the DTS shall check the logical state of the control bits (C_1 and C_2), transmit the data if both are a logical 1, or transmit a stop code if either is a logical 0. If the control bits are a logical 1, the DTS shall at the appropriate time place a demand pulse on the frame line requesting the next frame of data.

i. The process described in d through h is repeated until the TDS computer indicates that all the data has been transferred (either C_1 or C_2 a logical 0) or a recirculation fault occurs.

j. The DTS shall terminate the current transmission with the appropriate control codes (see 5.1.4.3.1). The amplitude of the interface pulses between the TDS computer and the DTS shall be measured across a 100 ohm load on the secondary winding of a terminating transformer.

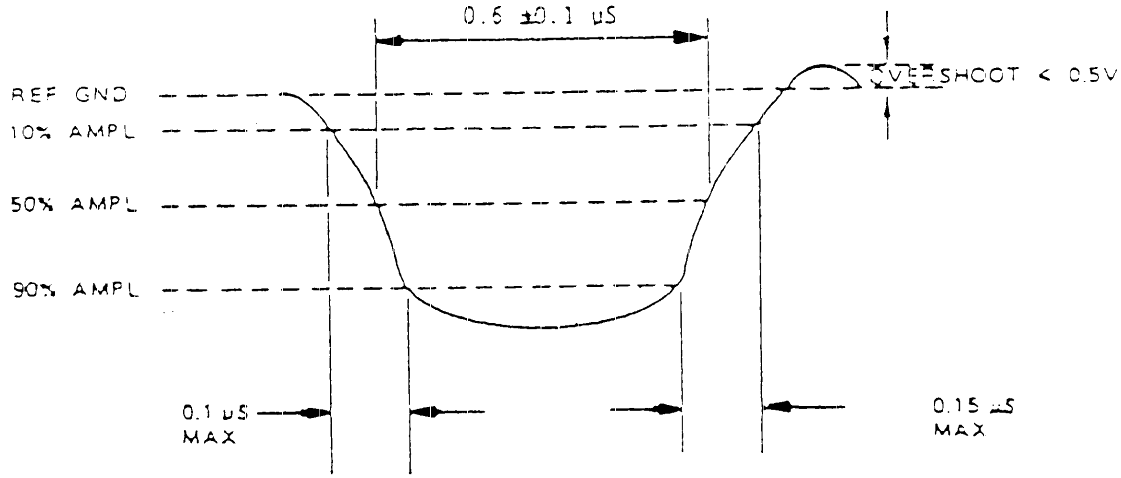
30.5 Electrical characteristics. The electrical characteristics of the interface between the TDS computer and the DTS shall be as follows. The amplitude of these pulses shall be measured across a 100 load on the secondary winding of a terminating transformer. The amplitude of all pulses shall be -6 V ±1 V with respect to ground. In the absence of a pulse, this voltage shall be 0 V ±1 V with respect to ground. The width of pulses from the TDS computer to the DTS shall be 200 nanoseconds ±50 nanoseconds. The width of pulses from the DTS to the TDS computer shall be 600 nanoseconds ±100 nanoseconds. The characteristics of these pulses shall be as specified in FIGURES 24 and 25, respectively.



Source = 100 ohms balanced pulse transformer
Pulsewidth: 0.2 ±0.05 μs
Rise time: 0.08 μs max
Fall time: 0.08 μs max
Source level: logic 1 = -6 ± 1 V
logic 0 + 0.0 ± 1 V

Receiver threshold levels: logic 0 =-1.5 to + 1 V
logic 1 = -4.5 to -7 V

FIGURE 24. Outgoing data line, data clock line, address data line, and address clock line pulse signal characteristics.



Termination = 100 ohms balanced pulse transformer

Pulsewidth: 0.6 ±0.1 μs
Rise time: 0.15 μs max
Fall time: 0.1 s max
Source level: logic 0 = 0.0 ±1 V
logic 1 = -6 ±1 V
Receiver threshold levels: logic 0 = -1.5 V to +1 V
logic 1 = -4.5 V to -7 V

FIGURE 25. Frame line and incoming data line pulse signal characteristics.

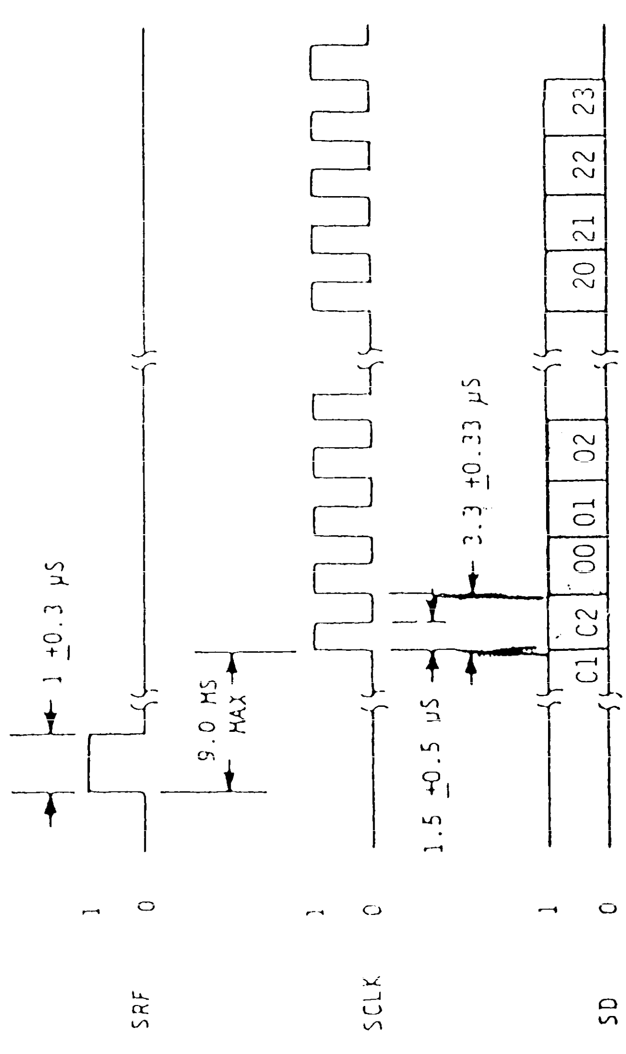
40. TDS computer nontactical interface. The nontactical interface lines between the TDS computer and DTS are shown in FIGURE 16 as side tone frame, sidetone data, and sidetone clock. The nontactical interface signals are used for test purposes. Transmitted data, when returned via the radio sidetone circuit, shall be available at the sidetone data interface.

40.1 Sidetone interface requirements. The sidetone interface drivers shall be open collector transistors with the capability of sinking a minimum of 20 mA. The sidetone interface timing requirements shall be as shown in FIGURE 26.

40.1.1 Sidetone frame line. The presence of new sidetone data shall be indicated by a pulse on the sidetone frame line from the DTS as shown in FIGURE 26.

40.1.2 Sidetone data line. Sidetone data from the DTS shall be placed on the sidetone data line in accordance with FIGURE 26.

40.1.3 Sidetone clock line. Clock pulses generated by the TDS computer will be placed on the sidetone clock line as shown in FIGURE 26 when accepting sidetone data from the DTS.



Source impedance: less than 100Ω
Receiver threshold levels: logic 1 3.5 V to 5.5 V
logic 0 -0.5 V to 1.5 V
Receiver impedance: greater than 3KΩ
Source level: logic 1 = 5 ±0.5 V
logic 0 = 0 ±0.5 V

FIGURE 26. Sidetone timing.

APPENDIX D3

DTS-TO-TDS COMPUTER INTERFACE - MIL-STD-188-114

This APPENDIX to be added at a later date.