



## 1. Description

### 1.1. Project

Project Name	lapwing2p2
Board Name	custom
Generated with:	STM32CubeMX 6.2.1
Date	09/23/2021

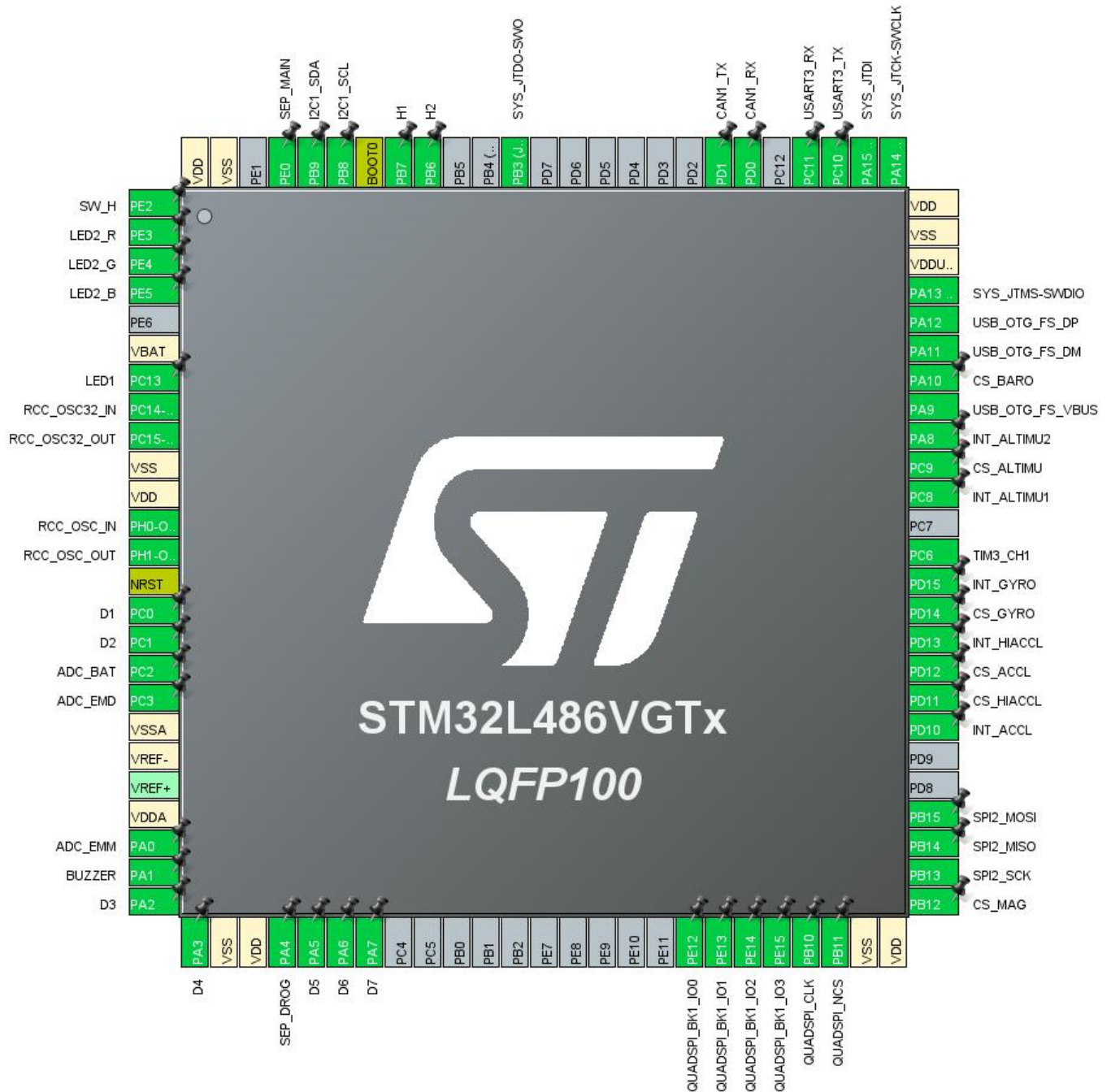
### 1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L486VGTx
MCU Package	LQFP100
MCU Pin number	100

### 1.3. Core(s) information

Core(s)	Arm Cortex-M4
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## 2. Pinout Configuration



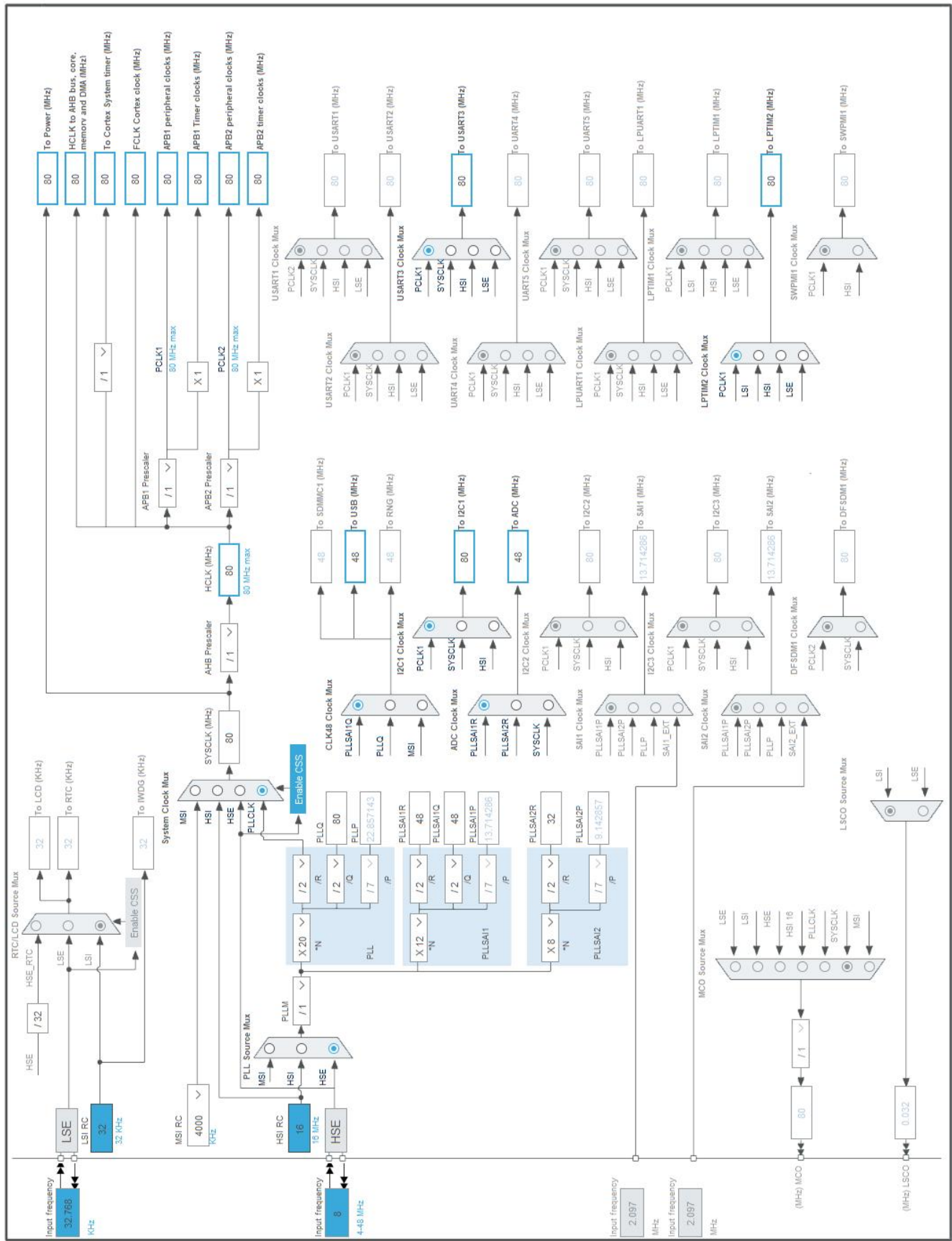
### 3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Input	SW_H
2	PE3 *	I/O	GPIO_Output	LED2_R
3	PE4 *	I/O	GPIO_Output	LED2_G
4	PE5 *	I/O	GPIO_Output	LED2_B
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Output	LED1
8	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0 *	I/O	GPIO_Output	D1
16	PC1 *	I/O	GPIO_Output	D2
17	PC2	I/O	ADC1_IN3	ADC_BAT
18	PC3	I/O	ADC1_IN4	ADC_EMD
19	VSSA	Power		
20	VREF-	Power		
22	VDDA	Power		
23	PA0	I/O	ADC1_IN5	ADC_EMM
24	PA1	I/O	TIM5_CH2	BUZZER
25	PA2 *	I/O	GPIO_Output	D3
26	PA3 *	I/O	GPIO_Output	D4
27	VSS	Power		
28	VDD	Power		
29	PA4 *	I/O	GPIO_Output	SEP_DROG
30	PA5 *	I/O	GPIO_Output	D5
31	PA6 *	I/O	GPIO_Output	D6
32	PA7 *	I/O	GPIO_Output	D7
43	PE12	I/O	QUADSPI_BK1_IO0	
44	PE13	I/O	QUADSPI_BK1_IO1	
45	PE14	I/O	QUADSPI_BK1_IO2	
46	PE15	I/O	QUADSPI_BK1_IO3	
47	PB10	I/O	QUADSPI_CLK	
48	PB11	I/O	QUADSPI_NCS	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
49	VSS	Power		
50	VDD	Power		
51	PB12 *	I/O	GPIO_Output	CS_MAG
52	PB13	I/O	SPI2_SCK	
53	PB14	I/O	SPI2_MISO	
54	PB15	I/O	SPI2_MOSI	
57	PD10 *	I/O	GPIO_Input	INT_ACCL
58	PD11 *	I/O	GPIO_Output	CS_HIACCL
59	PD12 *	I/O	GPIO_Output	CS_ACCL
60	PD13 *	I/O	GPIO_Input	INT_HIACCL
61	PD14 *	I/O	GPIO_Output	CS_GYRO
62	PD15 *	I/O	GPIO_Input	INT_GYRO
63	PC6	I/O	TIM3_CH1	
65	PC8 *	I/O	GPIO_Input	INT_ALTIMU1
66	PC9 *	I/O	GPIO_Output	CS_ALTIMU
67	PA8 *	I/O	GPIO_Input	INT_ALTIMU2
68	PA9	I/O	USB_OTG_FS_VBUS	
69	PA10 *	I/O	GPIO_Output	CS_BARO
70	PA11	I/O	USB_OTG_FS_DM	
71	PA12	I/O	USB_OTG_FS_DP	
72	PA13 (JTMS-SWDIO)	I/O	SYS_JTMS-SWDIO	
73	VDDUSB	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14 (JTCK-SWCLK)	I/O	SYS_JTCK-SWCLK	
77	PA15 (JTDI)	I/O	SYS_JTDI	
78	PC10	I/O	USART3_TX	
79	PC11	I/O	USART3_RX	
81	PD0	I/O	CAN1_RX	
82	PD1	I/O	CAN1_TX	
89	PB3 (JTDO-TRACESWO)	I/O	SYS_JTDO-SWO	
92	PB6 *	I/O	GPIO_Output	H2
93	PB7 *	I/O	GPIO_Output	H1
94	BOOT0	Boot		
95	PB8	I/O	I2C1_SCL	
96	PB9	I/O	I2C1_SDA	
97	PE0 *	I/O	GPIO_Output	SEP_MAIN
99	VSS	Power		
100	VDD	Power		

\* The pin is affected with an I/O function

## 4. Clock Tree Configuration



## 5. Software Project

### 5.1. Project Settings

Name	Value
Project Name	lapwing2p2
Project Folder	C:\Users\ultim\STM32CubeIDE\workspace_1.6.1\lapwing2p2
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_L4 V1.17.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_ADC1_Init	ADC1
4	MX_CAN1_Init	CAN1
5	MX_LPTIM2_Init	LPTIM2
6	MX_QUADSPI_Init	QUADSPI
7	MX_SPI2_Init	SPI2
8	MX_TIM2_Init	TIM2
9	MX_USART3_UART_Init	USART3
10	MX_USB_OTG_FS_PCD_Init	USB_OTG_FS
11	MX_I2C1_Init	I2C1



Rank	Function Name	Peripheral Instance Name
12	MX_TIM3_Init	TIM3
13	MX_TIM5_Init	TIM5

## 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L486VGTx
Datasheet	DS10199_Rev5

### 6.2. Parameter Selection

Temperature	25
Vdd	3.0

### 6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

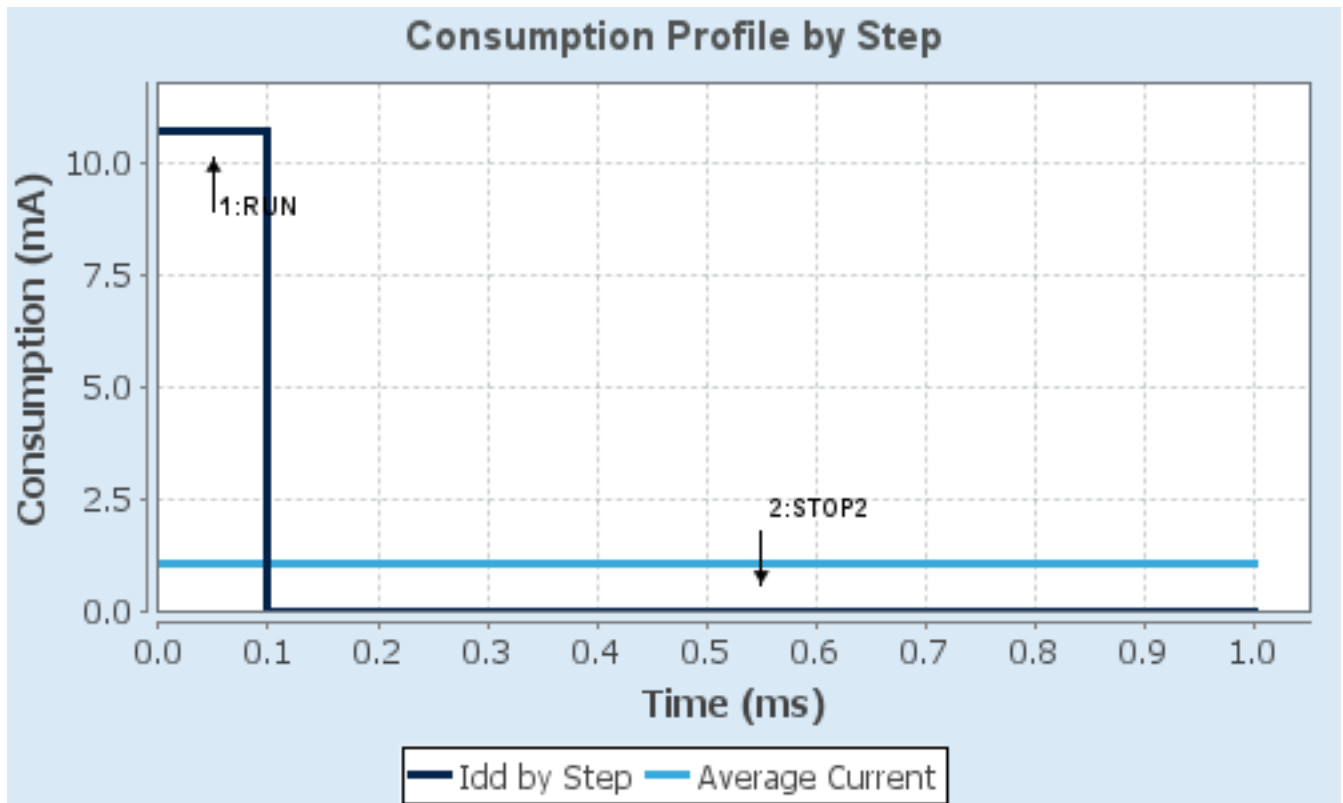
#### 6.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP2
<b>Vdd</b>	3.0	3.0
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	Range1-High	NoRange
<b>Fetch Type</b>	SRAM2	n/a
<b>CPU Frequency</b>	80 MHz	0 Hz
<b>Clock Configuration</b>	HSE PLL	ALL CLOCKS OFF
<b>Clock Source Frequency</b>	4 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	10.7 mA	1.18 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	100.0	0.0
<b>Ta Max</b>	103.65	105
<b>Category</b>	In DS Table	In DS Table

#### 6.5. Results

Sequence Time	1 ms	Average Current	1.07 mA
Battery Life	4 months, 10 days, 3 hours	Average DMIPS	100.0 DMIPS

#### 6.6. Chart



## 7. Peripherals and Middlewares Configuration

### 7.1. ADC1

**IN3: IN3 Single-ended**

**IN4: IN4 Single-ended**

**IN5: IN5 Single-ended**

#### 7.1.1. Parameter Settings:

##### ADCs\_Common\_Settings:

Mode Independent mode

##### ADC\_Settings:

Clock Prescaler Asynchronous clock mode divided by 1

Resolution ADC 12-bit resolution

Data Alignment Right alignment

Scan Conversion Mode Disabled

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data preserved

Low Power Auto Wait Disabled

##### ADC\_Regular\_ConversionMode:

Enable Regular Conversions Enable

Enable Regular Oversampling Disable

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

Rank 1

Channel Channel 3

Sampling Time 2.5 Cycles

Offset Number No offset

##### ADC\_Injected\_ConversionMode:

Enable Injected Conversions Disable

##### Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

##### Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

##### Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

## 7.2. CAN1

**mode: Activated**

### 7.2.1. Parameter Settings:

#### **Bit Timings Parameters:**

Prescaler (for Time Quantum)	16
Time Quantum	<b>200.0 *</b>
Time Quanta in Bit Segment 1	1 Time
Time Quanta in Bit Segment 2	1 Time
Time for one Bit	<b>600.00 *</b>
Baud Rate	<b>1666666 *</b>
ReSynchronization Jump Width	1 Time

#### **Basic Parameters:**

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

#### **Advanced Parameters:**

Operating Mode	Normal
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## 7.3. I2C1

**I2C: I2C**

### 7.3.1. Parameter Settings:

#### **Timing configuration:**

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	<b>0x10909CEC *</b>

#### **Slave Features:**

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

## 7.4. LPTIM2

**Mode: Counts internal clock events**

### 7.4.1. Parameter Settings:

**Clock:**

Clock Prescaler	Prescaler Div1
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**Preload:**

Update Mode	Update Immediate
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**Trigger:**

Trigger Source	Software Trigger
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## 7.5. QUADSPI

**Single Bank: Quad SPI Line**

### 7.5.1. Parameter Settings:

**General Parameters:**

Clock Prescaler	255
Fifo Threshold	1
Sample Shifting	No Sample Shifting
Flash Size	1
Chip Select High Time	1 Cycle
Clock Mode	Low

## 7.6. RCC

**High Speed Clock (HSE): Crystal/Ceramic Resonator**

**Low Speed Clock (LSE) : Crystal/Ceramic Resonator**

### 7.6.1. Parameter Settings:

**System Parameters:**

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

#### **RCC Parameters:**

HSI Calibration Value	16
MSI Calibration Value	0
MSI Auto Calibration	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

#### **Power Parameters:**

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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## **7.7. SPI2**

### **Mode: Full-Duplex Master**

#### 7.7.1. Parameter Settings:

##### **Basic Parameters:**

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

##### **Clock Parameters:**

Prescaler (for Baud Rate)	2
Baud Rate	<b>40.0 MBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

##### **Advanced Parameters:**

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

## **7.8. SYS**

### **Debug: JTAG (4 pins)**

### **Timebase Source: SysTick**



## 7.9. TIM2

### Clock Source : Internal Clock

#### 7.9.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value )	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

##### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

## 7.10. TIM3

### Channel1: PWM Generation CH1

#### 7.10.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

##### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

##### Clear Input:

Clear Input Source	Disable
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##### PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

## 7.11. TIM5

### Channel2: PWM Generation CH2

#### 7.11.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value )	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

##### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

##### Clear Input:

Clear Input Source	Disable
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##### PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

## 7.12. USART3

### Mode: Asynchronous

#### 7.12.1. Parameter Settings:

##### Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

##### Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

##### Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable

Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

### 7.13. USB\_OTG\_FS

**Mode: Device\_Only**

**Activate\_VBUS: VBUS sensing**

#### 7.13.1. Parameter Settings:

Speed	Full Speed 12MBit/s
Low power	Disabled
Battery charging	Enabled
Link Power Management	Disabled
VBUS sensing	Enabled
Signal start of frame	Disabled

**\* User modified value**

## 8. System Configuration

### 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC2	ADC1_IN3	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	ADC_BAT
	PC3	ADC1_IN4	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	ADC_EMD
	PA0	ADC1_IN5	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	ADC_EMM
CAN1	PD0	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PD1	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	Pull-up	Very High *	
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	Very High *	
QUADSPI	PE12	QUADSPI_BK1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PE13	QUADSPI_BK1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PE14	QUADSPI_BK1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PE15	QUADSPI_BK1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB10	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB11	QUADSPI_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
RCC	PC14-OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT (PC15)	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-	RCC_OSC_OUT	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	OSC_OUT (PH1)					
SPI2	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
SYS	PA13 (JTMS-SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK-SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PA15 (JTDI)	SYS_JTDI	n/a	n/a	n/a	
	PB3 (JTDO-TRACESWO)	SYS_JTDO-SWO	n/a	n/a	n/a	
TIM3	PC6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM5	PA1	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	BUZZER
USART3	PC10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
	PC11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
USB_OTG_FS	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	n/a	
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
GPIO	PE2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SW_H
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2_R
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2_G
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2_B
	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D1
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D2
	PA2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D3
	PA3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D4
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SEP_DROG
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D5

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D6
	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D7
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CS_MAG
	PD10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	INT_ACCL
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CS_HIACCL
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CS_ACCL
	PD13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	INT_HIACCL
	PD14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CS_GYRO
	PD15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	INT_GYRO
	PC8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	INT_ALTIMU1
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CS_ALTIMU
	PA8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	INT_ALTIMU2
	PA10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CS_BARO
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	H2
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	H1
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SEP_MAIN

## 8.2. DMA configuration

nothing configured in DMA service

### 8.3. NVIC configuration

#### 8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 interrupts	unused		
CAN1 TX interrupt	unused		
CAN1 RX0 interrupt	unused		
CAN1 RX1 interrupt	unused		
CAN1 SCE interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
SPI2 global interrupt	unused		
USART3 global interrupt	unused		
TIM5 global interrupt	unused		
LPTIM2 global interrupt	unused		
USB OTG FS global interrupt	unused		
QUADSPI global interrupt	unused		
FPU global interrupt	unused		

#### 8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

\* User modified value



## 9. System Views

9.1. Category view

9.1.1. Current

Middleware						
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
DMA	ADC1 ✓	LPTIM2 ✓	CAI1 ✗			
GPIO ✓		TIM2 ✓	I2C1 ✓			
IVVIC ✓		TIM3 ✓	QUADSPI ✓			
RCC ✓		TIM5 ✓	SPI2 ✓			
SYS ✓			USART3 ✓			
			USB_FS ✓			

## 10. Docs & Resources

Type	Link
Datasheet	<a href="http://www.st.com/resource/en/datasheet/DM00108833.pdf">http://www.st.com/resource/en/datasheet/DM00108833.pdf</a>
Reference manual	<a href="http://www.st.com/resource/en/reference_manual/DM00083560.pdf">http://www.st.com/resource/en/reference_manual/DM00083560.pdf</a>
Programming manual	<a href="http://www.st.com/resource/en/programming_manual/DM00046982.pdf">http://www.st.com/resource/en/programming_manual/DM00046982.pdf</a>
Errata sheet	<a href="http://www.st.com/resource/en/errata_sheet/DM00111498.pdf">http://www.st.com/resource/en/errata_sheet/DM00111498.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00160362.pdf">http://www.st.com/resource/en/application_note/CD00160362.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00167594.pdf">http://www.st.com/resource/en/application_note/CD00167594.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00211314.pdf">http://www.st.com/resource/en/application_note/CD00211314.pdf</a>
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