TDTS08: Lab Report

Lab 4: VLIW Processors

Name	PIN	Email
Alexander Yngve	930320-6651	aleyn573@student.liu.se
Pål Kastman	851212-7575	palka285@student.liu.se

Contents

1 Introduction

The purpose of this lab was to convert normal sequential code to VLIW instructions, so that we would get a greater performance. Basically we do what the VLIW compiler does during compilation time.

2 Method

The approach for this lab was the following:

1. Choose a basic block, and disassemble the block.
2. Find dependencies between the instruction in the block.
3. We pack the instruction into VLIWs.

2.1 Basic Block

2.2 Dependencies

2.3 VLIW

3 Result

We first choose to make our architecture with no limit, this design can be seen in 1.

Table 1

ALU			**MUL**	**FPU**	**BAU**				
					41b528	41b530	41b538	41b548	41b558
41b540	41b568	41b560			41b560				
41b570	41b588	41b580							
					41b578				
41b590									
					41b598	41b5a0			

We then tried to reduce some of the units without loosing any performance, we first by tried by removing one of the BAUs (figure 2), since those are the most expensive units. In table 6 we can see that this design (VLIW2) doesn't perform any worse than the first design (VLIW1), so we continued to reduce more units in search of an even better design for this block.

Table 2

ALU			MUL	FPU	BAU		
					41b528	41b558	41b538
41b568	41b540	41b560			41b548	41b530	
41b570	41b580				41b550		
41b588					41b578		
41b590							
					41b598	41b5a0	

Table 3

ALU		MUL	FPU	BAU	
				41b528	41b538
41b568	41b540			41b548	41b558
41b570	41b560			41b550	41b530
41b588	41b580			41b578	
41b590					
				41b598	41b5a0

Table 4

ALU		MUL	FPU	BAU
				41b528
				41b538
41b568	41b540			41b558
41b570	41b560			41b548
41b580				41b550
41b588				41b578
41b590				41b530
				41b598
				41b5a0

Table 5

Pricelist	
ALU cost	2
MUL cost	16
FPU cost	32
BAU cost	100

Table 6

Design	VLIW1	VLIW2	VLIW3	VLIW4
No. ALU	3	3	2	2
No. MUL	1	1	1	1
No. FPU	1	1	1	1
No. BAU	5	3	2	1
Total Cost	554	354	252	152
No. Cycles	6	6	6	9
Cost per. ratio	3324	2124	1512	1368

4 Discussion